*Functional Safety Information*

# *TMUX1308-Q1 and TMUX1309-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

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## Trademarks

# 1 Overview

This document contains information for TMUX1308-Q1 and TMUX1309-Q1 (TSSOP, SOT-23-THIN, and WQFN packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

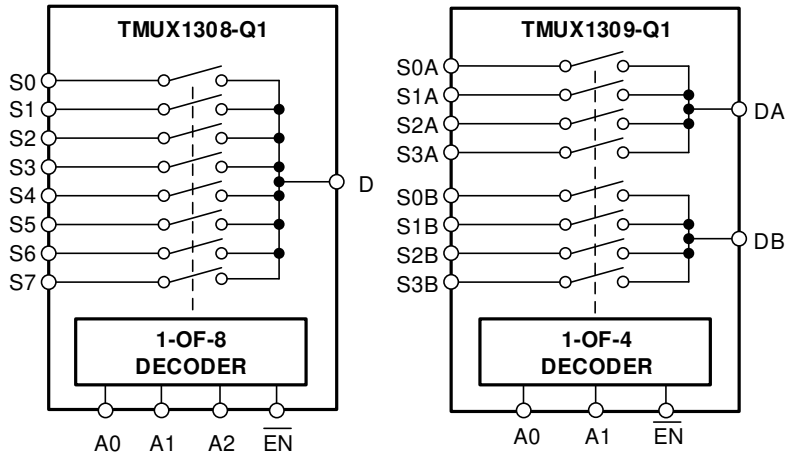


**Figure 1-1. Functional Block Diagram**

TMUX1308-Q1 and TMUX1309-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 TSSOP, SOT-23-THIN, and WQFN Packages

This section provides Functional Safety Failure In Time (FIT) rates for TSSOP, SOT-23-THIN, and WQFN packages of the TMUX1308-Q1 and TMUX1309-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-3 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 TSSOP**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 12 |
| Die FIT Rate | 3 |
| Package FIT Rate | 9 |

**Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 SOT-23-THIN and WQFN**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 8 |
| Die FIT Rate | 3 |
| Package FIT Rate | 5 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | BICMOS<br>ASICs Analog and Mixed =<50 V supply | 20 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TMUX1308-Q1 and TMUX1309-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| MUX no output (HIZ) | 20% |
| MUX channel stuck on | 10% |
| MUX channel stuck off | 10% |
| MUX functional out of specification voltage or timing | 60% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TMUX1308-Q1 and TMUX1309-Q1 (TSSOP, SOT-23-THIN, and WQFN packages). The failure modes covered in this document include the following typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-10)
- Pin open-circuited (see Table 4-3 and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-12)
- Pin short-circuited to VDD (see Table 4-5 and Table 4-13)

Table 4-2 through Table 4-4 also indicate how these pin conditions can affect the device per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

## 4.1 TMUX1308-Q1 TSSOP and SOT-23-THIN Package

Figure 4-1 and Figure 4-2 shows the TMUX1308-Q1 pin diagram for the TSSOP and SOT-23-THIN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMUX1308-Q1 and TMUX1309-Q1 data sheet.

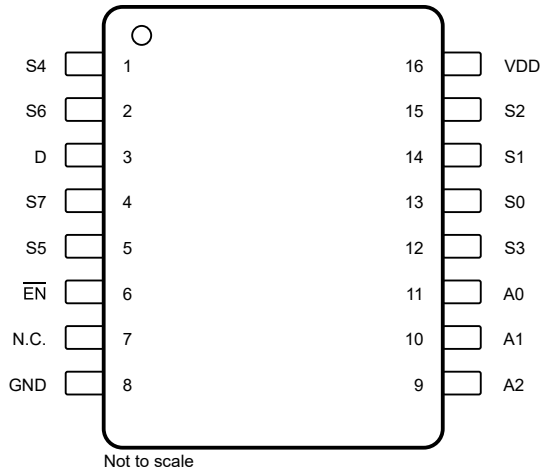


**Figure 4-1. Pin Diagram (TSSOP) Package**

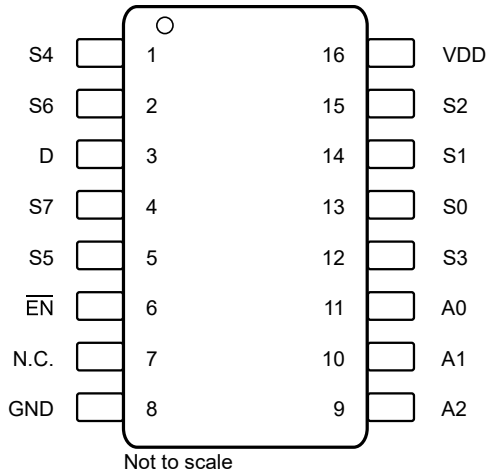


**Figure 4-2. Pin Diagram (SOT-23-THIN) Package**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S4 | 1 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S6 | 2 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| D | 3 | Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S7 | 4 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S5 | 5 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck low. Can no longer disable the device without power down | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | No effect, normal operation. | D |
| A2 | 9 | Address stuck low. Cannot control switch states. | B |
| A1 | 10 | Address stuck low. Cannot control switch states. | B |
| A0 | 11 | Address stuck low. Cannot control switch states. | B |
| S3 | 12 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0 | 13 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1 | 14 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2 | 15 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S4 | 1 | Corruption of the signal passed onto the D pin. | B |
| S6 | 2 | Corruption of the signal passed onto the D pin. | B |
| D | 3 | Corruption of the signal passed onto the S pins. | B |
| S7 | 4 | Corruption of the signal passed onto the D pin. | B |
| S5 | 5 | Corruption of the signal passed onto the D pin. | B |
| $\overline{EN}$ | 6 | Control of the $\overline{EN}$ pin is lost. Cannot disable switch. Will default to switches disabled. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| A2 | 9 | Control of the address pin is lost. Cannot control switch. | B |
| A1 | 10 | Control of the address pin is lost. Cannot control switch. | B |
| A0 | 11 | Control of the address pin is lost. Cannot control switch. | B |
| S3 | 12 | Corruption of the signal passed onto the D pin. | B |
| S0 | 13 | Corruption of the signal passed onto the D pin. | B |
| S1 | 14 | Corruption of the signal passed onto the D pin. | B |
| S2 | 15 | Corruption of the signal passed onto the D pin. | B |
| VDD | 16 | Device is unpowered. Device is not functional. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| S4 | 1 | S6 | Possible corruption of the signal passed onto the D pin. | B |
| S6 | 2 | D | Possible corruption of the signal passed onto the SX and D pin. | B |
| D | 3 | S7 | Possible corruption of the signal passed onto the SX and D pin. | B |
| S7 | 4 | S5 | Possible corruption of the signal passed onto the D pin. | B |
| S5 | 5 | $\overline{EN}$ | Possible corruption of the signal passed onto the D pin. Switch state will be undefined. | B |
| $\overline{EN}$ | 6 | N.C. | No connect pin electrically floating, no effect. | D |
| N.C. | 7 | GND | No connect pin electrically floating, no effect. | D |
| GND | 8 | A2 | Not considered, corner pin. | D |
| A2 | 9 | A1 | Control of the switch state is lost. | B |
| A1 | 10 | A0 | Control of the switch state is lost. | B |
| A0 | 11 | S3 | Possible corruption of the signal passed onto the D pin. Control of the switch state is lost. | B |
| S3 | 12 | S0 | Possible corruption of the signal passed onto the D pin. | B |
| S0 | 13 | S1 | Possible corruption of the signal passed onto the D pin. | B |
| S1 | 14 | S2 | Possible corruption of the signal passed onto the D pin. | B |
| S2 | 15 | VDD | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | S4 | Not considered, corner pin. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S4 | 1 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S6 | 2 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| D | 3 | Corruption of the signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S7 | 4 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S5 | 5 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck high. Can no longer enable the device. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| A2 | 9 | Address stuck high. Cannot control switch states. | B |
| A1 | 10 | Address stuck high. Cannot control switch states. | B |
| A0 | 11 | Address stuck high. Cannot control switch states. | B |
| S3 | 12 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0 | 13 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1 | 14 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2 | 15 | Corruption of the signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | No effect, normal operation. | D |

## 4.2 TMUX1308-Q1 WQFN Package

The figure below shows the TMUX1308-Q1 pin diagram for the WQFN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMUX1308-Q1 and TMUX1309-Q1 data sheet.

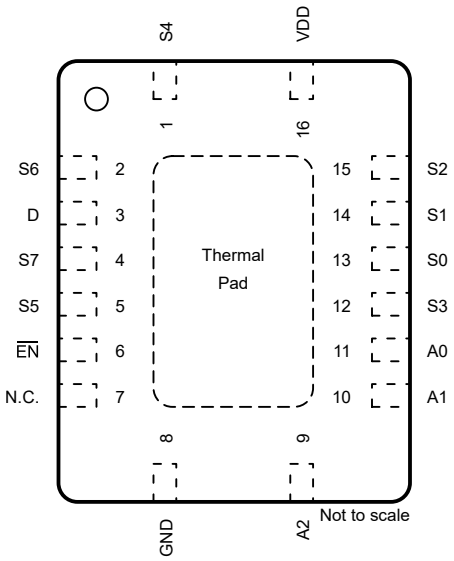


**Figure 4-3. Pin Diagram for TMUX1308-Q1 in WQFN Package**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S4 | 1 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S6 | 2 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| D | 3 | Corruption of signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S7 | 4 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S5 | 5 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck low. Can no longer disable the device without power down. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | No effect, normal operation. | D |
| A2 | 9 | Address stuck low. Cannot control switch states. | B |
| A1 | 10 | Address stuck low. Cannot control switch states. | B |
| A0 | 11 | Address stuck low. Cannot control switch states. | B |
| S3 | 12 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0 | 13 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1 | 14 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S2 | 15 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| Thermal pad | — | No effect, normal operation. | D |

**Table 4-7. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|
| S4 | 1 | Corruption of signal passed onto the D pin. | B |
| S6 | 2 | Corruption of signal passed onto the D pin. | B |
| D | 3 | Corruption of signal passed onto the S pins. | B |
| S7 | 4 | Corruption of signal passed onto the D pin. | B |
| S5 | 5 | Corruption of signal passed onto the D pin. | B |
| $\overline{EN}$ | 6 | Control of the $\overline{EN}$ pin is lost. Cannot disable switch. Will default to switches disabled. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| A2 | 9 | Control of the address pin is lost. Cannot control switch. | B |
| A1 | 10 | Control of the address pin is lost. Cannot control switch. | B |
| A0 | 11 | Control of the address pin is lost. Cannot control switch. | B |
| S3 | 12 | Corruption of signal passed onto the D pin. | B |
| S0 | 13 | Corruption of signal passed onto the D pin. | B |
| S1 | 14 | Corruption of signal passed onto the D pin. | B |
| S2 | 15 | Corruption of signal passed onto the D pin. | B |
| VDD | 16 | Device is unpowered. Device is not functional. | B |
| Thermal pad | — | No effect, normal operation. | D |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|---|
| S4 | 1 | S6 | Possible corruption of signal passed onto the D pin. | B |
| S6 | 2 | D | Possible corruption of signal passed onto the SX and D pin. | B |
| D | 3 | S7 | Possible corruption of signal passed onto the SX and D pin. | B |
| S7 | 4 | S5 | Possible corruption of signal passed onto the D pin. | B |
| S5 | 5 | $\overline{EN}$ | Possible corruption of signal passed onto the D pin. Switch state will be undefined. | B |
| $\overline{EN}$ | 6 | N.C. | No connect pin electrically floating, no effect. | D |
| N.C. | 7 | GND | No connect pin electrically floating, no effect. | D |
| GND | 8 | A2 | Not considered, corner pin. | D |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|---|
| A2 | 9 | A1 | Loss of control of switch state. | B |
| A1 | 10 | A0 | Loss of control of switch state. | B |
| A0 | 11 | S3 | Possible corruption of signal passed onto the D pin. Loss of control of switch state. | B |
| S3 | 12 | S0 | Possible corruption of signal passed onto the D pin. | B |
| S0 | 13 | S1 | Possible corruption of signal passed onto the D pin. | B |
| S1 | 14 | S2 | Possible corruption of signal passed onto the D pin. | B |
| S2 | 15 | VDD | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | S4 | Not considered, corner pin. | D |

**Table 4-9. Pin FMA for Device Pins Short-Circuited to VDD**

| Pin Name | Pin No. | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|
| S4 | 1 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S6 | 2 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| D | 3 | Corruption of signal passed onto the S pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S7 | 4 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S5 | 5 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck high. Can no longer enable the device. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| A2 | 9 | Address stuck high. Cannot control switch states. | B |
| A1 | 10 | Address stuck high. Cannot control switch states. | B |
| A0 | 11 | Address stuck high. Cannot control switch states. | B |
| S3 | 12 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0 | 13 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1 | 14 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2 | 15 | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | No effect, normal operation. | D |
| Thermal pad | — | No connect pin electrically floating, no effect. | D |

## 4.3 TMUX1309-Q1 TSSOP and SOT-23-THIN Package

Figure 4-1 and Figure 4-2 shows the TMUX1309-Q1 pin diagram for the TSSOP and SOT-23-THIN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMUX1308-Q1 and TMUX1309-Q1 data sheet.

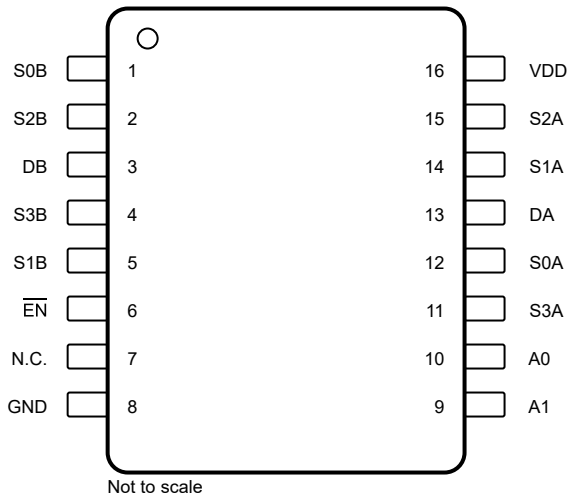


**Figure 4-4. Pin Diagram (TSSOP) Package**

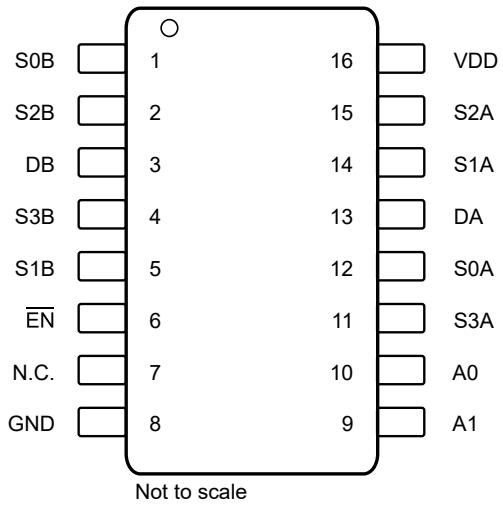


**Figure 4-5. Pin Diagram (SOT-23-THIN) Package**

**Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2B | 2 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DB | 3 | Corruption of signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S3B | 4 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1B | 5 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ Stuck low. Can no longer disable the device without power down. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | No effect, normal operation. | D |
| A1 | 9 | Address stuck low. Cannot control switch states. | B |
| A0 | 10 | Address stuck low. Cannot control switch states. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0A | 12 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DA | 13 | Corruption of signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1A | 14 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2A | 15 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |

**Table 4-11. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. | B |
| S2B | 2 | Corruption of signal passed onto the DB pin. | B |
| DB | 3 | Corruption of signal passed onto the SxB pins. | B |
| S3B | 4 | Corruption of signal passed onto the DB pin. | B |
| S1B | 5 | Corruption of signal passed onto the DB pin. | B |
| $\overline{EN}$ | 6 | Control of the $\overline{EN}$ pin is lost. Cannot disable switch. Will default to switches disabled. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional.<br>Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| A1 | 9 | Control of the address pin is lost. Cannot control switch. | B |
| A0 | 10 | Control of the address pin is lost. Cannot control switch. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. | B |
| S0A | 12 | Corruption of signal passed onto the DA pin. | B |
| DA | 13 | Corruption of signal passed onto the SxA pin. | B |
| S1A | 14 | Corruption of signal passed onto the DA pin. | B |
| S2A | 15 | Corruption of signal passed onto the DA pin. | B |
| VDD | 16 | Device is unpowered. Device is not functional. | B |

**Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| S0B | 1 | S2B | Possible corruption of signal passed onto the DB pin. | B |
| S2B | 2 | DB | Possible corruption of signal passed onto the SxB and DB pin. | B |
| DB | 3 | S3B | Possible corruption of signal passed onto the SxB and DB pin. | B |
| S3B | 4 | S1B | Possible corruption of signal passed onto the DB pin. | B |
| S1B | 5 | $\overline{EN}$ | Possible corruption of signal passed onto the DB pin. Switch state will be undefined. | B |
| $\overline{EN}$ | 6 | N.C. | No connect pin electrically floating, no effect. | D |
| N.C. | 7 | GND | No connect pin electrically floating, no effect. | D |
| GND | 8 | A1 | Not considered, corner pin. | D |
| A1 | 9 | A0 | Control of the switch state is lost. | B |
| A0 | 10 | S3A | Possible corruption of signal passed onto the DA pin. Control of the switch state is lost. | B |
| S3A | 11 | S0A | Possible corruption of signal passed onto the DA pin. | B |
| S0A | 12 | DA | Possible corruption of signal passed onto the SxA and DA pin. | B |
| DA | 13 | S1A | Possible corruption of signal passed onto the SxA and DA pin. | B |
| S1A | 14 | S2A | Possible corruption of signal passed onto the DA pin. | B |
| S2A | 15 | VDD | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | S0B | Not considered, corner pin. | D |

**Table 4-13. Pin FMA for Device Pins Short-Circuited to VDD**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2B | 2 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DB | 3 | Corruption of signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S3B | 4 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1B | 5 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck high. Can no longer enable the device. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| A1 | 9 | Address stuck high. Cannot control switch states. | B |
| A0 | 10 | Address stuck high. Cannot control switch states. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0A | 12 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DA | 13 | Corruption of signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1A | 14 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2A | 15 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | No effect, normal operation. | D |

## 4.4 TMUX1309-Q1 WQFN Package

The figure below shows the TMUX1309-Q1 pin diagram for the WQFN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMUX1308-Q1 and TMUX1309-Q1 data sheet.

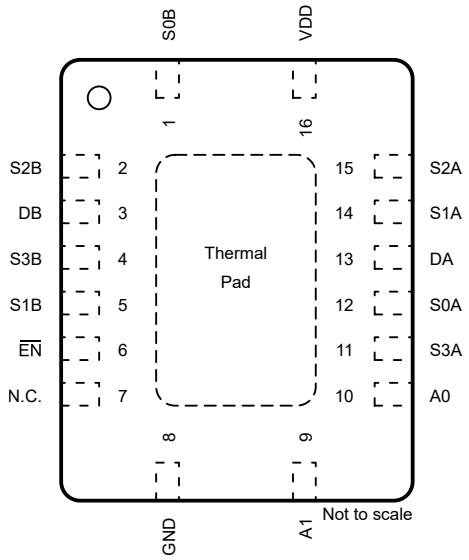


**Figure 4-6. Pin Diagram for TMUX1309-Q1 in WQFN Package**

**Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2B | 2 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DB | 3 | Corruption of signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S3B | 4 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1B | 5 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck low. Can no longer disable the device without power down. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | No effect, normal operation. | D |
| A1 | 9 | Address stuck low. Cannot control switch states. | B |
| A0 | 10 | Address stuck low. Cannot control switch states. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0A | 12 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DA | 13 | Corruption of signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1A | 14 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2A | 15 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| Thermal pad | — | No effect, normal operation. | D |

**Table 4-15. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. | B |
| S2B | 2 | Corruption of signal passed onto the DB pin. | B |
| DB | 3 | Corruption of signal passed onto the SxB pins. | B |
| S3B | 4 | Corruption of signal passed onto the DB pin. | B |
| S1B | 5 | Corruption of signal passed onto the DB pin. | B |
| $\overline{EN}$ | 6 | Loss of control of $\overline{EN}$ pin. Cannot disable switch. Will default to switches disabled. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible. | A |
| A1 | 9 | Loss of control of address pin. Cannot control switch. | B |

**Table 4-15. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|
| A0 | 10 | Loss of control of address pin. Cannot control switch. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. | B |
| S0A | 12 | Corruption of signal passed onto the DA pin. | B |
| DA | 13 | Corruption of signal passed onto the SxA pin. | B |
| S1A | 14 | Corruption of signal passed onto the DA pin. | B |
| S2A | 15 | Corruption of signal passed onto the DA pin. | B |
| VDD | 16 | Device is unpowered. Device is not functional. | B |
| Thermal pad | — | No effect, normal operation. | D |

**Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|---|
| S0B | 1 | S2B | Possible corruption of signal passed onto the DB pin. | B |
| S2B | 2 | DB | Possible corruption of signal passed onto the SxB and DB pin. | B |
| DB | 3 | S3B | Possible corruption of signal passed onto the SxB and DB pin. | B |
| S3B | 4 | S1B | Possible corruption of signal passed onto the DB pin. | B |
| S1B | 5 | $\overline{EN}$ | Possible corruption of signal passed onto the DB pin. Switch state will be undefined. | B |
| $\overline{EN}$ | 6 | N.C. | No connect pin electrically floating, no effect. | D |
| N.C. | 7 | GND | No connect pin electrically floating, no effect. | D |
| GND | 8 | A1 | Not considered, corner pin. | D |
| A1 | 9 | A0 | Control of switch state is lost. | B |
| A0 | 10 | S3A | Possible corruption of signal passed onto the DA pin. Control of switch state is lost. | B |
| S3A | 11 | S0A | Possible corruption of signal passed onto the DA pin. | B |
| S0A | 12 | DA | Possible corruption of signal passed onto the SxA and DA pin. | B |
| DA | 13 | S1A | Possible corruption of signal passed onto the SxA and DA pin. | B |
| S1A | 14 | S2A | Possible corruption of signal passed onto the DA pin. | B |
| S2A | 15 | VDD | Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | S0B | Not considered, corner pin. | D |

**Table 4-17. Pin FMA for Device Pins Short-Circuited to VDD**

| Pin Name | Pin No. | Description of potential failure effect(s) | Failure effect class |
|---|---|---|---|
| S0B | 1 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2B | 2 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DB | 3 | Corruption of signal passed onto the SxB pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S3B | 4 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1B | 5 | Corruption of signal passed onto the DB pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| $\overline{EN}$ | 6 | $\overline{EN}$ stuck high. Can no longer enable the device. | B |
| N.C. | 7 | No effect, unconnected pin. | D |
| GND | 8 | Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible. | A |
| A1 | 9 | Address stuck high. Cannot control switch states. | B |
| A0 | 10 | Address stuck high. Cannot control switch states. | B |
| S3A | 11 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S0A | 12 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| DA | 13 | Corruption of signal passed onto the SxA pins. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S1A | 14 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| S2A | 15 | Corruption of signal passed onto the DA pin. If there is no limiting resistor in the switch path, then device damage is possible. | A |
| VDD | 16 | No effect, normal operation. | D |
| Thermal pad | — | No connect pin electrically floating, no effect. | D |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (November 2020) to Revision B (January 2022)** **Page**

- Added information for the *WQFN* package to the report..... 2
- Added the *TMUX1309-Q1 TSSOP* and *SOT-23-THIN* pin configuration to the *TMUX1309-Q1 TSSOP and SOT-23-THIN Package* section.....10

**Changes from Revision * (April 2020) to Revision A (November 2020)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.....2
- Added *TMUX1309-Q1* to the report.....2

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