Application Brief

Thermal Considerations for AC Family Logic Buffers

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Introduction

The AC logic family provides some of the fastest and highest drive strength single-ended logic buffers on the market today. Along with high speeds and heavy loading comes large temperature increases. In this document, we show through examples how to utilize the provided thermal metrics to determine application specific limitations.

There are many different electronic products with specific use-cases of medium to high speed digital signal driving requirements. Pulse width modulation (PWM) is common in motor speed control, power regulation, LED control, and audio amplification. PWM signals are created by alternating between digital high state (ON) and low state (OFF) signals. These signals can be changed by varying pulse width (duration of the high state signal), increasing or decreasing duty cycle, as well as increasing or decreasing frequency. Digital buffers can be used to redrive PWM signals for a variety of applications across a wide range of frequencies and duty cycles.

Figure 1. Rack servers

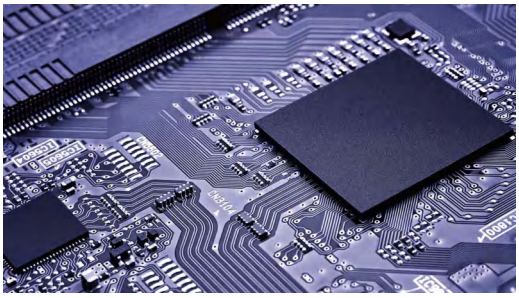

Figure 2. Printed circuit board traces

Rack servers commonly have controlled imepdance traces that require strong drivers. The AC logic family supports direct drive of 50Ω traces and can support relatively high speeds and heavy loads. Generally speaking, traces under 12cm add capacitance without creating transmission line effects, and traces over 12cm require controlled impedance and correct terminations to mitigate transmisison line effects. Source termination to match impedance of the transmission line is all that is required for an AC driver like the SN74AC244 to be used for this type of application. See *Design Considerations for Logic Products* for details.

Low voltage relays are common in test and measurement as well as other industrial applications. The high drive strength and integrated output clamp diodes of the AC logic family allow for direct drive of low voltage relays. These relays are often used to control higher amperage loads like servo motors, audio amplifiers, and temperature sensors. Low voltage relays can be actuated with 5V and up to 30mA of current. Microcontrollers, FPGAs, and CPUs seldom have the level of drive strength required to drive these directly. The SN74AC244 is capable of driving all eight channels with 24mA each making the SN74AC244 an excellent choice for this application and enabling the use of these relays within a system.

Power Calculation

Temperature increases are caused by power consumption in a semiconductor device. To accurately calculate power consumption for a CMOS logic gate, we must define a few terms and equations.

$$P_{TOTAL} = P_T + P_{LC} + P_S + P_{LRN} + P_{LRP} \quad (1)$$

In Equation 1 we have the total power (P_{TOTAL}), static power (P_S), transient power (P_T), capacitive load power (P_{LC}), negative resistive load power (P_{LRN}), and positive resistive load power (P_{LRP}). The load power values (P_{LC}, P_{LRN}, and P_{LRP}) are specifically the power consumed within the CMOS logic device to drive these loads. The power consumption equation components P_S, P_{LRN}, and P_{LRP} can be considered as a constant power draw, with no variation due to operating frequency, while the components P_T and P_{LC} are both frequency dependent.

$$P_T = V_{CC}^2 C_{pd} f_i N_{SW} \quad (2)$$

In Equation 2 we have the transient power consumption (P_T), power dissipation capacitance (C_{pd}), supply voltage (V_{CC}), input frequency (f_i), and number of channels switching, (N_{SW}). This equation assumes that all channels are switching at the same frequency and have the same power dissipation capacitance value.

$$P_{LC} = V_{CC}^2 C_L f_o N_{SW} \quad (3)$$

In Equation 3 we have the capacitive load power dissipation (P_{LC}), supply voltage (V_{CC}), capacitive load (C_L), output frequency (f_o), and number of channels switching (N_{SW}).

$$P_S = V_{CC} I_{CC} \quad (4)$$

In Equation 4 we have the static power consumption (P_S), supply voltage (V_{CC}), and static supply current (I_{CC}).

$$P_{LRN} = D_o (V_{CC} - V_{OH}) \left(\frac{V_{OH}}{R_{PD}} \right) \quad (5)$$

In Equation 5 we have the negative resistive load power dissipation (P_{LRN}), output duty cycle (D_o), supply voltage (V_{CC}), output high-state voltage (V_{OH}), and output pull-down resistance (R_{PD}).

$$P_{LRP} = (1 - D_o)(V_{OL}) \left(\frac{V_{CC} - V_{OL}}{R_{LP}} \right) \quad (6)$$

In Equation 6 we have the positive resistive load power dissipation (P_{LRP}), output duty cycle (D_o), supply voltage (V_{CC}), output high-state voltage (V_{OH}), and output pull-up resistance (R_{PU}).

The resistive and static power consumption values can often be ignored when doing thermal calculations for CMOS logic gates, as these values do not generally have a large impact on the total power consumption. For the sake completeness, these calculations are included in this document, but in the following examples you can see how these values are generally unnecessary for thermal dissipation calculations.

The following sections provide calculated and bench-verified thermal performance for the SN74AC244 device in common applications.

Application 1: Calculations

The SN74AC244 provides eight independent buffers. In this application, we tie together all eight inputs to a single 10MHz, 50% duty cycle clock source and drive independent loads with each output. Using shared clock inputs to split into multiple outputs is known as a clock fanout application.

The output loading is equivalent to approximately 10 CMOS device inputs, with a total capacitive load (C_L) of 56pF per channel and total resistive load of 500kΩ (R_{LP} and R_{LN}) per channel. C_L is the closes value to 50pF that was available locally at the time of testing. R_{LP} and R_{LN} values were calculated based on the supply voltage, 5V, and an assumed input leakage current maximum of 1µA per input. With 10 parallel inputs, this is 10µA maximum at 5V, which is equivalent to 500kΩ.

First, we calculate the static power consumption numbers. Before plugging values into the given equations, we need to determine the V_{OH} and V_{OL} values for this loading. The data sheet provides the worst-case 4.5V supply V_{OH} at 50µA load as V_{CC} – 0.1V, and V_{OL} at the same load as 0.1V. Our loading is ten times less, so the voltage is also scaled to be ten times less, resulting in V_{CC}-V_{OH} = 0.01V, and V_{OL} = 0.01V.

$$P_{S(max)} = V_{CC}I_{CC(max)} = 5 \cdot 40\mu A = 800\mu A \quad (7)$$

$$P_{LRN} = D_o(V_{CC} - V_{OH})\left(\frac{V_{OH}}{R_{PD}}\right) = 0.5(0.01)\left(\frac{4.99}{500k\Omega}\right) = 49.9nW \quad (8)$$

$$P_{LRP} = (1 - D_o)(V_{OL})\left(\frac{V_{CC} - V_{OL}}{R_{LP}}\right) = (1 - 0.5)(0.01)\left(\frac{5 - 0.01}{500k\Omega}\right) = 49.9nW \quad (9)$$

The total power consumption for all static sources is less than 1mW in this application. Rounding to 1mW and selecting the worst-case package selection for power dissipation, PW (TSSOP), we can calculate the temperature rise from this power consumption (1mW) and the given $R_{\theta JA}$ of 126.2°C/W given in the data sheet. The power consumption of 1mW and related thermal resistance value result in a temperature rise of less than 0.13°C, or in other words, a negligible amount. To be clear, the above calculations are not necessary for normal applications due to the small impact of those power values, but are included here for completeness and to demonstrate the reason static power consumption can be ignored in most applications for CMOS logic devices.

Moving on to the dynamic power dissipation, there is more power consumption. The C_{pd} value is taken from the data sheet as 45pF.

$$P_T = V_{CC}^2 C_{pd} f_i N_{SW} = 5^2 \cdot 45p \cdot 10M \cdot 8 = 90mW \quad (10)$$

$$P_{LC} = V_{CC}^2 C_L f_o N_{SW} = 5^2 \cdot 56p \cdot 10M \cdot 8 = 112mW \quad (11)$$

Together, these two values give 202mW, which is a considerable amount of power consumption. Given these numbers, the device has a temperature increase in the PW package of approximately 25.5C (0.202W × 126.2°C/W = 25.49°C).

$$T_{J(min)} = T_{A(min)} + P_{TOTAL}R_{\theta JA} = -40 + 25.5 = -14.5°C \quad (12)$$

$$T_{J(max)} = T_{A(max)} + P_{TOTAL}R_{\theta JA} = 125 + 25.5 = 150.5°C \quad (13)$$

Given that the junction temperature has a maximum of 150°C and the device has an ambient operating temperature maximum of 125°C, the SN74AC244 is capable of running at this power level across almost all of the entire ambient operating temperature range. At the high end, the device is limited to 124.5°C to avoid exceeding the maximum junction temperature of 150°C.

Repeating the above calculations for the DGS package ($R_{\theta JA}$ = 123.5°C/W), provides a temperature increase of 24.9°C, resulting in $T_{J(max)}$ of 149.9°C. The temperature increase indicates slightly better thermal performance of the DGS package, and the ability to use the device across the full temperature range in this application.

Application 1: Bench testing

In our experiments, we can only measure the case temperature of the device, and thus the junction temperature must be calculated from the experimental data. The PCBs used for this experiment are from the 14-24-LOGIC-EVM. These boards are not optimized for thermal conductivity per the application report *Semiconductor and IC Package Thermal Metrics*, but do represent a typical two-layer board design.

From the application report *Semiconductor and IC Package Thermal Metrics* , "$R_{\theta JA}$ is a variable function of not just the package, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the part is mounted. In effect, the test board is a heat sink that is soldered to the leads of the device. Changing the design or configuration of the test board changes the efficiency of the heat sink and therefore the measured $R_{\theta JA}$."

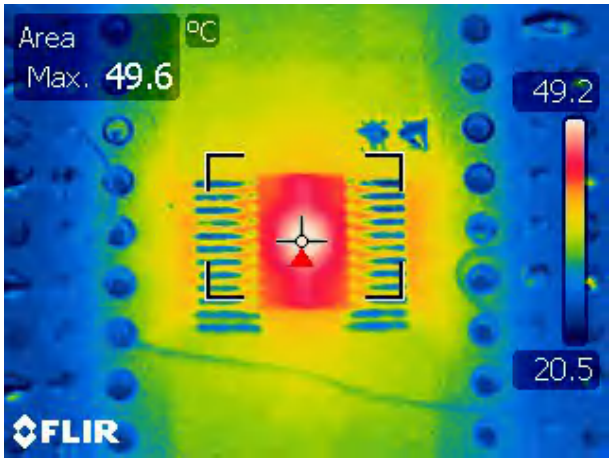

Figure 3. Thermal image of PW package operating at 10MHz, 5V supply, 8 channels switching with 56pF load each

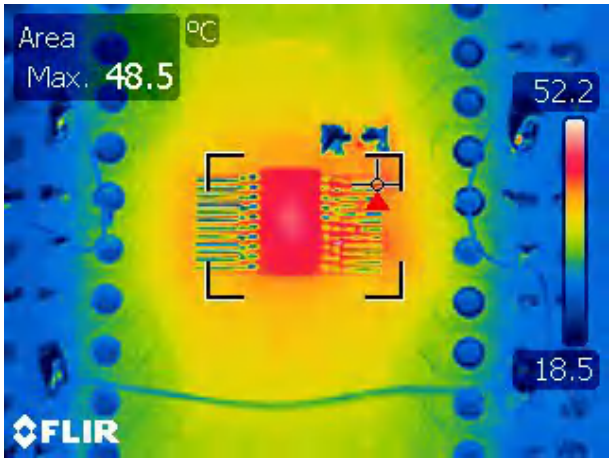

Figure 4. Thermal image of DGS package operating at 10MHz, 5V supply, 8 channels switching with 56pF load each

$$T_J = T_C + \psi_{JT} P_{TOTAL} \quad (14)$$

The operating junction temperature can be calculated from the measured case temperature using Equation 14. The temperature of each package was measured under the previously calculated conditions (T_A = 25°C, V_{CC} = 5V, f_{in} = 10MHz, C_L = 56pF, R_P = R_L = 500kΩ) and the values are provided in Table 1. The total calculated power consumption is 202mW for each case.

Table 1. Experimental Data for SN74AC244 in PW and DGS packages

	Measured Case Temperature (°C)	Ψ_{JT} (°C/W)	Calculated Junction Temp	Calculated Temperature Increase	Data sheet Specified $R_{\theta JA}$	Calculated Application Specific $R_{\theta JA}$
PW	49.6	22.3	53.8	28.8	126.2	151.8
DGS	48.5	7.8	50.0	25	123.5	131.5

There is a large discrepancy between the data sheet provided $R_{\theta JA}$ and the application specific $R_{\theta JA}$ for the PW package as calculated from this experiment. The discrepancy between data sheet calculated thermal resistance values and experimentally derived values is explained in detail in the application report *Semiconductor and IC Package Thermal Metrics* , however we can restate briefly here that the PCB design has an enormous impact on the thermal performance of a device, and this PCB is not optimized for thermal performance.

The core take-away from this experiment is that the DGS package provides significant space savings while also providing improved thermal conductivity. Additionally, the calculated temperature increase of 25.5°C based on the data sheet thermal specifications is close to the experimentally derived values of 28.8C and 25C, providing confirmation that calculated values are a valid method for thermal performance prior to board construction, even with non-ideal PCB design.

Application 2: Calculations

In this application, we again utilize the SN74AC244 and use the same conditions as those described in Application 1: Calculations . The difference from *Application 1* is the package and PCB. In this application, we utilize the RKS (WQFN) package and test one PCB with the thermal pad floating, and another PCB with the thermal pad connected to a ground plane per the data sheet recommendations.

See Application 1: Calculations for details, as the loading and power dissipation calculations are the same for this application.

The previously calculated power consumption was 202mW for this application. In the RKS package ($R_{\theta JA}$ = 67.7°C/W), the SN74AC244 has an expected temperature increase of approximately 13.7°C (0.202W × 67.7°C/W = 13.67°C) resulting in a junction temperature of 38.7°C at T_A = 25°C.

$$T_{J(min)} = T_{A(min)} + P_{TOTAL}R_{\theta JA} = -40 + 13.7 = -26.3°C \quad (15)$$

$$T_{J(max)} = T_{A(max)} + P_{TOTAL}R_{\theta JA} = 125 + 13.7 = 138.7°C \quad (16)$$

Given that the junction temperature has a maximum of 150°C and the device has an ambient operating temperature maximum of 125°C, the SN74AC244 is capable of continuously running at this power level across the entire ambient operating temperature range based on the calculated temperature increase.

Application 2: Bench testing

In our experiments, we can only measure the case temperature of the device, and thus the junction temperature must be calculated from the experimental data. One PCB used for this experiment was from the 14-24-LOGIC-EVM, while the other was a modified version to include vias connecting the thermal pad to ground while maintaining all other board features, stackup, and geometry. These boards are not optimized for thermal conductivity per the application report *Semiconductor and IC Package Thermal Metrics*, but do represent a typical two-layer board design.

From the application report *Semiconductor and IC Package Thermal Metrics* , "$R_{\theta JA}$ is a variable function of not just the package, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the part is mounted. In effect, the test board is a heat sink that is soldered to the leads of the device. Changing the design or configuration of the test board changes the efficiency of the heat sink and therefore the measured $R_{\theta JA}$."

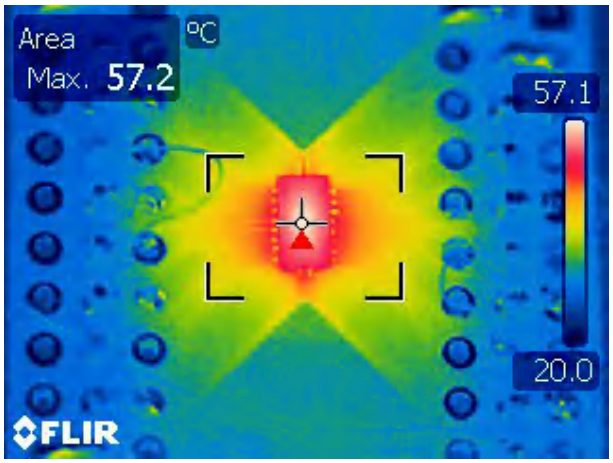

Figure 5. Thermal image of RKS package operating at 10MHz, 5V supply, 8 channels switching with 56pF load each with a floating thermal pad connection

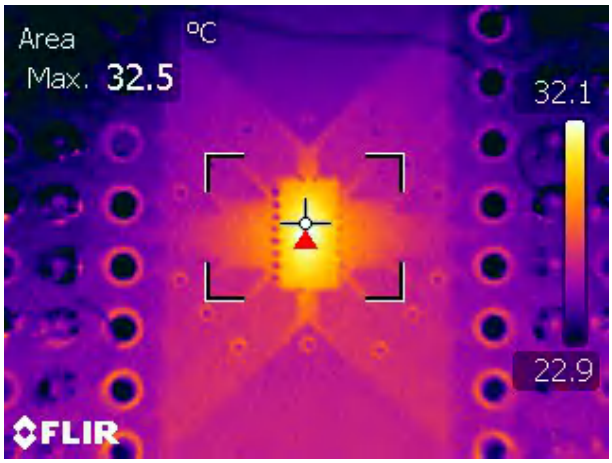

Figure 6. Thermal image of RKS package operating at 10MHz, 5V supply, 8 channels switching with 56pF load each with the thermal pad connected to a ground plane

The operating junction temperature can be calculated from the measured case temperature using Equation 14. The temperature of each package was measured under the previously calculated conditions (T_A = 25°C, V_{CC} = 5V, f_{in} = 10MHz, C_L = 56pF, R_P = R_L = 500kΩ) and the values are provided in Table 1. The total calculated power consumption is 202mW for each case.

Table 2. Experimental Data for SN74AC244 in RKS package

	Measured Case Temperature (°C)	Ψ_{JT} (°C/W)	Calculated Junction Temp (°C)	Calculated(1) Temperature Increase (°C)	Data sheet Specified $R_{\theta JA}$ (°C/W)	Calculated(2) Application Specific $R_{\theta JA}$ (°C/W)
RKS with floating thermal pad	57.2	10.3	59.3	34.3	67.7	169.7
RKS with grounded thermal pad	32.5	10.3	34.6	9.6	67.7	47.4

(1) Temperature increase from ambient, T_A = 25°C
(2) $R_{\theta JA}$ is calculated from $R_{\theta JA} = (T_J - T_A)/P_{TOTAL}$

As mentioned in the previous application, the PCB design has an enormous impact on the thermal performance of a device. The data provided shows that the thermal performance of the RKS package is drastically improved by connecting the thermal pad to an underlying ground plane per the data sheet recommendations. With good thermal design, the RKS package has excellent thermal characteristics and saves space over other package options.

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