# Phase Noise/Phase Jitter Performance of CDCM7005 at Various UMTS, CDMA-xx, and 802.16 Frequencies

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**ABSTRACT**

This application brief presents phase-noise data taken on Texas Instruments CDCM7005 jitter cleaner and synchronizer PLL. The phase noise performance of the CDCM7005 depends on the phase noise of the reference clock, VCXO clock, and the CDC7005 itself. This applications brief shows the phase noise performance of Texas Instruments clock synthesizer CDCM7005 at most popular UMTS, CDMA, and 802.16 frequencies. It helps the user in choosing the right clocking solution for their particular applications. These test results confirm that the CDCM7005 can provide clocks better than –145 dBc/Hz phase noises at 1-MHz offset from the carrier frequency. Low phase noise is required for most base station application such as UMTS, CDMAxx, and 802.16 and their derivatives as well as many other jitter stringent applications.

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# 1 Introduction

The CDCM7005 is a low phase noise/low jitter clock synthesizer and jitter cleaner with programmable LVPECL and LVCMOS outputs. An external low-pass loop filter in addition to an external VCXO (VCO) is required to complete the phase locked loop circuitry. Proper selection of the VCXO and loop bandwidth is critical to achieve the best performance from the CDCM7005. A loop bandwidth calculator is available on Texas Instruments website (www.ti.com).

This report includes phase noise plots of most common frequencies used in base station and customer premise equipment (CPE) applications. In addition, the phase noise of the clock source feeding the CDCM7005 is included for completeness.

The phase noise of the 10-MHz reference, the various Toyocom's VCXOs (TCO-2111), and output phase noise of the CDCM7005 are included. The peak-to-peak and the RMS jitter were calculated from the phase noise plots over a frequency band of interest using the PN9000 phase noise measurement system. In addition, additive phase jitter of the CDCM7005 is included. The jitter data is taken with a Toyocom's 245.76-MHz VCXO and a divided ratio of this frequency. This data illustrates the jitter performance of the CDCM7005 alone and precludes jitter contributions of external clock reference and the VCXO being used. Additive time/phase jitter plots are shown in Figure 13.

## *1.1 Definitions*

**The timing budget** is defined by dynamic (jitter) and static errors (skew). Depending on the system architecture, a sub-set of parameters out of the data sheet is only affecting the timing budget. Jitter is a timing distribution of the clock signal and expresses the edge deviation from ideal. Jitter is composed of both deterministic and random (Gaussian) content.

**Jitter** is any edge deviation from the ideal. The causes of jitter include: power supply noise, thermal and mechanical noise from the input signal, reflection, EMI, and random noise. A few suggestions for reducing jitter include: power supply bypassing (10-47 μF) to prevent voltage droop and ripple due to current surges, filtering each VCC pin (w/ 0.1 μF) low effective series resistance capacitor, using proper termination, using differential signaling as opposed to single-ended signaling, and minimizing noise coupling by isolating other high frequency signals from the clock driver.

**Phase Noise (PN)** is the short-term instability caused by variation of frequency (phase) of a signal referenced to the carrier level and a function of the carrier offset (i.e., relative noise level within a 1-Hz bandwidth). Integration of PN over a given frequency band yields phase jitter RMS.

**Phase jitter or accumulated jitter** is the absolute deviation of a clock edge from its ideal position in timing. While period jitter only accounts for the variation between clock periods, phase jitter accumulates the error of each period and therefore is always larger. The wider the recording time window is, the more frequency bandwidth becomes integrated into the total phase jitter. Phase jitter can also be measured by integrating phase noise over the frequency band of interest. Either way, the system designer must specify the minimum and maximum frequency for the integration.

For set-up and hold-time budget calculation, the PP value of the phase jitter is important. Note that only the added phase noise by the clock driver is of interest to find the worse edge position between the master clock in the system and the subsystem. The absolute phase jitter of the master clock itself adds to all clock signals in the system, thus canceling its effect.

**Period jitter** is the deviation in cycle time of a signal with respect to an ideal period over a random sample of cycles. Period jitter is important since it includes the max/min frequency and it specifics the shortest clock period. It is important for the set-up and hold-time budget. Calculation with period jitter is sufficient for sub-systems using clock and data signals derived by the same clock source. Use phase jitter to calculate your jitter budget in case a signal comes into such subsystem from an external clock source (e.g., use of ADC, SerDes) or is generated from the clock source that feeds the clock buffer of interest. Period jitter can be measured with any oscilloscope. The trigger input and signal input both must be driven from the output of the clock driver.

**Peak-to-peak (PP) period jitter** is the total jitter range from minimum to maximum values of a clock signal. PP jitter increases indefinitely with recording time. Thus, PP jitter values are only meaningful if either the recording length or the relative bit error rate is known.

**RMS period jitter** is one standard deviation (1 $\sigma$) of the PP jitter of a clock signal. RMS jitter is only valid for Gaussian (normal) distribution. RMS jitter is independent of the sampling window, and thus, better suited to compare performance of two or more devices where sampling time window differs or is unknown.

**Cycle-to-cycle (CC) period jitter**, a.k.a. *adjacent cycle jitter*, is the variation in cycle time of a signal between consecutive cycles over a random sample of successive cycle pairs. CC jitter is also a good value to calculate the set-up and hold-time budget since it defines the min/max variation of the timing variation from ideal for the next clock edge.

**Crosstalk**, another name for parasitic coupling between signals, is the effect of capacitive coupling to cause a logic transition. Capacitive coupling is the transfer of energy between nearby switching integrated circuits. The coupling depends on factors such as the distance between the traces, the signal swing, the operating frequency, and the permittivity of the silicon dioxide. Coupling can be improved by physically increasing the distance between the traces. Power and ground planes can also act as shields to minimize crosstalk

### *1.2 ADC and SerDes System*

When using the AD converter and SerDes transceiver, the incoming data is often sourced by a completely independent clock source and not synchronized to the main system clock (at least no short-term synchronization). Thus, the absolute phase jitter becomes important. A lower frequency band limit must be established (e.g., 12 kHz to full range). For the AD converter, the limit on the low side relates to the sampling window of the ADC that becomes further processed by digital algorithms (e.g. DSP tap size for a FFT). For a SerDes PLL, low phase jitter is critical around the PLL's bandwidth. Thus, jitter frequency has an upper and low limit (e.g., 12 kHz–20 MHz for OC-48).

## 2 Test Equipment and Setup

All measurements were taken at nominal 3.3-V power supply, room temperature, and PLL lock condition. The CDCM7005 evaluation module (EVM) in 1x mode, various Toyocom's VCXOs, the Agilent E8257C signal generator and the PN9000 phase noise test system. The below test setup were used for the all phase noise testing. The phase noise can be measured up to 100 MHz from carrier frequency. Although some measurements were taken up to 10 MHz or 1 MHz from the carrier depending upon the desired clock frequency.

The PN9000 automatic phase noise test system from Aeroflex was used to measure the phase noise and the phase jitter was calculated from phase noise plots at various bandwidths.

Several CDCM7005 EVMs was used to take the output phase noise measurement.

All LVPECL and LVCMOS outputs were properly terminated. Figure 1 shows the test setup used for all phase noise testing.

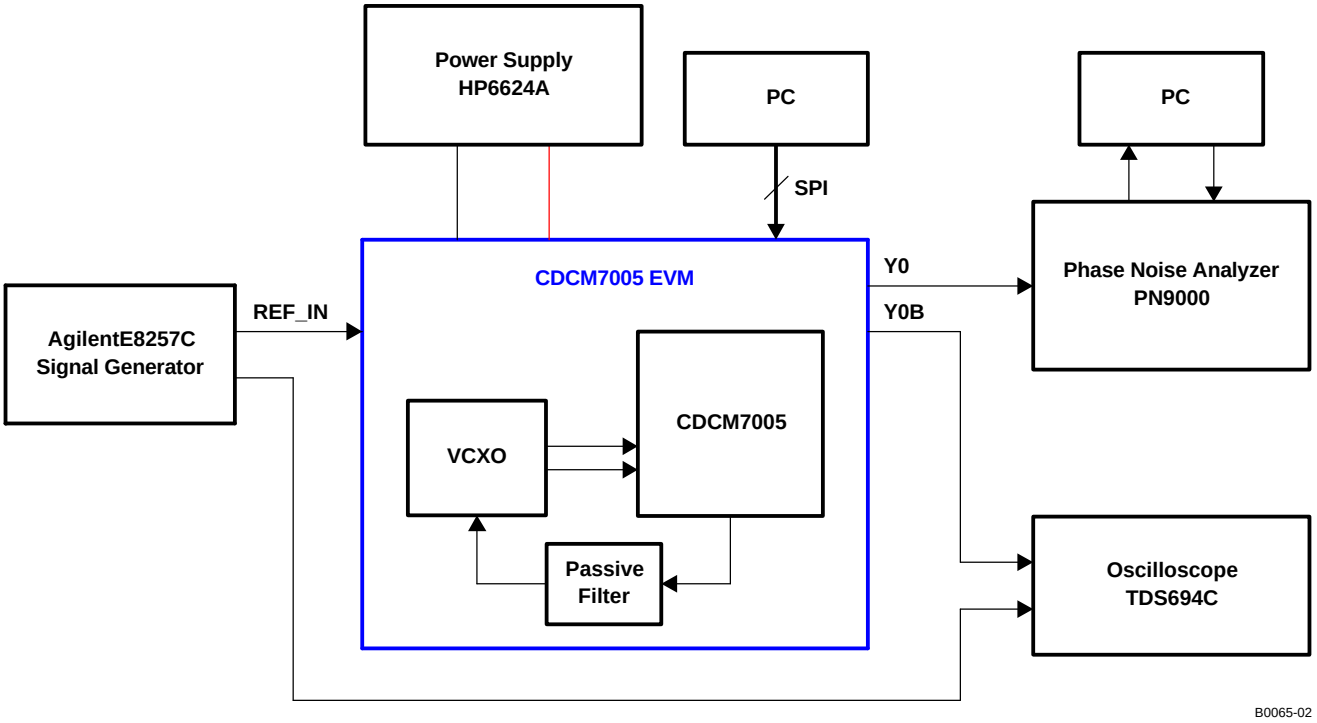



**Figure 1. Test Equipment Setup**

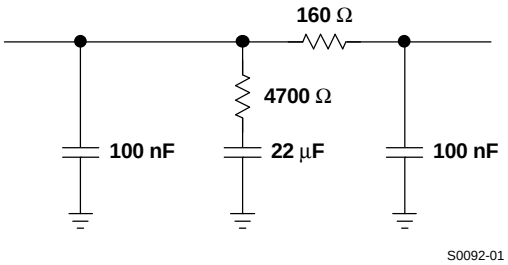



**Figure 2. Passive Loop Filter Circuit**

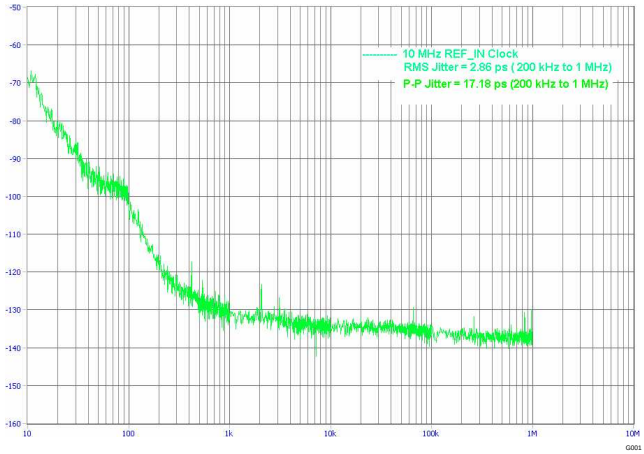



**Figure 3. Phase Noise Performance of Agilent E8257C 10MHz REF_IN**

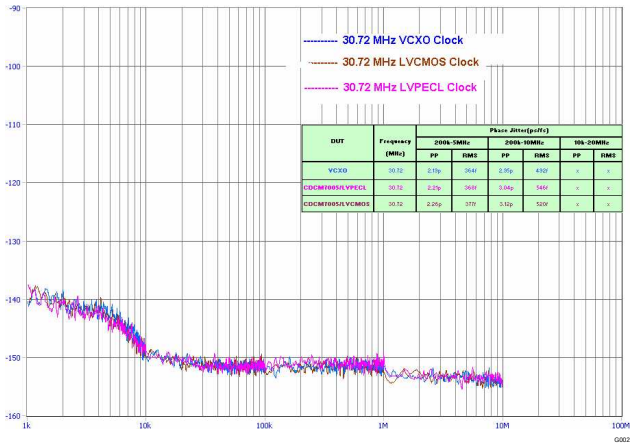
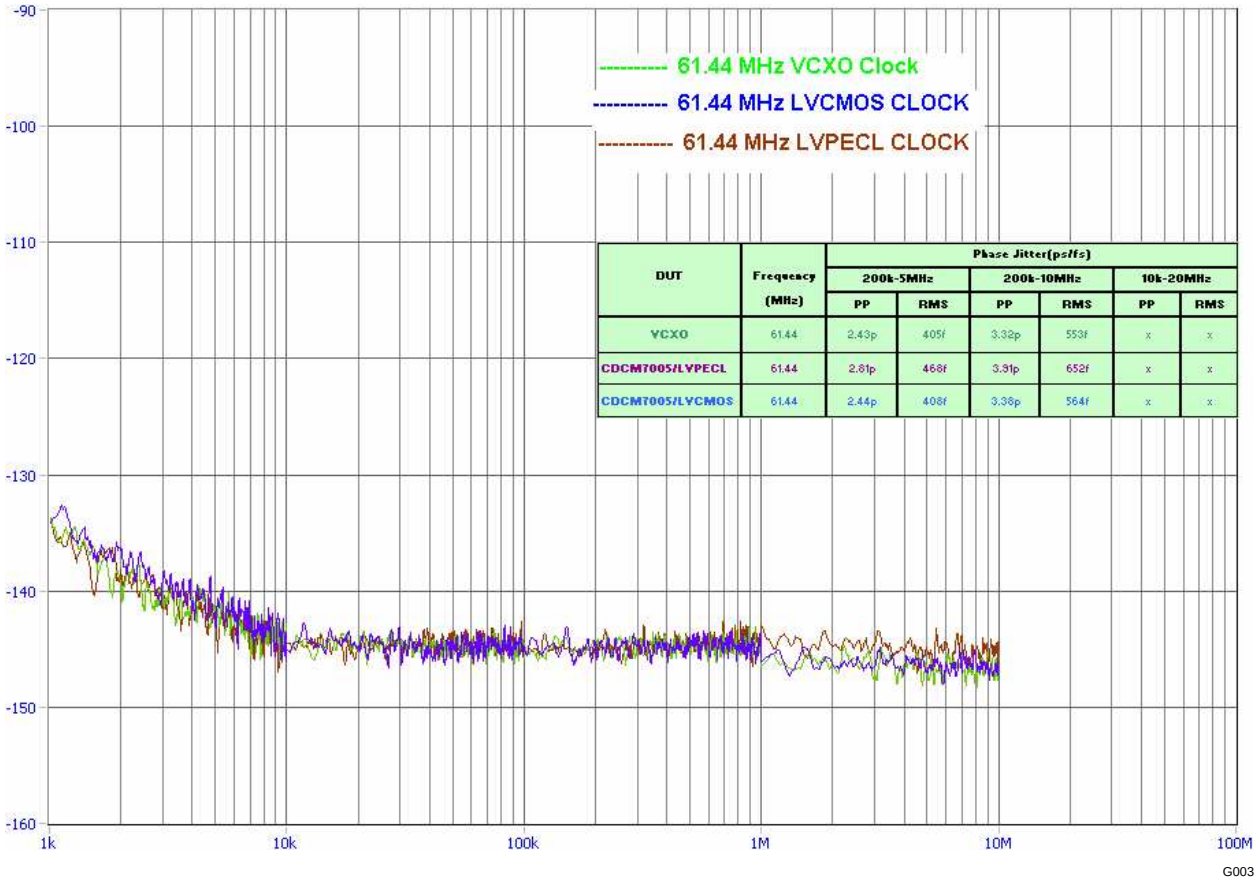
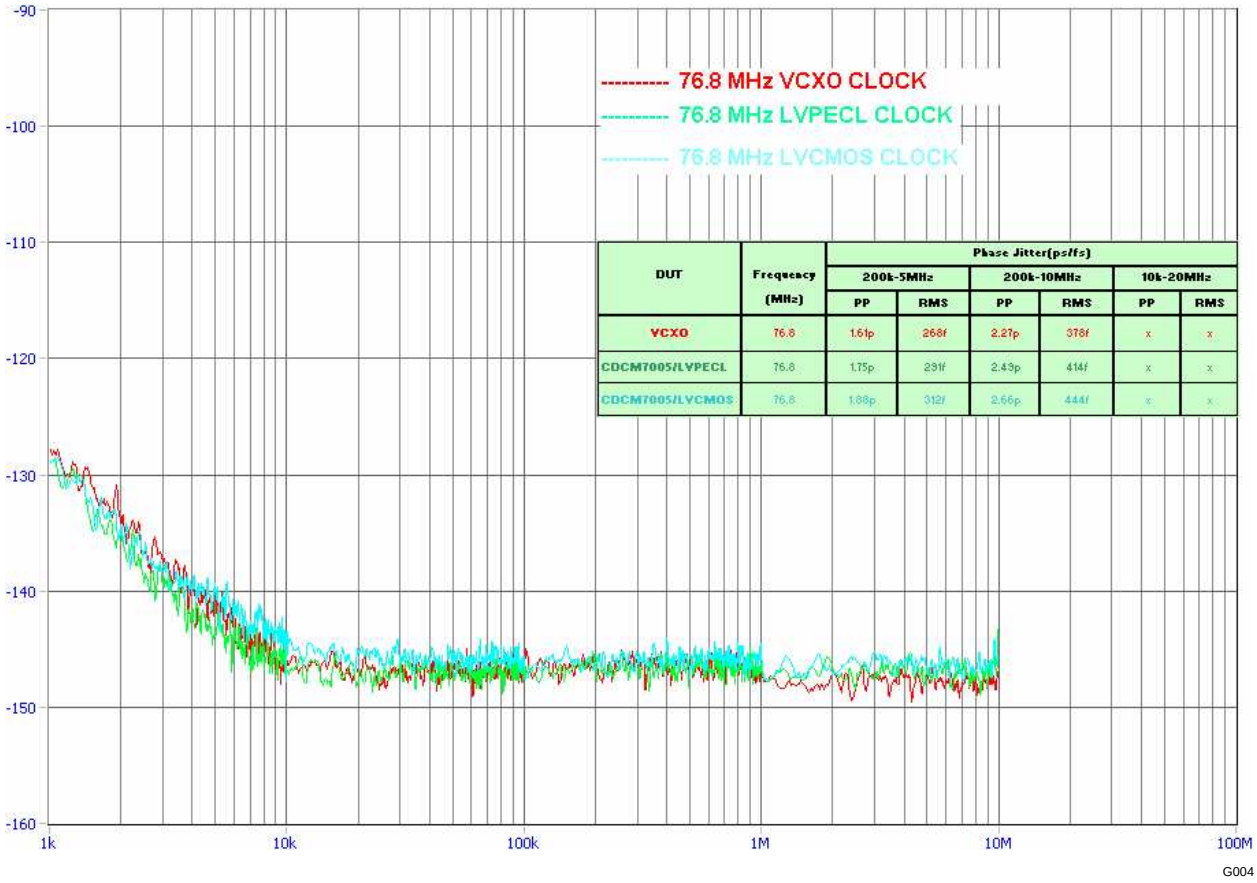



**Figure 4. Phase Noise Performance of CDCM7005 Outputs at 30.72 MHz**



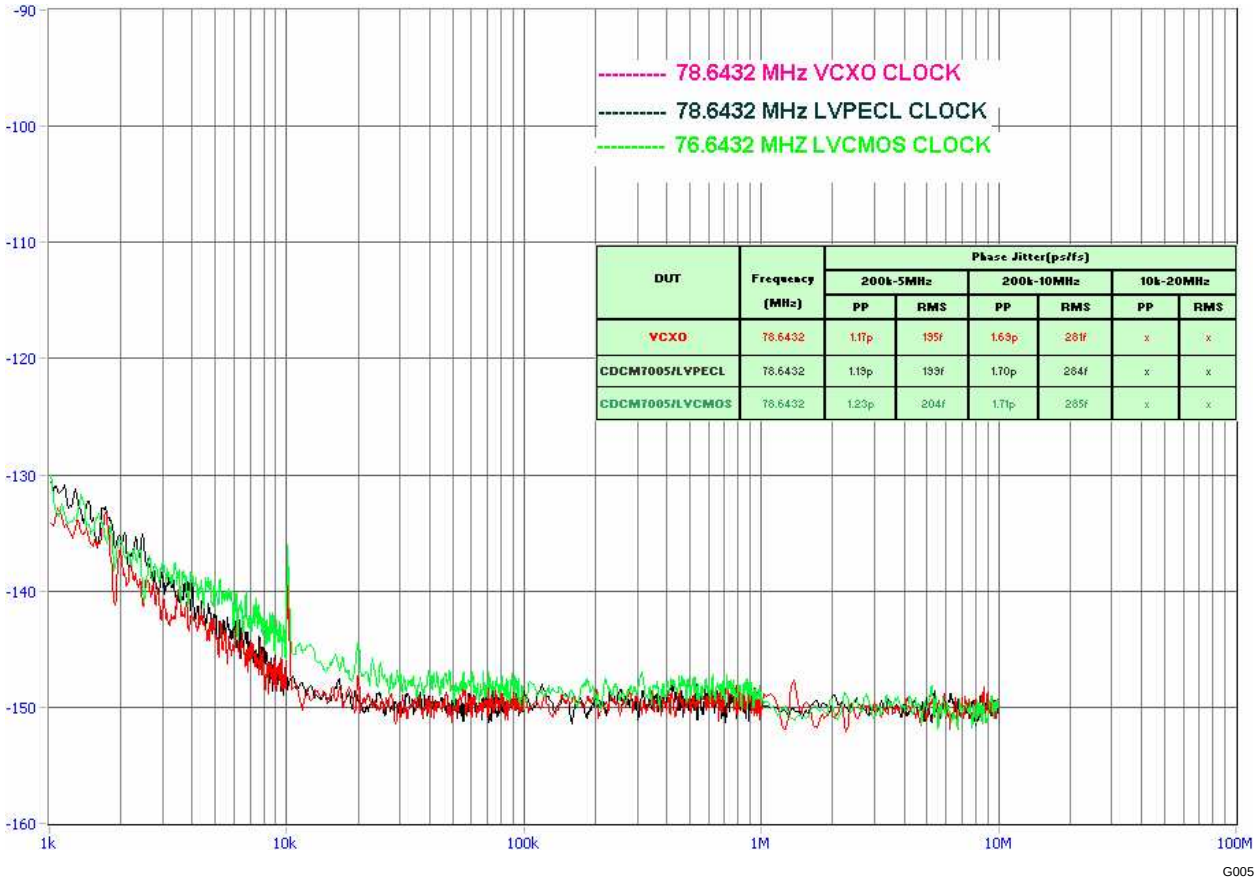

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 61.44 | 2.43p | 405f | 3.32p | 553f | x | x |
| CDCM7005/LVPECL | 61.44 | 2.81p | 468f | 3.91p | 652f | x | x |
| CDCM7005/LVCMOS | 61.44 | 2.44p | 408f | 3.38p | 564f | x | x |

**Figure 5. Phase Noise Performance of CDCM7005 Outputs at 61.44 MHz**



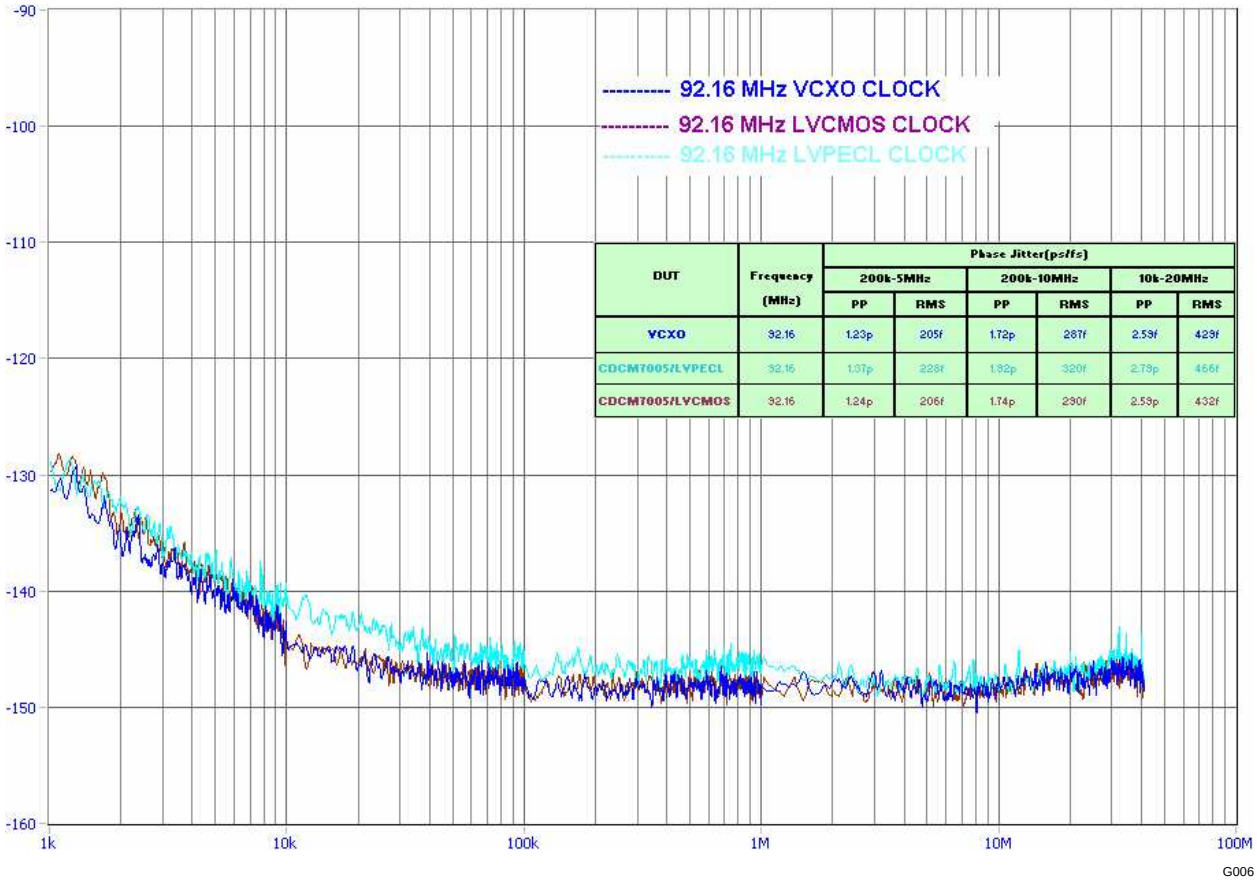

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 76.8 | 1.61p | 268f | 2.27p | 378f | x | x |
| CDCM7005/LVPECL | 76.8 | 1.75p | 291f | 2.43p | 414f | x | x |
| CDCM7005/LVCMOS | 76.8 | 1.88p | 312f | 2.66p | 444f | x | x |

**Figure 6. Phase Noise Performance of CDCM7005 Outputs at 76.80 MHz**



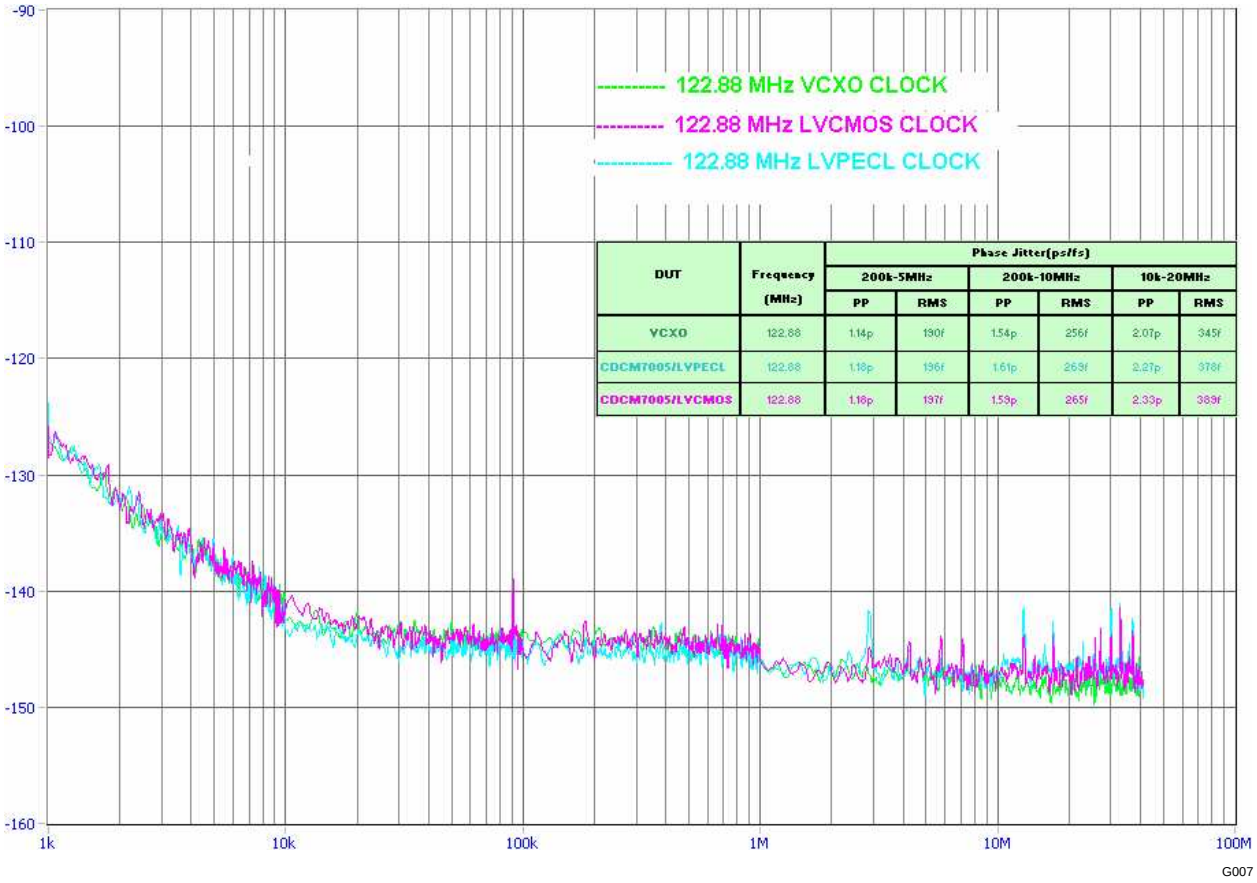

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 78.6432 | 1.17p | 195f | 1.63p | 281f | x | x |
| CDCM7005/LVPECL | 78.6432 | 1.13p | 193f | 1.70p | 284f | x | x |
| CDCM7005/LVCMOS | 78.6432 | 1.23p | 204f | 1.71p | 285f | x | x |

**Figure 7. Phase Noise Performance of CDCM7005 Outputs at 78.6432 MHz**



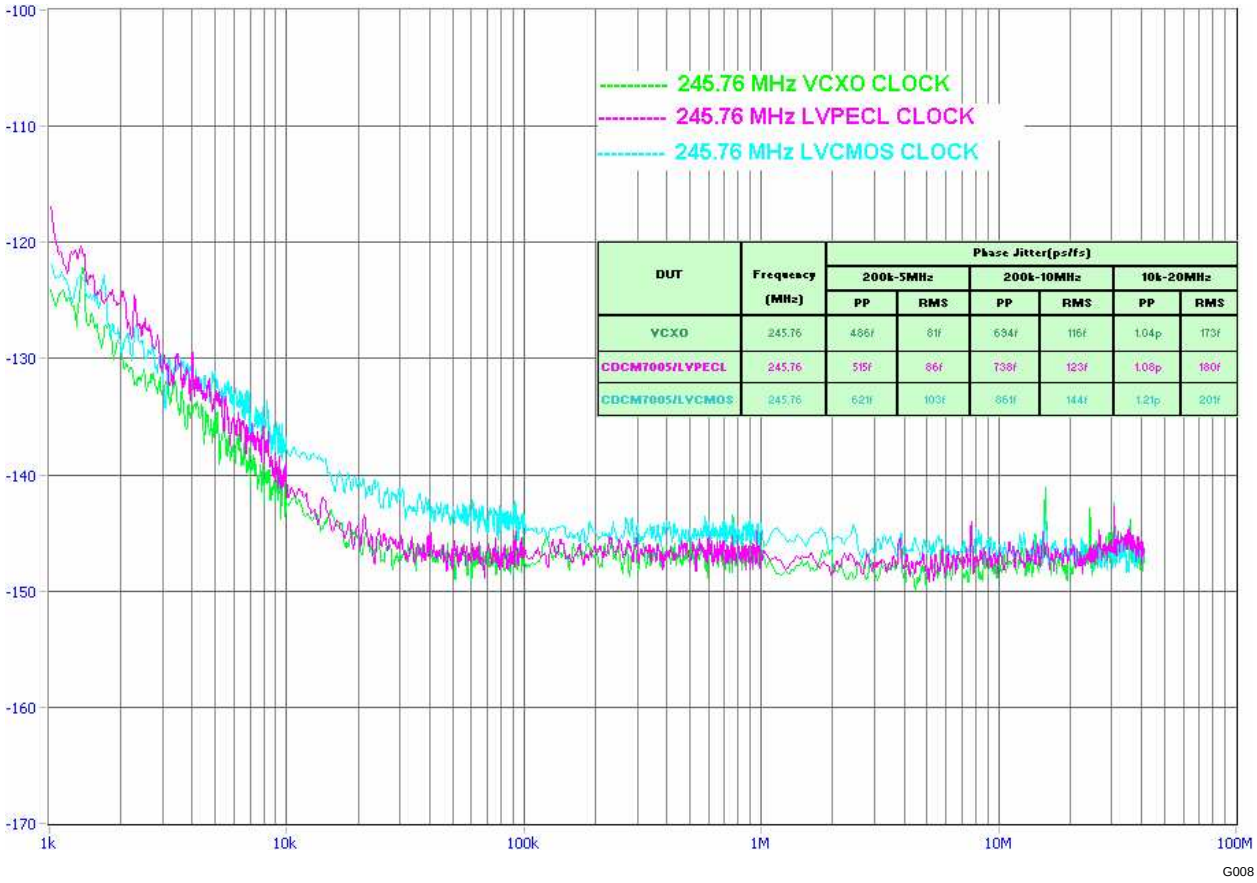

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 92.16 | 1.23p | 205f | 1.72p | 287f | 2.53f | 429f |
| CDCM7005/LVPECL | 92.16 | 1.37p | 228f | 1.92p | 320f | 2.79p | 466f |
| CDCM7005/LVCMOS | 92.16 | 1.24p | 206f | 1.74p | 290f | 2.53p | 432f |

**Figure 8. Phase Noise Performance of CDCM7005 Outputs at 92.160 MHz**



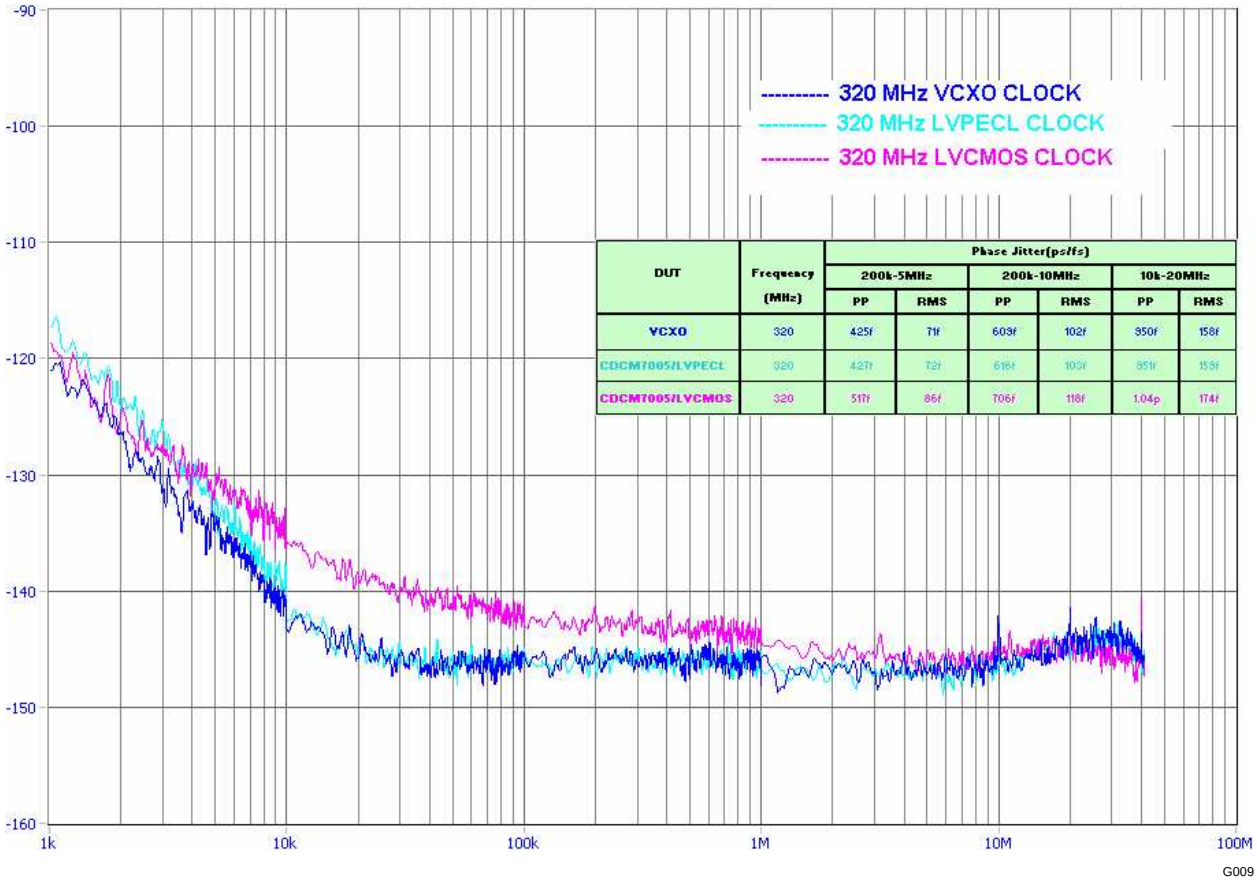

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 122.88 | 1.14p | 190f | 1.54p | 256f | 2.07p | 345f |
| CDCM7005/LVPECL | 122.88 | 1.18p | 196f | 1.61p | 269f | 2.27p | 378f |
| CDCM7005/LVCMOS | 122.88 | 1.16p | 197f | 1.59p | 265f | 2.33p | 389f |

**Figure 9. Phase Noise Performance of CDCM7005 Outputs at 122.88 MHz**



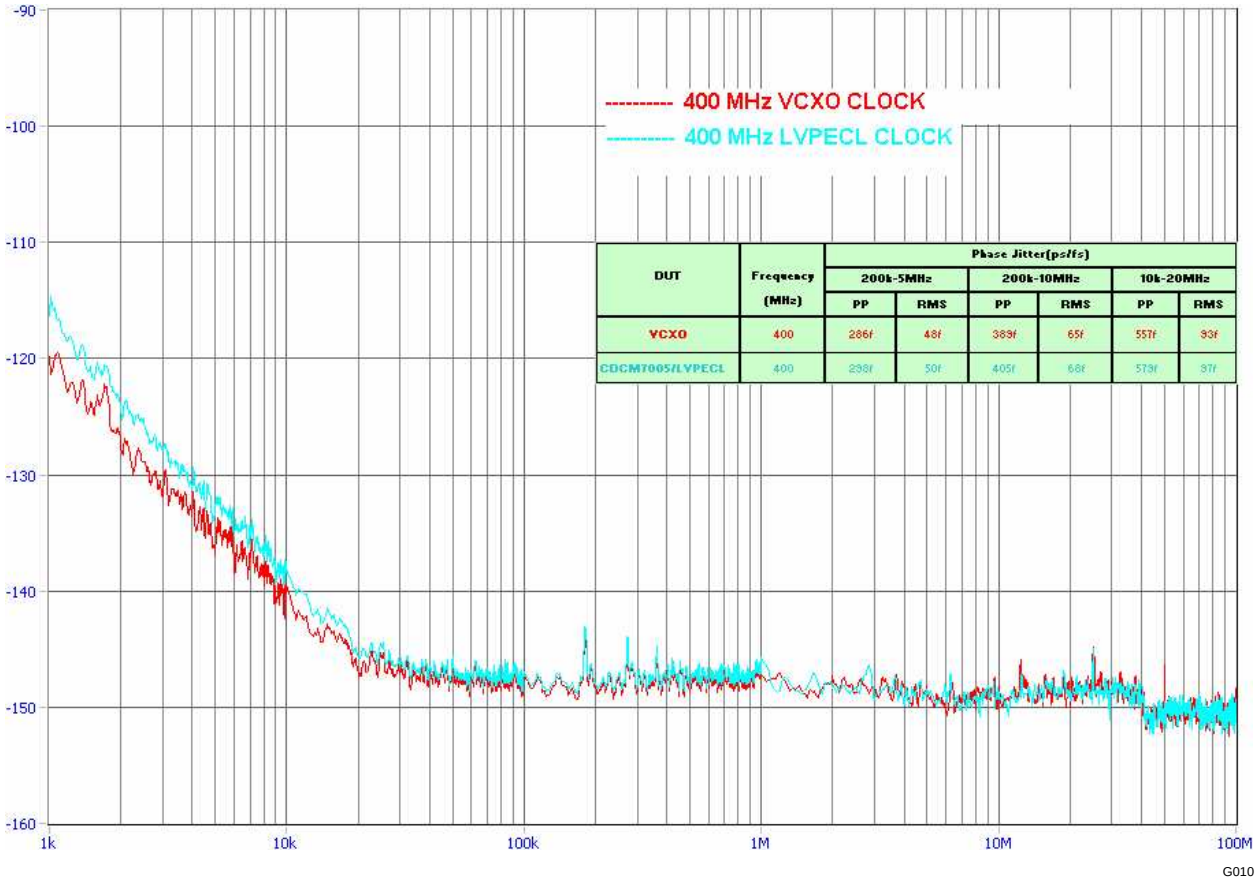

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 245.76 | 486f | 81f | 634f | 116f | 1.04p | 173f |
| CDCM7005/LVPECL | 245.76 | 515f | 86f | 738f | 123f | 1.08p | 180f |
| CDCM7005/LVCMOS | 245.76 | 621f | 103f | 861f | 144f | 1.21p | 201f |

**Figure 10. Phase Noise Performance of CDCM7005 Outputs at 245.76 MHz**



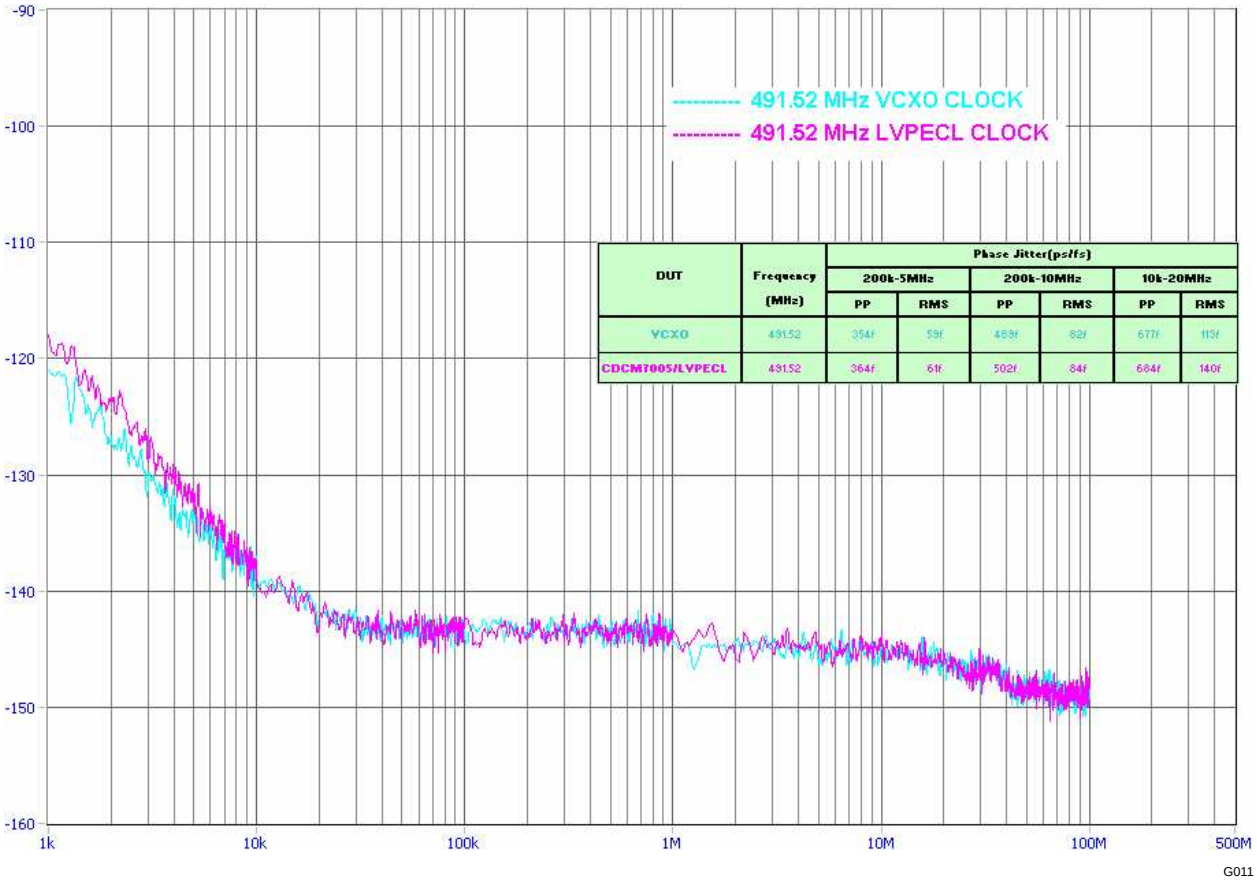

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 320 | 425f | 71f | 603f | 102f | 350f | 158f |
| CDCM7005/LVPECL | 320 | 427f | 72f | 616f | 103f | 351f | 159f |
| CDCM7005/LVCMOS | 320 | 517f | 86f | 706f | 118f | 1.04p | 174f |

**Figure 11. Phase Noise Performance of CDCM7005 Outputs at 320 MHz**



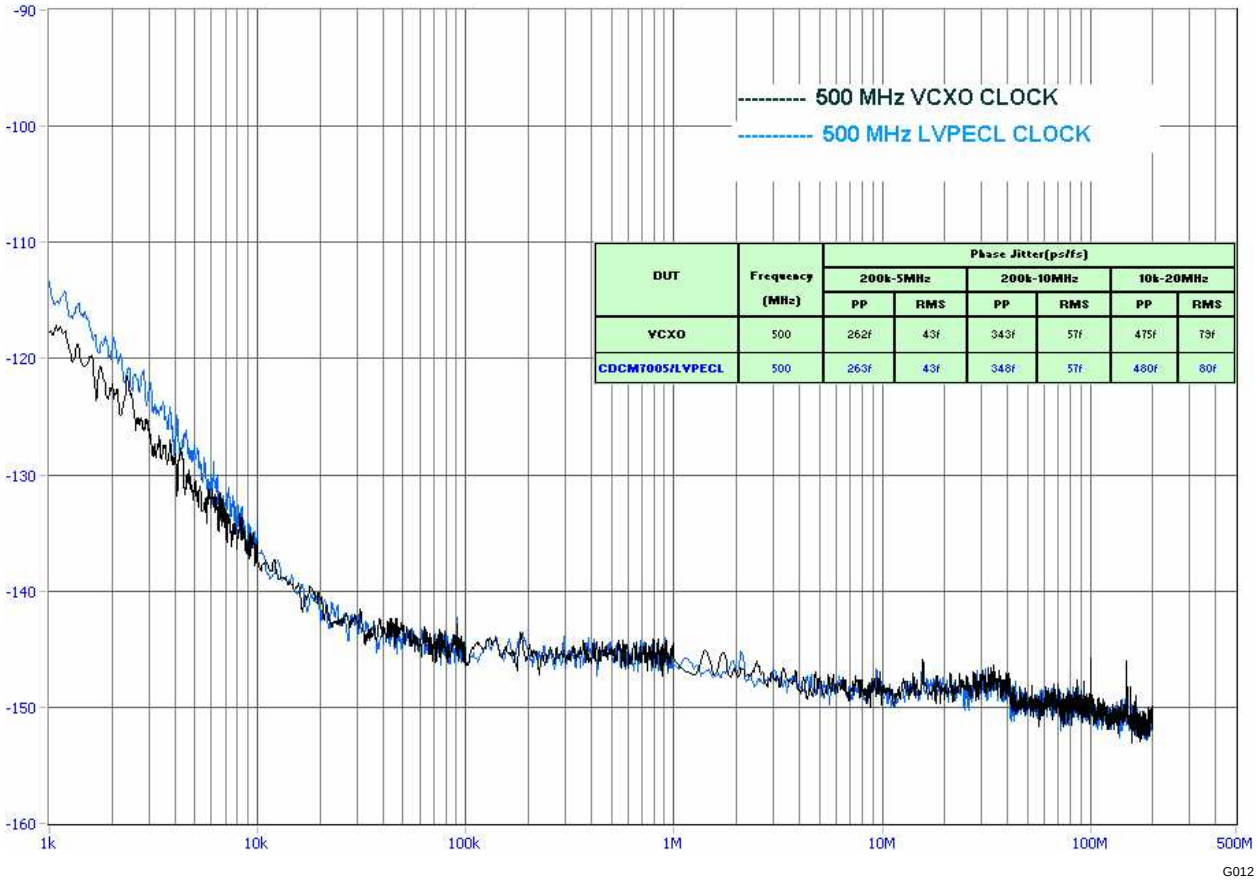

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 400 | 286f | 48f | 389f | 65f | 557f | 93f |
| CDCM7005/LVPECL | 400 | 298f | 50f | 405f | 68f | 573f | 97f |

**Figure 12. Phase Noise Performance of CDCM7005 Outputs at 400 MHz**



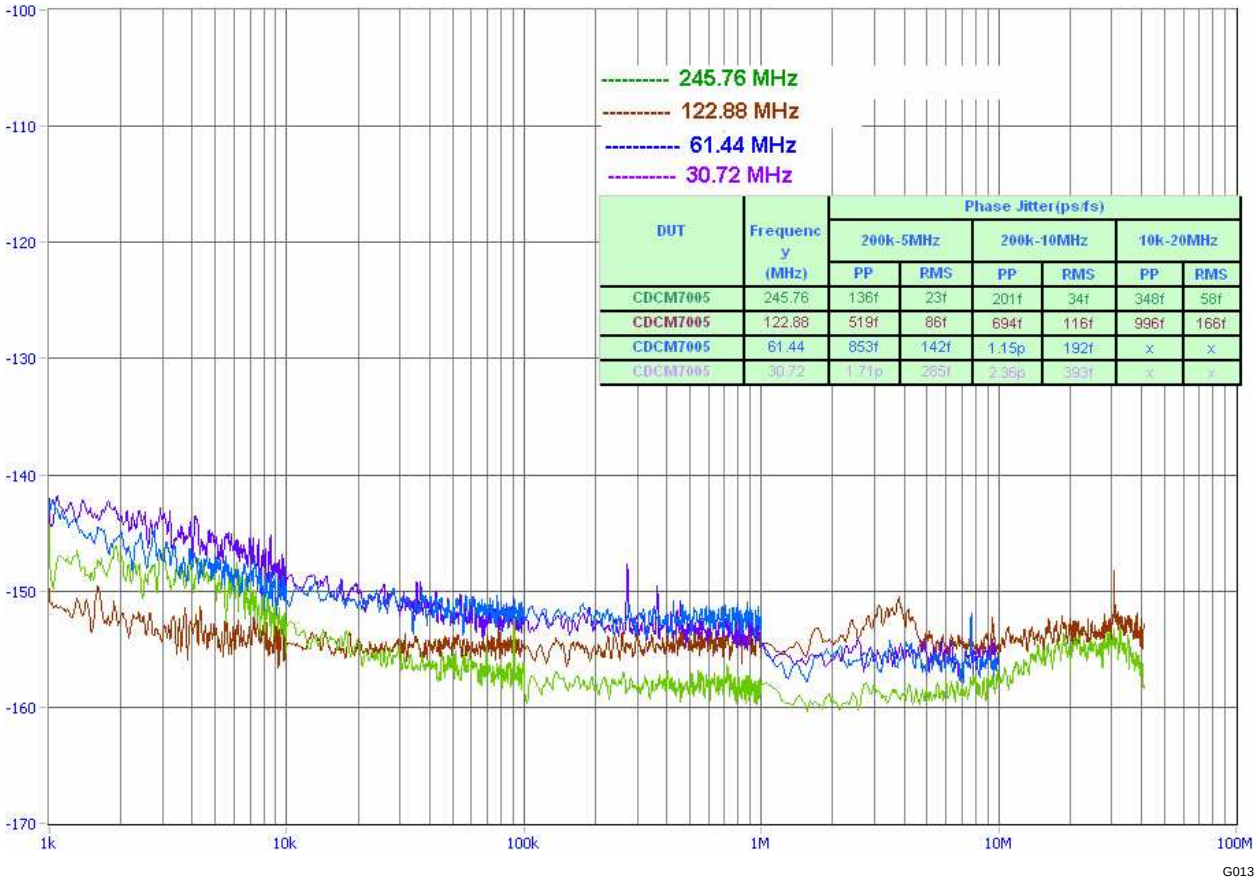

| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 491.52 | 354f | 59f | 489f | 82f | 677f | 113f |
| CDCM7005/LVPECL | 491.52 | 364f | 61f | 502f | 84f | 684f | 140f |

**Figure 13. Phase Noise Performance of CDCM7005 Outputs at 491.52 MHz**




| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| VCXO | 500 | 262f | 43f | 343f | 57f | 475f | 79f |
| CDCM7005/LVPECL | 500 | 263f | 43f | 348f | 57f | 480f | 80f |

**Figure 14. Phase Noise Performance of CDCM7005 Outputs at 500 MHz**




| DUT | Frequency (MHz) | Phase Jitter(ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200k-5MHz | | 200k-10MHz | | 10k-20MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| CDCM7005 | 245.76 | 136f | 23f | 201f | 34f | 348f | 58f |
| CDCM7005 | 122.88 | 519f | 86f | 694f | 116f | 996f | 166f |
| CDCM7005 | 61.44 | 853f | 142f | 1.15p | 192f | x | x |
| CDCM7005 | 30.72 | 1.71p | 285f | 2.36p | 393f | x | x |

**Figure 15. Additive Phase Noise Performance of CDCM7005 LVPECL Output at 245.76 MHz (Buffer Mode)**

**Table 1. Additive Phase Jitter (CDCM7005 Jitter Contribution Without REF and VCXO)**

| DUT | FREQUENCY (MHz) | PHASE JITTER (ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200 kHz – 5 MHz | | 200 kHz – 10 MHz | | 10 kHz – 20 MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| CDCM7005 | 245.76 | 136 | 23 | 201 | 34 | 348 | 58 |
| CDCM7005 | 122.88 | 519 | 86 | 694 | 116 | 996 | 166 |
| CDCM7005 | 61.44 | 853 | 142 | 1.15p | 192 | x | x |
| CDCM7005 | 30.72 | 1.71p | 285 | 2.36p | 393 | x | x |

**Table 2. Summary of Phase Jitter Measurements Across Various Frequencies**

| DUT | FREQUENCY (MHz) | PHASE JITTER (ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200 kHz – 5 MHz | | 200 kHz – 10 MHz | | 10 kHz – 20 MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| Agilent E8257C Sig Gen | 10 | 17.18p(1) | 2.68p(1) | x | x | x | x |
| **VCXO** | **30.72** | **2.19p** | **364** | **2.95p** | **492** | **x** | **x** |
| CDCM7005/LVPECL | 30.72 | 2.21p | 368 | 3.04p | 546 | x | x |
| CDCM7005/LVCMOS | 30.72 | 2.26p | 377 | 3.12p | 520 | x | x |

(1) This data is taken from 200 kHz to 1 MHz.

**Table 2. Summary of Phase Jitter Measurements Across Various Frequencies (continued)**

| DUT | FREQUENCY (MHz) | PHASE JITTER (ps/fs) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 200 kHz – 5 MHz | | 200 kHz – 10 MHz | | 10 kHz – 20 MHz | |
| | | PP | RMS | PP | RMS | PP | RMS |
| **VCXO** | **61.44** | **2.43p** | **405** | **3.32p** | **553** | **x** | **x** |
| CDCM7005/LVPECL | 61.44 | 2.81p | 468 | 3.91p | 652 | x | x |
| CDCM7005/LVCMOS | 61.44 | 2.44p | 408 | 3.38p | 564 | x | x |
| **VCXO** | **76.8** | **1.61p** | **268** | **2.27p** | **378** | **x** | **x** |
| CDCM7005/LVPECL | 76.8 | 1.75p | 291 | 2.49p | 414 | x | x |
| CDCM7005/LVCMOS | 76.8 | 1.88p | 312 | 2.66p | 444 | x | x |
| **VCXO** | **78.6432** | **1.17p** | **195** | **1.69p** | **281** | **x** | **x** |
| CDCM7005/LVPECL | 78.6432 | 1.19p | 199 | 1.70p | 284 | x | x |
| CDCM7005/LVCMOS | 78.6432 | 1.23p | 204 | 1.71p | 285 | x | x |
| **VCXO** | **92.16** | **1.23p** | **205** | **1.72p** | **287** | **2.59p** | **429** |
| CDCM7005/LVPECL | 92.16 | 1.37p | 228 | 1.92p | 320 | 2.79p | 466 |
| CDCM7005/LVCMOS | 92.16 | 1.24p | 206 | 1.74p | 290 | 2.59p | 432 |
| **VCXO** | **122.88** | **1.14p** | **190** | **1.54p** | **256** | **2.07p** | **345** |
| CDCM7005/LVPECL | 122.88 | 1.18p | 196 | 1.61p | 269 | 2.27p | 378 |
| CDCM7005/LVCMOS | 122.88 | 1.18p | 197 | 1.59p | 265 | 2.33p | 389 |
| **VCXO** | **245.76** | **486** | **81** | **694** | **116** | **1.04p** | **173** |
| CDCM7005/LVPECL | 245.76 | 515 | 86 | 738 | 123 | 1.08p | 180 |
| CDCM7005/LVCMOS | 245.76 | 621 | 103 | 861 | 144 | 1.21p | 201 |
| **VCXO** | **320** | **425** | **71** | **609** | **102** | **950** | **158** |
| CDCM7005/LVPECL | 320 | 428 | 71 | 616 | 103 | 951 | 159 |
| CDCM7005/LVCMOS | 320 | 517 | 86 | 706 | 117 | 1.04p | 174 |
| **VCXO** | **400** | **286** | **48** | **389** | **65** | **557** | **93** |
| CDCM7005/LVPECL | 400 | 298 | 50 | 405 | 68 | 579 | 97 |
| **VCXO** | **491.52** | **354** | **59** | **489** | **82** | **677** | **113** |
| CDCM7005/LVPECL | 491.52 | 364 | 61 | 502 | 84 | 684 | 140 |
| **VCXO** | **500** | **262** | **43** | **343** | **57** | **475** | **79** |
| CDCM7005/LVPECL | 500 | 263 | 43 | 348 | 57 | 480 | 80 |

## 3 Summary and Conclusion

The CDC7005 PLL tracks the input reference signal up to the loop bandwidth, while it follows the VCO (here VCXO) phase noise floor at frequencies above the loop bandwidth. The VCXO performance is critical for achieving good PLL's phase noise performance and meeting stringent requirements in base station applications. From the above data it is evident that a low phase noise clock output is easily attainable from the CDCM7005 with the proper selection of VCXO. These test results confirm that the CDCM7005 can provide clocks better than –145-dBc/Hz phase noises at 1-MHz offset from the carrier frequency. Low phase noise is required for most base station applications such as UMTS, CDMAxx, and 802.16 and their derivatives as well as many other jitter stringent applications.

The additive phase-noise data clearly indicates that as a buffer, the CDCM7005 adds a few femto-second jitter to its input. The added jitter number may vary over frequency. For more information about the CDCM7005, see the device data sheet.

## 4 Acknowledgement

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2. Paul Woodley, O&M Sales, Inc., Paul, Woodley@o-m-sales.com
3. Kory Moser, Toyocom USA, moser@toyocom.com
4. Heather McClendon, Texas Instruments, heather.mcclendon@ti.com

## 5 References

1. CDCM7005 data sheet, Texas Instruments, (SCAS685)
2. CDC7005 EVM User's Guide, Texas Instruments, (SCAU005)

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