Using TI's CDCV304 with Backplane Transceiver (TLK1201, TLK1501, TLK2201, TLK2501, TLK2701, TLK2711, and TLK3101)

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ABSTRACT

This application note discusses TI's CDCV304 output jitter when driving serial backplane transceivers, namely, TLK1201, TLK1501, TLK2201, TLK2501, TLK2701, TLK2711, and TLK3101. Measurement shows that the CDCV304 clock driver generates 20-ps p-p jitter on average; hence it is suitable to drive any serial backplane transceivers fulfilling all the requirements.

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Introduction

This application report discusses various jitter measurements of TI's CDCV304 clock driver. The CDCV304 is a 1:4 low-skew, low-jitter, single-ended LVTTL clock driver. The CDCV304 is characterized for industrial temperature (-40°C to 85°C) and has a maximum operating frequency of 140 MHz. The four output signals are low-skew, low-jitter copies of the input clock. These properties make the CDCV304 ideal for various datacom and telecom applications

Jitter Performance of CDCV304 (Driven by HP8133A Signal Generator)

TI's backplane transceivers require an input reference clock with maximum peak-to-peak jitter of 40 ps and of 40%–60% duty cycle. The worst-case output peak-to-peak jitter of the CDCV304 driver is less than 30 ps over a –40°C to 85°C range at nominal power supply. This characteristic makes the CDCV304 an excellent choice to drive a backplane transceiver at the specified clock frequency.

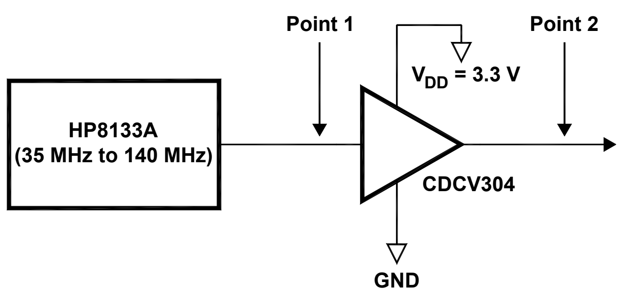

Figure 1. Indicates Various Jitter Measurement Points

Jitter measurements were taken at point 1 (output jitter of the signal generator and input jitter to the CDCV304 clock driver) and point 2 (output jitter of the HP8133A+CDCV304 combination and input jitter to the backplane transceiver). See Figures 2, 3, and 4 for results.

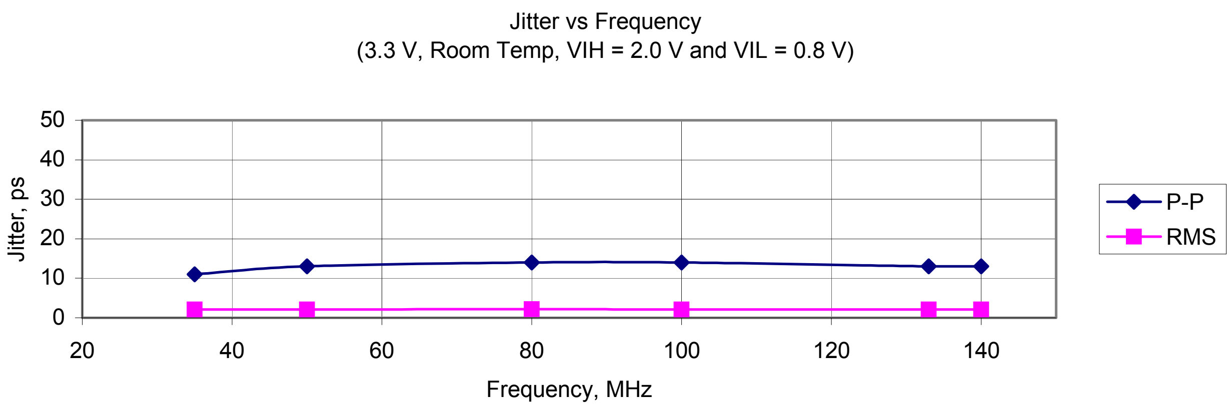

Figure 2. Peak-to-Peak and RMS Jitter of HP Signal Generator (Point 1)

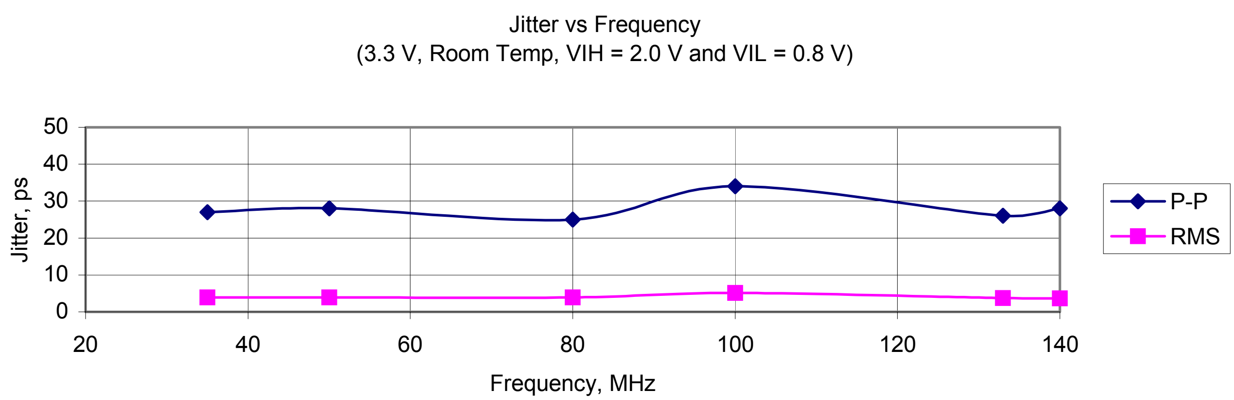

Figure 3. Peak-to-Peak and RMS Jitter of CDCV304 Driver Output (Point 2)

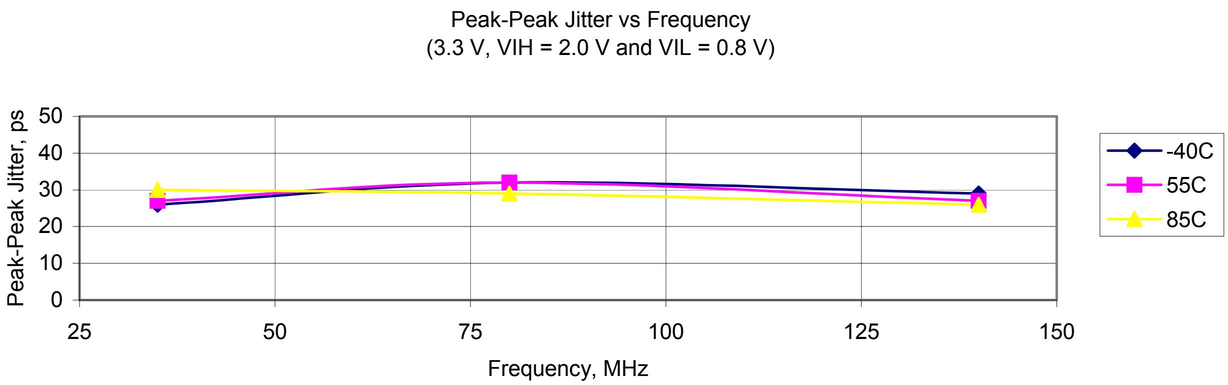

Figure 4. Peak-to-Peak Jitter of CDCV304 Driver Output (Point 2 Over Industrial Temperature Range)

Figure 4 shows that temperature has negligible impact on jitter performance of the CDCV304 clock driver.

Test Equipment Setup for Driving Backplane Transceiver

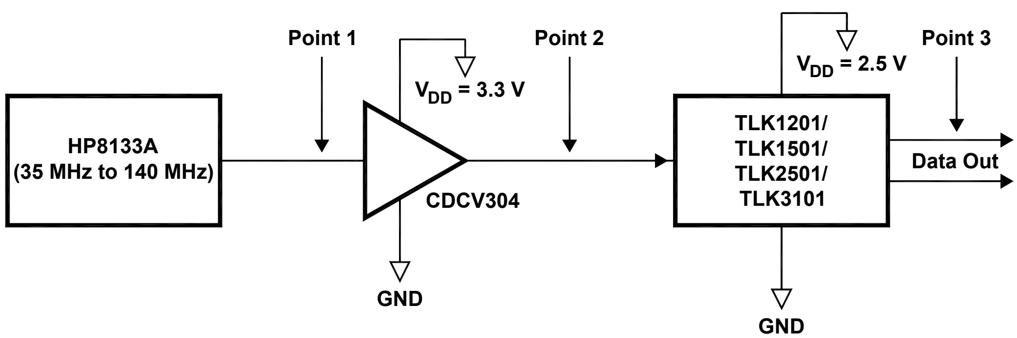

Figure 5. Test Equipment Setup

In this setup, the CDCV304 is used to provide the input clock for TI's backplane transceiver. The main objective of performing this experiment is to observe how TI's backplane transceiver performs when driven by the CDCV304 clock driver.

Recommended Termination for CDCV304 Clock Driver

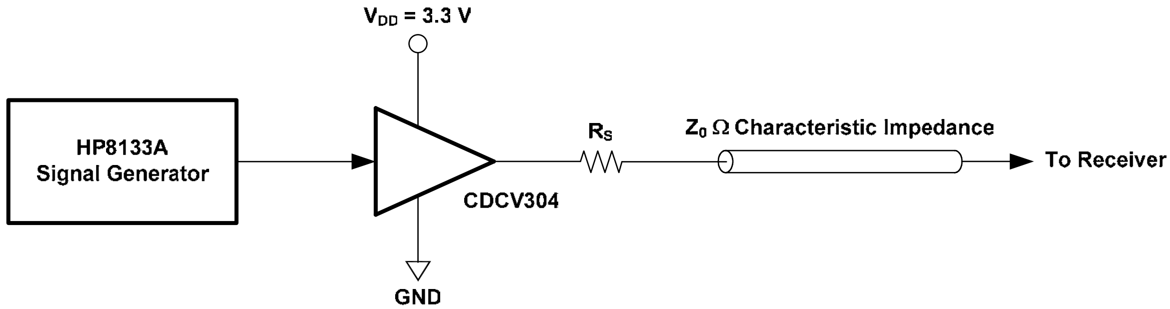

Figure 6. Series Termination for CDCV304 Clock Driver

Usually the value of the characteristic impedance (Z_0) lies between 50 Ω and 70 Ω.

Typical impedance for this LVCMOS output is 20 Ω.

Series termination (with a 30-Ω resistor) is recommended to terminate the driver outputs.

This clock driver can drive a 10-pF capacitive load. Because the input load of TI's backplane receiver is only 4 pF, the CDCV304 is capable of driving multiple loads of the backplane transceivers.

Test Summary

The following graphs (Figures 7, 8, 9, and 10) illustrate the worst case peak-to-peak and RMS jitter measurements taken at various points as indicated in Figure 5. Point 1 is the output jitter of the corresponding HP8133A frequencies. Point 2 is the output jitter of the CDCV304 when driven by the HP clock source. Point 3 is the output jitter at the end of the chain, where the transceiver is driven by the CDCV304 clock driver.

Jitter Performance of CDCV304 + TLK1201 Combination

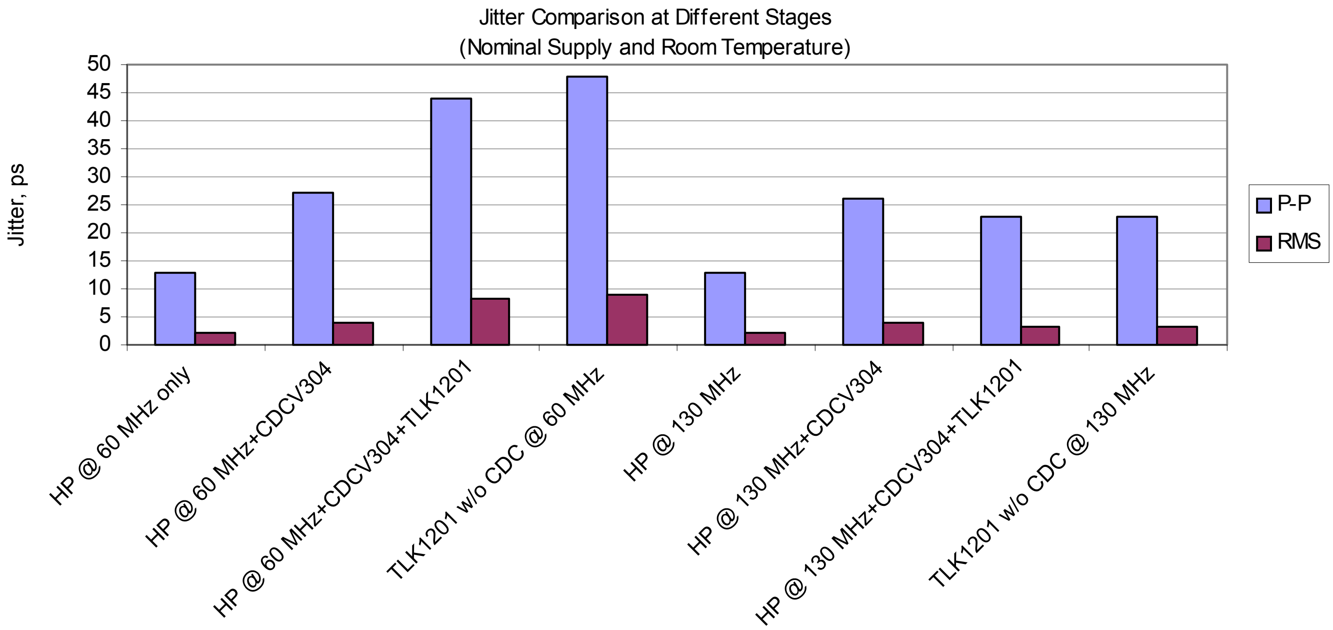

Figure 7. Jitter Values at Different Points Shown in Figure 5 With TLK1201

Jitter Performance of CDCV304 + TLK1501 Combination

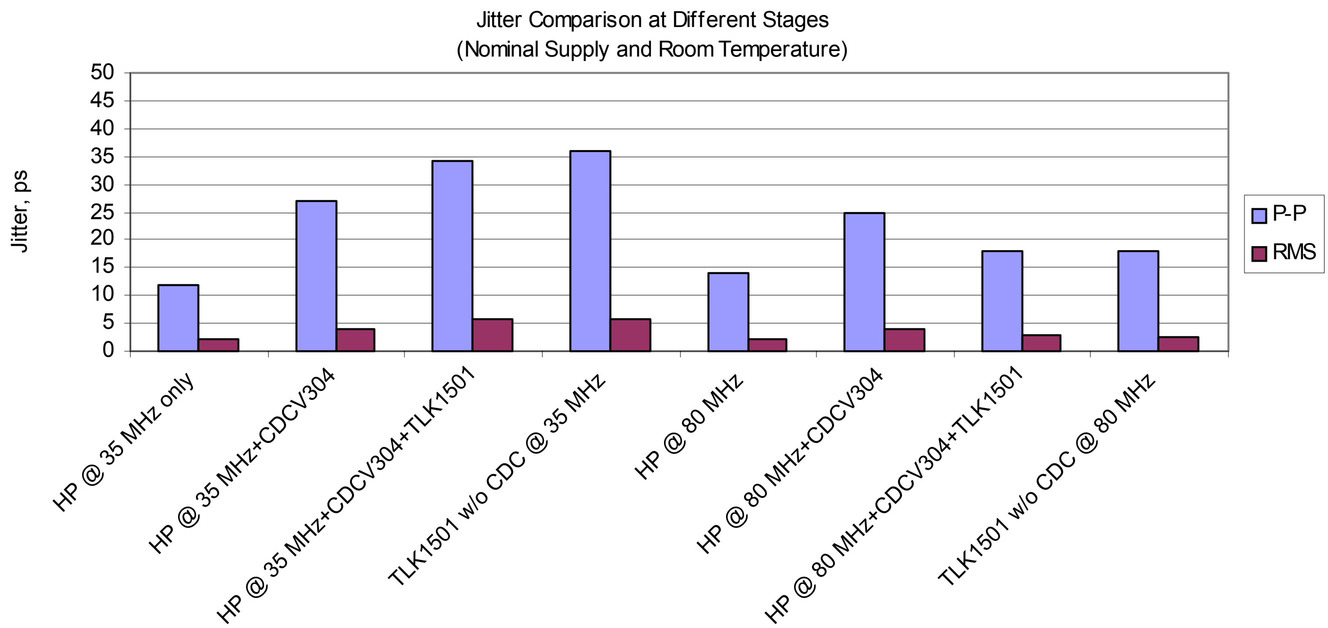

Figure 8. Jitter Values at Different Points Shown in Figure 5 With TLK1501

Jitter Performance of CDCV304 + TLK2501 Combination

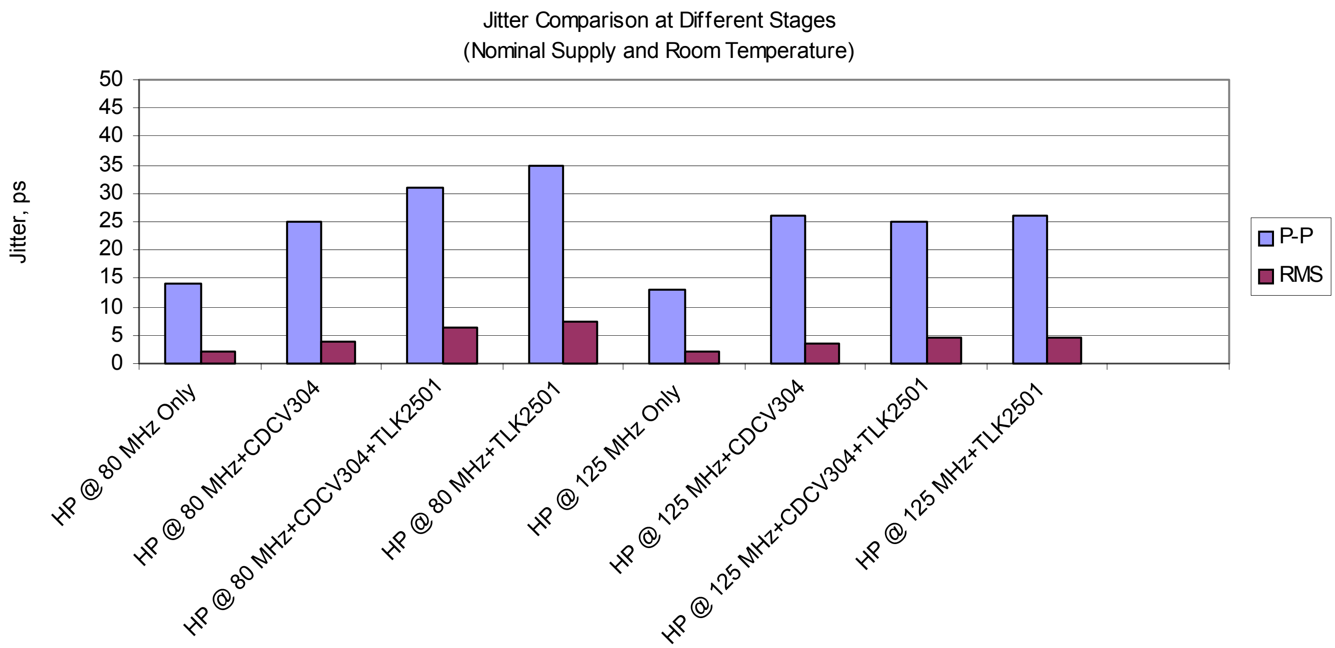

Figure 9. Jitter Values at Different Points Shown in Figure 5 With TLK2501

Jitter Performance of CDCV304 + TLK3101 Combination

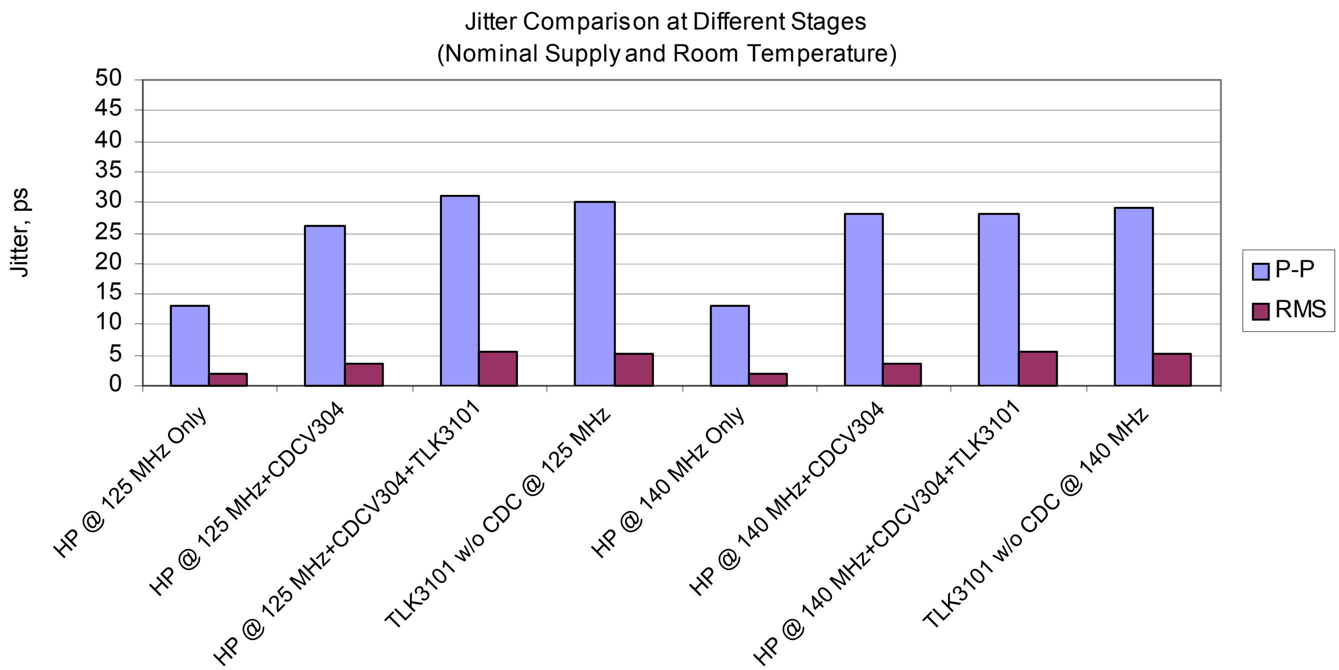

Figure 10. Jitter Values at Different Points Shown in Figure 5 With TLK3101

Conclusion

The graphs above show that the CDCV304 adds less than 20 ps of peak-to-peak jitter to its buffered outputs. The clock output jitter is less than 40 ps, which is the maximum jitter tolerance of the clock input of the aforementioned backplane transceivers, over the data-sheet-specified frequency and temperature range. Consequently, the CDCV304 clock driver satisfies all specified requirements for the input clock and can be used to drive any of these backplane transceivers.

Table 1. Recommended Clock Drivers for Serial / Gigabit Transceivers

Serial / Gigabit Transceiver	Recommended CDC Clock Drivers
SLK2501	CDCVF111 up to 622.08 MHz
	CDC111 up to 500 MHz
TLK3104A	CDC111 and CDCVF111
TLK3104SC	CDCVF111 up to 622.08 MHz
	CDC111 up to 500 MHz
TLK1201, TLK1501, TLK2201, TNETE2201B, TLK2501, TLK2701, TLK2711, TLK3101	CDCV304 up to 140 MHz
TLK3114SA	CDC111/CDCVF111

References

1. *CDCV304 140-MHz PCI-X Clock Buffer* data sheet, Texas Instruments, 2000 (SCAS643)
2. *Clock Distribution Circuits (CDC) Data Book*, Texas Instruments, 1999 (SCAD004)
3. *TLK1201RCP, TLK1201IRCP Ethernet Transceivers* data sheet, Texas Instruments, 2001 (SLLS506)
4. *TLK1501 0.6 to 1.5 Gbps Transceiver* data sheet, Texas Instruments, 2001 (SLLS428)
5. *TLK2201, TLK2201I Ethernet Transceivers* data sheet, Texas Instruments, 2001 (SLLS420)
6. *TLK2501 1.5 to 2.5 Gbps Transceiver* data sheet, Texas Instruments, 2001 (SLLS427)
7. *TLK2701 1.6 to 2.7 Gbps Transceiver* data sheet, Texas Instruments, 2000 (SLLS429)
8. *TLK2711 1.6 to 2.7 Gbps Transceiver* data sheet, Texas Instruments, 2001 (SLLS501)
9. *TLK3101 2.5 Gbps to 3.125 Gbps Transceiver* data sheet, Texas Instruments, 2001 (SCAS649)

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