User's Guide

TPS51397A Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS51397A evaluation module (EVM) as well as for the TPS51397A DC/DC converter. Also included are the performance specifications, schematic, layout and, the bill of materials for the TPS51397AEVM.

Table of Contents

Trademarks

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1 Introduction

The TPS51397A is a synchronous buck converter designed to provide up to a 10-A output. The input voltage is rated for 4.5 V to 24 V. The TPS51397A uses a proprietary D-CAP3™ control mode. It provides a fast transient response with no external compensation, and supports low ESR output capacitors. A MODE pin is used to set Eco-mode or OOA mode for light-load running and 500-kHz or 800-kHz switching frequency. Rated input voltage and output current range for the evaluation module are given in Table 1-1. The high-side and low-side switching MOSFETs are integrated inside the TPS51397A package along with the gate-driver circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS51397A to achieve high efficiencies and helps to keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS51397A provides adjustable soft start and undervoltage lockout inputs and an open drain power good output.

This user's guide describes the TPS51397AEVM performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) RANGE	OUTPUT CURRENT (I_{OUT}) RANGE
TPS51397AEVM	4.5 V to 24 V	0 A to 10 A

2 Performance Specification Summary

The TPS51397AEVM is a single, synchronous buck converter providing 5 V at 10 A from 5.5-V to 24-V input. For 5-V output application, it can support Vin from 5.5 V. While for lower output application, for example, a 1.05-V output, it can support Vin from 4.5 V.

A summary of the TPS51397AEVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of 12 V and an output voltage of 5 V, unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2-1. TPS51397AEVM Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Input voltage		5.5	12	24	V
Output voltage setpoint			5		V
Output current range	V_{IN} = 5.5 V to 24 V	0		10	A
Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 10 A		30		mVPP
Output rise time	Soft start pin floating		1.2		ms

3 Modifications

The evaluation module is designed to provide access to the features of the TPS51397A. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R4 ($R_{(TOP)}$) and R6 ($R_{(BOT)}$). R6 is fixed at 15.0 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R4. Changing the value of R4 can change the output voltage above the 0.6-V reference voltage V_{REF}. The value of R4 for a specific output voltage can be calculated using Equation 1.

$$R_{(TOP)} = \frac{R_{(BOT)} \cdot (V_{OUT} - V_{REF})}{V_{REF}} \quad (1)$$

3.2 Mode Selection

The TPS51397A has a MODE pin to select the operation mode. The device reads the voltage on MODE pin during start-up and latches onto one of the MODE options listed below in Table 3-1.

Table 3-1. Mode Pin Resistor Settings

VOLTAGE ON MODE	R9/10/11/12 (kΩ)	R13/14/15/16 (kΩ)	OPERATION	FREQUENCY (kHz)
(0~10%)*VCC	330	15	Eco-mode	500
(10~20%)*VCC	180	33	OOA	500
(20~30%)*VCC	160	51	Eco-mode	800
(30~50%)*VCC	75	51	OOA	800

Change the position of the jumper on J4 to modify the MODE configuration before start up.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS51397AEVM evaluation module. The section also includes test results typical for the evaluation module and covers start up, shut down, load transient response, and output voltage ripple.

4.1 Input/Output Connections

The TPS51397AEVM is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying greater than 10 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 10 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the V_{IN} input voltages with TP8 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP11 as the ground reference.

In this user's guide, the device is set in Eco-mode with 500-KHz frequency by using a jumper at J4-1 and J4-2.

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} input connector (see Table 1-1 for V_{IN} range.)
J2	V_{OUT} output connector. 5 V at 10-A maximum
J3	Soft start selection. Remove the shunt to set the soft start time as internal default value.
J4	MODE selection. Refer to *Section 3.2*.
J5	EN control. Short pin2 and pin3 to disable. Short pin1 and pin2 to enable.
TP1	VCC
TP2	V_{IN} terminal
TP3	V_{IN} test point
TP4	V_{OUT} terminal
TP5	V_{OUT} test point
TP6	SW node test point
TP7	Bode plot test point
TP8—11	GND test point
TP12	PGOOD test point
TP13—15	GND test point
TP16	EN test point

4.2 Start-Up

Figure 4-1 and Figure 4-2 show the start-up waveforms for the TPS51397AEVM. In Figure 4-1, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 4-2, the input voltage is initially applied and the output is inhibited by using a jumper at J5 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 5 V. The input voltage for these plots is 12 V and the load is 1 Ω.

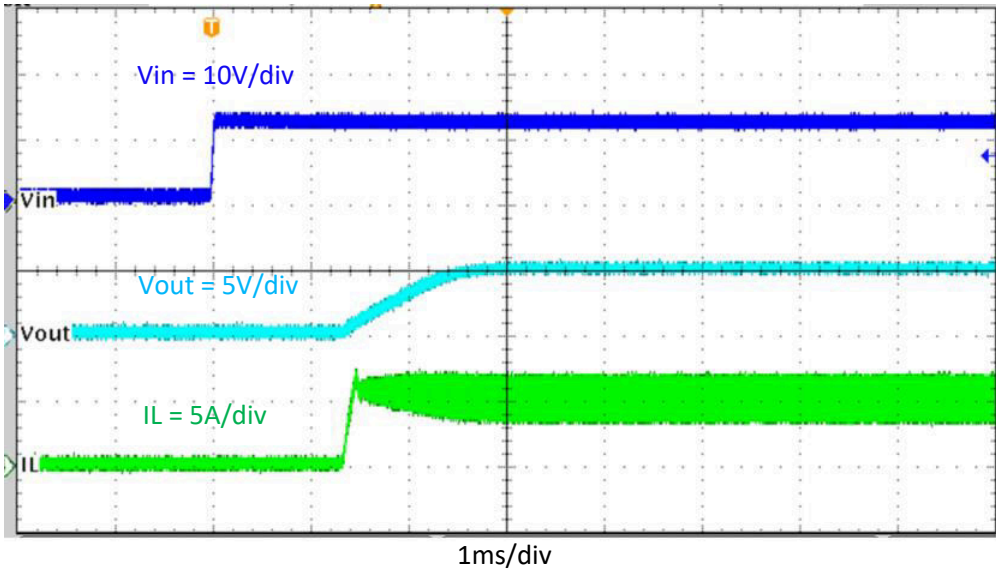

Figure 4-1. Start-Up Relative to V_{IN}, Iout = 5 A

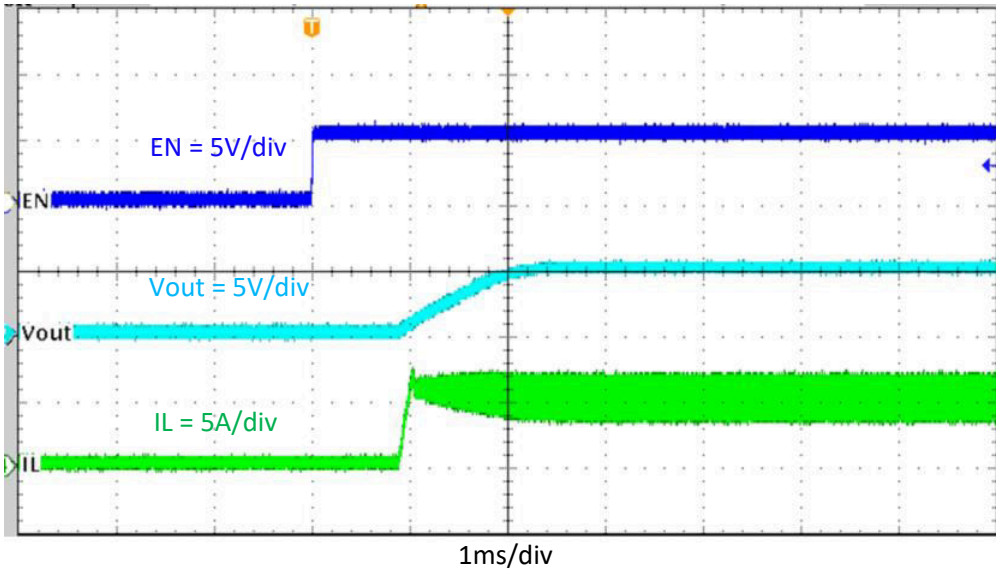

Figure 4-2. Start-Up Relative to Enable, Iout = 5 A

4.3 Shutdown

Figure 4-3 and Figure 4-4 show the shutdown waveforms for the TPS51397AEVM. The input voltage for these plots is 12 V and the load is 1 Ω.

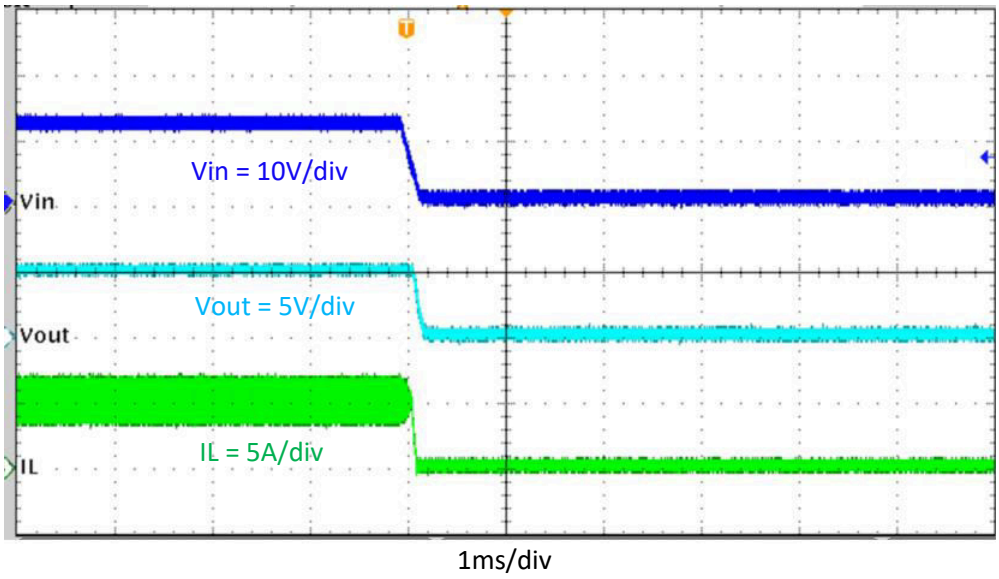

Figure 4-3. Shutdown Relative to V_{IN}, Iout = 5 A

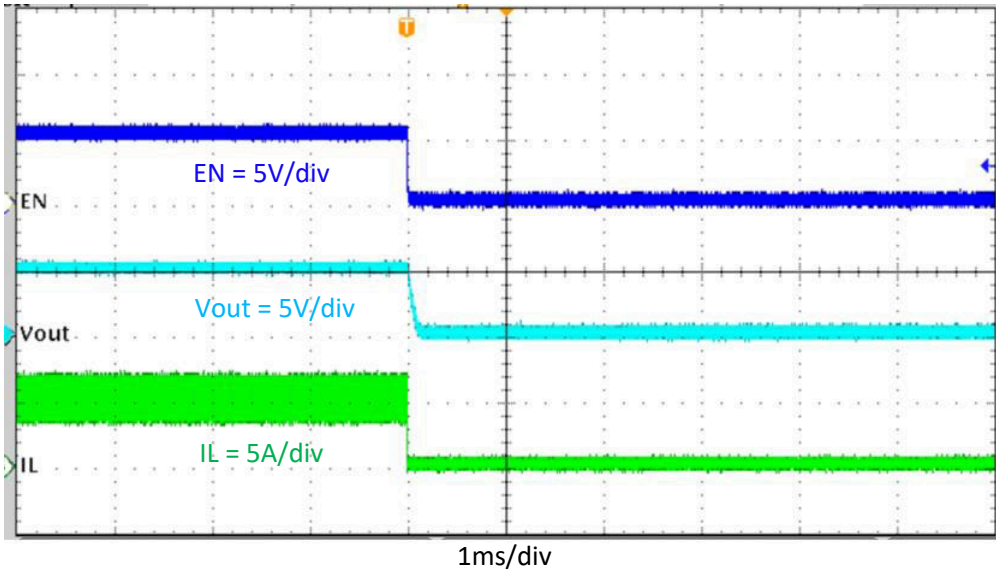

Figure 4-4. Shutdown Relative to Enable, Iout = 5 A

4.4 Load Transient Response

The TPS51397AEVM response to load transient is shown in Figure 4-5 and Figure 4-6.

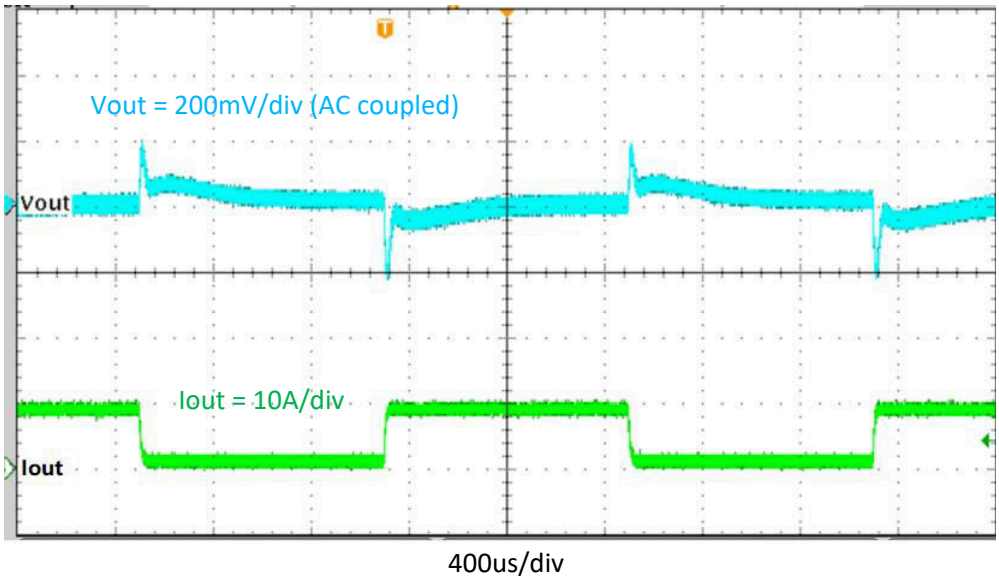

Figure 4-5. Load Transient Response, 1-9 A

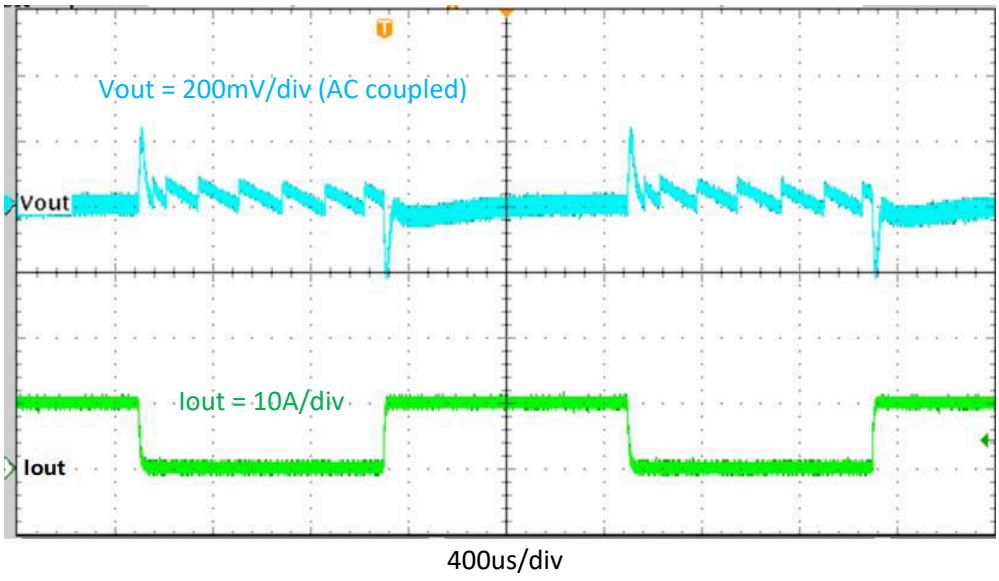

Figure 4-6. Load Transient Response, 0-10 A

4.5 Output Voltage Ripple

Figure 4-7 and Figure 4-8 show the TPS51397AEVM output voltage ripple.

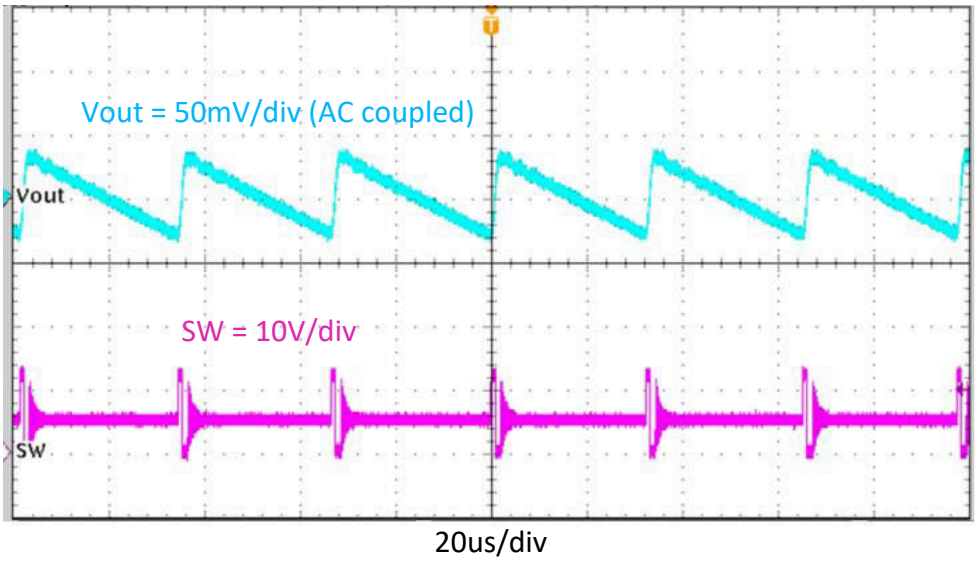

Figure 4-7. Output Ripple, 100-mA Load

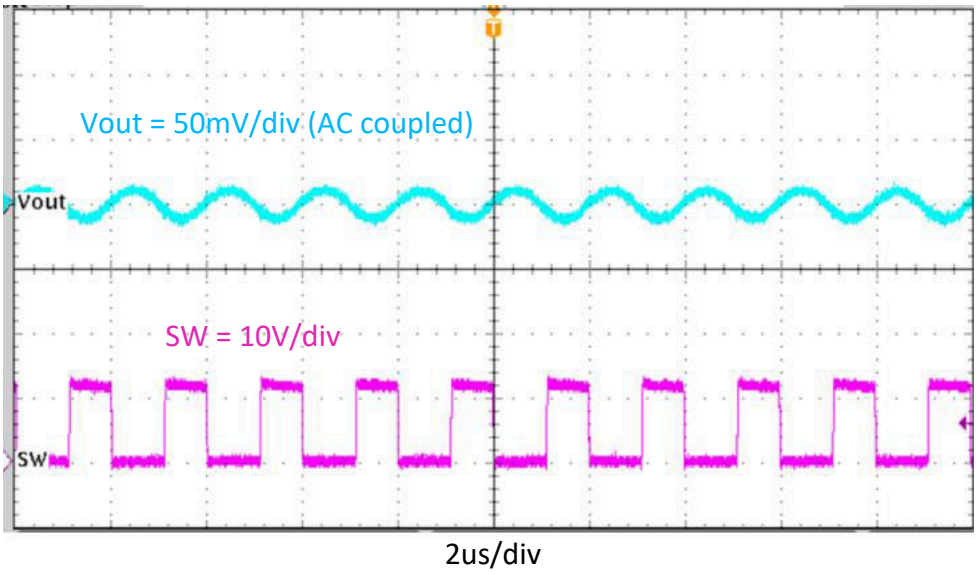

Figure 4-8. Output Ripple, 10-A Load

5 Board Layout

This section provides a description of the TPS51397AEVM, board layout, and layer illustrations.

5.1 Layout

The board assembly and layout for the TPS51397AEVM is shown in Figure 5-1 to Figure 5-5. The top and bottom layers are 2-oz copper thickness. Internal layers are 1-oz copper thickness.

The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS51397A and a large area filled with ground. Most of the signal traces are located on the bottom left side, surrounded by a ground plane with an island for quiet analog ground that is connected to the main power ground at a single point. The internal layer-1 and internal layer-2 are dedicated ground planes. The bottom layer is another ground copper area with additional SW, VIN, and VOUT copper fill. Ground traces on different layers are connected to each other with multiple vias placed on the board.

The input decoupling capacitors are located as close to the IC as possible. Critical analog circuits, such as the voltage set point divider, EN resister, SS capacitor, Mode resistor, VCC, and AGND pin, are terminated to quiet analog ground island on the top layer. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, VIN and VOUT copper fill, and the feedback trace from the point of regulation to the top of the resistor divider network.

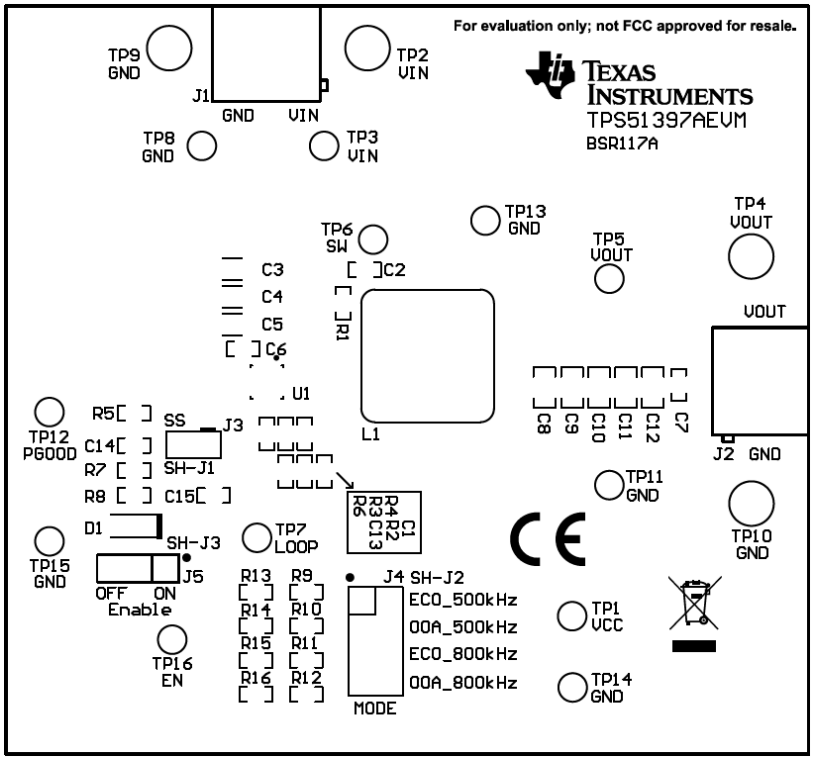

Figure 5-1. Top Assembly

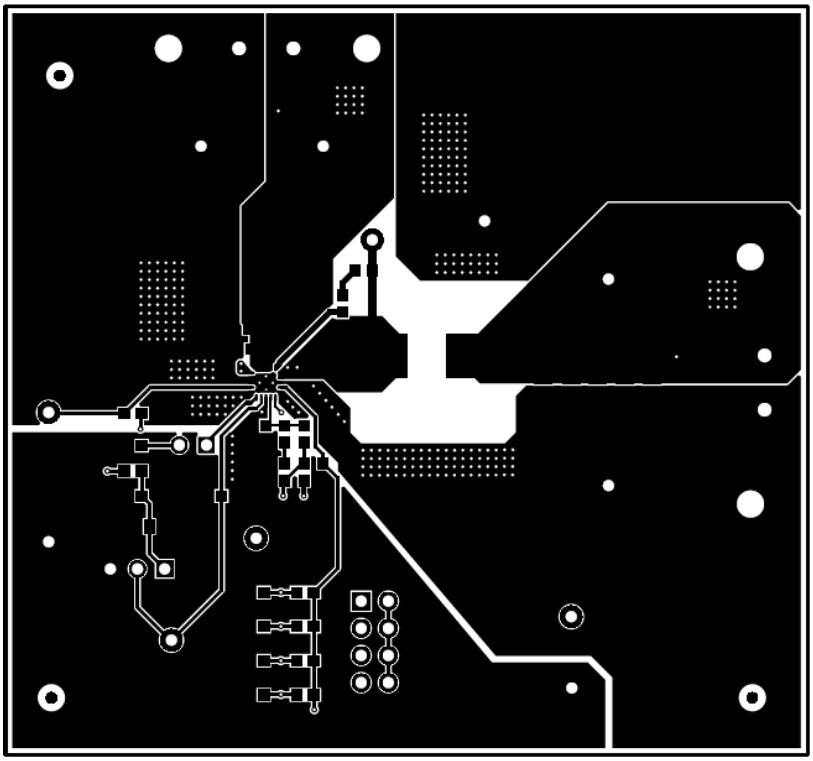

Figure 5-2. Top Layer Layout

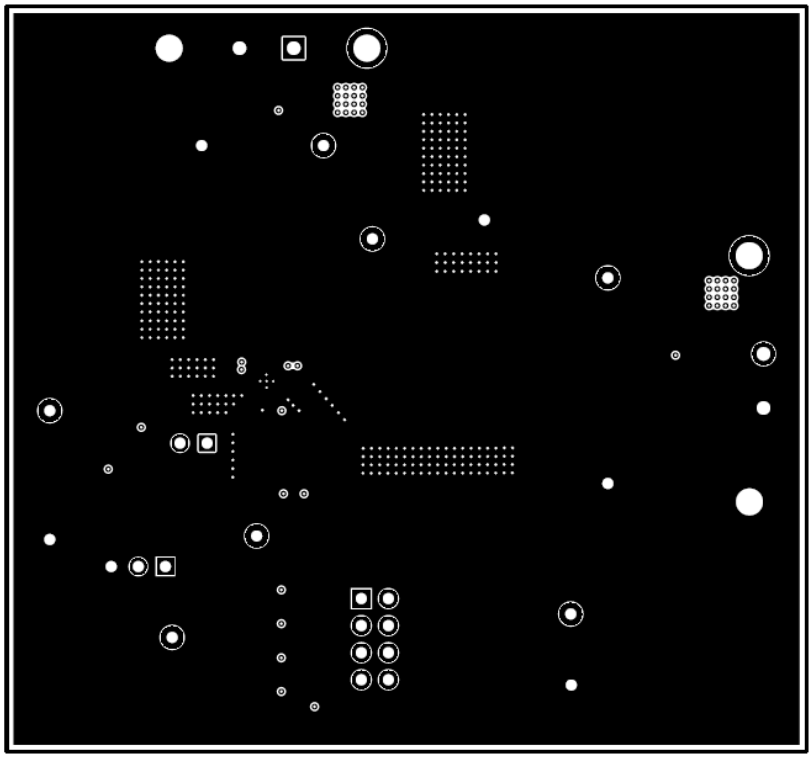

Figure 5-3. Internal Layer-1 Layout

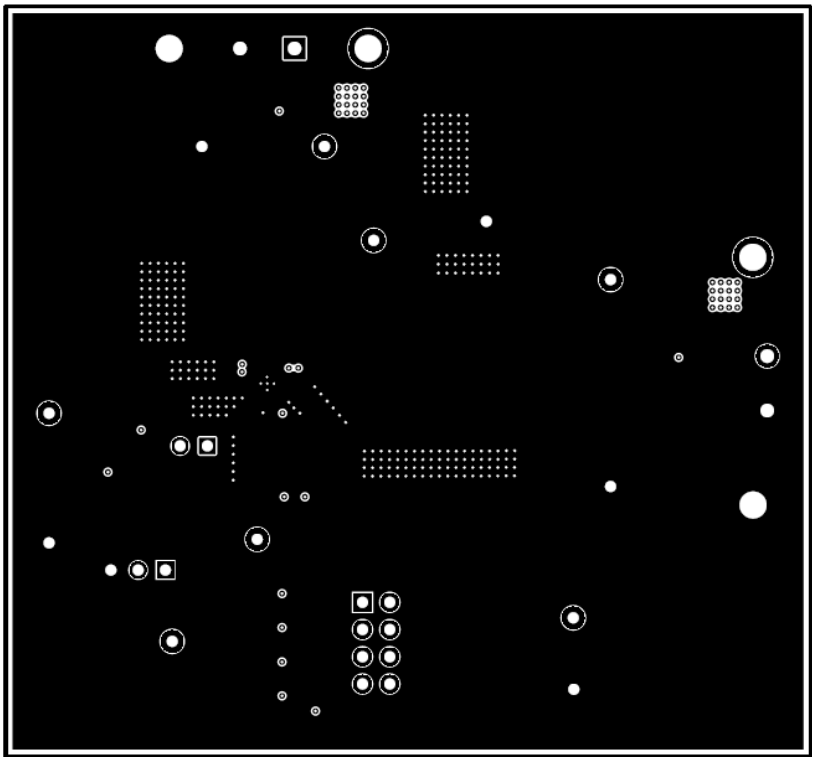

Figure 5-4. Internal Layer-2 Layout

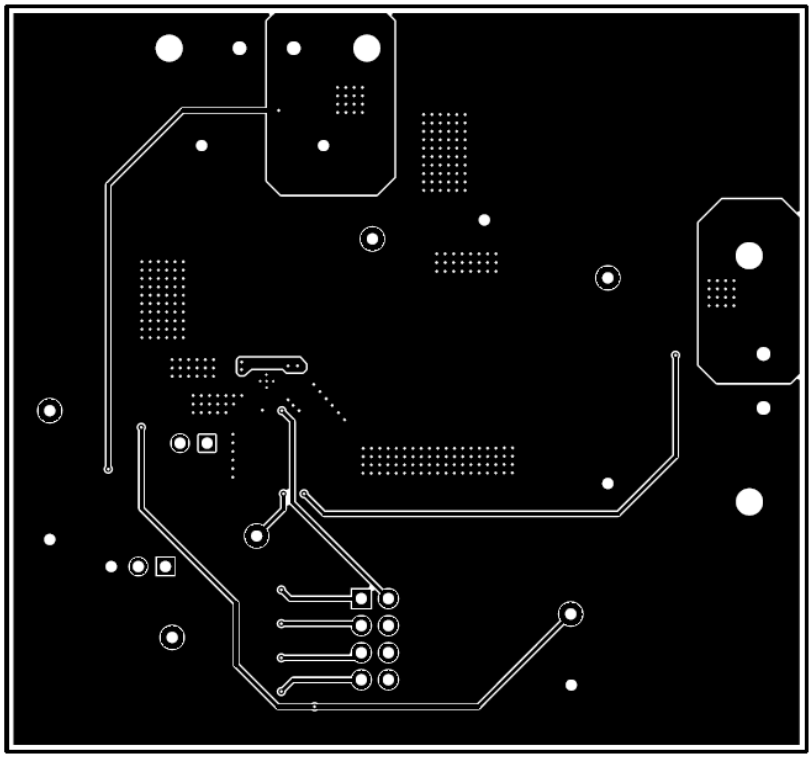

Figure 5-5. Bottom Layer Layout

The board top and bottom view for the TPS51397AEVM is shown in Figure 5-6 and Figure 5-7.

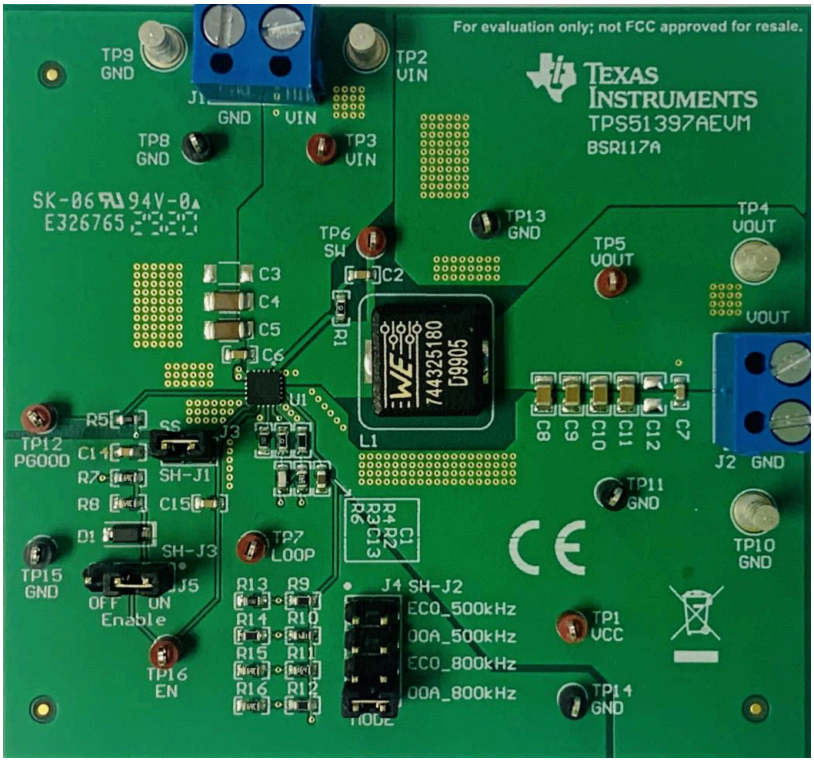

Figure 5-6. Board Top View

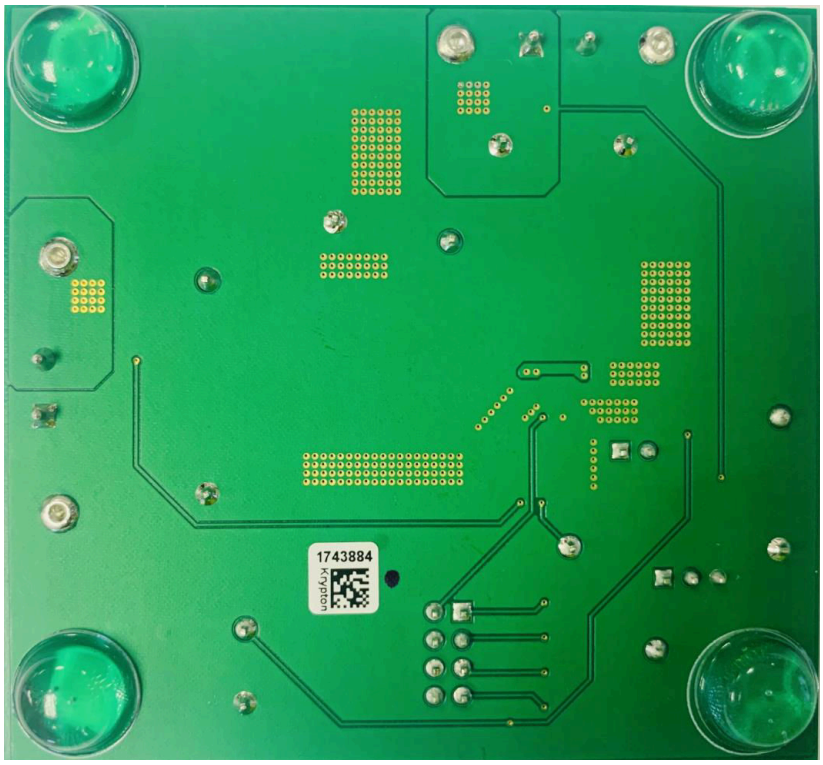

Figure 5-7. Board Bottom View

6 Schematic and Bill of Materials

6.1 Schematic

Figure 6-1 shows the schematic for TPS51397AEVM.

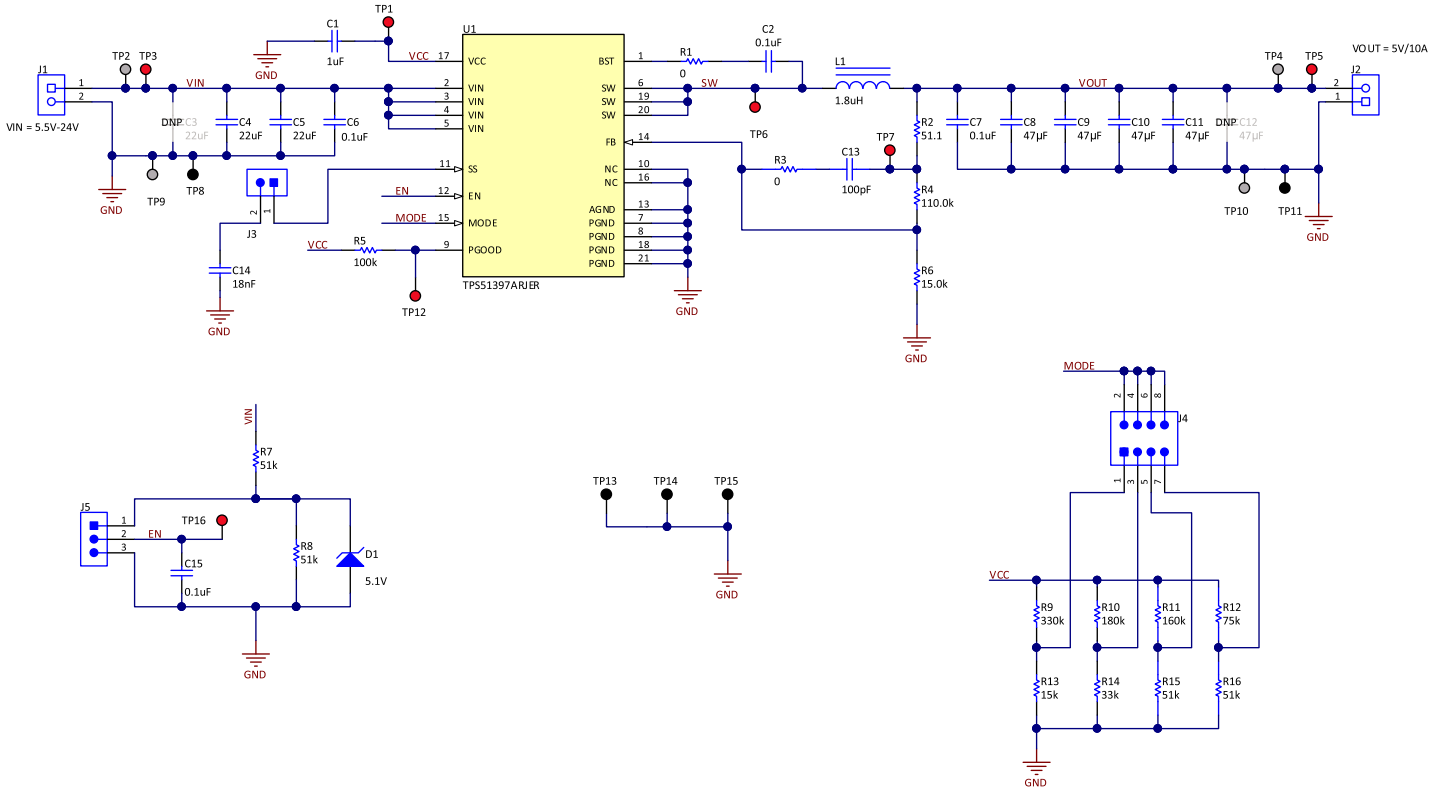

Figure 6-1. TPS51397AEVM Schematic

6.2 Bill of Materials

Table 6-1 presents the list of materials for the TPS51397AEVM.

Table 6-1. TPS51397AEVM List of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed circuit board	BSR117	Any
C1	1	CAP, CERM, 1 µF, 25 V, ±10%, X5R, 0603	C1608X5R1E105K080AC	TDK
C2, C6, C7, C15	4	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	C1608X7R1H104K080AA	TDK
C4, C5	2	CAP, CERM, 22 µF, 35 V, ±20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C8, C9, C10, C11	4	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C13	1	CAP, CERM, 100 pF, 100 V, ±1%, C0G/NP0, 0603	C1608C0G2A101F080AA	TDK
C14	1	CAP, CERM, 0.018 µF, 100 V, ±10%, X7R, 0603	C0603C183K1RACTU	Kemet
D1	1	Diode, Zener, 5.1 V, 500 mW, SOD-123	MMSZ5231B-7-F	Diodes Inc.
H1, H2, H3, H4	4	Bumpon, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2x1, tin, TH	PEC02SAAN	Sullins Connector Solutions
J4	1	Header, 100 mil, 4x2, tin, TH	PEC04DAAN	Sullins Connector Solutions
J5	1	Header, 100 mil, 3x1, tin, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, Shielded Drum Core, Superflux, 1.8 µH, 16 A, 0.0035 Ω, SMD	744325180	Wurth Elektronik
R1, R3	2	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R2	1	RES, 51.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060351R1FKEA	Vishay-Dale
R4	1	RES, 110 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603110KFKEA	Vishay-Dale
R5	1	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R6	1	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060315K0FKEA	Vishay-Dale
R7, R8, R15, R16	4	RES, 51 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060351K0JNEA	Vishay-Dale
R9	1	RES, 330 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603330KJNEA	Vishay-Dale
R10	1	RES, 180 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603180KJNEA	Vishay-Dale
R11	1	RES, 160 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603160KJNEA	Vishay-Dale
R12	1	RES, 75 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060375K0JNEA	Vishay-Dale
R13	1	RES, 15 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060315K0JNEA	Vishay-Dale
R14	1	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333K0JNEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP3, TP5, TP6, TP7, TP12, TP16	7	Test point, miniature, red, TH	5000	Keystone
TP2, TP4, TP9, TP10	4	Terminal, turret, TH, triple	1598-2	Keystone
TP8, TP11, TP13, TP14, TP15	5	Test point, miniature, black, TH	5001	Keystone
U1	1	4.5-V to 24-V, 10-A Synchronous Step-Down Voltage Regulator	TPS51397ARJER	Texas Instruments
C3	0	CAP, CERM, 22 µF, 35 V, ±20%, X5R, 1206	C3216X5R1V226M160AC	TDK
C12	0	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A476ME15L	MuRata

Table 6-1. TPS51397AEVM List of Materials (continued)

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

7 References

1. *TPS51397A 4.3-V to 24-V Input, 10-A Synchronous Step-Down Converter Data Sheet*

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2020) to Revision A (April 2021)	Page
• Changed user's guide title	2

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