NanoStar™ Wafer Chip-Scale Package Design

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ABSTRACT

To satisfy market demand for an ultra-small, staggered 5-ball wafer-level chip-scale (WCSP) package, Texas Instruments has introduced the 170µm NanoStar™ YEQ package. Since staggered ball WCSPs are not registered under the JEDEC MO-211 standard, there are no formal industry-standard guidelines on proper use of devices in this package. This application note gives guidelines for reliable, high-performance use of the YEQ package.

1 Package Construction

NanoStar™ is a wafer-level chip-scale package produced by Texas Instruments. TI has both direct-bump and redistribution layer (RDL) technologies, allowing placement of solder bumps both directly above the bond pad as well as elsewhere on the die.

The NanoStar packaging process starts by repassivating the bare silicon wafer, leaving the original bond pads exposed. For direct-bump devices, an under-bump metal (UBM) is added to the original bond pads; solder bumps are then placed on the UBM. (See Figure 1.)

For RDL devices, a copper layer is used after repassivation to route the original bond pads to the ball array locations. A second polymer passivation is applied to isolate the copper RDL. A new UBM bond pad is now fabricated where the solder bumps will be placed. Then, 170µm solder balls are placed on the wafer. (See Figure 2.)

For both types of devices, the die are singulated after the bumps are placed.

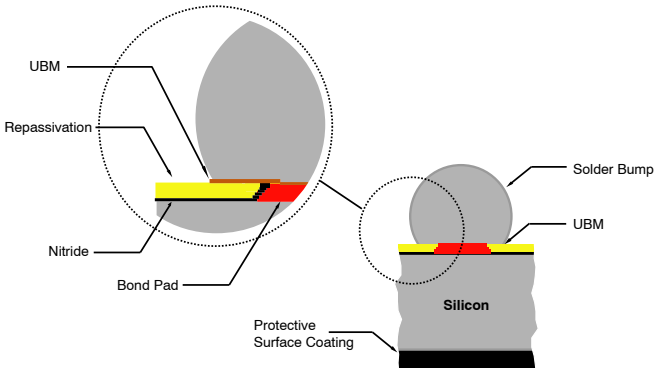


Figure 1. Direct-Bump WCSP Cross Section

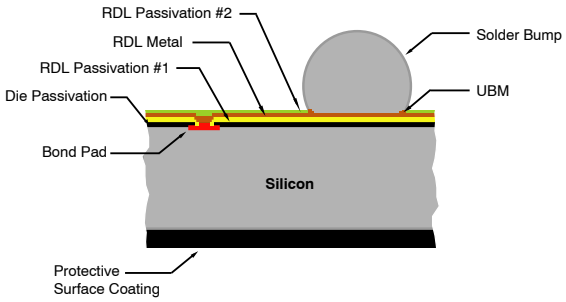


Figure 2. RDL WCSP Cross Section

2 NanoFree™: Lead-Free NanoStar™ Package

The NanoFree™ package is a lead-free version of the NanoStar™ package, and will be introduced by Texas Instruments during late 2003. The package cross-section is identical to that of NanoStar™ except for differences in the materials, which are necessary for the lead-free solder bumps. Contact TI for availability.

3 NanoStar™ YEQ Package Data

Table 1. NanoStar™ Package Data

Parameter	Value	Units
Length(1)	1.17 – 1.67	mm
Width(1)	0.80 – 1.30	mm
Height	0.625 max	mm
Bump Diameter	170	µm
Bump Pitch	50 BSC	µm
Bump Co-planarity	50	µm
Bump Composition	SnPb	-
Seating Plane	0.10 – 0.18	mm
Moisture Sensitivity	MSL-1	-
$R_{\theta,J\text{-}A}$	190	°C/W
$R_{\theta,J\text{-}C}$	39	°C/W

(1) These length and width ranges cover any device that could be put into this WCSP. The device specific min/max sizes can be found in a given product data sheet. For more information, please visit the Texas Instruments web site.

4 Pad Design

Non-solder mask defined (NSMD) pads should be used with the YEQ package. The recommended pad design is shown in Figure 3. To assure self-centering of the device, there should only be one connecting trace per pad; the arrangement should be symmetric, similar to that shown in Figure 3.

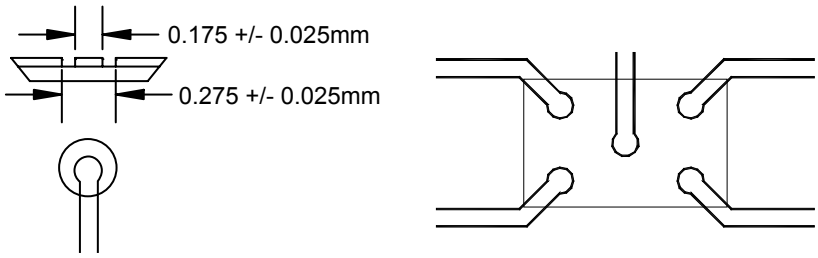


Figure 3. Recommended Pad and Connecting Trace Layout

5 Solder Paste Stencil Details

While paste selection is normally driven by overall system assembly requirements, Texas Instruments recommends Type 3 or finer “no clean” solder paste for mounting the NanoStar™ package. Figure 4 shows the recommended stencil layout.

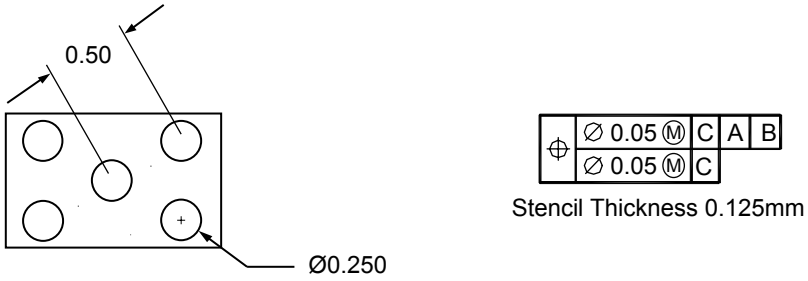


Figure 4. Recommended Stencil Layout

6 Component Placement, Solder Reflow, and Rework

6.2 Component Placement

Standard fine-pitch pick and place equipment can be used to assemble NanoStar™ devices. Mechanical centering placement machines should not be used, due to the risk of damage to the device. Placing force should be no more than 25 grams/bump, or 125 grams total.

6.3 Solder Reflow

Standard solder reflow processes can be used with the NanoStar™ package. Figure 5 shows a typical eutectic reflow profile. Table 2 denotes reflow parameter guidelines.

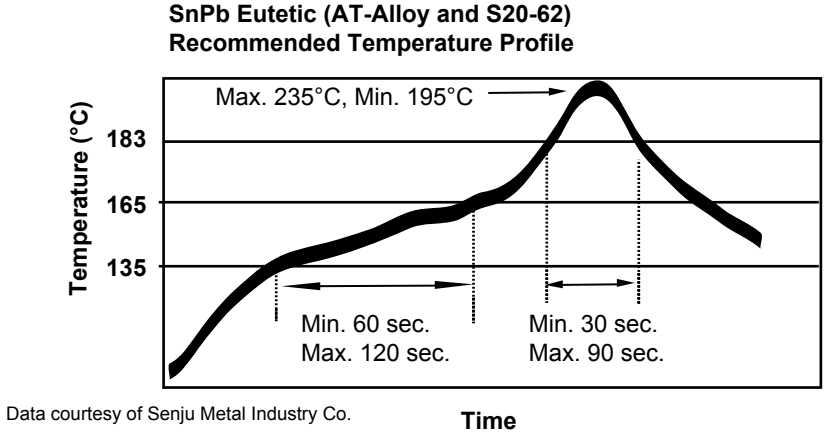


Figure 5. Recommended Reflow Profiles

Table 2. Recommended Critical Reflow Parameters

Process Step	Tin Lead Solder
Ramp Rate	3°C/sec Maximum
PreHeat	165°C 60 to 120 sec.
Time Above Liquidus	183°C 30 to 90 sec.
Peak Temperature	235°C
Time within 5°C of Peak Temp.	10 to 20 sec.
Ramp Down Rate	6 °C/sec. Max.

6.4 Rework

The rework procedure for the NanoStar™ package is similar to that used for many ball-grid array (BGA) and chip-scale (CSP) packages. While Texas Instruments does not recommend any particular rework tools or vendors, the Air-Vac Engineering DRS24 with hot gas nozzle N09DVG-7 has been shown to work successfully on 0.056-inch thick FR4 with the following process:

1. Apply flux to component using Auto Flux feature of DRS24
2. Align device over pads
3. Place device on board
4. Raise nozzle 0.050 inches
5. Preheat board to 90°C, nozzle warming up 20% air flow, 100°C
6. Soak Stage – 20% air flow, 200°C, 90 seconds
7. Ramp Stage – 20% air flow, 300°C, 30 seconds
8. Reflow Stage – 25% air flow, 325°C, 55 seconds
9. Cooldown Stage – 40% air flow, 25°C, 30 seconds

7 Board-Level Reliability Results for RDL Technology

Table 3 presents the results from the board-level reliability testing that was performed for the RDL version of the NanoStar package.

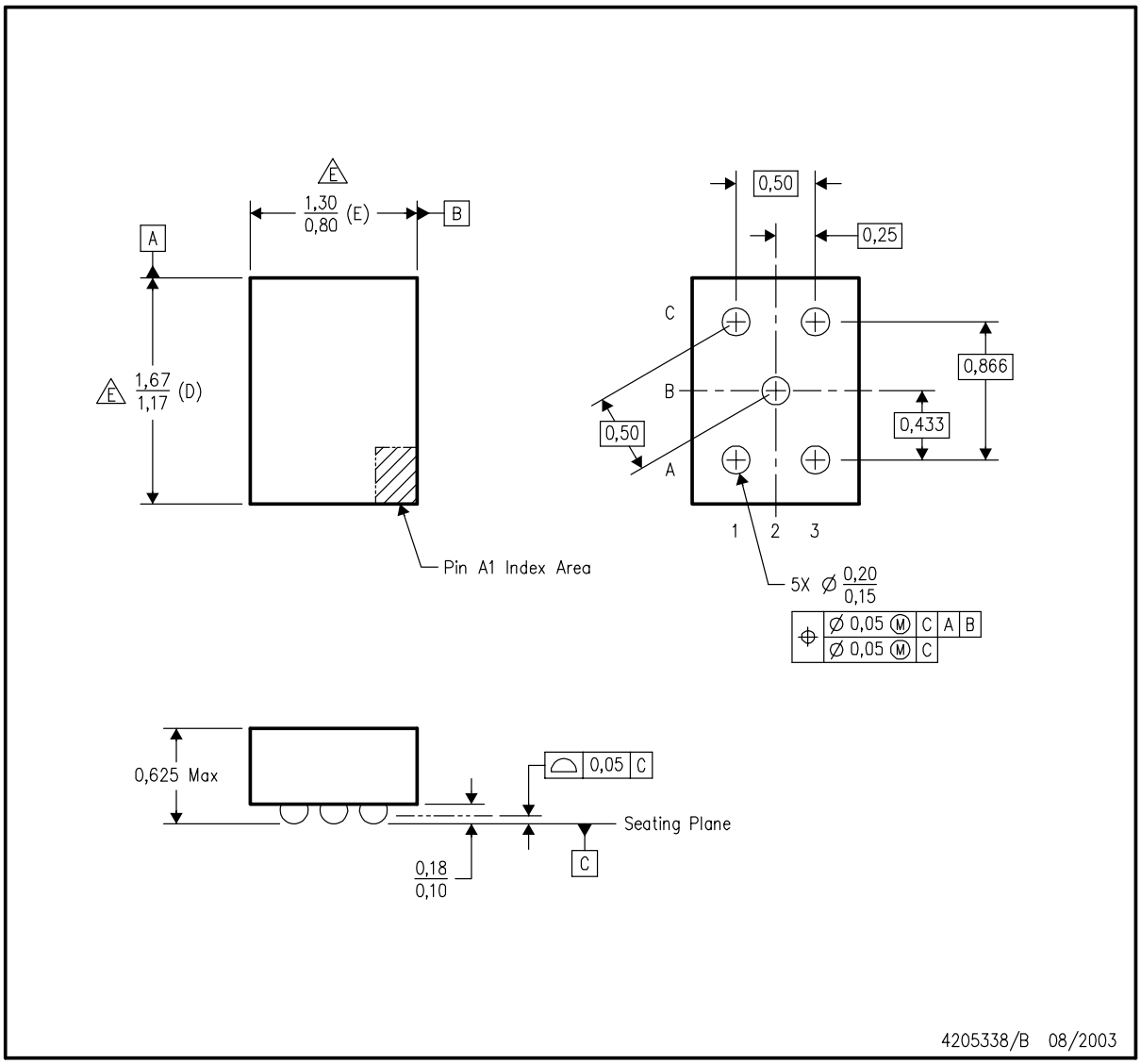
Table 3. Board-Level Reliability Results for RDL Technology

Test	Condition	Criteria	Sample Size	Results
Temperature Cycle	-40 to 125C, 1 cycle/hr, 15 minute ramp†	1000 cycles, R<1.2X from R_0	36	0/36, 1450 cycles 2/36, 1940 cycles (ongoing)
Drop	1.5 meter	10 drops, R<1.2X from R_0	5	200 drops 0 of 8 failed
Key Push	100 cycle/min, 20N max force, 1300 uε, Displacement = 2.7 mm max	20K cycles, R<1.2X from R_0,	5	500,000 cycles 0 of 8 failed
3-point Bend	Strain Rate 5 mm/min, 100 mm span	R<1.2X from R_0	5	35mm bend 0 of 8 failed

† Per IPC9701

Appendix A. Mechanical Drawing

YEQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb).
E. This drawing provides a range for acceptable die sizes. Reference Product Data Sheet for exact die size and tolerances per symbols D and E.

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