Application Note

Determine Optimal Isolation Resistance for Driving Capacitive Load

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ABSTRACT

This application note describes how an amplifier's open-loop output impedance can be used to calculate an optimal isolation resistance for driving large capacitive loads. An example calculation is applied to select a resistor value to stabilize an amplifier that is oscillating due to a large capacitance at the output. The relationship between open-loop output impedance and capacitive load-drive is explored, and an equation is derived to quickly determine an optimal isolation resistance.

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Trademarks

1 Introduction: Open-Loop Output Impedance (R_O)

The ideal op amp has infinite input impedance and zero output impedance. In practice, every real amplifier has a non-zero output impedance typically in the range of Ω to kΩ. Texas Instruments op amp data sheets include a plot of the open-loop output impedance (R_O) over frequency. R_O is not to be confused with the closed-loop output impedance (R_{OUT}), although the two are closely related by the loop gain.

Figure 1-1 shows the open-loop output impedance over frequency for the OPA392, which is flat at approximately 120 Ω across frequency. This flat portion of the curve implies that the open-loop output impedance acts as a resistor (R_O) across the effective bandwidth of the amplifier. Some amplifiers have an output impedance that changes over frequency, implying a complex impedance (Z_O). The analysis in this document applies to amplifiers that have a flat, resistive output impedance across the effective bandwidth of the amplifier.

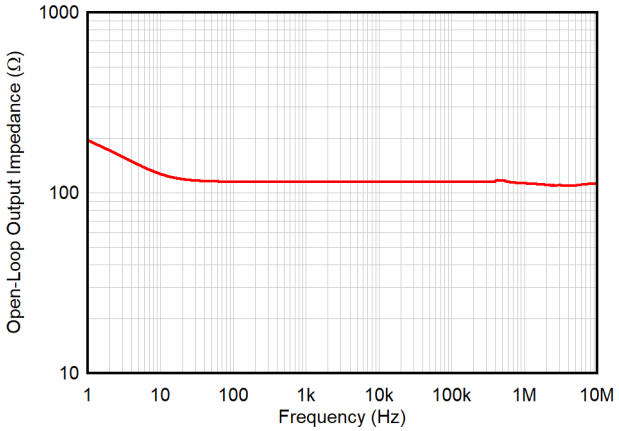


Figure 1-1. Open-Loop Output Impedance vs Frequency, OPA392

R_O is also specified in the electrical characteristics section of the data sheet, which confirms the resistance is 120 Ω. This data sheet specification for R_O is used to determine an optimal value for R_{ISO} when driving a large capacitive load, as described in Section 3.

R_O	Open-loop output impedance	f = 1 MHz	120	Ω

2 Overview: Closed-Loop Amplifier Stability

Amplifier stability is a primary concern for designers, as amplifier circuits are expected to operate under a variety of output loading conditions. Capacitance directly at the output of an amplifier can cause time delays between the input and output pins. These time delays are often represented as phase shifts between the output and feedback nodes, which can result in oscillations at the output of the amplifier.

An amplifier's closed-loop gain (A_{cl}) over frequency is defined by Equation 1. The derivations for this equation can be found in *Stability Analysis of Voltage-Feedback Op Amps* application note.

$$A_{cl} = \frac{A_{OL}}{1 + A_{OL}\beta} \quad (1)$$

Where,

- A_{OL} is the amplifier's open-loop gain
- β is the feedback factor

When the magnitude of $A_{OL}\beta$ is 1 and the phase shift is 180°, $A_{OL}\beta$ can be expressed in phasor notation as $1\angle 180°$ which is equal to -1. This -1 term in the denominator results in a division by zero, and the equation is undefined. Systems with $A_{OL}\beta$ approaching 180° phase shift at unity gain begin to exhibit signs of instability in the form of oscillations or *ringing* at the output. The term phase margin is used to account for this, and is defined as how close a system is to the 180° total phase-inversion when the magnitude of $A_{OL}\beta$ is 0dB. A phase margin of 45° is a common benchmark for assessing the stability of a system. Designers commonly target a minimum phase margin of 45° to avoid instability.

A common technique for analyzing amplifier stability, is simulating the open-loop gain (A_{OL}) and feedback factor (β) of the amplifier circuit over frequency. A stable circuit will show 20-dB rate of closure between the A_{OL} and 1/β curves and 45-90 degrees of phase margin. Rate of closure, phase margin, and other details related to stability analysis are explained in detail in the *Texas Instruments Precision Labs (TIPL) video series on stability*.

3 Example, Calculate Optimal Isolation Resistance to Drive Large Load Capacitance

A common case for amplifiers to exhibit instability is when configured to directly drive a large capacitive load. Figure 3-1 shows the OPA392 configured as a buffer with a 10 µF capacitor connected between the output of the amplifier and ground. The 10 µF load causes the circuit to exhibit an undesirable ringing behavior. This ringing behavior indicates that the circuit is unstable. The analysis techniques described in TIPL Video Series on Stability confirm the circuit is unstable with a phase margin of less than 1°.

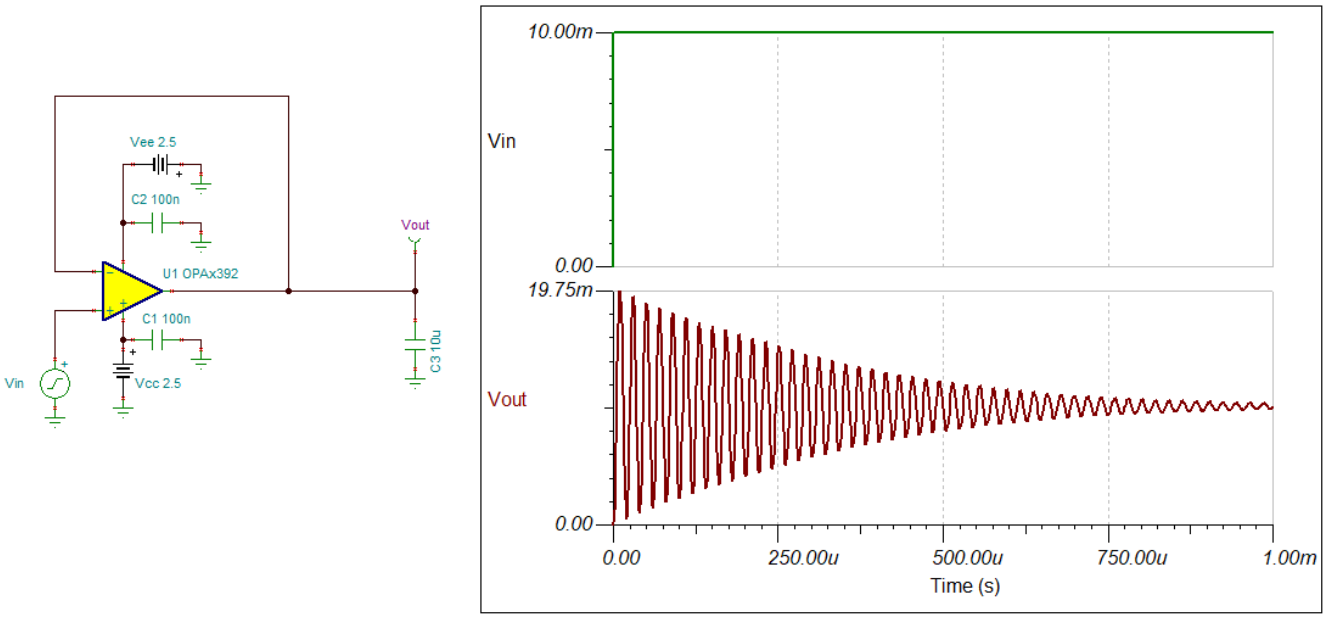


Figure 3-1. Unstable Buffer Configuration, 10 µF Load

It is not recommended to directly load an amplifier's output with a large capacitor. However, in certain cases such as an ADC reference driver, this load capacitor is essential to the circuit's function and the capacitance cannot be removed or reduced. A common technique to stabilize an amplifier driving a capacitive load, is to place a resistor in series between the amplifier's output and the load capacitance. This is referred to as an isolation resistor or R_{ISO}, as it serves to *isolate* the output and feedback of the amplifier from the capacitive load.

Implementing a small 380 mΩ isolation resistor in the OPA392 buffer circuit improves the phase margin to 60°, and the circuit is stable. Figure 3-2 shows the small-signal step response in which the output settles without oscillations or ringing.

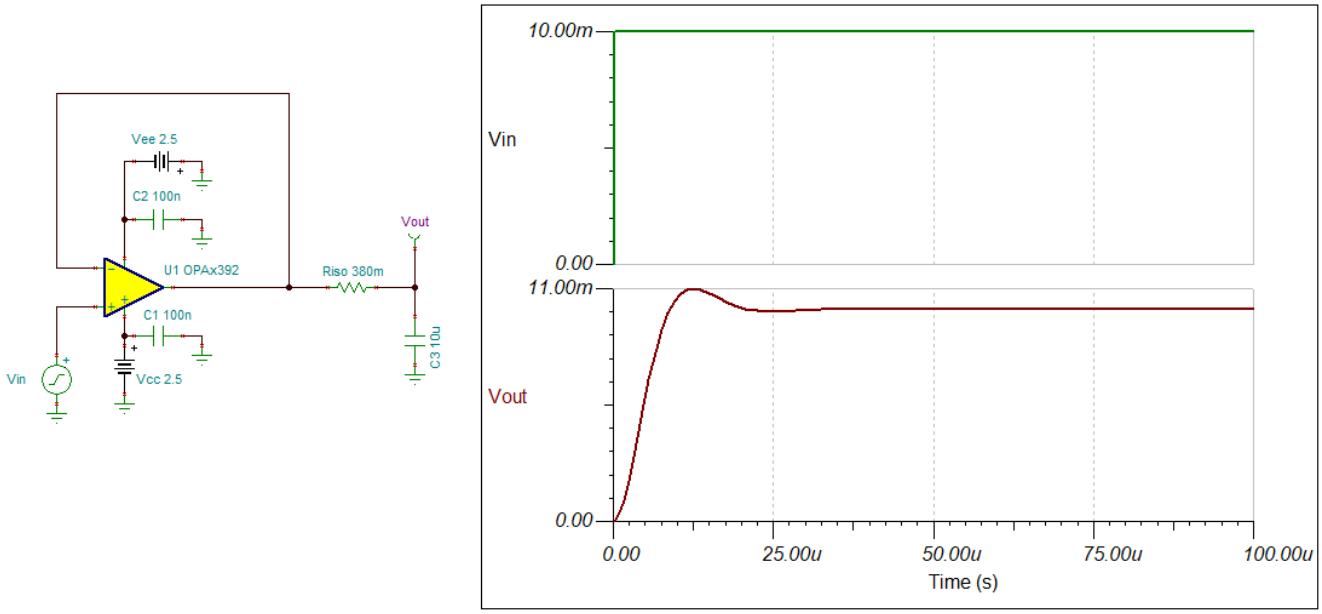


Figure 3-2. Stable Buffer Configuration with Optimal R_{ISO}

The magnitude of the isolation resistance was determined by Equation 2.

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \cdot R_O \cdot C_{LOAD} \cdot f_{gbw}\right)}}{4\pi \cdot C_{LOAD} \cdot f_{gbw}} \quad (2)$$

Where,

- f_{gbw} is the gain bandwidth of the amplifier in Hz, as defined in the data sheet
- R_O is the amplifier's open-loop output impedance in Ohms, as defined in the data sheet
- C_{LOAD} is the load capacitance in Farads

With the data sheet specifications for gain bandwidth and open-loop output impedance, Equation 2 can be used to quickly determine an optimal isolation resistance to stabilize a circuit driving a large capacitive load. Always use Spice simulation tools such as TINA-TI to verify the circuit is stable and operating with the R_{ISO} value chosen.

The relationship between open-loop output impedance, capacitive loading, and closed-loop stability is explored in detail in Section 4. This relationship is then used to derive Equation 2 for optimal R_{ISO} when driving a capacitive load.

4 R_O, R_{ISO}, and Capacitive Load Drive

The output impedance, also referred to as output resistance, can be modeled as a series resistor at the output of the amplifier.

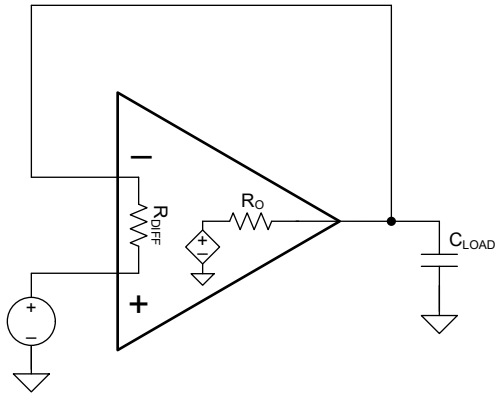


Figure 4-1. Op Amp Output Resistance Internal Model

The load capacitance (C_{LOAD}) interacts with the output impedance of the amplifier (R_O), producing an additional pole in the amplifier's A_{OL} curve, as shown in Figure 4-2. This additional pole (f_{p2}) causes the A_{OL} to decrease an additional 20 dB/decade resulting in a total of 40dB/decade rate of closure with 1/β. The rate of closure (ROC) is defined by the difference in slopes of the A_{OL} and 1/β curves at the frequency in which the two curves intersect. A stable circuit exhibits a rate of closure of approximately 20 dB/decade.

$$f_{p2} = \frac{1}{2\pi \cdot R_O \cdot C_{LOAD}} \tag{3}$$

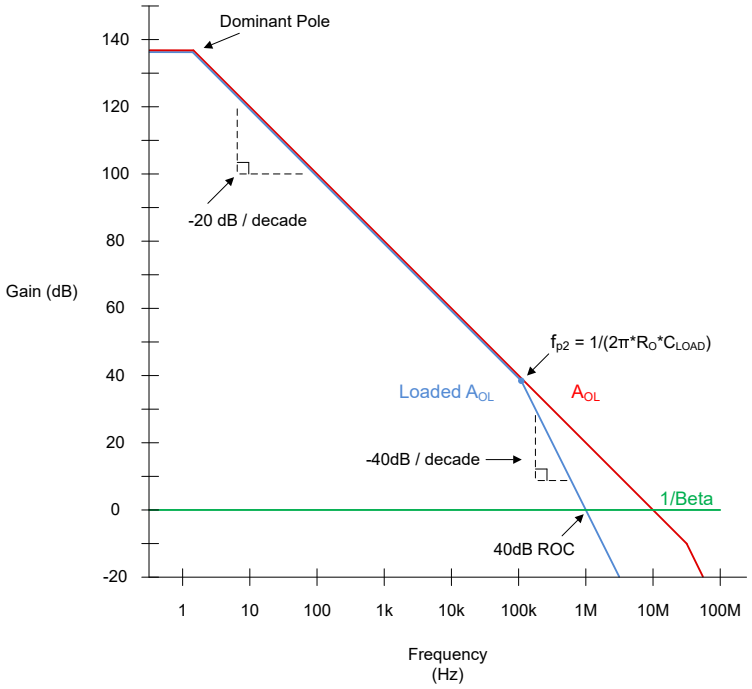
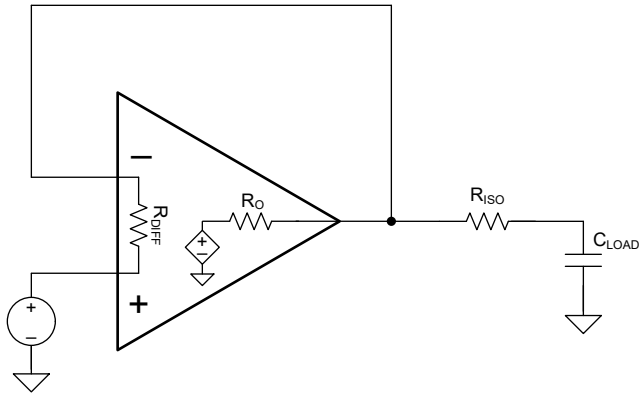


Figure 4-2. Effects of Capacitive Load on Amplifier Open-Loop Gain

Considering the rate of closure between A_{OL} and 1/β, stability issues arise when f_{p2} occurs at a frequency less than the bandwidth of the amplifier. For amplifiers with comparable bandwidth, an amplifier with lower open-loop output impedance is capable of driving larger capacitive loads, while maintaining stability.

When R_{ISO} is implemented in the circuit, the isolation resistance interacts with the load capacitance to produce a zero in the A_{OL} curve. This zero (f_{z1}) causes the A_{OL} curve to increase by 20 dB/decade, canceling out the effect of f_{p2}, and restoring the rate of closure to 20 dB per decade.



$$f_{z1} = \frac{1}{2\pi \cdot R_{ISO} \cdot C_{LOAD}} \quad (4)$$

Figure 4-3. Op Amp Output Resistance with R_{ISO} and Capacitive Load

R_{ISO} also causes a shift in the pole frequency from f_{p2} to f_{p2}* as defined in Equation 5.

$$f_{p2}^* = \frac{1}{2\pi[R_O + R_{ISO}]C_{LOAD}} \quad (5)$$

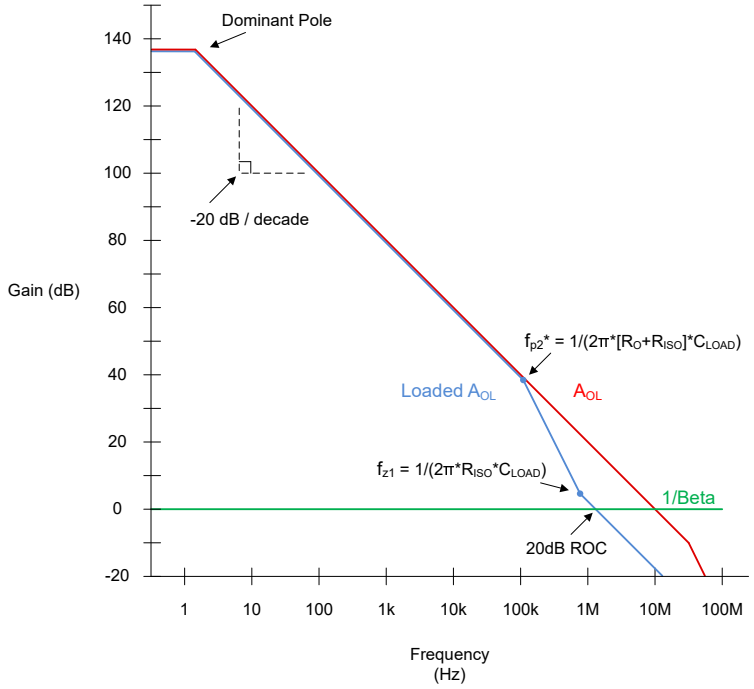


Figure 4-4. Effects of R_{ISO} on Amplifier Open-Loop Gain with Capacitive Load

R_{ISO} is designed to be as small as tolerable while maintaining closed-loop stability. A larger isolation resistor increases the phase margin, but at the cost of voltage error and settling time. If the load has a resistive element, R_{ISO} creates a resistor divider between the output of the amplifier and the load resistance, resulting in a voltage error. If the load resistance is much greater than R_{ISO}, this voltage error can be negligible. Figure 4-5 shows two amplifiers driving complex loads with a resistive element of 10 kΩ and 5 nF of capacitance. The voltage error caused by the 20 Ω isolation resistor can be tolerable for the application, whereas the 200 Ω isolation resistor produces an unacceptable error. For DC applications, if the R_{ISO} required to stabilize the amplifier is too large, the *dual feedback* method can be used. For AC applications, choose an op amp with a low output impedance to minimize the isolation resistance required for stability.

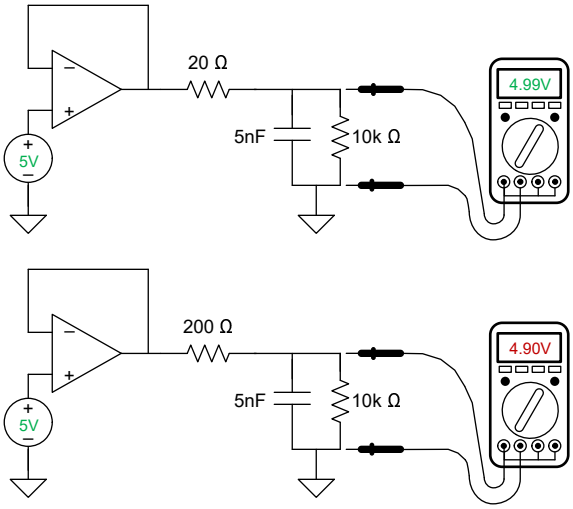


Figure 4-5. R_{ISO} Voltage Divider with Resistive-Capacitive Load

5 Derive Equation for Optimal Isolation Resistance

To reduce errors while maintaining closed-loop stability, the *optimal* R_{ISO} resistance must be determined. The optimal isolation resistance is the smallest series resistance that produces an acceptable transient response when driving the capacitive load. While a phase margin of 45° is generally considered stable, this may not be sufficient for applications that demand low overshoot. In certain cases, it is typical for a phase margin of 60° to be considered *optimally damped*. If voltage error is of primary concern, a phase margin of 45° can be targeted as this allows the smallest isolation resistance to be used.

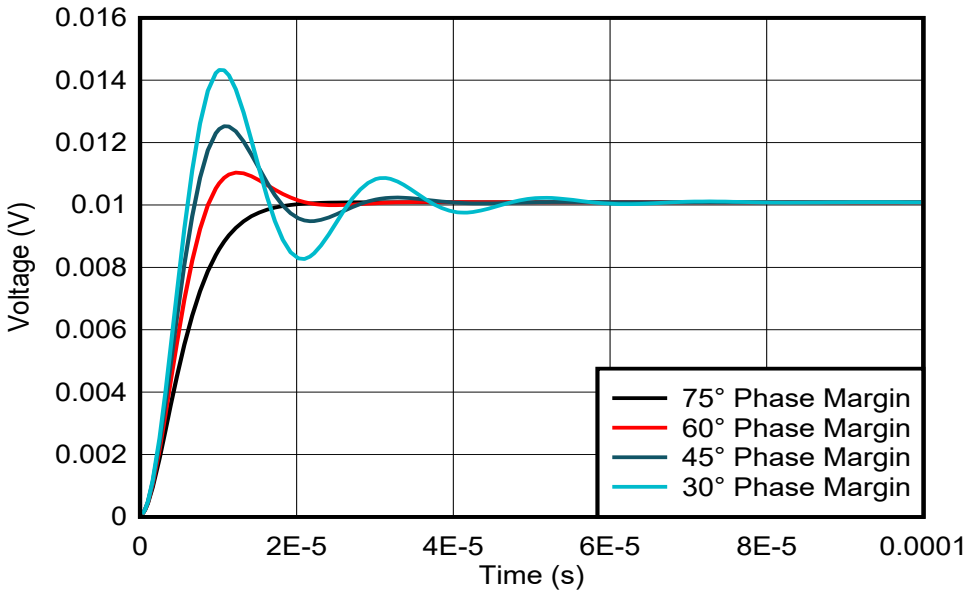


Figure 5-1. Small-Signal Step Response and Phase Margin

The closure frequency (f_{cl}) is the frequency in which the A_{OL} and 1/β curves intersect. Selecting an R_{ISO} resistance that places f_{z1} exactly at the closure frequency, targets a phase margin between 50°-60°, and is a good tradeoff between voltage error and transient performance. In this case, the optimal R_{ISO} results in f_{z1} such that,

$$f_{z1} = f_{cl} \tag{6}$$

For a typical amplifier in a buffer configuration, the closure frequency is simply the gain bandwidth (f_{gbw}) of the op amp. However, in the case of the loaded A_{OL} curve in which f_{p2} causes an additional 20 dB decrease in A_{OL} per decade, the closure frequency is always less than the gain bandwidth. The exact closure frequency must be determined to accurately select the optimal f_{z1} frequency.

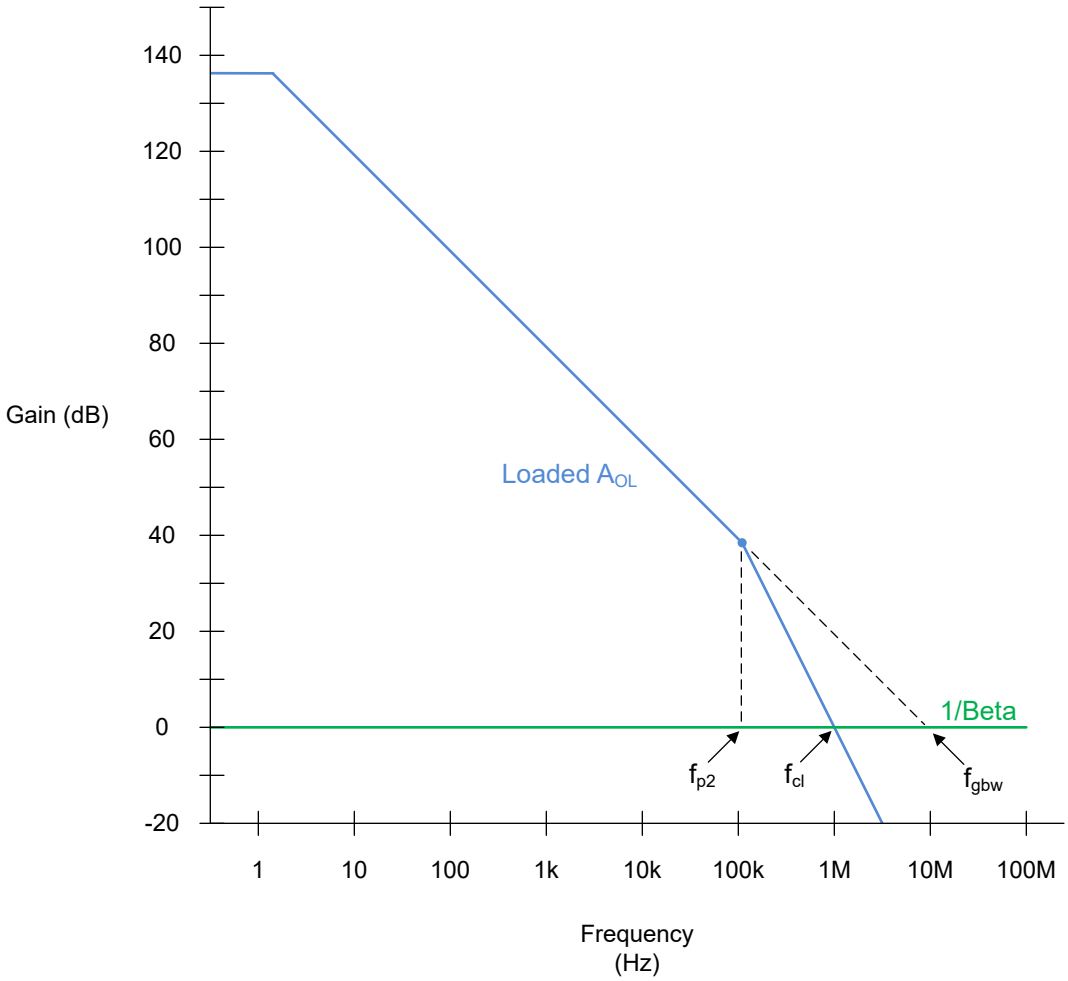


Figure 5-2. Amplifier Open-Loop Gain with Capacitive Loading

Figure 5-2 plots an amplifier's loaded A_{OL} curve in relation to the frequencies f_{p2} and f_{gbw}. Looking at this bode plot geometrically reveals two triangles with known slopes and vertices that intercept at f_{cl}. Assuming a second order system with consistent slopes of -20 dB/decade and -40 dB/decade, f_{cl} is always located at the midpoint between f_{p2} and f_{gbw} on the logarithmic axis. With a known load capacitance, and data sheet extracted values for R_O and f_{gbw}, the following equations can be used to solve for f_{cl}.

$$log_{10}\left(f_{cl}\right) = \frac{log_{10}\left(f_{p2}\right) + log_{10}\left(f_{gbw}\right)}{2} \tag{7}$$

$$f_{cl} = 10^{\frac{log_{10}\left(f_{p2} \cdot f_{gbw}\right)}{2}} \tag{8}$$

$$f_{cl} = \sqrt{f_{p2} \cdot f_{gbw}} \tag{9}$$

Setting f_{z1} equal to f_{cl}, and considering the shift in f_{p2} due to R_{ISO} results in Equation 10.

$$f_{z1} = \sqrt{f_{p2}^{*} \cdot f_{gbw}} \tag{10}$$

Combining Equation 10 with Equation 5 produces Equation 11.

$$\frac{1}{2\pi \cdot R_{ISO} \cdot C_{LOAD}} = \sqrt{\frac{f_{gbw}}{2\pi[R_O + R_{ISO}]C_{LOAD}}} \tag{11}$$

Simplification results in the following quadratic equation for R_{ISO} in standard form.

$$\left(2\pi \cdot C_{LOAD} \cdot f_{gbw}\right){R_{ISO}}^{2} - R_{ISO} + R_O = 0 \quad (12)$$

Using the quadratic formula to solve for R_{ISO} with the assumption that R_{ISO} must be positive results in the equation that was used to determine the optimal R_{ISO} in Section 3.

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \cdot R_O \cdot C_{LOAD} \cdot f_{gbw}\right)}}{4\pi \cdot C_{LOAD} \cdot f_{gbw}} \quad (13)$$

Where,

- f_{gbw} is the gain bandwidth of the amplifier in Hz, as defined in the data sheet
- R_O is the amplifier's open-loop output impedance in Ohms, as defined in the data sheet
- C_{LOAD} is the load capacitance in Farads

For an amplifier driving a large capacitive load, Equation 13 can be used to quickly derive the isolation resistance required to target 50°-60° of phase margin. Spice simulation tools such as TINA-TI must be used to verify the resultant phase margin, as this can vary considerable depending on the initial phase margin and other circuit conditions. TI Precision Labs online training videos show how to perform stability analysis for amplifier circuits in a variety of conditions.

Equation 13 is derived for amplifiers in a buffer configuration, but this equation can also be used for gain stages by adjusting the frequency term to account for the gain bandwidth, as in Equation 14.

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \cdot R_O \cdot C_{LOAD} \cdot \frac{f_{gbw}}{A_V}\right)}}{4\pi \cdot C_{LOAD} \cdot \frac{f_{gbw}}{A_V}} \quad (14)$$

Where A_V equals the non-inverting gain of the amplifier stage in V/V.

The feedback network in gain configurations can produce additional poles and zeros in the amplifier's 1/Beta and loaded A_{OL} curves that can contribute to instability. In these cases, further analysis is required and additional stabilization techniques such as feedback compensation can be implemented. Always use spice simulation tools such as TINA-TI to verify that the circuit is stable and operating properly.

6 Summary

Amplifier circuits driving large capacitive loads become unstable due to the interaction between the open-loop output impedance and the load capacitance. When driving a large capacitive load, an optimal isolation resistor must be implemented to maintain closed-loop stability with minimal voltage error. For amplifiers with resistive open-loop output impedance, an equation was derived to quickly determine an optimal R_{ISO} value. The magnitude of R_{ISO} is dependent on the magnitude of the load capacitance, the gain bandwidth of the amplifier, and the open-loop output impedance. Amplifiers with low open-loop output impedance are best for driving capacitive loads.

The analysis in this document considers amplifiers with resistive output impedance over frequency. Certain amplifier architectures exhibit a complex output impedance, Z_O, across the bandwidth of the amplifier. Amplifiers with complex output impedance require further analysis and additional techniques to optimize capacitive load-drive stability. The scope of this article is limited to amplifiers that exhibit a resistive output impedance similar to the OPA392 output impedance shown in Figure 1-1.

7 References

- Texas Instruments, *OPAx392 Precision, Low-Offset-Voltage, Low-Noise, Low-Input-Bias-Current, Rail-to-Rail I/O, e-trim™ Operational Amplifiers*, data sheet.
- Texas Instruments, *Stability Analysis of Voltage-Feedback Op Amps*, application note.
- Texas Instruments, *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using Z_{OUT}*, application note.
- Texas Instruments, *TI Precision Labs – Stability*.
- Texas Instruments, *TINA-TI*.

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