Application Report
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Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031

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ABSTRACT

Designing an analog front-end (AFE) for a power-line modem can be very challenging. Using the AFE031 simplifies this task and allows the designer to focus on the critical elements of the design, such as the line coupling interface, circuit protection, and printed circuit board (PCB) thermal design. This report uses the AFE031 to demonstrate an effective method of designing and testing an AFE for a power-line communications modem.

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1 Introduction

The AFE031 is an integrated power-line communications analog front-end device that consists of a variety of functional blocks; the device is driven by a microcontroller. The AFE031 is designed to work with a minimum of external components, and only a few additional passive components are required for the device to work in a range of AFE designs.

Table 1 summarizes the different functional blocks within the AFE031.

Table 1. AFE031 Functional Blocks

Block	Description
PA	The PA block includes the power amplifier (PA) and associated biasing circuitry
TX	The TX block includes the Tx Filter and the Tx_PGA
RX	The RX block includes the Rx_PGA1, the Rx Filter, and the Rx_PGA2
ERX	The ERX block includes the two-wire receiver support circuitry
ETX	The ETX block includes the two-wire transmitter support circuitry
DAC	Digital-to-analog converter block
ZC	The ZC block includes two zero-crossing detectors
REF1	Midscale bias generator for PA block
REF2	Midscale bias generator for TX, RX, ERX, and ETX blocks

This application report contains the following sections:

- Section 2 describes in detail how to connect each of the functional blocks and signals to the AFE031.
- Section 3 discusses how to interface the AFE031 to the ac mains.
- Section 4 explains how to protect the AFE031 from line transients.
- Section 5 summarizes the power-supply requirements for a power-line communications modem design.
- Section 6 reviews the general concepts related to power consumption in these designs.
- Section 7 presents the recommended method for thermal management using this device.

2 Interfacing the AFE031 to the Microcontroller

Figure 1 shows the digital circuitry of the AFE031 connected to a TMS320F28x microcontroller (MCU).

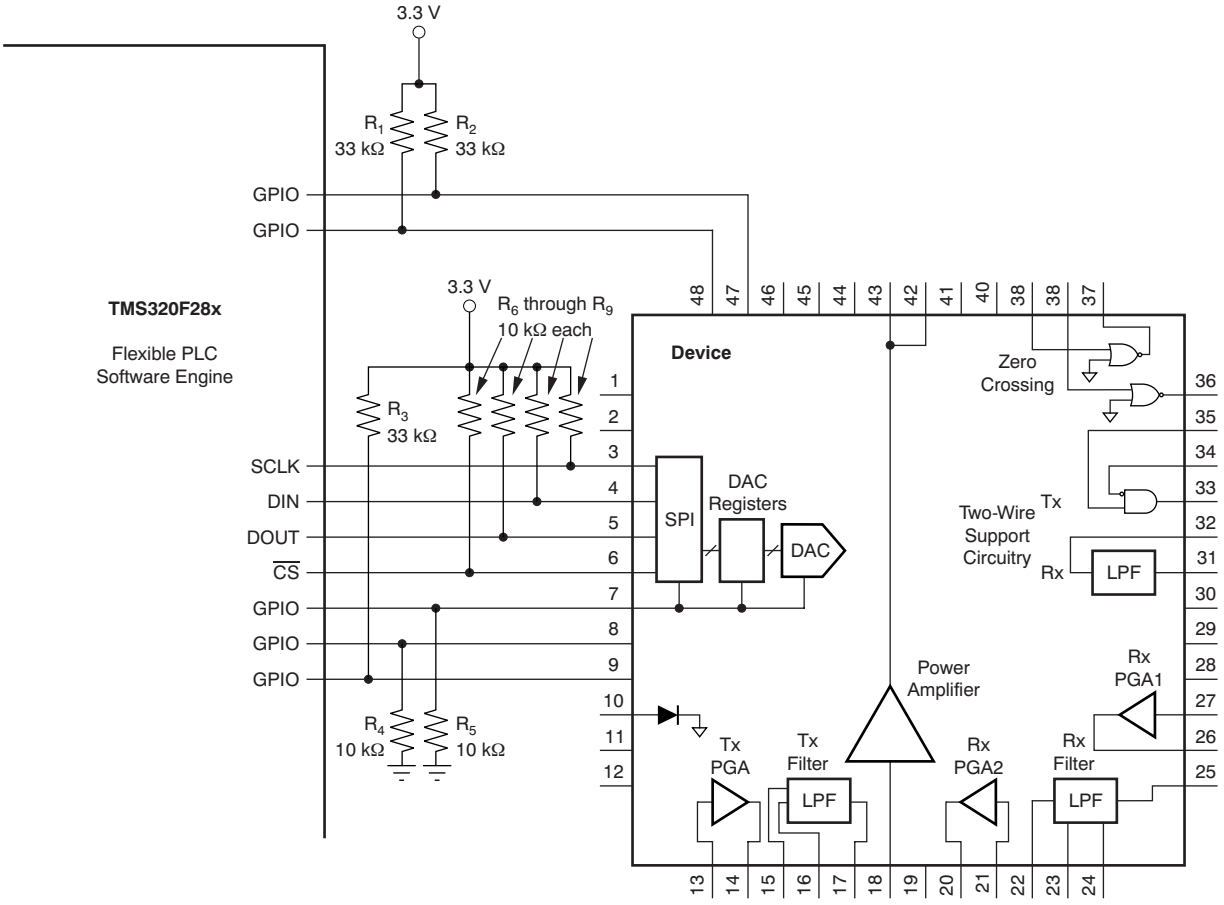


Figure 1. Digital Connections from AFE031 to the MCU

2.1 Serial Interface

The AFE031 incorporates a four-wire serial peripheral interface (SPI™) with these signals:

- DIN: Data input driven by the master
- DOUT: Data output driven by the slave
- SCLK: Clock sourced by the SPI master
- $\overline{CS}$: Chip select driven by the master to select the slave

It is recommended to use 10-kΩ or greater pull-up resistors to pull the signals into a default state when the master outputs are 3-stated, such as when the MCU master is in reset. The serial interface is used to program the AFE031 Tx gain and frequency response, Rx gain and frequency response, and various power-saving modes.

The AFE031 provides five additional connections to the microcontroller. Use of these pins is strictly optional and will depend upon the specific application requirements.

- Digital-to-analog converter (DAC) and SD, both defined as inputs
- TX_FLAG, RX_FLAG, and INT, defined as open-drain outputs

The *DAC* input is used to place the AFE031 into DAC mode in order to transmit data.

SD is used to enable or disable all circuit blocks inside the AFE031, including the SPI. Using the SD pin to disable the AFE031 places the device in its lowest power consumption operating mode.

TX_FLAG is used to indicate that both the Tx_PGA and Tx_Filter are configured and ready for transmission. A low TX_FLAG signals that the device is ready for transmission; TX_FLAG high signals that the device is not ready for transmission.

RX_FLAG is used to indicate that the Rx_PGA1, Rx_Filter, and Rx_PGA2 are configured and ready for reception. A low Rx_Flag indicates that the device is ready for reception. Rx_Flag high signals that the device is not ready for reception.

The *INT* pin is used to detect an interrupt condition. The AFE031 can be programmed to be interrupted under the following conditions:

- Current overload
- Thermal overload

Current Overload

The user can program the maximum output current from the Power Amplifier (PA) with the external R_{SET} resistor connected between PA_I_{SET} (pin 46) and ground. If a fault condition should occur and cause an overcurrent condition, the I_Flag register is then set to a '1' if the I_Flag_En bit is enabled. Refer to the AFE031 product data sheet for a description of the relationship between R_{SET} and the current limit.

Thermal Overload

The AFE031 contains internal protection circuitry that automatically disables the PA output stage if the junction temperature exceeds +150°C. If a fault condition should occur that causes a thermal overload, the T_Flag register is set to a '1' if the T_Flag_En bit is enabled. The AFE031 includes a thermal hysteresis feature, and allows the PA to resume normal operation when the junction temperature drops to +135°C.

2.2 Transmitter (TX)

The transmission path includes four separate circuit functions: DAC, Tx_PGA, Tx Filter, and the PA.

- The DAC block features a 10-bit, rail-to-rail DAC
- The Tx programmable gain amplifier (PGA) features four different gains: –12 dB, –6 dB, –3 dB, and 0 dB.
- The Tx Filter response works with either the Cenelec A band or the Cenelec B, C, and D bands
- The Power Amplifier block is capable of generating up to 26 V at 1.5 A.

Figure 2 shows a block diagram of the transmitter signal chain.

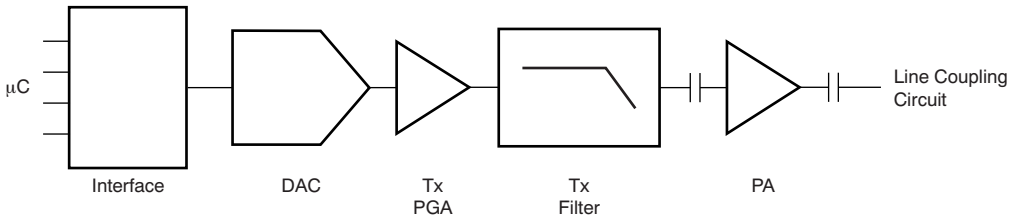


Figure 2. Block Diagram of TX Signal Chain

The MCU drives the transmitter using the serial interface in a special data streaming mode called *DAC mode*.

DAC mode allows the user to configure the AFE031 to receive data from the microcontroller during signal transmission. When the DAC pin is high, the SPI enters DAC mode; this mode streams data directly into the DAC registers. The sequence to write data into the DAC registers is:

- Set DAC pin high.
- Set $\overline{CS}$ pin low.
- Write a 10-bit word into DIN (inputs greater than 10 bits are truncated and left-justified).
- When the $\overline{CS}$ pin goes high, the DAC updates.

Figure 3 illustrates this sequence for '0000100000'.

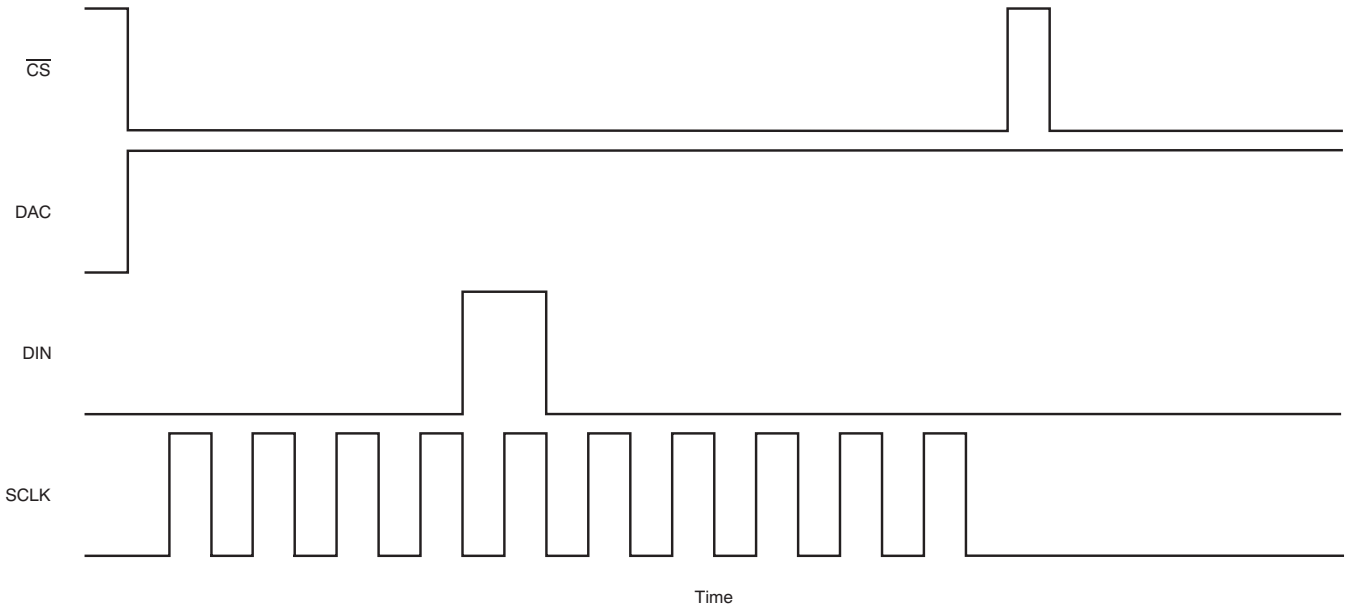


Figure 3. DAC Timing Illustration

Refer to Figure 4 for the recommended connections for the transmission section of the AFE031. Note that only three passive external components are required: R_{SET}, C_8 (the ac coupling capacitor), and C_9 (the noise reduction capacitor).

R_{SET} is used to program the maximum output current from the PA. This resistor is selected according to Equation 1.

$$R_{SET} = \left(20\ k\Omega \times \frac{1.2\ V}{\text{Current Limit}}\right) - 5\ k\Omega \quad (1)$$

Capacitor C_8 is used to ac-couple the output of the transmision low-pass filter (LPF) to the input of the PA. This capacitance blocks any dc offsets from the PA input, decouples the high-voltage circuitry of the PA from the low-voltage circuitry of the Tx filter, and forms a high-pass response in the overall transmission filter transfer function. The high-pass cutoff is calculated using Equation 2.

$$C_8 = \frac{1}{(2 \times \pi \times \text{High-Pass Cutoff Frequency} \times 2\ k\Omega)} \quad (2)$$

NOTE: C_8 should have a minimum voltage rating equal to that of the PA supply voltage.

C_9 is optional, and is used to reduce noise coupled in from the PA supply voltage. A single-order LPF is formed by C_9 and the internal midscale bias generator input impedance. The midscale bias generator associated with REF1 provides a stable, one-half PA supply voltage at the PA output; the output signal swings around this voltage.

The filter frequency associated with C_9 is determined as shown in Equation 3.

$$f = \frac{1}{[2 \times \pi \times 4\ k\Omega \times (C_9 + 10\ pF)]} \quad (3)$$

Figure 4 shows the AFE031 transmitter connections.

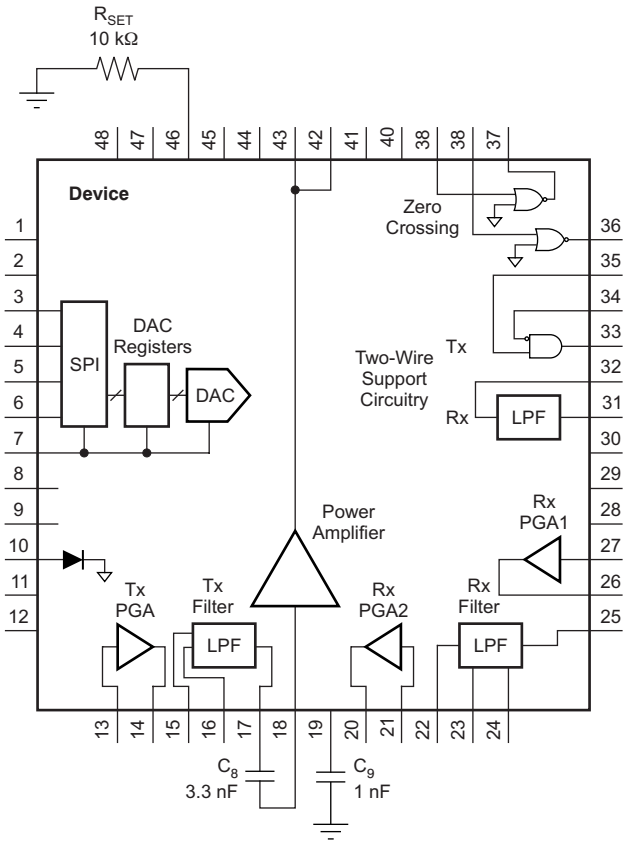


Figure 4. AFE031 Transmitter Connections

2.3 Receiver (RX)

The receiver path includes three separate circuit functions (Rx_PGA1, Rx Filter, and Rx_PGA2).

- The Rx_PGA1 has four different gains: –12 dB, –6 dB, 0 dB, and 6 dB
- The Rx Filter Response block can be configured for either the CENELEC A band or the CENELEC B, C, and D bands
- The Rx_PGA2 also has four different gains: 0 dB, 12 dB, 24 dB, and 36 dB

Figure 5 shows the block diagram of the receiver signal chain.

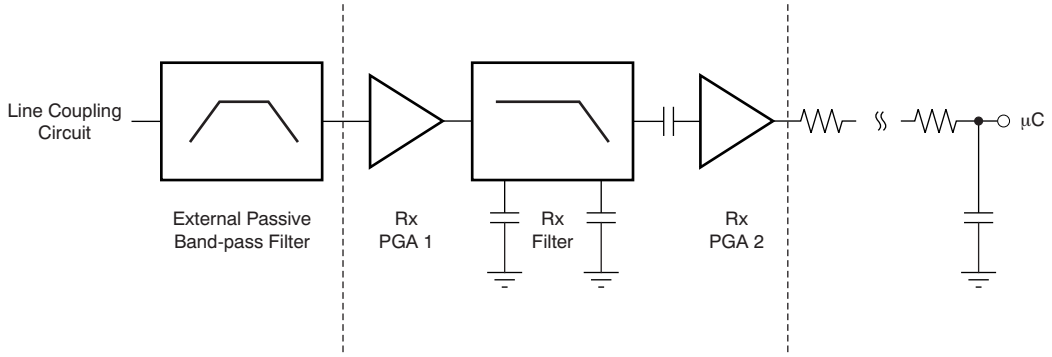
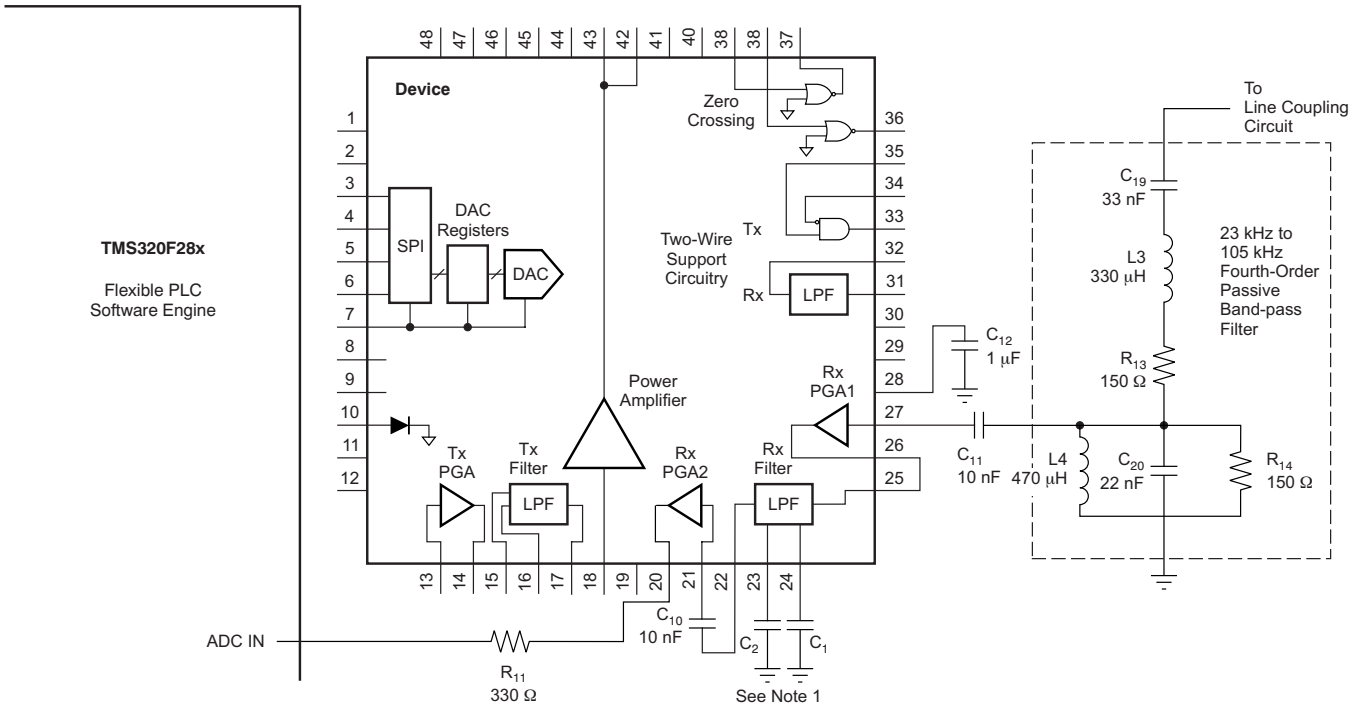


Figure 5. Block Diagram of Rx Signal Chain

Figure 6 shows the recommended connections for the receiver section of the AFE031. Note that only six passive external components are required.



(1) Recommended values for C_1 and C_2:

1. C_1:
   - Cenelec A: 680 pF
   - Cenelec B, C, D: 270 pF
2. C_2:
   - Cenelec A: 680 pF
   - Cenelec B, C, D: 560 pF

Figure 6. AFE031 Receiver Connections

R_{11} is optional and is used to isolate the Rx_PGA2 output from the input of the analog-to-digital converter (ADC) internal to the MCU. Additional filtering for the Rx_PGA2 output can be added if deisred, but is generally not required.

Capacitor C_{10} is used to ac-couple the output of the receiver LPF to the input of the Rx_PGA2. This capacitance blocks any dc offsets from the Rx_PGA2 input and forms a high-pass response in the overall receive filter transfer function. The high-pass cutoff frequency is calculated using Equation 4.

$$C_{10} = \frac{1}{(2 \times \pi \times \text{High-pass Cutoff Frequency} \times \text{Rx PGA2 Input Resistance})} \quad (4)$$

NOTE: C_{10} should have a minimum voltage rating equal to that of the AVDD supply voltage.

Table 2 shows the input impedance of Rx_PGA2.

Table 2. Input Impedance of Rx_PGA2

PGA	PGA Gain	Input Impedance
Rx_PGA2	G = 64 V/V	1.7 kΩ
Rx_PGA2	G = 16 V/V	6.3 kΩ
Rx_PGA2	G = 4 V/V	21 kΩ
Rx_PGA2	G = 1 V/V	53 kΩ

Capacitors C_1 and C_2 are used to set the Rx filter bandwidth. These two external capacitors are required for proper frequency response and low-noise operation. Table 3 lists the recommended values for C_1 and C_2.

Table 3. C_1 and C_2 Recommended Values

Component	C_1	C_2
Cenelec A	680 pF	680 pF
Cenelec B, C, D	270 pF	560 pF

C_{12} is optional and is used to reduce noise coupled in from the AVDD supply voltage. A single-order LPF is formed by C_{12} and the internal midscale bias generator input impedance. The midscale bias generator associated with REF2 provides a stable, one-half AVDD supply voltage that is used for biasing many of the internal low-voltage signal paths in both the Tx and Rx blocks.

The filter frequency associated with C_{12} is determined by Equation 5.

$$f = \frac{1}{[2 \times \pi \times 4\ \text{k}\Omega \times (C_9 + 10\ \text{pF})]} \quad (5)$$

The voltage at the input of Rx_PGA1 is internally level-shifted to $\frac{AV_{DD}}{2}$.

C_{11} is used to ac-couple the incoming signals from the line coupling circuit into the level-shifted Rx_PGA1 input.

2.4 Passive Bandpass Filter

The fourth-order passive bandpass filter is optional, but recommended for applications where high performance is required. This filter removes any unwanted out-of-band signals from reaching the active filters internal to the AFE031. Figure 7 shows the passive filter response for the values shown in Figure 6, with f_1 = 24 kHz and f_2 = 105 kHz.

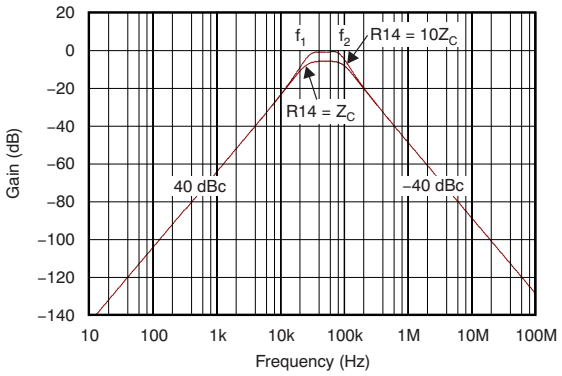


Figure 7. Recommended Passive Filter Response

For a passive filter response different from the recommended response, the following steps can be referenced:

Step 1. Choose the filter characteristic impedance, Z_C.

- For –6-db passband attenuation: Set $R_{12} = R_{14} = Z_C$
- For 0-db passband attenuation: Set $R_{12} = Z_C$, and $R_{14} = 10 \times Z_C$

Z_C can be determined using Equation 6.

$$C_{19} = \frac{1}{(2 \times \pi \times f_1 \times Z_C)}$$

$$C_{20} = \frac{1}{(2 \times \pi \times f_2 \times Z_C)}$$

$$L_3 = \frac{Z_C}{(2 \times \pi \times f_2)}$$

$$L_4 = \frac{Z_C}{(2 \times \pi \times f_1)} \quad (6)$$

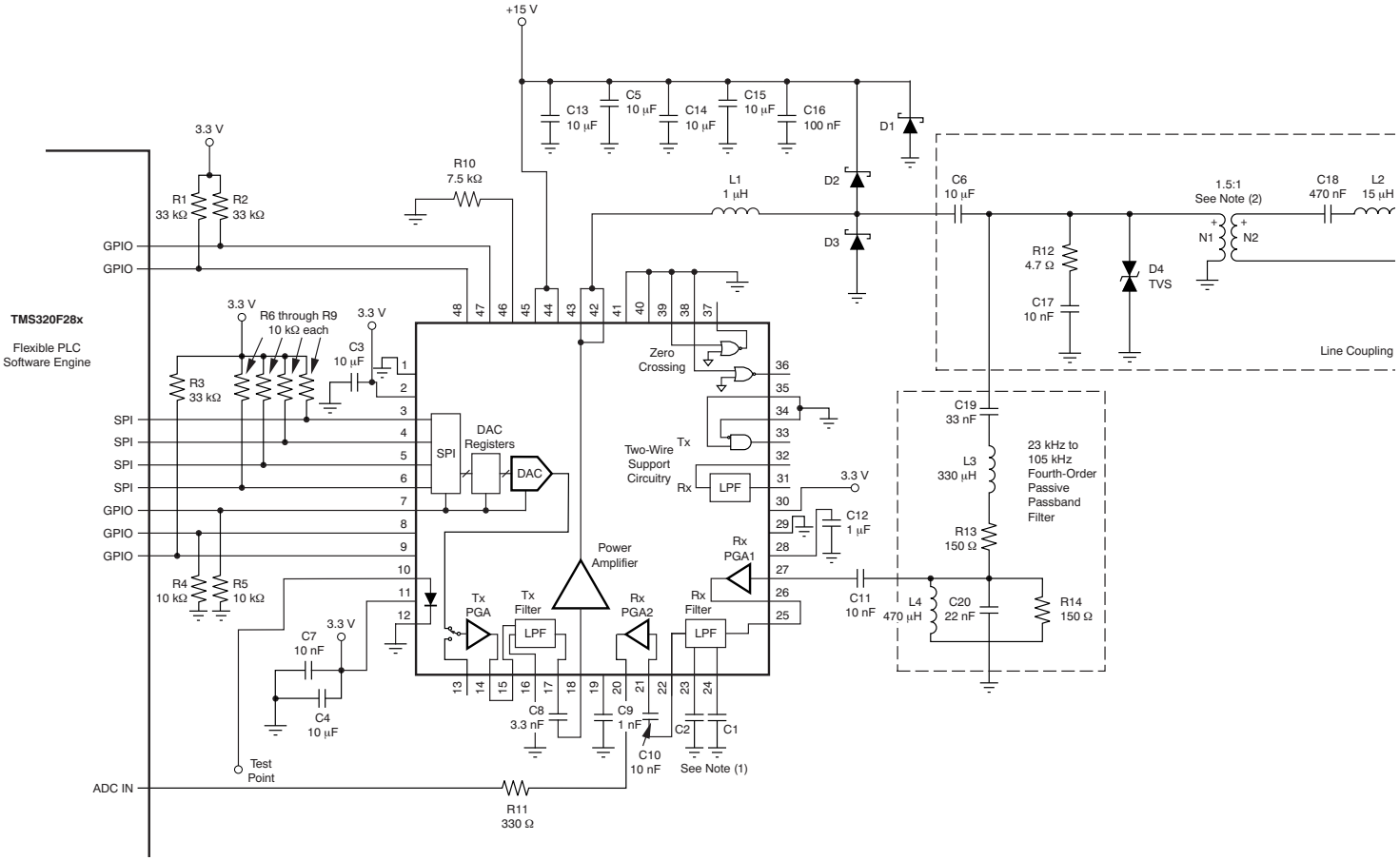
Step 2. Capacitor C_{11} is used to ac-couple the input of the Rx_PGA1. This capacitance blocks any dc signal from entering the receiver and forms a high-pass response in the overall receiver filter transfer function. The high-pass cutoff is calculated from Equation 7 and the values listed in Table 4.

$$C_{11} = \frac{1}{(2 \bullet \pi \bullet \text{High-pass Cutoff Frequency} \bullet \text{Rx PGA2 Input Resistance})} \quad (7)$$

Table 4. Input Impedance of Rx_PGA1

PGA	PGA Gain	Input Impedance
Rx_PGA1	G = 2 V/V	10 kΩ
Rx_PGA1	G = 1V/V	15 kΩ
Rx_PGA1	G = 0.5 V/V	20 kΩ
Rx_PGA1	G = 0.25 V/V	24 kΩ

Figure 8 shows the complete schematic for the basic analog front-end for power-line communications applications.



A Recommended values for C_1 and C_2:

1. C_1:
   - Cenelec A: 680 pF
   - Cenelec B, C, D: 270 pF
2. C2:
   - Cenelec A: 680 pF
   - Cenelec B, C, D: 560 pF

Figure 8. Basic Analog Front-End Application Schematic

2.5 Zero Crossing Block

The Zero Crossing block consists of two independent zero crossing detectors (ZCDs). These components are used for detecting the ac mains signal when crossing zero voltage. Applications such as power-line communications typically need this type of information or signal to properly synchronize. Only one ZCD is generally used; however, in two-phase or three-phase applications, multiple ZCDs can be used.

Figure 9 shows the internal structure of the zero crossing detector.

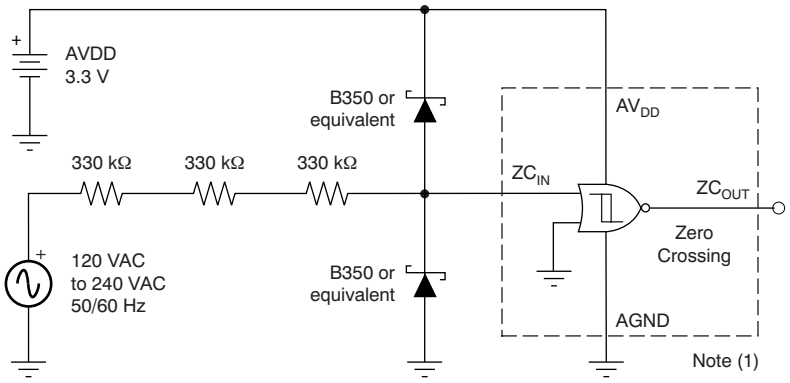


Figure 9. Zero Crossing Detector Block

Figure 10 illustrates the zero crossing detector response.

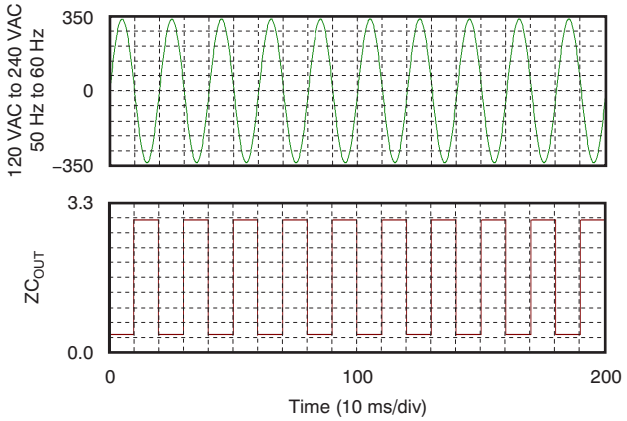


Figure 10. Zero Crossing Detector Response

The ZC_OUT pin is connected to any microcontroller GPIO.

2.6 Two-Wire Support Circuitry (ETx and ERx Blocks)

The AFE031 contains a two-wire transmitter block, ETx, and a two-wire receiver block, ERx. These blocks support communications that use amplitude shift keying (ASK) with on-off keying (OOK) modulation.

The ETx block is a gated driver that allows for transmission of a carrier input signal and modulating input signal. For typical applications, a 50-kHz square wave carrier signal is applied to E_Tx_Clk while the modulating signal is applied to E_Tx_In. The output (E_Tx_Out) is then in a high-impedance state when E_Tx_In is '1'. Figure 11 shows the relationship between E_Tx_Clk, E_Tx_In, and E_Tx_Out.

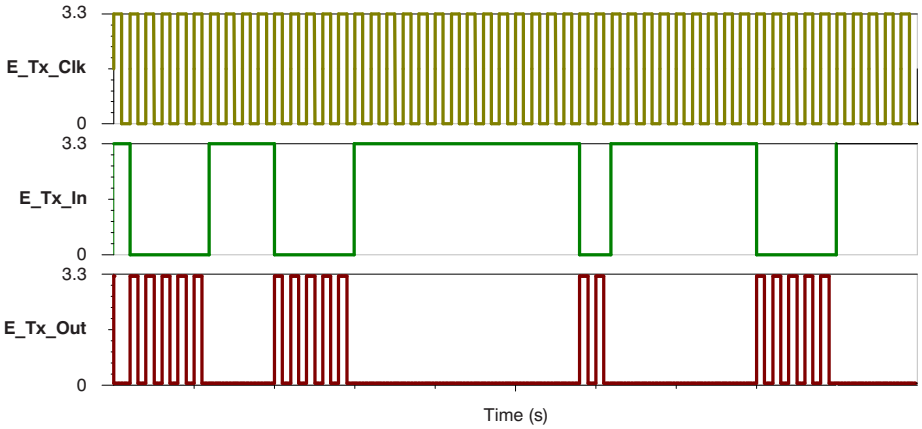


Figure 11. ETx Block Transfer Function

The ERx Block consists of a low-pass analog filter configured in an inverting gain of –4.5 dB. This block, along with an external capacitor, can be used to create a passband filter response as shown in Figure 12.

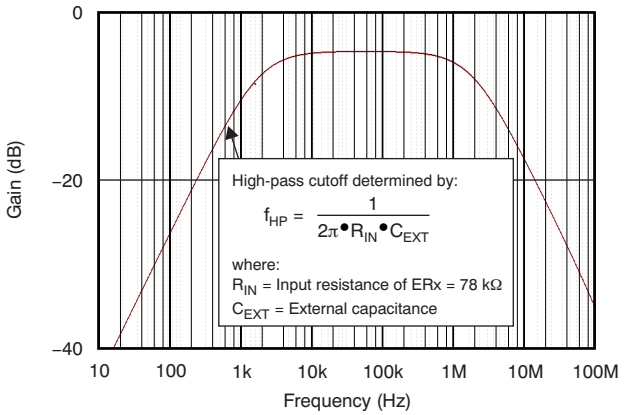


Figure 12. ERx Block Frequency Response

The E_Rx_Out pin can be directly connected to either an available analog-to-digital converter (ADC) input or GPIO on the host microcontroller. Figure 13 illustrates a typical two-wire application for ETx and ERx.

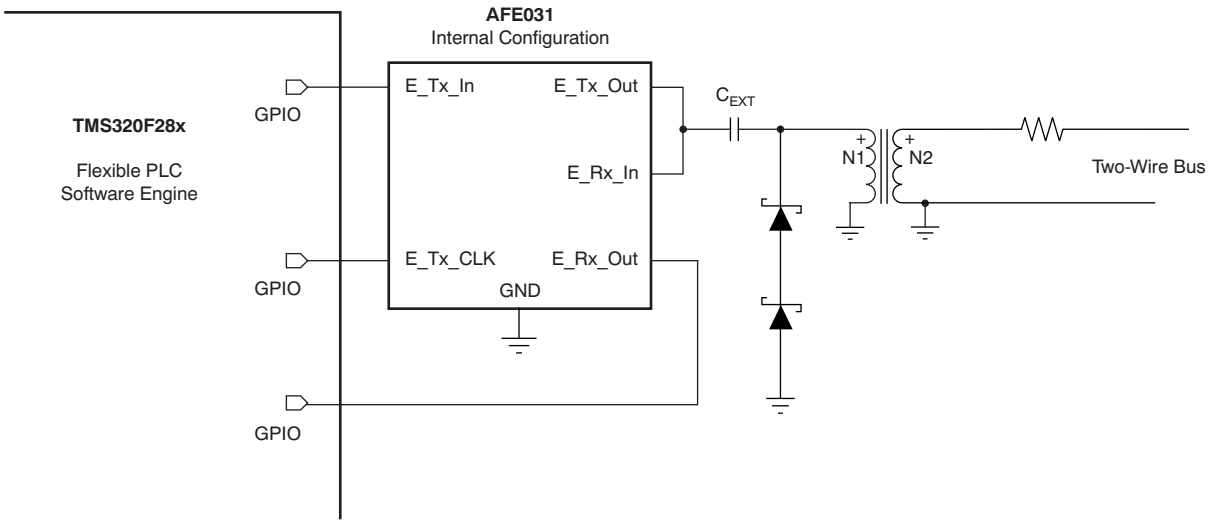


Figure 13. Typical Two-Wire Application for ETx and ERx

3 Interfacing the AFE031 to the AC Mains

The line coupling circuit is one of the most critical segments of a power-line modem. The line coupling circuit has two primary functions: first, to prevent the high voltage, low frequency of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry; and second, as the name implies, to couple the modem signal to and from the ac mains. A simplified, typical line coupling circuit is shown in Figure 14.

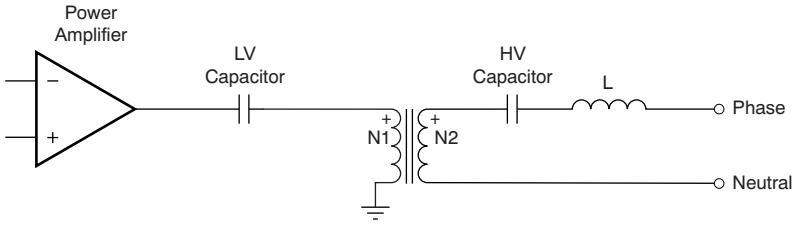


Figure 14. A Simplified Line Coupling Circuit

3.1 Low-Voltage Capacitor

The low-voltage capacitor, or LV Cap, couples the time-varying components of the PA output signal into the line coupling transformer. The LV Cap should have a large enough capacitance to appear as a low impedance throughout the signal band of interest; 10-µF is a common value for signals in the range of 35 kHz to 150 kHz. The voltage rating of the LV cap should be sufficient to withstand the clamping voltage of the TVS diode (that is, the transient voltage suppressor; see Section 4.2 for more information) operating under surge conditions. Generally, this limit should be equal to the PA supply voltage or slightly higher.

3.2 High-Voltage Capacitor

The high-voltage capacitor (HV Cap) blocks the low-frequency mains voltage by forming a voltage divider with the winding inductance of the line coupling transformer. In many applications, a maximum reactive power (VA limit) on the HV Cap may be required. To meet this requirement, the HV Cap value is calculated by Equation 8.

$$HVCap = \frac{VA_{LIMIT}}{VAC^2(2 \times \pi \times F)} \quad (8)$$

For a 240-VAC, 50-Hz application with a 10-VA limit, the maximum value for the HV Cap is shown in Equation 9.

$$HVCap \leq \frac{10}{(240^2 \times 2 \times \pi \times f)} \cong 550 \text{ nF} \quad (9)$$

A 470-nF capacitor is frequenly used in these types of applications. A metallized polypropylene electromagnetic interference and radio frequency interference (EMI/RFI) suppression capacitor is recommended because of the low loss factor associated with the dielectric, which results in minimal internal self-heating. Operating the capacitor at approximately 80% of its ac-rated voltage ensures a long component operating life. See Section 6 of this document for additional discussion on selecting the correct HV Cap value to withstand impulses on the mains.

3.3 Inductor

The inductor that is connected in series with the HV Cap is required when driving low line impedances and the HV Cap is restricted to approximately 470 nF for the reasons previously stated. In applications that operate in the Cenelec A band, the impedance of the 470-nF capacitance at 40 kHz is approximately 8.5 Ω. If the application requires the ability to drive a 2-Ω load, for example, this series impedance is restrictive. Adding the series inductor can mitigate this effect. To properly select the value of the inductance, the operating frequency range of the system must be known. A common example would be the PRIME frequency band, which is approximately 40 kHz to 90 kHz. Selecting the HV Cap and inductor to have a resonant frequency in the center of the frequency band is recommended, and results in a series inductor value of 12.8 µH and HV Cap value of 470 nF. The inductor should be sized to be capable of withstanding the maximum load current without saturation, using Equation 10 as a guideline.

$$L = \frac{1}{HVCap \times (2 \times \pi \times f)^2} \quad (10)$$

3.4 Line Coupling Transformer

Most power-line communication transformers are compact, with turns ratios between 1:1 and 4:1, low leakage inductance, and approximately 1-mH of winding inductance. It is the voltage divider formed by the HV Cap and winding inductance that divides down the ac mains voltage and reduces it to negligible levels at the modem output. Figure 15 shows the equivalent circuit formed with the HV Cap and the line coupling transformer.

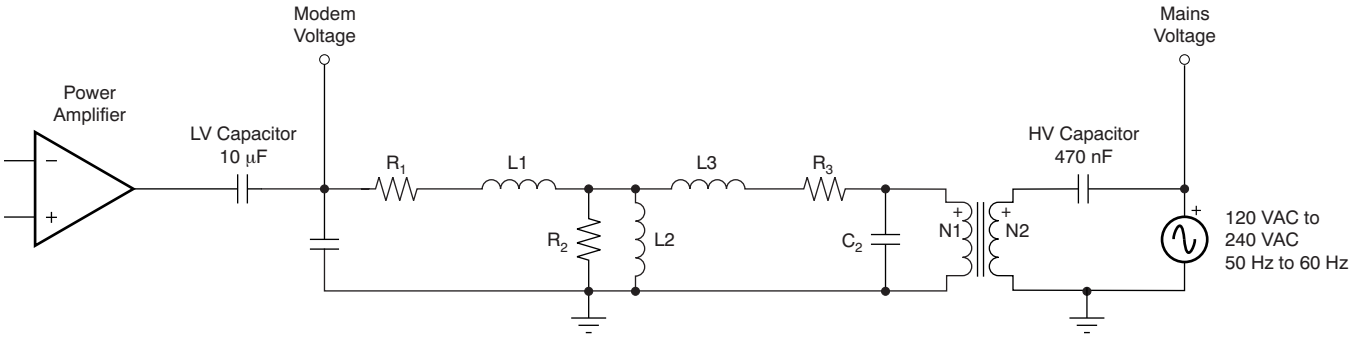


Figure 15. Voltage Divider with HV Cap and Transformer Equivalent Circuit

where:

- R_1 is the series dc resistance of the primary winding
- R_2 is the shunt resistance reflecting losses in the core
- R_3 is the series dc resistance of the secondary winding, reflected to the primary side
- L1 is the primary leakage inductance
- L2 is the open circuit inductance of the primary winding
- L3 is the secondary leakage inductance reflected to the primary side
- C_1 is the self-capacitance of the primary winding
- C_2 is the self-capacitance of the secondary winding reflected to the primary side

For the purposes of analysis, this circuit can be simplified as shown in Figure 16.

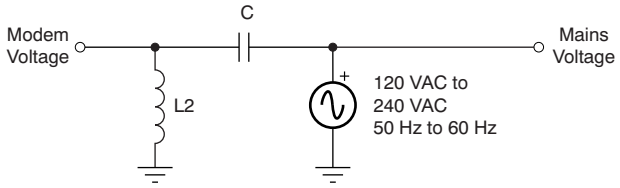


Figure 16. Simplified AC Mains Voltage Divider

where:

- L2 = OCL of the transformer primary
- C = HV Cap reflected to the primary side

In a typical line coupling circuit the ac mains voltage injected into the modem is approximately 20 mV_{PP}.

Table 5 lists the typical equivalent circuit component values for the power-line communication transformer (VITEC part number 70P7282) used in the Texas Instruments Power-Line Communications Evaluation Kit (available for purchase through the TI website; part number TMDSPLCKIT-V3).

Table 5. PLC Kit Transformer Parameters

Parameter	Label	Value	Units
Turns ratio	N1/N2	1.5:1	—
Primary DCR	R_1	0.028	Ω
Shunt Resistance	R_2	1M	Ω
Secondary DCR reflected to the primary side	R_3	0.045	Ω
Primary leakage inductance	L1	290	nH
Primary OCL	L2	1.1	mH
Secondary leakage inductance reflected to the primary side	L3	225	nH
Primary self-capacitance	C_1	24	pF
Secondary self-capacitance reflected to the primary side	C_2	11	pF

Determining the optimal turns ratio (N1/N2) for the power-line communication transformer is simple, and based on the principle of using the maximum output swing capability of the PA together with the maximum output current capability of the PA to achieve maximum power transfer efficiency into the load. Assuming the power-supply voltage and target load impedance are known, the turns ratio is determined as shown in Figure 17, and calculated with Equation 11 and Equation 12.

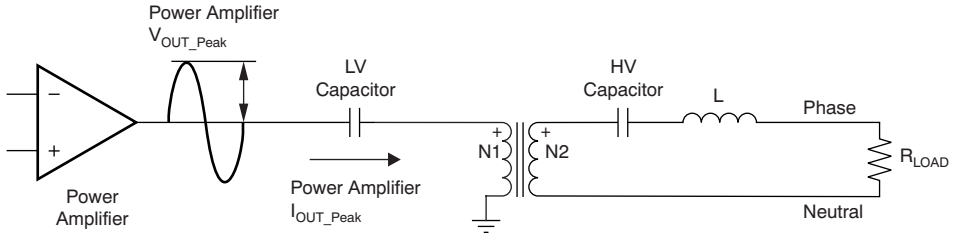


Figure 17. Line Coupling Circuit

$$\frac{PA,V_{OUT\_Peak}}{PA,\ I_{OUT\_Peak}} = R_{LOAD} \times \left(\frac{N_1}{N_2}\right)^2 \quad (11)$$

$$\text{Turns Ratio} = \frac{N_1}{N_2} = \sqrt{\frac{PA,V_{OUT\_Peak}}{PA,\ I_{OUT\_Peak} \times R_{LOAD}}} \quad (12)$$

If the actual transformer ratio turns ratio of N_1/N_2 is selected to be greater than the ideal value, the overall circuit output is then limited by the voltage swing of the PA. If N_1/N_2 is selected to be less than the ideal ratio, the output is limited by the maximum output current from the PA. If the ideal transformer ratio is used, the maximum output occurs as the amplifier approaches both its maximum output voltage and maximum output current. This condition results in the maximum power transfer efficiency to the load.

4 Protecting the AFE031 from Line Transients

Power-line communications are frequently harsh operating environment for electrical components connected to the ac line. Noise or surges from electrical anomalies such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions can damage high-performance integrated circuits if they are not properly protected. The AFE031 can survive even these harsh conditions but several simple recommendations must be followed. One recommendation is to clamp as much of the electrical disturbance before it reaches the AFE031 device with a multi-layer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a zener diode.

4.1 Metal Oxide Varistors

An MOV, as shown in Figure 18, is a device that has high resistance until its triggering voltage is exceeded. Once this voltage level has been exceeded, the MOV reduces its resistance and absorbs the energy from the pulse.

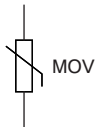


Figure 18. Metal Oxide Varistor

A typical MOV current-to-voltage (I/V) characteristic is shown in Figure 19.

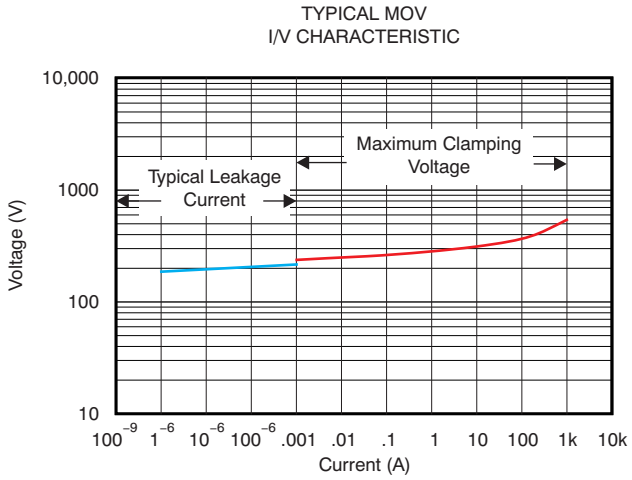


Figure 19. Typical MOV I/V Characteristic

By the nature of the materials and techniques used in the construction of these components, MOVs respond quickly to a fast transient pulse, have high instantaneous power ratings, and are well-suited for protection on the ac line. The maximum clamping voltages are typically specified in response to a high-speed transient similar to that shown in Figure 20. The 8/20 µs waveform is commonly associated as a waveform that represents the spectral content of lightning strikes.

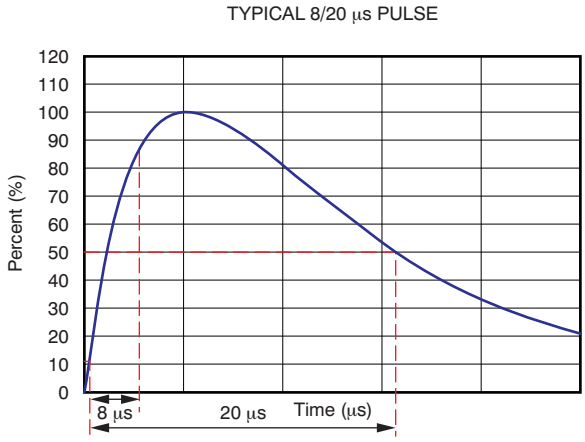


Figure 20. Typical 8/20-µs Pulse For MOV and TVS Performance Specification

There are several factors to consider when selecting an MOV:

- Working voltage
- Required amount of transient energy to be absorbed by the MOV
- Peak transient current
- Power dissipation

4.2 Transient Voltage Suppressors

Figure 21 shows a transient voltage suppressor.

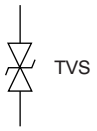


Figure 21. Transient Voltage Suppressor

A TVS is a very fast-acting clamping device that turns on in the case of an overvoltage condition, shunting the surge of current into ground. TVSs are rated primarily by the power handling capability and the clamping voltage. TVSs are available in either unidirectional or bi-directional configurations. For power-line communication applications, a bi-directional TVS is recommended; the component is placed next to the line coupling transformer.

Figure 22 shows the I/V characteristics for a typical bi-directional TVS.

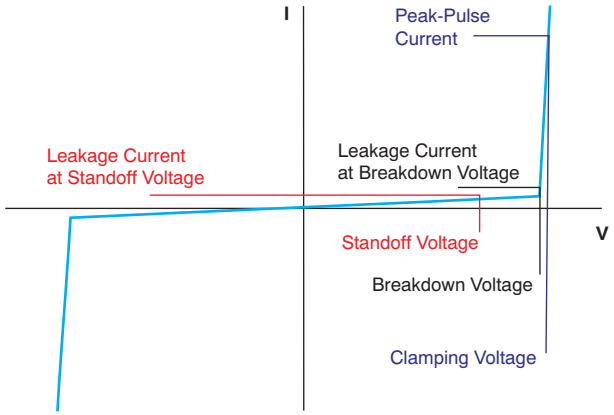


Figure 22. Typical Bi-Directional TVS I/V Characteristics

As a surge or pulse on the ac line occurs, the voltage rises across the TVS. If the voltage rises higher than the TVS breakdown voltage, the TVS turns on and rapidly changes from high impedance to low impedance, shunting current into ground. Note that the low-voltage capacitor between the PA output and the TVS blocks any dc voltage at the TVS. As a result, the normal FSK or OFDM signal from the PA appears to be centered around ground at the TVS. This condition requires the TVS to be bi-directional. Figure 23 illustrates this concept.

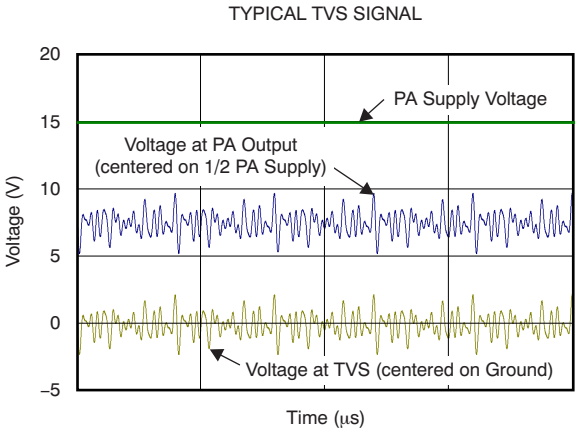


Figure 23. Typical Signal at the TVS

Because the signal is symmetric around ground at the TVS, the TVS breakdown voltage should be equal to approximately one-half of the PA power-supply voltage. It is important for the TVS to remain off during normal operation to avoid clipping and introducing distortions to the output signal. It is also important that the TVS turn on and clamp at the lowest possible voltage beyond normal operation to provide maximum protection.

4.3 Current-Steering Diodes

Current-steering diodes are shown in Figure 24.

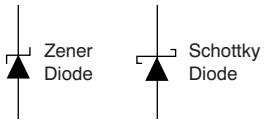


Figure 24. Current-Steering Diodes

While the MOV and TVS components clamp the pulse and either dissipate or re-direct most of the energy to ground, it is also recommended to place current-steering diodes at the output of the PA section of the AFE031. In the unlikely event a transient surge increases the PA output pin beyond its power-supply rail, low-drop Schottky diodes can steer the current around the AFE031 safely to ground. Maintaining a low (less than 0.8 V) forward voltage drop on the Schottky diode is recommended for maximum protection.

If the Schottky diode that connects the output of the PA to the power-supply rail turns on and becomes forward-biased, it is important to steer the current to ground without significantly disturbing the PA power-supply voltage. Placing a zener diode at the PA power-supply pins to ground provides a low-impedance path for surges that attempt to raise the power-supply voltage beyond the absolute maximum rated voltage for the AFE031.

Figure 25 shows the complete recommended line transient protection circuitry.

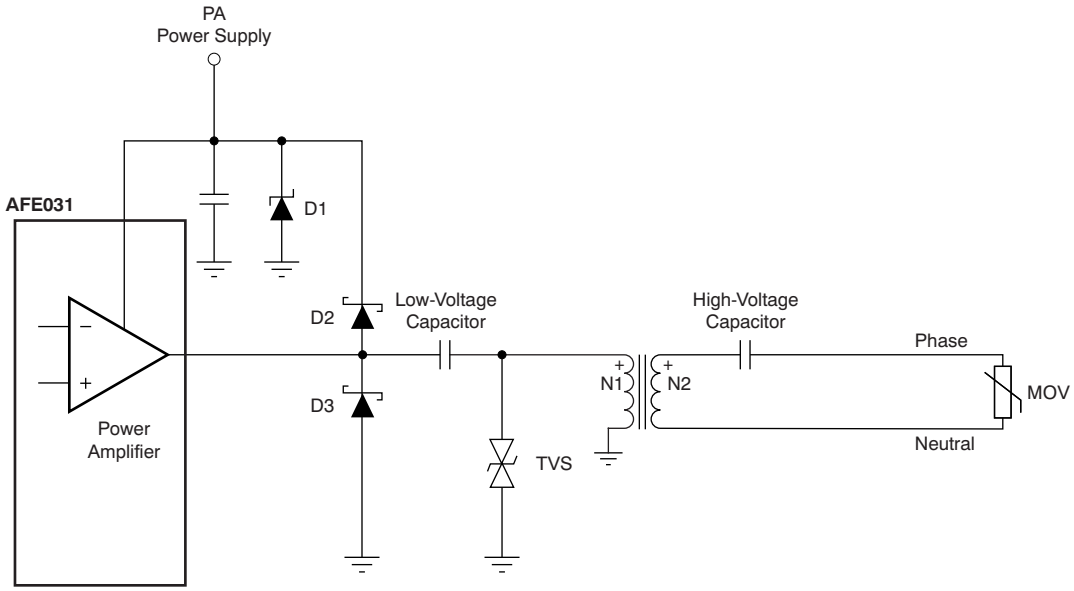


Figure 25. Recommended Line Transient Protection

Note that the HV Cap must be able to withstand pulses up to the clamping protection afforded by the MOV. A metallized polypropylene capacitor such as the 474MKP275KA from Illinois Capacitor, Inc.™ is rated for 50 Hz to 60 Hz, 250 VAC to 310 VAC and can withstand 24 impulses of 2.5 kV.

Table 6 lists the recommended transient protection devices.

Table 6. Recommended Transient Protection Devices

Component	120 VAC, 60 Hz		
	Description	**Manufacturer**	**Mfr Part No (or Equivalent)**
D1	Zener diode	Diodes, Inc.	1SMB59xxB(1)
D2, D3	Schottky diode	Diodes, Inc.	1N5819HW
TVS	Transient voltage suppressor	Diodec Semiconductor	P6SMBJxxC(2)
MOV	Varistor	LittleFuse	TMOV20RP140E
HV Cap	High-voltage capacitor	Illinois Capacitor, Inc	474MKP275KA(3)
Component	**240 VAC, 50 Hz**		
	Description	**Manufacturer**	**Mfr Part No (or Equivalent)**
D1	Zener diode	Diodes, Inc.	1SMB59xxB(1)
D2, D3	Schottky diode	Diodes, Inc.	1N5819HW
TVS	Transient voltage suppressor	Diodec Semiconductor	P6SMBJxxC(2)
MOV	Varistor	LittleFuse	TMOV20RP300E
HV Cap	High-voltage capacitor	Illinois Capacitor, Inc	474MKP275KA(3)

(1) Select the Zener breakdown voltage at the lowest available rating beyond the normal power-supply operating range.
(2) Select the TVS breakdown voltage at or slightly greater than (0.5 × PA_V_S).
(3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the requirements of the application. Note that when making a substitution, it is important in terms of reliability that the capacitor be selected from the same familiy or equivalent family of capacitors rated to withstand high-voltage surges.

5 Power-Supply Requirements

Determining the power-supply requirements requires only a straightforward analysis. The desired load voltage, load impedance, and available power-supply voltage or desired transformer ratio are all the parameters that must be known. In many power-line communication applications, such as PRIME, it is required to drive a 1-V_{RMS} signal into a 2-Ω load. From Figure 26, we calculate the minimum power-supply voltage required by adding the peak-to-peak load voltage; the voltage dropped across the HV Cap and inductor, V_2; the voltage dropped across the LV Cap, V_1; and twice the output swing to rail limit of the PA, V_{SWING}. For FSK and SFSK systems, the peak to average ratio is $\sqrt{2}$, while for OFDM systems this ratio is approximately 3:1.

These ratios must be considered when performing calculations that relate the RMS voltages and peak voltages during an analysis. Choosing a large value for the LV Cap results in the voltage drop (V_1) becoming negligible in most circumstances. The losses in the transformer are also negligible, even at high load currents, if the proper transformer with a low DCR is used. For FSK and SFSK systems, the voltage drop across the HV Cap and inductor, V_2, is also usually negligible; in OFDM systems, because of the wider operating bandwidth, voltage drop V_2 can be ignored and accounted for by using a 1.5x multiplier on the load voltage as an approximation. (**Note:** this approximation is only valid with a load impedance of 2 Ω for PRIME and G3. Voltage drop V_2 becomes negligible with increasing load impedance.

These assumptions greatly simplify the analysis.

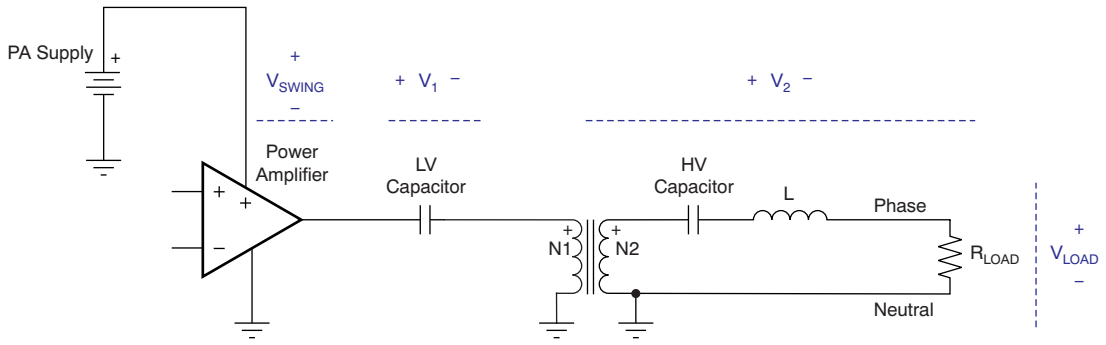


Figure 26. Typical Line Coupling Circuit

Table 7 summarizes the power-supply requirements for various power-line communication systems.

Table 7. Power-Supply Requirements

Parameter	FSK or SFSK	PRIME or G3 OFDM	Units
Frequency range	63 to 74	35 to 95	kHz
R_{LOAD}	2	2	Ω
V_{LOAD}	1	1	V_{RMS}
V_{LOAD}	1.414	3	V_{PEAK}
V_{LOAD}	2.828	6	V_{PP}
OFDM multiplier	—	1.5	—
V_{SWING}	2	2	V
Turns ratio, N1/N2	1.5	1.5	—
PA supply	8.25	17.5	V

Example:

For PRIME or G3 using an OFDM signal with a 2-Ω load and 1-V_{RMS} load voltage:

$PA_{Supply} = V_{LOAD} \times$ OFDM Multiplier × Turns Ratio + (2 × V swing)

$PA_{Supply} = 6\ V \times 1.5 \times 1.5 + (2 \times 2V)$

$PA_{Supply} = 17.5\ V$

See Figure 27 for an illustration of the recommended ac-dc power supply configuration using the UC28610.

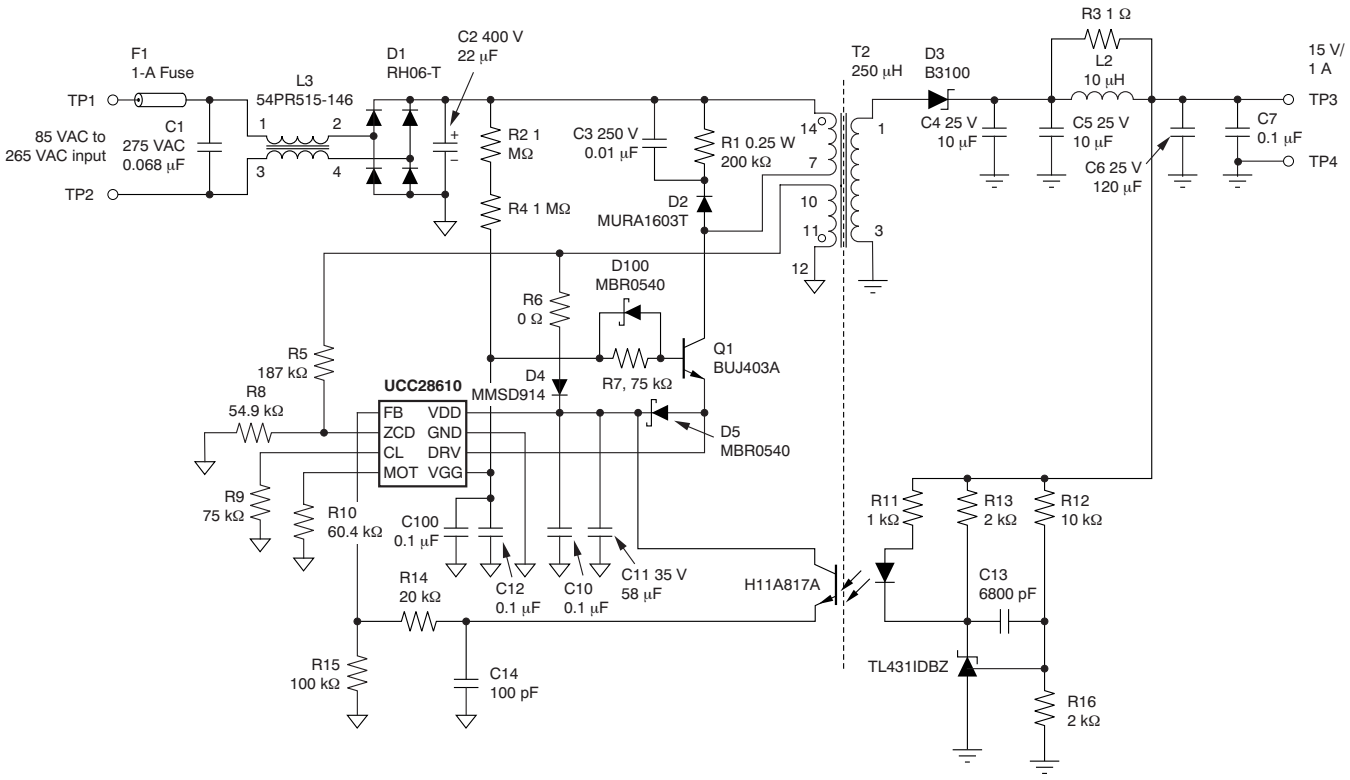


Figure 27. AC-DC Power Supply

6 Power Consumption

Calculating the power dissipation in the load and in the PA also requires only several direct calculations. The desired load voltage, load impedance, available powerr-supply voltage, and the transformer ratio are the only parameters required. In many power-line communication applications, such as PRIME, it is required to drive a 1-V_{RMS} signal into a 2-Ω load.

As Figure 28 shows, the power dissipation in the PA is determined by calculating the RMS value of the PA output current, and the voltage difference between the PA supply and RMS value of the PA output voltage. These two values are multiplied, and the the quiescent power of the PA is added.

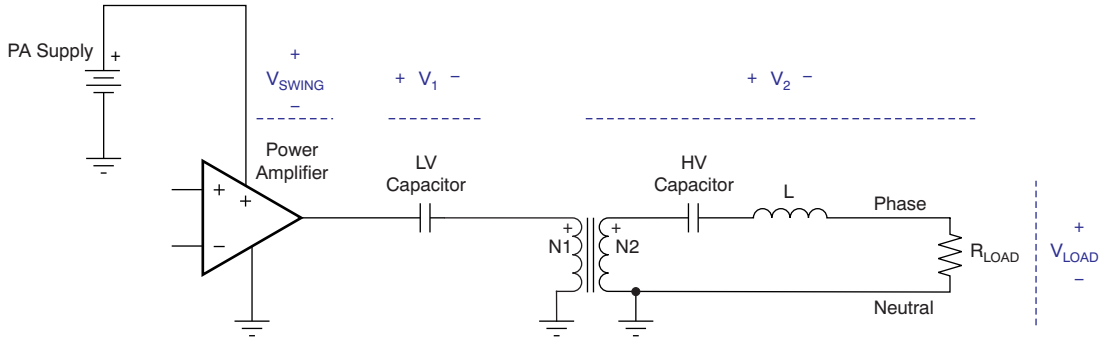


Figure 28. Line Coupling Circuit

The power in the load is given as Equation 13 shows.

$$P_{LOAD} = \frac{V_{LOAD\_RMS}^{2}}{R_{LOAD}} \quad (13)$$

The PA output current is given as calculated by Equation 14.

$$\text{PA, } I_{OUT\_RMS} = \frac{V_{LOAD\_RMS}}{R_{LOAD} \times \frac{N_1}{N_2}} \quad (14)$$

Because the output of the PA is always symmetric around $\frac{PA_{Supply}}{2}$, only the voltage difference between the PA supply and the RMS values of the PA output must be considered.

Figure 29 illustrates this concept for an OFDM signal.

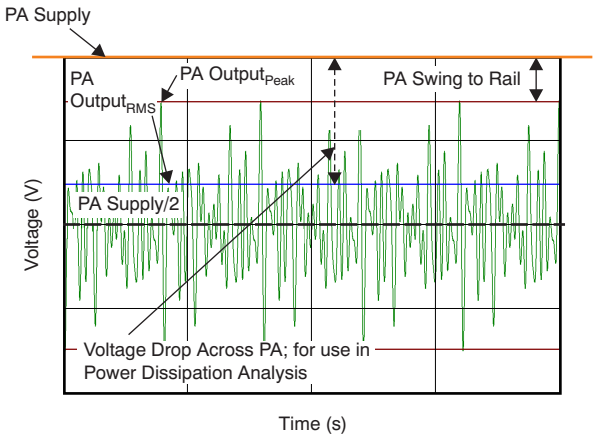


Figure 29. Typical OFDM Output Waveforms

$$\text{PA Output Voltage}_{RMS} = \frac{PA_{Supply}}{2} + V_{LOAD\_RMS} \times \frac{N_1}{N_2} \quad (15)$$

$$\text{PA Power Dissipation} = \text{Voltage Drop Across PA} \times \text{PA } I_{OUT\_RMS} \quad (16)$$

Table 8 summarizes the power dissipation values for common PLC applications.

Table 8. Power Dissipation

Parameter	FSK or SFSK	PRIME or G3 OFDM	Units
Turns ratio, N_1/N_2	1.5	1.5	—
R_{LOAD}	2	2	Ω
V_{LOAD}	1	1	V_{RMS}
I_{LOAD}	0.5	0.5	A_{RMS}
PA output voltage	6	10.75	V_{RMS}
Voltage drop across PA	3	6.25	V_{RMS}
PA output current	0.333	0.333	A_{RMS}
PA supply	9	17	V
PA power dissipation	1	2.1	W
Load power dissipation	0.5	0.5	W
Total	1.5	2.6	W

The power supply itself does not need to be designed to supply the peak PA current continuously. The peak demand for current is supplied by the power-supply bypass capacitance. The power-supply voltage is shown in Figure 30, along with the signal voltage at the 2-Ω load.

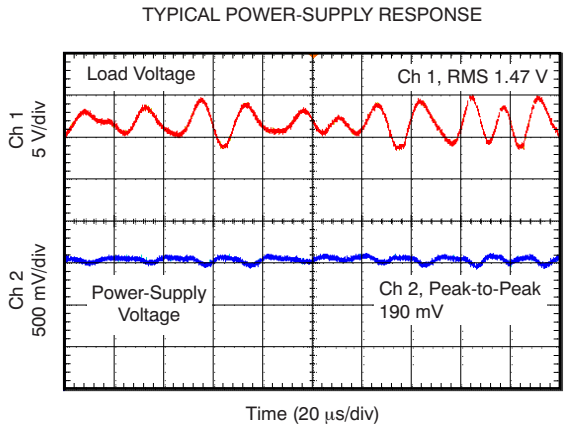


Figure 30. Typical Power-Supply AC Response

7 Thermal Management

In a typical power-line communications application, the AFE031 can dissipate 2 W of power when transmitting into the low impedance of the ac line. This amount of power dissipation can increase the junction temperature, which in turn can lead to a thermal overload and result in interruptions in the signal transmission if the proper thermal design of the printed circuit board (PCB) has not been undertaken. This section illustrates how heat flows from the AFE031, and how proper PCB design and construction can be used to manage this flow of heat, lower the device temperature, and maximize device performance and operating life.

The AFE031 is assembled in a 7 mm^2 x 7 mm^2, 48-lead QFN package. As Figure 31 clearly shows, this QFN package has a large area, exposed thermal pad on the underside of the device, which is used to conduct heat away from the AFE031 and into the underlying board.

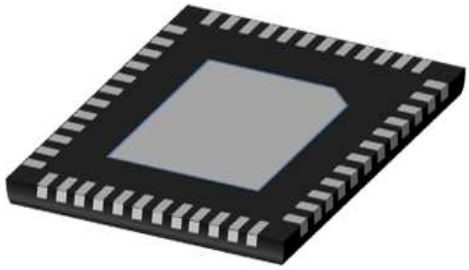


Figure 31. QFN Package with Large Area, Exposed Thermal Pad

Figure 32 shows a cross-section view of the QFN package and illustrates the key components in the AFE031 construction. Housed in a high-performance plastic mold compound, the AFE031 silicon die is mounted to the copper (Cu) lead-frame by a thermally-conductive, die attach epoxy. Wire bonds connect the bond pads that are located on the top surface of the silicon die to the external leads of the QFN package.

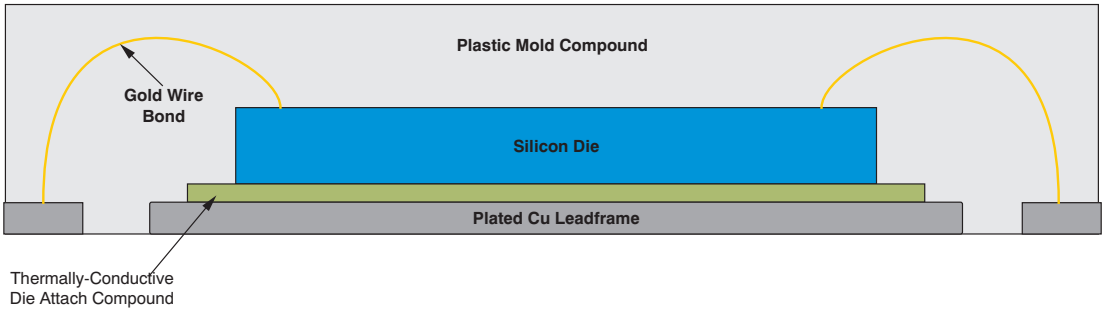


Figure 32. Cross-Section View of the QFN Package

When dissipating power, heat flows in all directions and seeks the lowest thermally-resistant path from the device, as illustrated in Figure 33. It can easily be seen that some heat is conducted from the silicon die surface through the plastic packaging material and transferred into the ambient environment. Because plastic is a relatively poor conductor of heat, this path is not the primary thermal path for heat flow. Heat also flows across the silicon die surface to the bond pads, through the wire bonds, into the package leads, and finally into the top layer of the PCB. While both of these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward, through the silicon die, into the thermally-conductive, die attach epoxy and into the exposed thermal pad on the underside of the package. Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the design and the device.

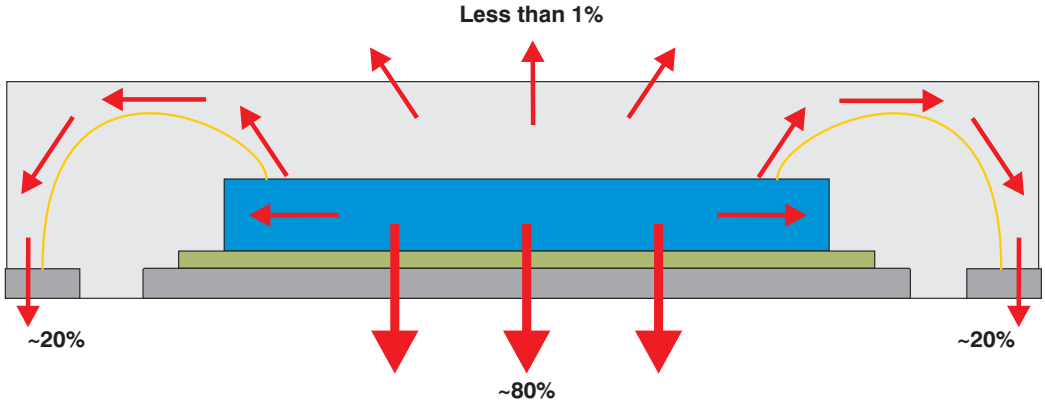


Figure 33. Heat Flow Through the QFN Package

The first consideration when minimizing the thermal resistance of this downward path is to ensure a reliable and low thermal resistance connection of the exposed thermal pad (on the underside of the QFN package) to a thermal pad on the top layer of the PCB. The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB should be the same size as the exposed thermal pad on the underside of the QFN.

Figure 34 shows the recommended design of the thermal pad on the PCB.

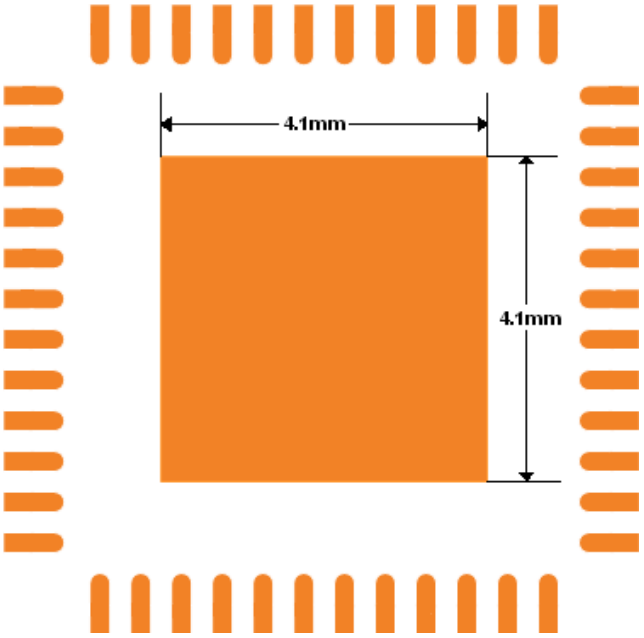


Figure 34. Recommended PCB Thermal Pad

Figure 35 shows the recommended stencil design for proper solder coverage and thickness.

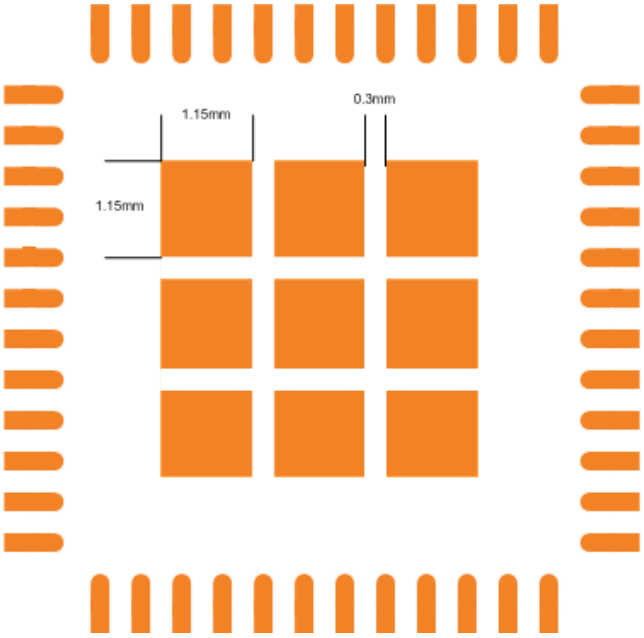


Figure 35. Recommended Stencil Pattern

Figure 36 shows the recommended thermal via pattern.

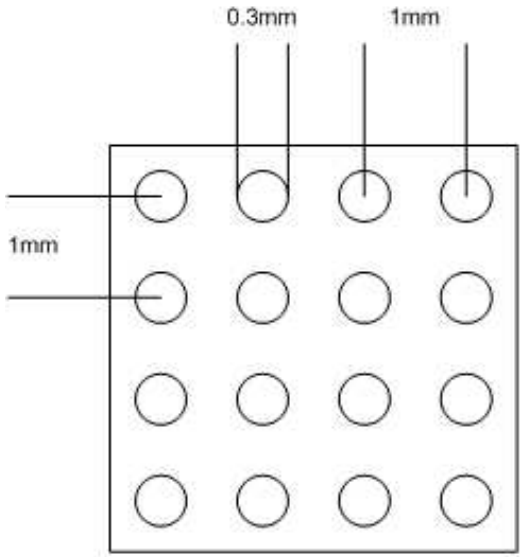


Figure 36. Recommended Thermal Via Pattern

To ensure a reliable connection and a low thermal resistive path from the AFE031 to the PCB, care must be taken to avoid a poor solder connection of the exposed thermal pad as a result of solder voids. Refer to TI application report , *QFN/SON PCB Attachment* (SLUA271A) for recommended techniques to attach the QFN package to the board.

The heat flows from the exposed thermal pad on the underside of the QFN through the solder connection to the thermal pad on the PCB. For most applications, additional heat spreading is required. The use of thermal vias allows the heat to conduct away from the thermal pad on the top layer of the board to the inner layers as well as the bottom layer. A cross-sectional diagram showing these recommended thermal vias is shown in Figure 37.

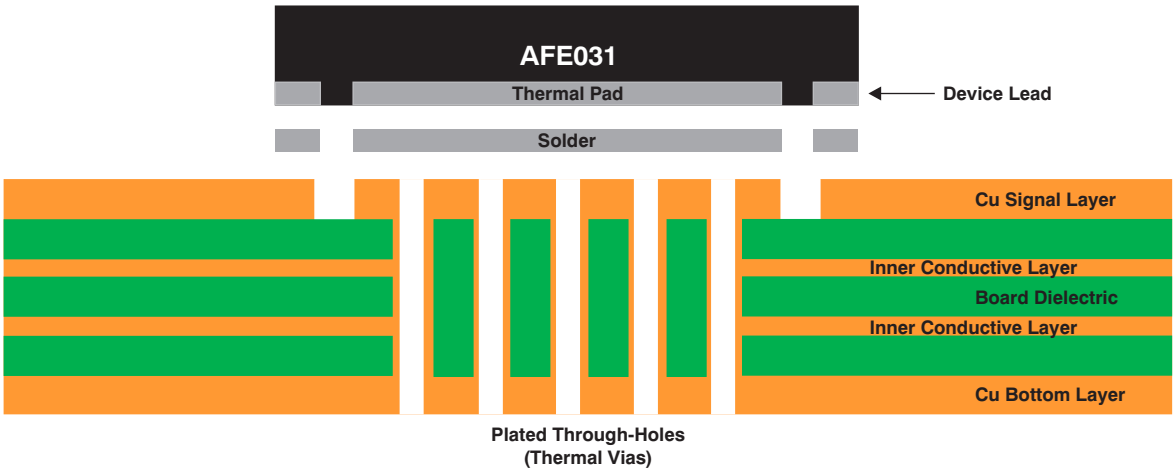


Figure 37. PCB with Recommended Thermal Via Construction

The best practice for removing heat from the AFE031 is to spread it into the board. Figure 38 shows how heat flows from the AFE031 into the board.

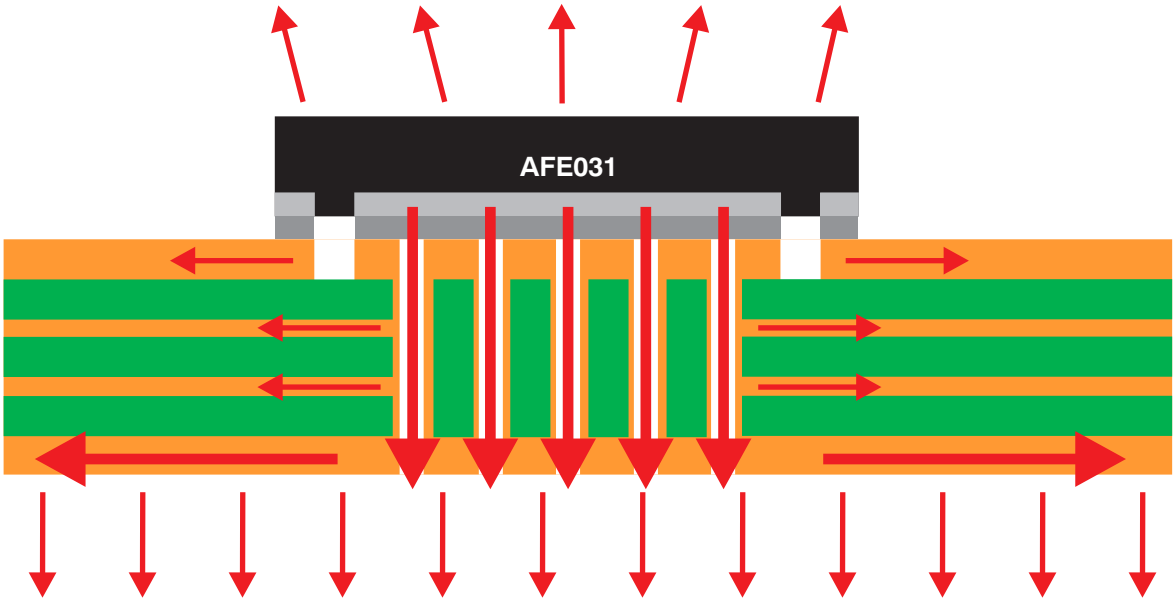


Figure 38. Heat Flows from AFE031 into the PCB

The heat spreading into the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with Cu to the greatest extent possible, to maximize the area coverage on each layer. As an example, a thermally-robust, multi-layer PCB design may consist of four layers with copper coverage of 60% in the top layer, 85% and 90% in the inner layers, and 95% on the bottom layer.

Increasing the number of layers in the board can improve the heat spreading. Figure 39 shows the effect of adding layers to improve the board thermal performance.

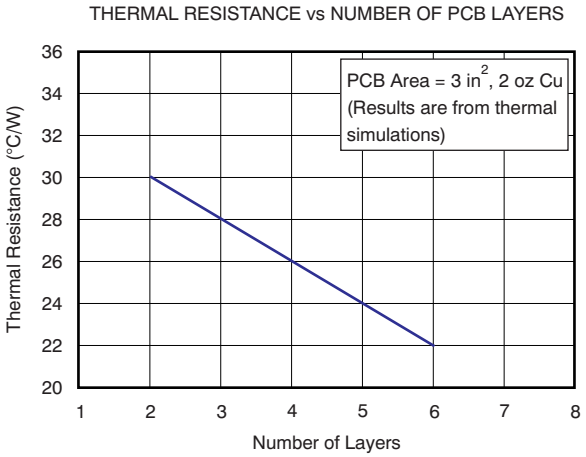


Figure 39. Thermal Resistance as a Function of the Number of Layers in the PCB

The thermal performance of the board can also be improved as the board area is increased. Increasing the PCB surface area provides a larger heat spreading area and a larger surface area over which to transfer the heat into the ambient environment. Figure 40 illustrates this relationship.

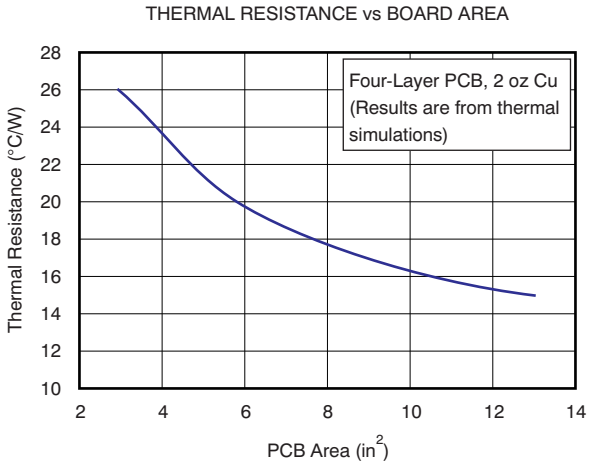


Figure 40. Thermal Resistance as a Function of PCB Area

Increasing the volume of copper in the PCB design further improves the thermal performance. The relationship between copper thickness and thermal performance is shown in Figure 41.

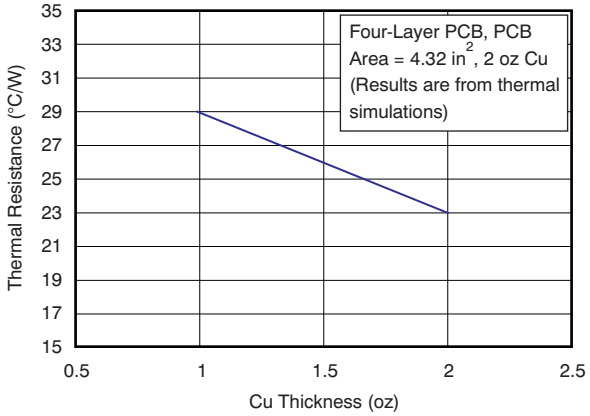


Figure 41. Thermal Resistance as a Function of Copper Thickness

All simulation and measured results were taken with an ambient temperature of +75°C in natural convection.

Figure 42 and Figure 43 show the top side and bottom side, respectively, of a 2.4-in^2 x 1.8-in^2 example layout. Note the large percentage area of copper coverage on the thermal layer.

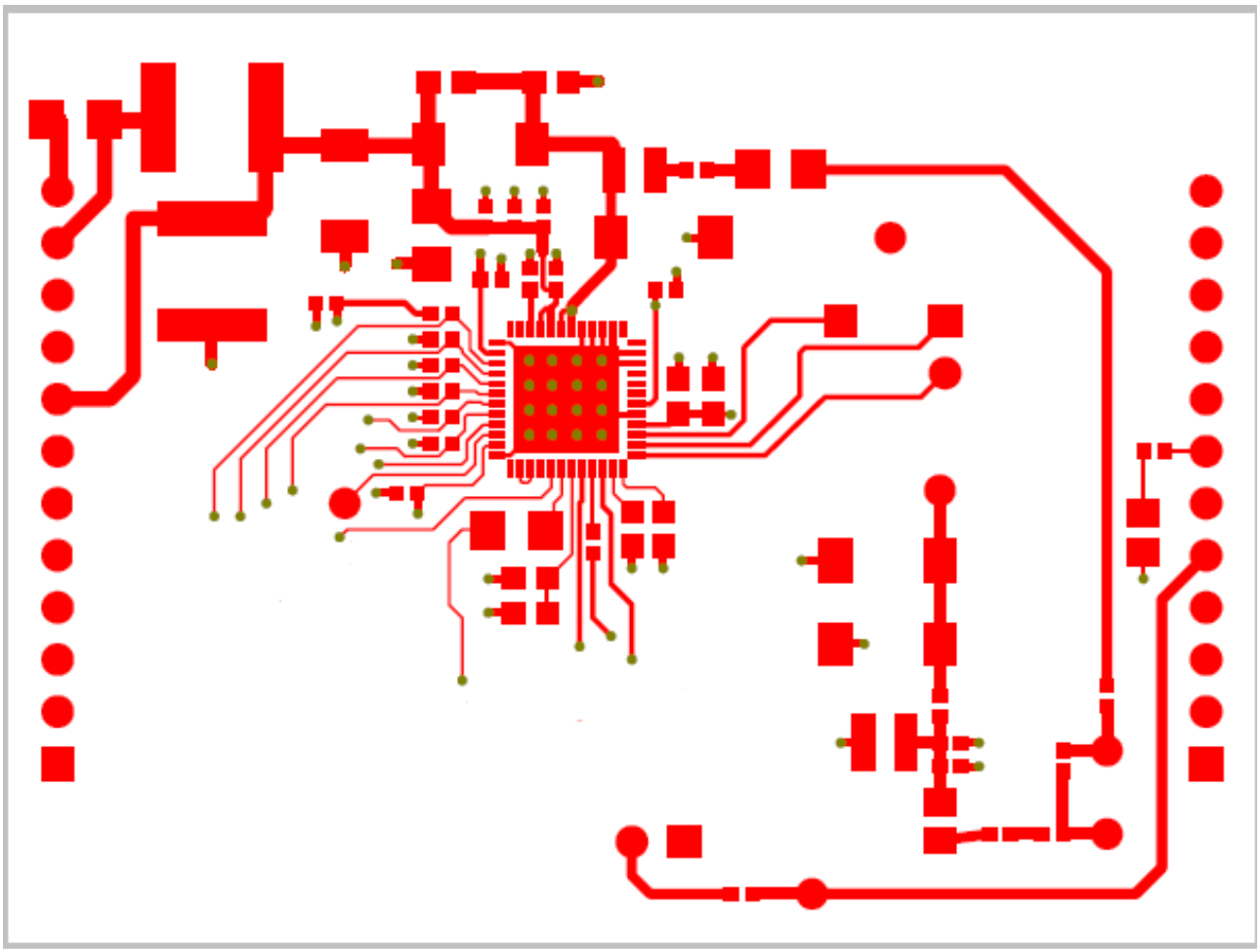


Figure 42. Top Side of PCB Layout used in TMDSPLCKIT-V3 PLC Evaluation Kit

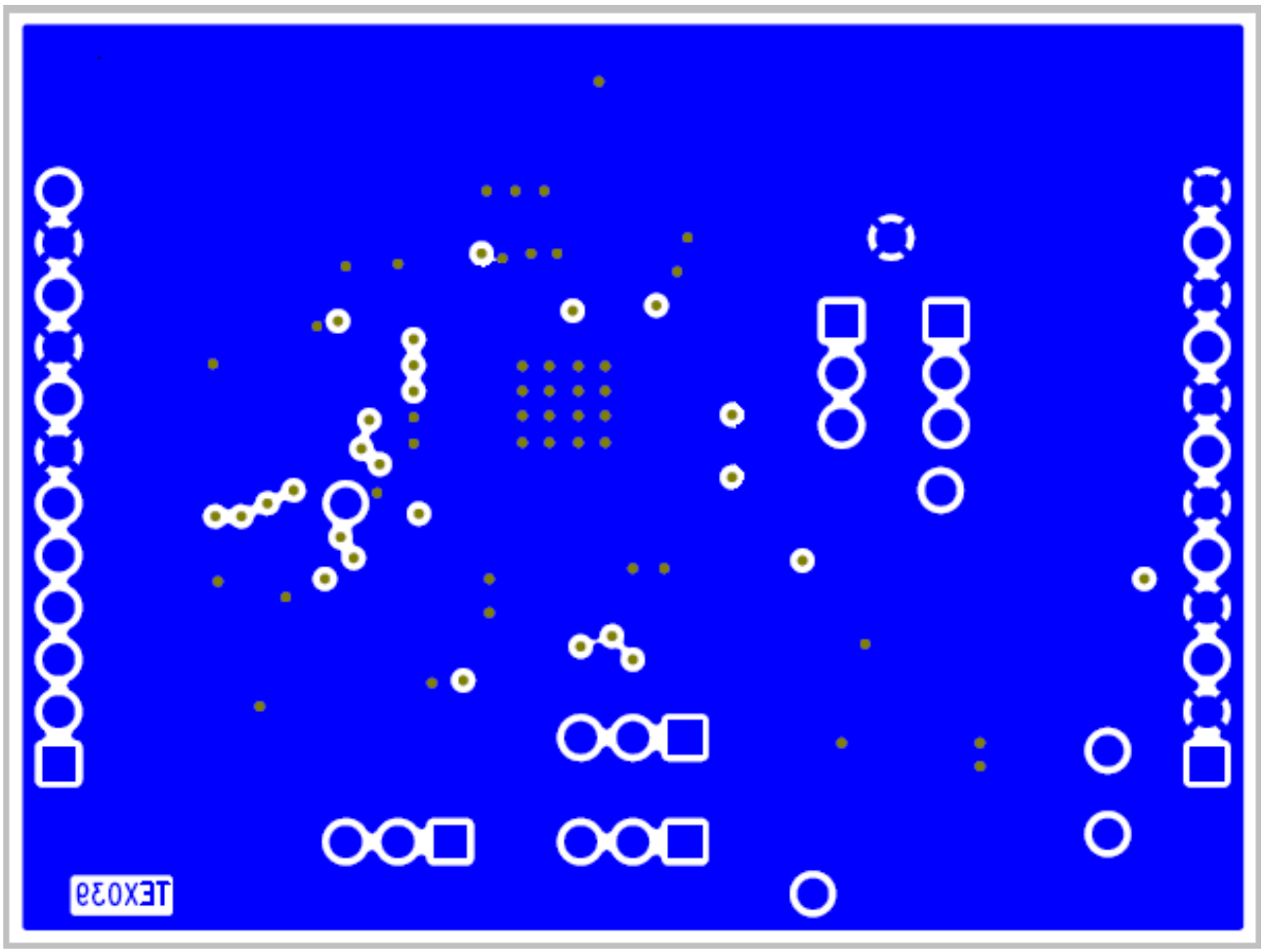


Figure 43. Bottom Side of PCB Layout used in TMDSPLCKIT-V3 PLC Evaluation Kit

The relationship between heat flow, thermal resistance, and temperature can be easily modeled using simple circuit analysis. Figure 44 shows a circuit that can be used to perform this type of thermal calculation.

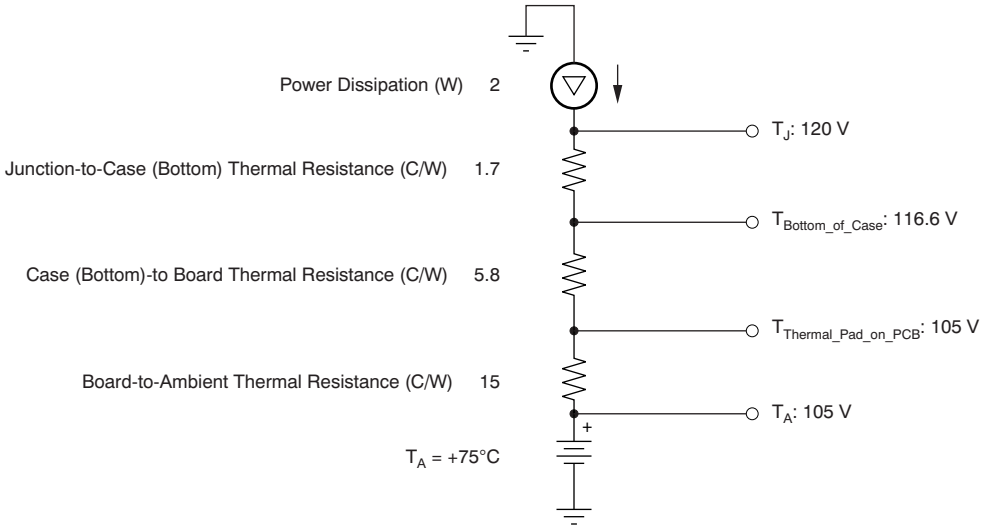


Figure 44. Simple Circuit to Simulate Thermal Performance

The heat source in the AFE031 is the PA. In the schematic in Figure 44, this heat source is represented by a current source with a magnitude of 2 A. This 2-A current source is used to represent the 2 W of power dissipation in the AFE031. The voltage source in Figure 44 represents the ambient temperature. In this example, it is 75 V, which corresponds to an ambient temperature of +75°C. The three resistances represent the thermal resistance between the silicon junction and bottom of the case, Φ_{JCBot}; the bottom of the case to the PCB; and from the board to the ambient environment.

Table 9 shows the relationship between the thermal model and electrical analog.

Table 9. Relationship Between the Thermal Model and Electrical Analog

Thermal Model	Electrical Model	Relationship
Ambient temperature (°C)	Voltage source (V)	1°C = 1 V
Power dissipation (W)	Current source (A)	1 W = 1 A
Thermal resistance (°C/W)	Electrical resistance (Ω)	1°C/W = 1 Ω
Heat flow (W)	Current flow (A)	1 W = 1 A
Temperature (°C)	Voltage (V)	1°C = 1 V

Thermal information for the AFE301 is summarized in Table 10.

Table 10. AFE031 Thermal Information

Thermal Information		Min	Typ	Max	Unit
Specified temperature range (QFN-48 PowerPAD™)		–40		+125	°C
Junction-to-ambient thermal resistance	θ_{JA}		27.8		°C/W
Junction-to-case (top) thermal resistance	θ_{JCTop}		12.1		°C/W
Junction-to-board thermal resistance	θ_{JB}		7.5		°C/W
Junction-to-top characterization parameter	Ψ_{JT}		0.4		°C/W
Junction-to-board characterization parameter	Ψ_{JB}		7.4		°C/W
Junction-to-case (bottom) thermal resistance	θ_{JCBot}		1.7		°C/W

In Table 10, the thermal resistance junction to case bottom, Φ_{JCBot}, is given as 1.7°C/W. This value is the thermal resistance if the AFE031 is perfectly connected to an infinite heat sink.

The thermal resistance from case bottom to board is calculated as Equation 17.

$$\theta_{JB} - \theta_{JCBot} = 7.5 - 1.5 = 5.8°C/W \quad (17)$$

This amount of thermal resistance is expected when the recommendations for thermal pad design and proper package soldering to the board are followed. Failure to follow these recommendations results in a larger thermal resistance from the case bottom to board. The thermal resistance from the board to the ambient is variable and based on the PCB size, number of layers, and copper thickness.

The electrical analog shown in Table 9 is a very simplistic method of determining the required board thermal resistance for a given application. Best results are achieved by performing board-level thermal simulations to verify the design before release to manufacturing occurs.

8 Conclusion

The AFE031 is the industry's first and most flexible analog front-end designed specifically to meet the rigorous demands of power-line communication applications. Using the AFE031 saves design time, increases reliability, and reduces risk. The AFE031 can connect to virtually all microprocessors. The device can be driven with both digital or analog inputs; it conditions and filters the signals, and then transmits the signals to the power line through the integrated power amplifier. The integrated, low-noise receiver can be configured to provide either attenuation or gain, depending upon the signal and noise levels on the power line and drives the analog-to-digital converter found in most microcontrollers. The AFE031 can work with multiple signal types, including FSK, SFSK, or OFDM. With proper line-coupling circuit design, the AFE031 can be used in a wide variety of applications that range from dc busses to MV (7.2 kV) transmission lines.

Revision History

Changes from Original (October 2011) to A Revision **Page**

- Updated Equation 16 24
- Changed *PA power dissipation* and *Total* parameter rows in Table 8 24

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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