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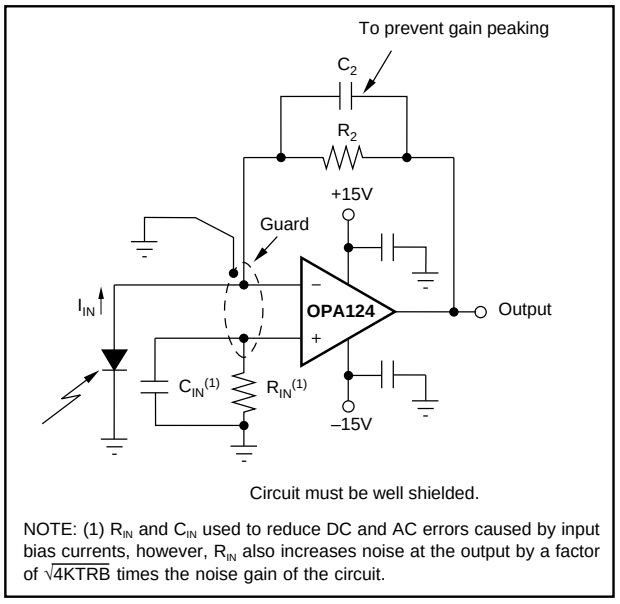
COMPARISON OF NOISE PERFORMANCE BETWEEN A FET TRANSIMPEDANCE AMPLIFIER AND A SWITCHED INTEGRATOR

By Bonnie C. Baker

Low-input current FET operational amplifiers are universally used to monitor photodetector, or more commonly photodiode currents. These photodetectors bridge the gap between a physical event, light, and electronics. There are a variety of amplifier configurations to select from and the choice is based on noise, bandwidth, offset, and linearity. The most popular design approach is shown in Figure 1. A considerable amount has been written on the performance of this traditional transimpedance amplifier. This topology has dominated applications such as CT scanners, star-tracking instruments, electron microscopes, etc., where a light-to-voltage conversion is required.



NOTE: (1) R_{IN} and C_{IN} used to reduce DC and AC errors caused by input bias currents, however, R_{IN} also increases noise at the output by a factor of $\sqrt{4KTRB}$ times the noise gain of the circuit.

FIGURE 1. Most Popular Design Approach to Gain Precise Low Level Currents from a Photodetector.

Until now, the only feasible solution to the high precision, current-to-voltage design problem has been an op amp network with a resistor in the feedback loop. Variations such as using resistor T-networks or an instrumentation amplifier, as shown in Figure 2, still use the fundamental concept of a resistive feedback loop to perform the I/V conversion function. In these circuits, the fundamental transfer function is:

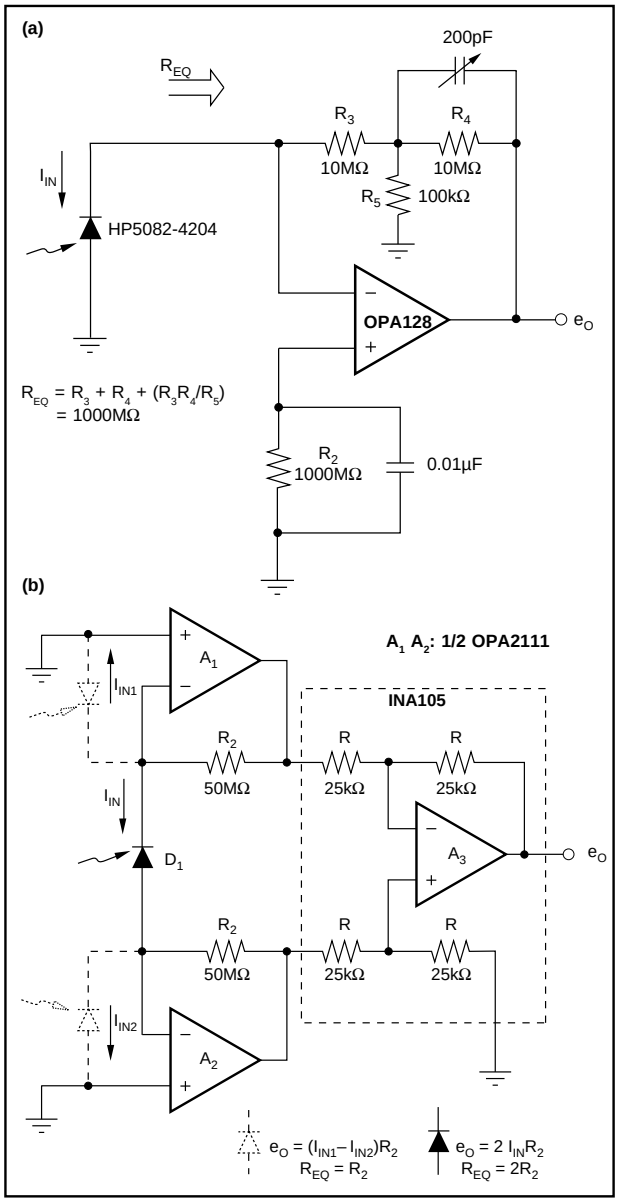


FIGURE 2 (a) Using a T-Network to Design the Feedback Resistor for a Transimpedance Circuit.
(b) An Instrumentation Amplifier Topology Can Be Used to Convert Low-Level Photodiode Currents to a Voltage Output.

$V_{OUT} = R_{EQ} \bullet I_{IN}$,

where V_{OUT} = Output voltage

R_{EQ} = Equivalent resistive feedback element

I_{IN} = Current generated by the photodetector

An alternative design method, a switched integrator, is shown in Figure 3. With this topology, the capacitor in the feedback loop of the amplifier dominates the transfer function. The switches perform the functions of removing the excitation signal from the input of the amplifier (S_1) and resetting the output of the amplifier to ground (S_2). The fundamental transfer function of this circuit is:

$$V_{OUT} = -\frac{1}{C_2}\int_0^t I_{IN}\, dt,$$

where V_{OUT} = Output voltage

C_2 = Capacitive feedback element

I_{IN} = Current generated by the photodetector

The discrete design of the switched integrator is impractical for low noise, precision applications because of the switching noise of S_1 and S_2. The switching noise is caused by the injection of charge across the parasitic gate-to-source, gate-to-drain, and source-to-drain capacitances of the FET switches. The ACF2101 (block diagram shown in Figure 3) implements the switched integrator design on a monolithic chip and uses a charge injection cancellation design for S_1 and S_2 (see Figure 4) to reduce the switch contribution to DC offset and noise.

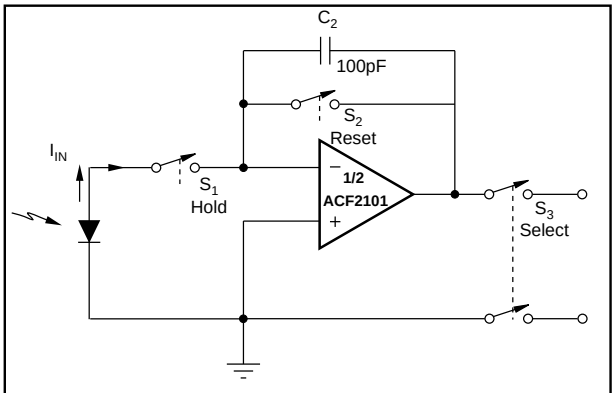


FIGURE 3. Block Diagram of 1/2 of the Dual ACF2101 Switched Integrator.

As illustrated in Figure 4, when the LOGIC node changes from low to high the voltage change (V_1) across the capacitors, C_A and C_B, pull charge out of the SIGNAL IN node and SIGNAL OUT node. The inverted LOGIC signal at V_2 pushes an equal amount of charge through C_C and C_D back into the SIGNAL IN node and SIGNAL OUT node. If

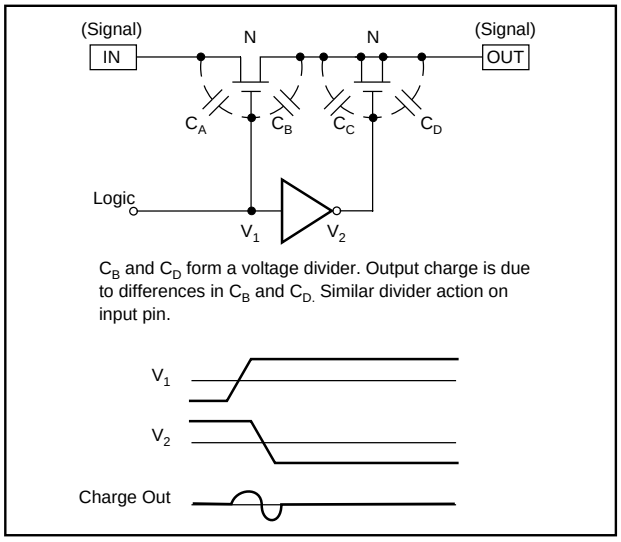


FIGURE 4. Topology Used for the Switches in the ACF2101 Switched Integrator to Reduce Charge Injection Errors.

parasitic capacitors C_A, C_B, C_C and C_D are carefully matched, the total charge injection caused by switching at the SIGNAL IN node and the SIGNAL OUT node is zero.

The comparison of the noise performance of the traditional resistor feedback transimpedance amplifier and the switched integrator starts with the analysis of the input sensor, the photodetector.

PHOTO DETECTOR CHARACTERISTICS

Photodiodes generate low level currents that are proportional to the level of illumination. An equivalent circuit for the photodiode is shown in Figure 5. The value of the junction capacitor, C_1, can have a wide range of values dependent of the diode junction area and bias voltage. A value of 50pF at zero bias is typical for small area diodes. The value of the shunt resistor, R_1, is usually in the order of $10^8\Omega$ at room temperature and decreases by a factor of two every 10°C rise in temperature. The range of the shunt resistor, R_1, can be as high as 100GΩ and low as 10kΩ at room temperature. There is no direct correlation between the values of C_1 and R_1. C_1 can usually be found in the product data sheet of the photodiode. The value of R_1 is not always published by the manufacturer, however, its effect on noise

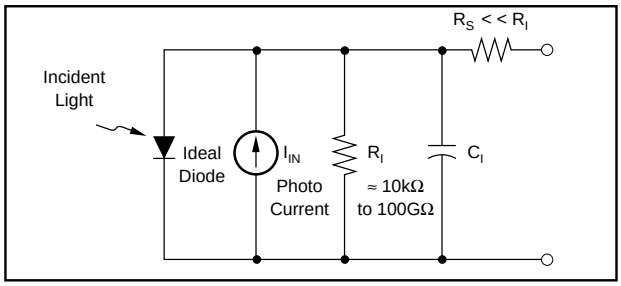


FIGURE 5. Equivalent Circuit for a Photodiode.

in both the traditional transimpedance amplifier and the switched integrator occur at lower frequencies. The overall noise contribution in the lower frequencies is usually very small compared to the contribution at higher frequencies, therefore, knowing the exact value of R_1 is not critical.

NOISE ANALYSIS OF TRADITIONAL TRANSIMPEDANCE AMPLIFIER

For the noise comparison between the transimpedance amplifier and the switched integrator refer to Figure 6 for a more complete circuit diagram. The optimum amplifier would have infinite bandwidth, zero voltage noise, zero input bias current, and zero offset voltage. The optimum amplifier does not exist; however, several op amps come close to meeting one or a few of these general requirements. Table I summarizes key specifications of the FET amplifiers OPA111, OPA124, OPA128, OPA404, OPA2111, OPA2107 and OPA627, which are usually used in transimpedance applications.

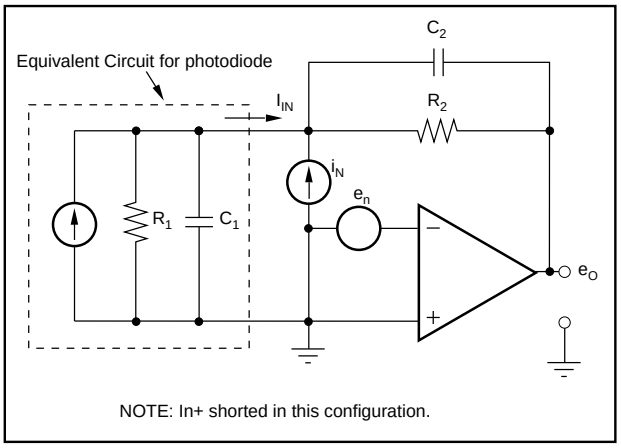


FIGURE 6. Complete Circuit Diagram Used for the Evaluation of the Noise and Bandwidth Performance of the Classical Transimpedance Amplifier and the Switched Integrator.

PRODUCT	NOISE at 10kHz ($nV/\sqrt{Hz}$)	BANDWIDTH (MHz, typ)	INPUT CAPACITANCE (pF, typ)	INPUT BIAS CURRENT (pA, max)
OPA111BM	8	2	4	1
OPA124BP	8	1.6	4	1
OPA627BP	6	16	15	5
OPA404G	12(1)	6.4	4	4
OPA128BM	15(1)	1	3	0.15
OPA2111BM	8	2	4	4
OPA2107BM	8(1)	4.5	6	5

NOTE: (1) Denotes typical values.

TABLE I. Low Noise FET Input Op Amps Typically Used In Transimpedance Amplifier Applications. In transimpedance applications, the input capacitance of the amplifier equals input common-mode capacitance plus input differential capacitance.

The first step in designing the transimpedance amplifier is selecting the feedback resistor, R_2. By knowing the maximum expected I_{IN}, R_2 is selected to optimize the signal-to-noise ratio with the formula:

$$R_2 = \frac{V_{OUT(max)}}{I_{IN(max)}},$$

where $V_{OUT(max)}$ = maximum output voltage of the op amp

$I_{IN(max)}$ = maximum current from the photodiode based on maximum expected light intensity

Typical values for R_2 would be between 10kΩ and 100MΩ. It is possible that optimum noise performance can be obtained with a $V_{OUT(max)}$ that is less than the full output swing of the amplifier, in which case the above equations are not applicable. The above equation is designed to optimize the signal-to-noise ratio at the output of the amplifier.

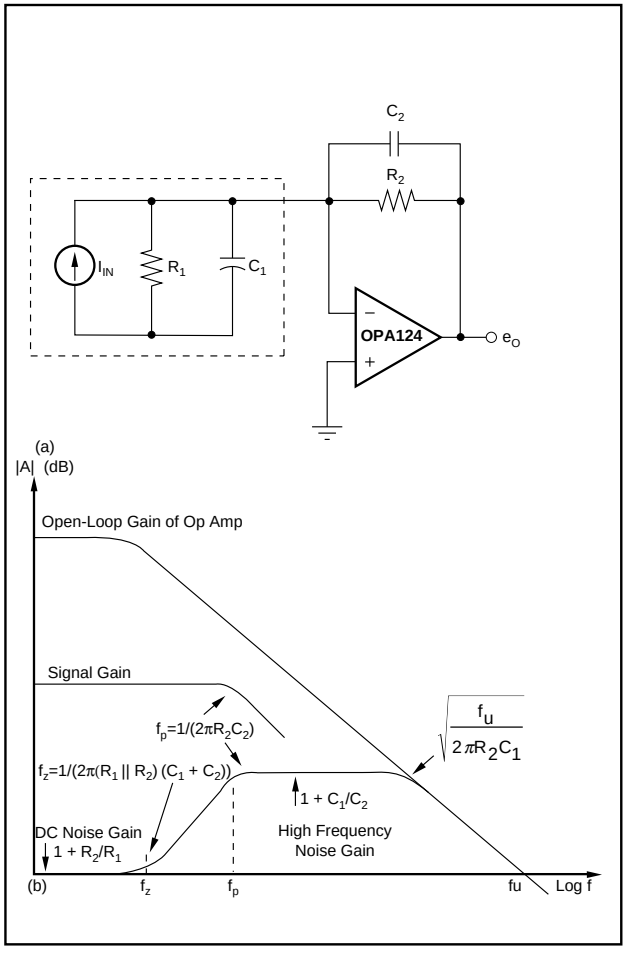


FIGURE 7. Noise And Signal Response of the Classical Transimpedance Amplifier.

The model in Figure 7 shows the overall noise gain response of the transimpedance circuit. The signal bandwidth is determined by a pole generated by R_2 and C_2. The noise bandwidth is determined by the open loop gain roll off of the op amp. To maximize the signal bandwidth and insure an approximate 45° phase margin with a 25% step function overshoot, C_2 is selected using the formula below:

$$C_2 = \sqrt{\frac{C_1}{2\pi R_2 \bullet f_u}}$$

where f_u = op amp unity gain bandwidth

Here the signal bandwidth and noise bandwidth are identical and equal to:

$$BW = \frac{1}{2\pi R_2 C_2}$$

In some applications, an overshoot of 25% may be too much. A more conservative 5% overshoot can be designed with a phase margin of 65° by using the formula below to select C_2:

$$C_2 = 2 \bullet \sqrt{\frac{C_1}{2\pi R_2 \bullet f_u}}$$

where f_u = op amp unity gain bandwidth

Typical calculated values for C_2 would be from sub-pico farads to 20 or 30pF. Actual minimum circuit values for C_2 are dependent on the stray capacitance of R_2 and PC board layout. Typically, a resistor has 0.5pF of stray capacitance. Using the C_2 value calculated above (for a 65° phase margin), the effective noise bandwidth is equivalent to the noise gain 3dB bandwidth times $\pi/2$ or:

$$BW_{\text{effective noise}} = \frac{1}{2R_2C_2}$$

and the signal bandwidth is:

$$BW_{\text{signal}} = \frac{1}{2\pi R_2 C_2}$$

Usually it is necessary to follow the transimpedance amplifier with a low pass filter to further reduce the wideband noise beyond the signal bandwidth. A single pole, low-pass filter with a bandwidth at twice the signal bandwidth of the transimpedance amplifier can easily improve the dynamic range of the transimpedance amplifier by 4 or 5 dB.

Brute force calculations should be performed to understand the noise contributions of the regions illustrated in Figure 7 (see OPA101 data sheet). For instance, R_1 contributes to overall noise gain in the lower frequencies and can be mostly ignored. This insight is valuable when considering design options to further improve the circuit. Once the details are understood, an easier approach is to use a macromodel and simulate the results. The macromodel must be able to simulate the noise performance of the op amp. The appropriate

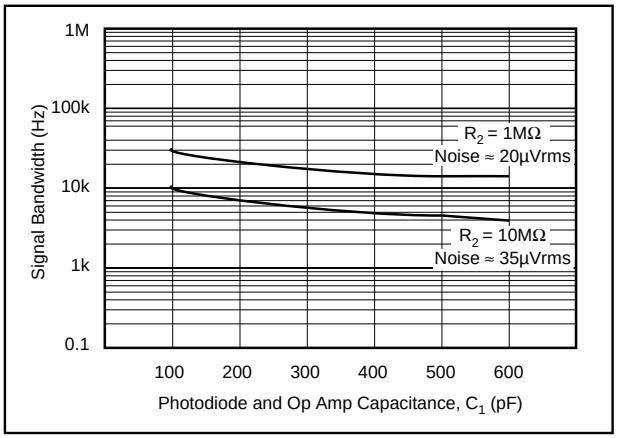


FIGURE 8. Signal Bandwidth and Output Noise Change With Changes in Input Capacitance, C_1, of a Transimpedance Amplifier Using the OPA111 as the Op Amp.

Burr-Brown macromodel for the OPA627 is the OPA627E.MOD. The PSpice Probe command needed to calculate the cumulative rms noise is SQRT(S(V(ONOISE) • V(ONOISE))). Figure 8 shows how a transimpedance amplifier's (designed using the OPA124) signal bandwidth and output noise change with values of input capacitance. Note that the output noise is unexpectedly flat across changes in C_1. This is because the signal and noise bandwidth decrease with increases of C_2. A lower noise bandwidth yields lower rms noise at the output of the amplifier. The signal-to-noise ratio improves.

To improve the signal-to-noise ratio of a transimpedance amplifier, the designer can select a lower noise amplifier, reduce the $(1+C_1/C_2)$ noise gain, reduce the feedback resistor value, or reduce the signal bandwidth of the system with an additional filter or a slower op amp. Lower noise FET amplifiers usually have a wider bandwidth and higher input capacitance than the higher noise FET amplifiers. If a lower noise, wider bandwidth amplifier is selected as the op amp for the transimpedance amplifier, the increase in bandwidth and input capacitance may cause more noise in the system than the original op amp. A filter can be used to reduce the overall bandwidth and reduce the noise. Additionally, the noise gain of the transimpedance amplifier can be reduced by increasing C_2 or decreasing C_1. The photodetector can be selected in order to reduce C_1. Sometimes this is not possible because of the design constraints of photodetector vs the signal source. C_2 can be increased at the expense of reduced bandwidth. More elaborate techniques can be used to reduce noise, such as a more complex feedback network around the amplifier or boot-strapping the photodetector. These techniques are beyond the scope of this application note. Refer to the reference articles for more depth.

One fundamental performance difference between the traditional transimpedance amplifier and the switched integrator is that the amplifier gives a real time representation of the light excitation at the output of the amplifier, and the switched integrator gives a time-averaged representation of

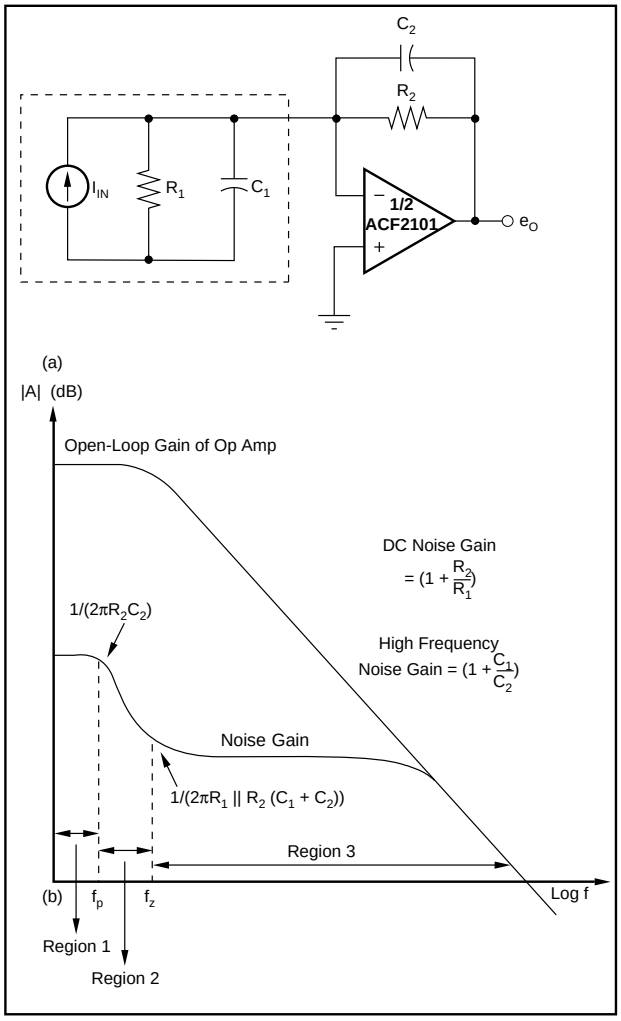


FIGURE 9. Noise and Signal Response of a Switched Integrator.

the input information from the photodetector. The real time solution is limited in bandwidth by the selected amplifier, the settling time of the amplifier, and the required feedback capacitor and resistor (C_2 and R_2). Additionally, a filter is usually used following the output of the transimpedance amplifier to further reduce noise at higher frequencies.

This approach is optimal for low and medium bandwidth applications where information about the amplitude and shape of the input signal is critical. The design problem is complex because of the trade-offs between noise and bandwidth and the abundance of op amp choices. Also, the capacitor and resistor accuracy requirements make this design difficult and sometimes expensive to manufacture in a production environment.

NOISE ANALYSIS OF SWITCHED INTEGRATOR AMPLIFIER

Where the traditional transimpedance transfer function is dominated by the feedback resistor, R_2, the switched integrator amplifier transfer function is dominated by the ratio of the feedback capacitor, C_2, and time. Referring to Figure 3, when S_1 is closed, the input current flows past the inverting node of the op amp (which is held at virtual ground) and charges C_2. The input current consequently causes the voltage at the output of the op amp to change in the negative direction over time. The voltage output of the switched integrator represents the average current input signal over a specified time, as opposed to the real time signal of the previous example. The ACF2101 switched integrator, shown in Figure 3, has a maximum input current specified at 100µA. The input current is restricted by the internal capacitor of the ACF2101 (100pF) and the 1V/µs slew rate of the amplifier. If an external capacitor is used, input currents can exceed 100µA as long as the following ratio is true:

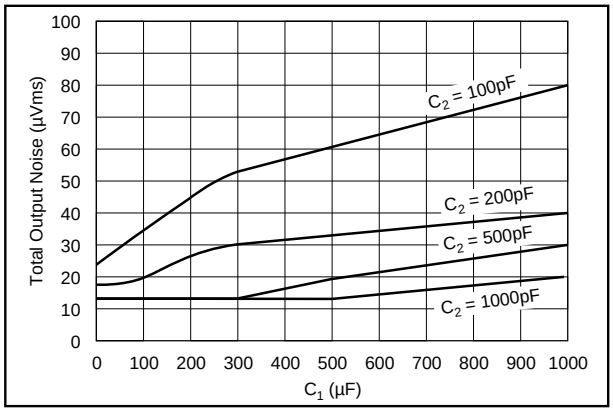


FIGURE 10. Total Output Noise vs C_1 and C_2 of the ACF2101 Switched Integrator.

$$\frac{C_2}{(\text{integration time})} \geq 10^{6}{}_{(\text{farad/sec})}$$

where the integration time equals the amount of time between samples.

If that ratio is less than 10^6 (farad/sec), the ACF2101 may loose accuracy at the output. Whenever possible, the internal capacitor should be used with the ACF2101 to insure greater gain and linearity accuracy. Figure 9 is used to evaluate the noise contribution of the op amp, gained by the feedback network of the ACF2101 and the photodiode. Here the reset switch, (S_2 as illustrated in Figure 3) is modeled as a noiseless resistor (R_2). The typical resistance of S_2, when it is open, is 1000GΩ. The switched integrator, ACF2101, has an internal feedback capacitor, C_2, of 100pF. The user may choose to use an external capacitor instead of the internal capacitor provided. Typical values can range up to 2000pF. If an external capacitor is used, care must be taken to choose an integration capacitor with a low voltage coefficient, temperature coefficient, memory, and leakage current. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica.

The total noise contribution of the op amp and the feedback network of the switched integrator is equivalent to the

square root of the sum of the squares of three regions as shown in Figure 9. The noise in the first region is equal to the average op amp noise over that region times the square root of the region bandwidth. The pole in the noise gain of the switched integrator circuit generated by R_2 and C_2 is in the sub-Hertz region. For example, if C_2 = 100pF and R_2 = 1000GΩ the pole generated by the RC pair is equal to 1.59mHz. To calculate the noise contribution of this region the average noise over the region is multiplied times the square root of 1.59mHz which is equal to $39.87E^{-3}$. Quick calculations show that any noise gained by the DC gain $(1+R_2/R_1)$ of the switched integrator is negligible. In addition, the zero generated by the $(R_1 \| R_2)(C_1+C_2)$ combination is also in the low frequency range. Using a typical value of 100MΩ for R_1, 50pF for C_1, 1000GΩ for R_2 and 100pF for C_2, the zero is located at 10.6Hz. Again, the noise contribution from this region is negligible. Consequently, the noise contribution from the op amp and its feedback network in conjunction with the photodiode is dominated by the op amp noise times $(1 + C_1/C_2)$.

In addition to the gained op amp noise mentioned above, charge injection and $^{KT}/_{C}$ (capacitor noise) also contribute to the total noise figure of the switched integrator. The switch network shown in Figure 4 is used for the switches of the ACF2101 to reduce charge injection noise. Figure 10 illustrates the total output noise of the switched integrator with various C_1 and C_2 values.

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (f_S), which is usually dominated by the integration time. The fastest feasible sampling frequency for the ACF2101 is 42.55kHz. This assumes that the internal capacitor (100pF) is used. The full scale output is –10V and the settling time requirements are to 0.01% accuracy. Input signals should be below the Nyquist frequency ($f_S/2$) to avoid aliasing errors. The bandwidth of the ACF2101 is determined by the slew rate of the amplifier, settling times of the reset (S_2) and select (S_3) switches as well as the on-to-off and off-to-on switching speeds. The slew rate of the amplifier is guaranteed a minimum of 1V/µs. The output node requires at least 10µs to reach full scale. This time restraint can be reduced if the full 10V swing capability of the ACF2101 is not used.

The settling time of the reset switch (S_2) is 5µs to 0.01% accuracy, which is limited by slew rate of the amplifier and the $R_2 \| C_2$ time constant. The reset switch settling time increases with larger values of C_2; however, if the user also reduces the full scale signal output as described above, this time is reduced proportionally to the output swing maximum. The select switch (S_3) has a 2µs settling time to 0.01% accuracy for loads ≤ 100pF and the delay between switching should be about 0.5µs.

The signal-to-noise ratio of the switched integrator can be reduced by selecting a higher value integration capacitor, C_2. The switched integrator is limited in bandwidth by the amplifier and the nature of the transfer function. The output signal of the integrator is time averaged. The sampling frequency is restricted by the size of the integrating capacitor, the slew rate of the amplifier, the settling time of the switches and amplifier. The bandwidth of the switched integrator can be improved by decreasing the integration capacitor, C_2. As shown in Figure 11, the settling time of the reset switch is increased with increases in C_2.

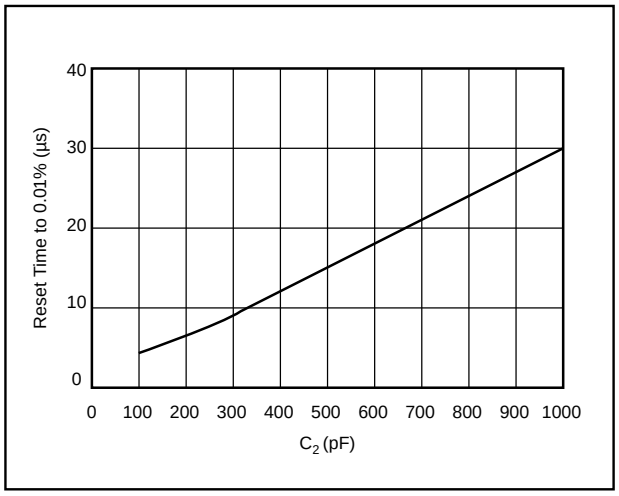


FIGURE 11. Reset Time C_2 vs the ACF2101 Switched Integrator.

The switched integrator requires external digital support circuitry to drive the hold, reset and select switches. If an external integration capacitor (C_2) is used, gain accuracy can be compromised due to the accuracy of the capacitor. The select switch allows the user of the ACF2101 switched integrator to eliminate a sample hold amplifier.

COMPARING THE TRADITIONAL TRANSIMPEDANCE AMPLIFIER TO THE SWITCHED INTEGRATOR

Two examples are selected for comparison of the transimpedance amplifier and the switched integrator amplifier. In both examples, optimum noise solutions and optimum bandwidth solutions are considered.

	OPTIMUM NOISE PERFORMANCE		OPTIMUM BANDWIDTH PERFORMANCE	
	TRANS-IMPEDANCE	SWITCHED INTEGRATOR	TRANS-IMPEDANCE	SWITCHED INTEGRATOR
Device	OPA124	ACF2101	OPA627	ACF2101
I_B	1pA	1pA	5pA	1pA
C_2	0.5pF	100pF	0.5pF	1.5pF
Signal Bandwidth	3.2kHz	50Hz	3.2kHz	3.35kHz
Noise Bandwidth	5kHz	250kHz	79kHz	250kHz
Noise	200µVrms	35µVrms	400µVrms	100µVrms
SNR	94dB	109dB	88dB	100dB

TABLE II. Transimpedance and Switched Integrator Design Comparison Using a 100pF Photodiode with Maximum Output Current of 100nA. Values of R_2 were calculated assuming a 65° phase margin.

The first design problem uses an average sized photo diode (C_1 = 100pF) with a maximum output current of 100nA. As shown in Table II, the OPA124 was selected for the low noise comparison and the OPA627 was selected for the wide-bandwidth comparison. The fullscale output of the transimpedance amplifier is designed to be –10V. R_2 is selected to be 100MΩ. C_2 of the OPA124 low noise circuit is restricted by the parasitic capacitance of the feedback resistor, 0.5pF. The OPA124 has a maximum input bias current of 1pA, low drift of 1µV/°C, and low offset voltage. The signal-to-noise ratio of this design is 94dB with a signal bandwidth of 3.2kHz.

In contrast, the ACF2101 is configured to minimize noise by using the on-chip capacitor C_2 = 100pF. As shown in Figure 10, the rms noise performance is typically 35µVrms. This noise performance can be improved by using a higher value external capacitor, but, the bandwidth performance of the circuit is compromised. The signal-to-noise ratio of the switched integrator is better than the transimpedance configuration at 109dB, but the bandwidth is only 50Hz.

In the second section of Table II, the two circuits are optimized for bandwidth. Here the OPA627 is selected as the preferred op amp in hopes of improving the bandwidth of the transimpedance amplifier. The transimpedance design using the OPA627 does indeed change the bandwidth of the circuit, but in an undesirable way. C_2 is still limited to 0.5pF because of the stray capacitance of R_2, consequently the signal bandwidth does not change from the OPA124 design. The noise bandwidth, however, does change by a factor of ~16, causing a significant increase in noise. The signal-to-noise ratio of this circuit is 88dB. The designer would be better off using the OPA124 as the amplifier instead of the OPA627 for this application.

In contrast, the ACF2101 is also configured to maximize bandwidth. Here a feedback capacitor of 1.5pF is selected. PC board layout precautions should be taken to reduce stray capacitance. The signal bandwidth of the circuit is designed to 3.35kHz with a signal-to-noise ratio of 100dB. In this example, the noise and bandwidth performance of the ACF2101 switched integrator is better than the transimpedance configuration. The ACF2101 switched integrator is best optimized for low input current, high input capacitance applications.

Table III illustrates the second design problem where the photodiode has the same stray capacitance (C_1) of 100pF but a maximum current signal of 100µA. The OPA124 is selected for the low noise transimpedance amplifier. In this case, R_2 is selected to be 100kΩ and C_2 equal to 18.2pF. The noise performance of this amplifier is 31µVrms with a signal-to-noise ratio of 110dB.

	OPTIMUM NOISE PERFORMANCE		OPTIMUM BANDWIDTH PERFORMANCE	
	TRANS-IMPEDANCE	SWITCHED INTEGRATOR	TRANS-IMPEDANCE	SWITCHED INTEGRATOR
Device	OPA124	ACF2101	OPA627	ACF2101
I_B	1pA	1pA	5pA	1pA
C_2	18.2pF	500pF	6.76pF	210pF
Signal Bandwidth	87kHz	10kHz	235kHz	24kHz
Noise Bandwidth	275kHz	250kHz	740kHz	250kHz
Noise	31µVrms	15µVrms	108µVrms	20µVrms
SNR	110dB	116dB	99dB	114dB

TABLE III. Transimpedance and Switched Integrator Design Comparison Using a 100pF Photodiode With Maximum Output Current of 100µA. Values of R_2 were calculated assuming a 65° phase margin.

The switched integrator is designed with C_2 = 500pF (external capacitor). A larger capacitor is used to improve the noise performance of the circuit. The noise performance of the switched integrator is improved over the transimpedance amplifier, yet the bandwidth is considerably smaller.

The bandwidth and noise performance of the transimpedance amplifier can be improved by using the OPA627 in place of the OPA124. As shown in Table III, the signal bandwidth is nearly tripled. On the other hand, the switched integrator is designed for improved bandwidth performance by decreasing C_2 to equal 210pF. Although the noise performance is better than the transimpedance amplifier, the bandwidth is restricted by the slew rate, settling times, and switching times of the switched integrator.

IN CONCLUSION

This application note has taken a look at a few variables that optimize the performance of circuits that amplify photodiode signals. In addition to the solutions presented, alternatives should also be explored before the final design is released to production.

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