

EVM User's Guide: TRF1108-DAC39RFEVM

TRF1108-DAC39RFEVM Evaluation Module



Description

The TRF1108-DAC39RFEVM is an evaluation board used to evaluate the DAC39RF10 digital-to-analog converter (DAC) paired with the TRF1108 differential to single ended RF amplifier from Texas Instruments. The EVM offers device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FPGA using SPI through FMC+ connector.

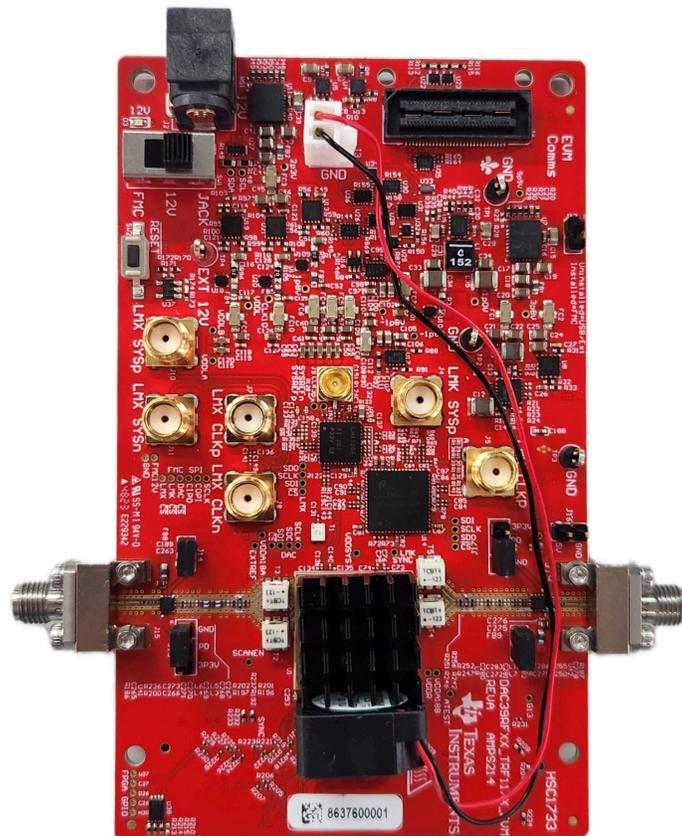
Features

- A channel featuring TI's high speed differential to single-ended amplifier (TRF1108) allowing a single-ended signal output along with an image rejection filter with bandwidth from near-DC to 4GHz.

- A channel featuring TI's high speed differential to single ended amplifier (TRF1108) configured for multi-Nyquist operation allowing a single-ended signal output with bandwidth from near-DC to 12GHz.
- DAC39RF10, a digital to analog converter with 16-bit resolution and maximum input data rate of 20.48 GSPS.

Applications

- Satellite communications (SATCOM)
- Phased array antenna systems
- Synthetic aperture radar (SAR) exciter
- Wireless communications testers
- Arbitrary waveform generator (AWG)



EVM

1 Evaluation Module Overview

1.1 Introduction

This evaluation board also includes the following important features:

- The LMX1204 clock chip distributes the DAC sampling clock
- The LMK04828, clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the DAC performance with an external low-noise clock source
- High-speed serial data output over a High Pin Count FMC+ interface connector

Note

To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in [Table 2-6](#)).

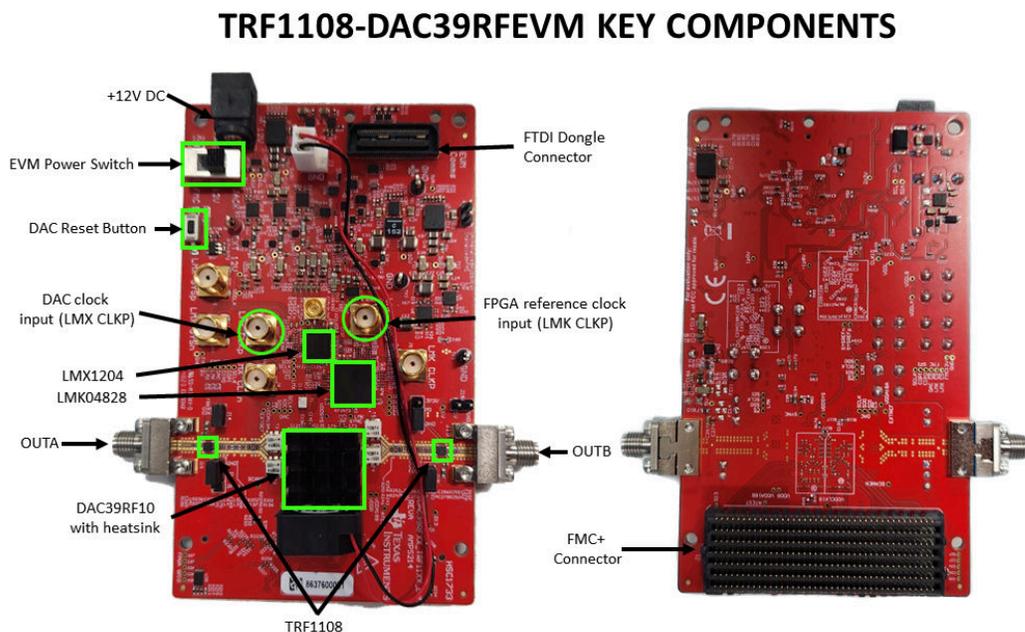


Figure 1-1. EVM Orientation

TRF1108-DAC39RFEVM can be used with the TSW14J59EVM board (pattern generator board). TSW14J59EVM can quickly and easily interface with the TRF1108-DAC39RFEVM.

Note

For now, only 64b/66b encoding modes from serializer/deserializer (SerDes) data rate from 6Gbps to 12.8Gbps are supported by the TSW14J59EVM. The support for 8b/10b modes and lower SerDes rate will be added to future release of HSDCpro software.

The High-Speed Data Converter Pro (HSDC Pro) software is used to communicate with the TSW14J59EVM and is used to generate the data pattern for DAC39RF10.

The TSW14J59EVM takes the generated data pattern, encodes the data, stores the data in memory, and then sends to TRF1108-DAC39RFEVM through the high-speed serial data link (JESD interface).

With proper hardware selection in the HSDC Pro software, the TSW14J59 board is automatically configured to support a wide range of operating speeds of the TRF1108-DAC39RFEVM, but there is a possibility the TSW14J59EVM board does not cover the full operating range of the DAC device.



1.2 Kit Contents

The following equipment and documents are included in the TRF1108-DAC39RFEVM kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable
- USB Type-C® cable
- FTDI dongle to program the DAC EVM with FTDI

1.3 Specification

The TRF1108 is a very high performance, differential- to-single-ended (D2S) amplifier optimized for radio-frequency (RF) applications. The device is excellent choice for applications that require a D2S conversion when driven by a digital-to-analog converter (DAC) such as the high-performance DAC39RF10 or AFE7950.

1.4 Device Information

The DAC39RF10 is a family of single and dual channel digital-to-analog converter (DAC) with 16-bit resolution. The devices can be used as single channel or dual channel non-interpolation DACs. The device can also be used as interpolating DACs in either direct RF sampling mode or baseband mode. The maximum input data rate is 20.48GSPS in single channel mode or 10.24GSPS in dual channel mode or baseband mode. The device can generate signals of up to 10, 7.5, and 5GHz signal bandwidth (8, 12, and 16-bit input resolution) at carrier frequencies exceeding 8GHz enabling direct sampling through C-band and into X-band. The TRF1108 enables this extreme bandwidth, offering a wide frequency band from near-DC to 12GHz.

2 Hardware

2.1 Required Equipment

The following equipments are **not** included in the TRF1108-DAC39RFEVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- High-Speed Data Converter Pro software.
- PC computer running Microsoft® Windows® 10
- Low-noise signal generator for DEVCLK (sampling clock). TI recommends the following generators:
 - Rohde & Schwarz® SMA100B
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the TRF1108-DAC39RFEVM uses LMX1204 clocking chip to distribute the external clock signal to DAC39RF10 and also to LMK04828 to generate necessary clocks needed for the TSW14J59EVM. A few board modifications enables user to test the DAC39RF10 with other clocking options.

2.2 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.

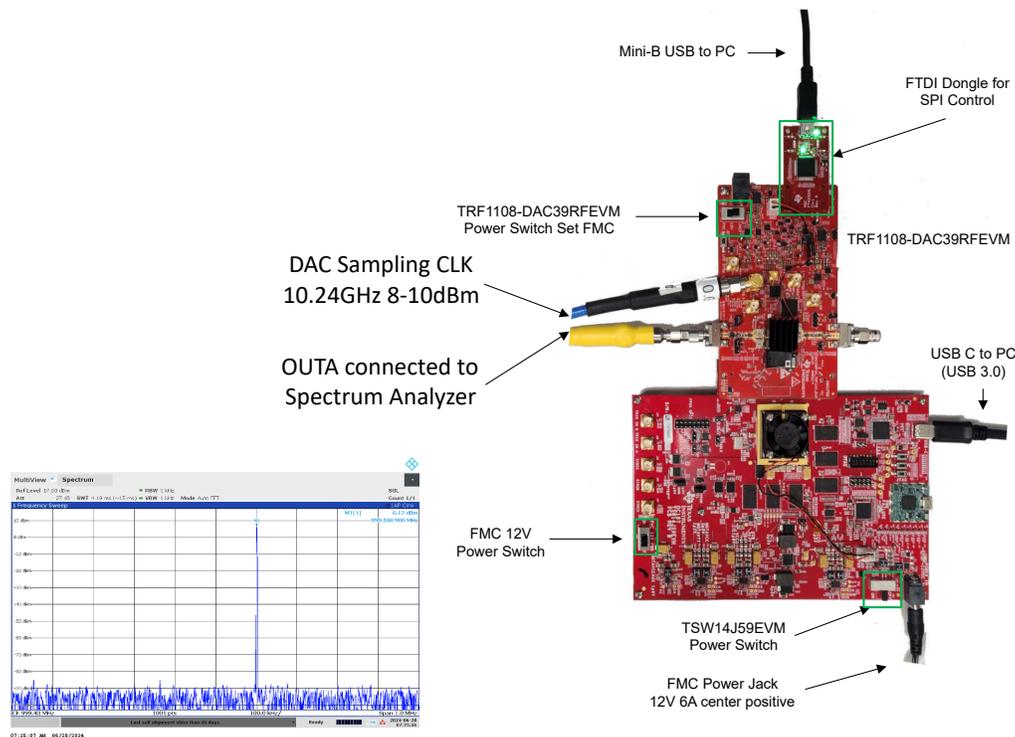


Figure 2-1. TRF1108-DAC39RFEVM Test Setup

Note

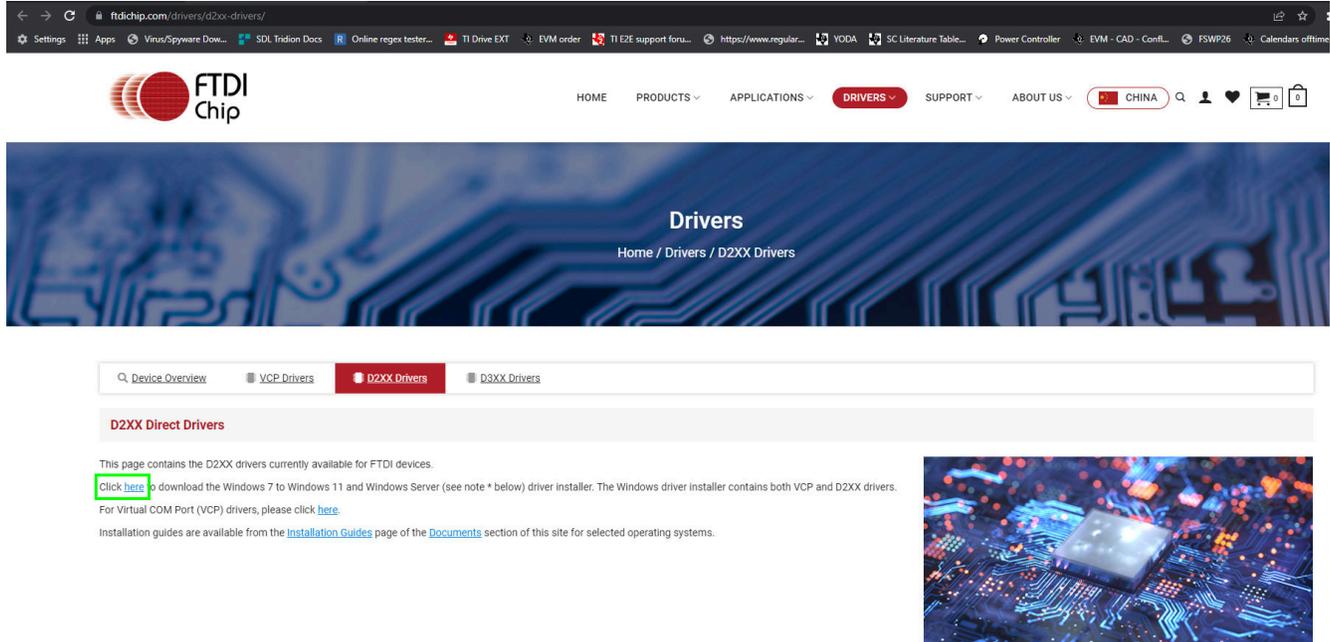
The HSDC Pro software must be installed before connecting the TSW14J59EVM to the PC for the first time.

2.2.1 Installing the High Speed Data Converter (HSDC) Pro Software

1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

2.2.2 Installing the DAC39RF10EVM Configuration GUI Software

1. If installing the DAC GUI for the first time, then download and install the FTDI drivers from the [FTDI website](#). Restarting the PC can be required after installing the driver.
2. Download the Configuration GUI software from the [DAC39RF10EVM tool folder](#).
3. Extract files from the .zip file.
4. Run the executable file (DAC39RF10 .exe).



Name	Date modified	Type	Size
DAC39RF10 User Files	4/23/2023 3:10 PM	File folder	
supportfiles	4/23/2023 3:10 PM	File folder	
DAC39RF10.exe	4/22/2023 5:35 AM	Application	15,251 KB

Figure 2-2. FTDI Website To Download And Install The Driver

2.2.3 Connect the TRF1108-DAC39RFEVM and TSW14J59EVM

1. With the power off, connect the TRF1108-DAC39RFEVM to the TSW14J59EVM through the FMC+ connector as shown in [Section 2.2](#). Make sure that the standoffs provide the proper height for robust connector connections.

2.2.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12V DC (minimum 6A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the TSW14J59EVM power connector.
2. TRF1108-DAC39RFEVM can be powered with 12V DC (minimum 2A) though the connector jack (J1) on the TRF1108-DAC39RFEVM or can be powered from the TSW14J59EVM via FMC+ connector. There is a switch (SW1) which can be used to select power from the barrel jack on the DAC EVM or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the power supply of the TRF1108-DAC39RFEVM is set to the opposite position (jack) from which power flows through. If using the barrel jack option, then connect the power cable to a 12V DC (minimum 2A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector. To power the DAC EVM, see [Table 2-1](#).

Table 2-1. Powering the TRF1108-DAC39RFEVM

TRF1108-DAC39RFEVM Powered from	TRF1108-DAC39RFEVM Power Switch Position	TSW14J59EVM FMC Switch Position	Power Supply Needed
TSW14J59EVM via FMC+ connector	FMC (Default option)	ON	12V 6A for TSW14J59EVM
External supply with jack on TRF1108-DAC39RFEVM	JACK	OFF	12V 5A for TSW14J59 and 12V 2A for TRF1108-DAC39RFEVM

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so can result in immediate damage. Leave the power switches in the off position until directed later.

2.2.5 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the OUTA SMA connector of the TRF1108-DAC39RFEVM.

When LMX->DACCLK | LMX/LMK->FPGA Clocking option is Used (Default)

1. Connect a signal generator to the LMX CLKp input of the EVM. This signal generator must be a low-noise signal generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 10.24GHz (for this example 10.24GHz is used). For best performance when using an RF signal generator, the power input to the LMX CLKp SMA connector must be 8-10 dBm (2Vpp into 50Ω).
2. This step is only needed if third clocking option(EXT-> DACLK | LMK->FPGA) is used otherwise skip to next step. Connect a signal generator to the SMA labeled LMK CLKp input of the EVM. This signal is used to generate the necessary FPGA clock signal. Configure the signal generator for the desired (160MHz) clock frequency. Set the output power to approximately 5–7 dBm.

Note

- a. The FPGA REF clock frequency can be obtained from the DAC39RF10EVM GUI. Once the DAC39RF10EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown in [Figure 2-3](#).
- b. Make sure that the DEVCLK and Reference clock sources are frequency-locked using a common 10MHz reference to for functionality.
- c. Do not turn on the RF output of any signal generator at this time.

2.2.6 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a USB-C[®] cable from the PC to the TSW14J59EVM.
3. If this is the first time connecting the TSW14J59EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. For specific instructions, see the [TSW14J59EVM JESD204C Data Capture and Pattern Generator Card](#) user's guide.

2.2.7 Turn On the TRF1108-DAC39RFEVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on TSW14J59EVM needs to be set to the ON position, and the power switch on the TRF1108-DAC39RFEVM needs to be set to FMC (default). If external power supply is used to power the DAC EVM, then turn on the 12V power supply connected to the barrel jack on the DAC EVM and set the power switch position on TRF1108-DAC39RFEVM to JACK position.

The green LED (D3) on DAC EVM turns on, indicating DAC EVM is getting power.

2. Connect the DAC EVM to the PC with the mini-USB cable via the FTDI DONGLE provided with the EVM.

2.2.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to LMX CLKp. If external clocking option is used, turn on the RF signal outputs connected to LMK CLKp(FPGA reference clock).

2.2.9 Launch the DAC39RF10EVM GUI and Program the DAC EVM

The DAC39RF10EVM configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Note

The max clock rate supported by TRF1108-DAC39RFEVM is 10240MHz

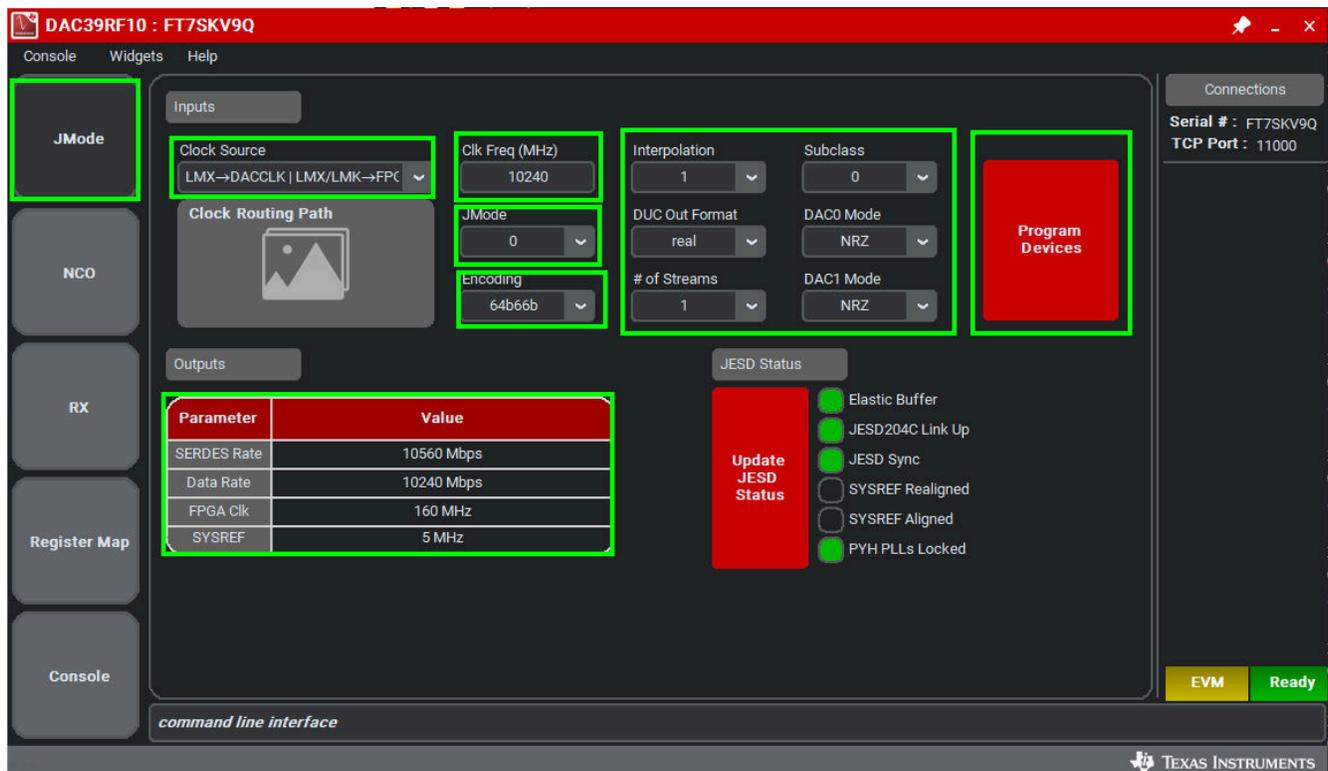


Figure 2-3. Configuration of DAC39RF10EVM GUI

The GUI opened to the *JMODE* tab and *NCO* tab, respectively, is shown in [Figure 2-3](#) and [Figure 2-5](#). Tabs at the left of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the DAC39RF10, LMX1204 and LMK04828. The register map for each device is provided in the device data sheet; see [Section 5.1](#).

1. Launch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240MHz.
4. Select JMODE0 for JMODE option.
5. Select 64b66b for Encoding option.
6. The other option can be left to default settings.
7. Click *Program Devices*.

Note

This action overwrites any previous device register settings.

2.2.10 Programming the NCO

The following steps are only needed when DAC is programmed to JMODE 1 to 7. For JMODE0 the NCO configuration can be skipped to [Section 2.2.11](#). For JMODEs 1 to 7 when number of streams *M* is greater than or equal to 2 and interpolation factor is also set to greater than or equal to 2, the NCO (numerically controlled oscillator) can be used to mix I/Q baseband signal to generate a higher output frequency signal from the output of the DAC.

CAUTION

Mixer Scaling

The DUC (digital up convertor) mixer supports complex-to-complex or complex-to-real-mixing of the complex interpolated input signal with the NCO frequency. The scaling in the mixer is exactly 1:1, so a full-scale 16-bit (absolute amplitude = 32767) complex tone results in a full-scale real or complex tone at the output. If the input absolute value of the complex amplitude exceeds 32767 the mixer saturates, then resulting in a corrupted waveform. The valid circular region in white and invalid corners in gray are shown in [Figure 2-4](#).

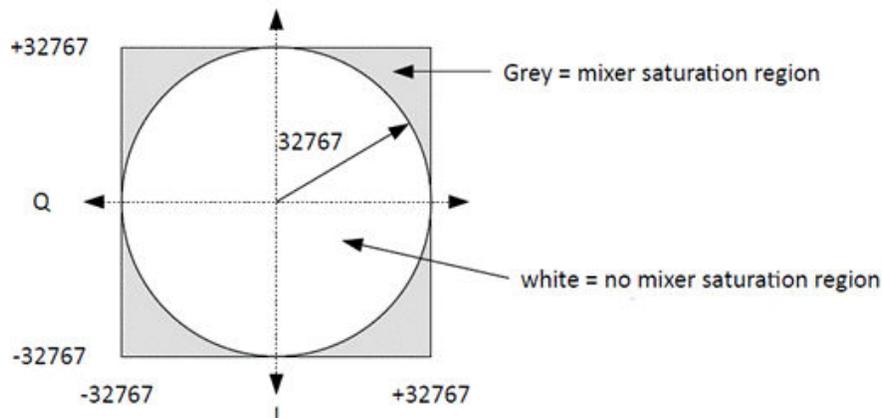


Figure 2-4. Mixer Saturation Region for the 16-bit Complex Input

The relationship of interpolation factor and number of streams to number of DUCs that can be used is shown in [Table 2-2](#).

Table 2-2. Supported Interpolation Factors vs Number of DUCs Enabled

Number of Streams	Interpolation Factors	DUCs Enabled
2	2-256x	DUC0
4	4-256x	DUC0, DUC1
6	8-256x	DUC0, DUC1, DUC2
8	8-256x	DUC0, DUC1, DUC2, DUC3

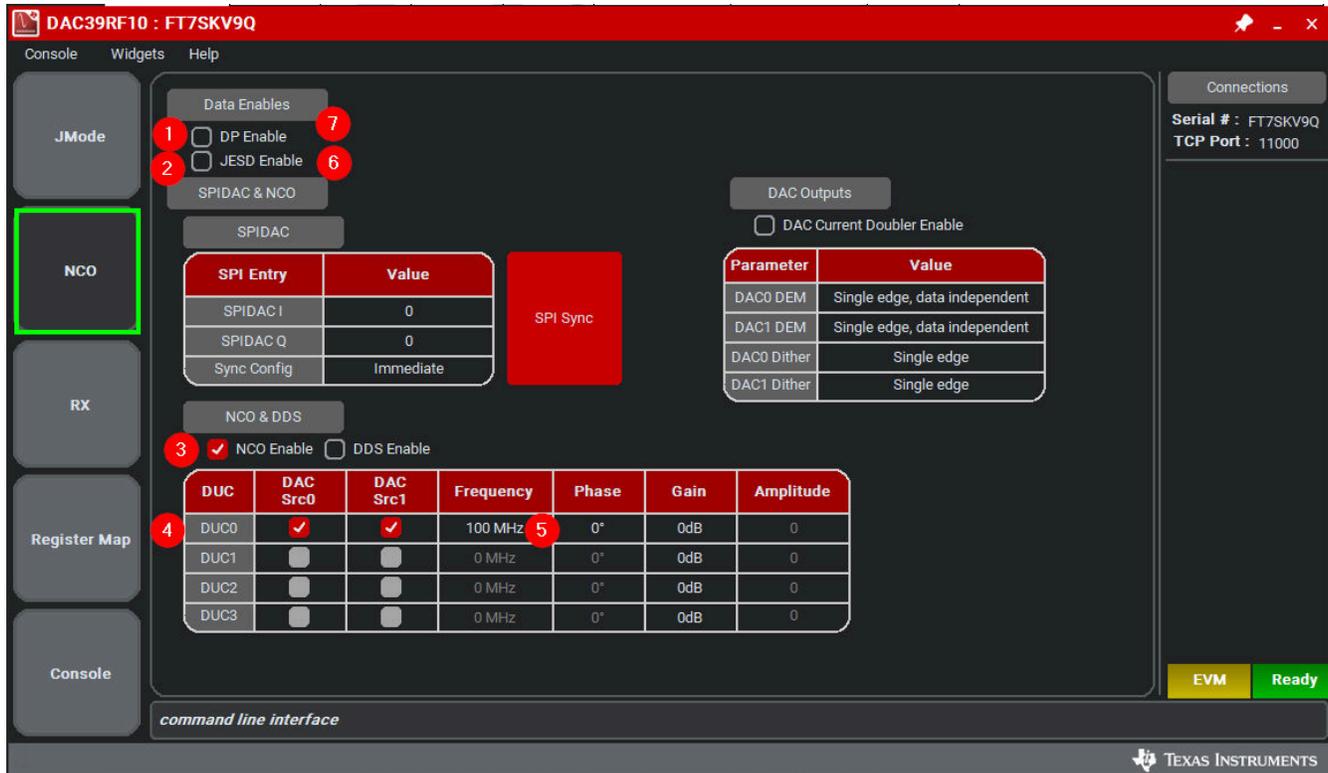


Figure 2-5. NCO TAB CONTROLS

With the EVM GUI open on the PC, navigate to NCO tab on upper left side of the GUI.

1. To set the NCO, uncheck the DP Enable box.
2. Uncheck the JESD Enable box.
3. Check the NCO Enable box.
4. In this example, JMODE was set to 1 and number of stream is set to 2. The interpolation factor is set to 2. Only DUC0 can be used, and other DUCs have been grayed out as shown in [Table 2-2](#). The data from DUC0 is routed to DAC0 and DAC1.
5. Enter the Frequency in MHz.
6. Check the JESD Enable box.
7. Check the DP Enable box.

2.2.10.1 SPIDAC (NCO only) Operation

The DAC can also be configured in SPIDAC Operation (NCO only mode). In NCO only mode, data streamed from JESD is ignored and DUCs inputs are driven by SPIDAC I and SPIDAC Q. This mode can be enabled when JESD Enable is set to 0, interpolation factor is greater than or equal to 2, DP Enable is set to 1, and the DAC is configured in NCO only mode. The correct combination of number of streams and interpolation factor needs to be selected to enable the desired number of DUCs and setting the desired outputs from respective DACs, as shown in [Table 2-2](#).

In the example, all the four DUCs are enabled. DUC0 and DUC1 are routed to DAC0. DUC2 and DUC3 are routed to DAC1. If more than one DUC is routed per DAC, then the DUC data into the DAC must be attenuated to prevent the DAC from saturating.

The NCO only mode can be configured through the GUI by following steps.

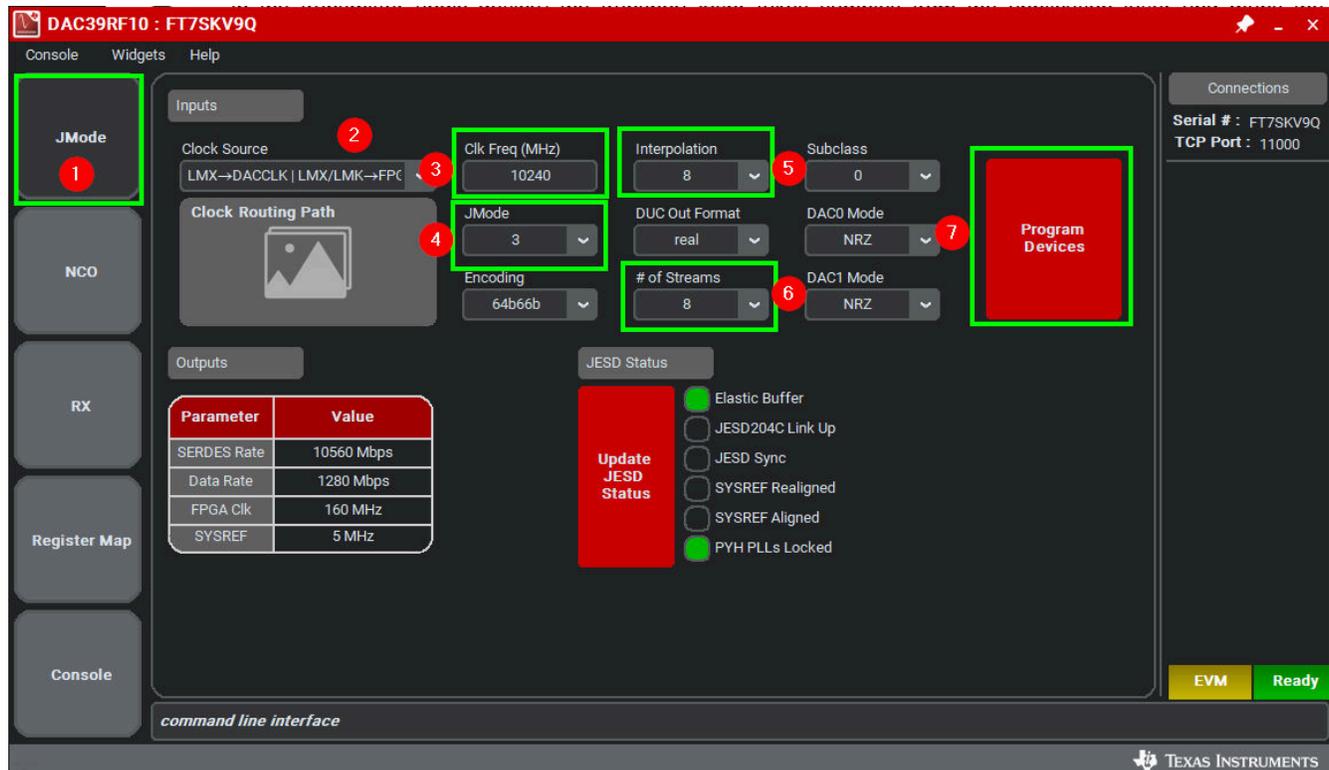


Figure 2-6. NCO only JMODE settings for GUI.

1. Launch the DAC39RF10EVM GUI.
2. Select the LMX->DACCLK | LMX/LMK->FPGA as the clock source.
3. Enter Clk Freq 10240MHz.
4. Select JMODE3 for JMODE option.
5. Select 8 for Interpolation.
6. Select 8 for number of streams.
7. Click the *Program Devices* button.
8. On the NCO tab, uncheck the DP Enable box.
9. Uncheck the JESD Enable box.
10. For SPIDAC I, enter the value of 32767 for full scale output power.
11. Check the NCO Enable box.
12. Select the correct DUC routing (DUC0 and DUC1 routed to DAC0 and DUC2; DUC3 routed to DAC1). Since two DUC are routed to single DAC, the gain value needs to be adjusted to -6dB to prevent the DAC from saturating.
13. Enter the desired frequency
14. Check the DP Enable.

15. Both channels on the DAC have outputs.

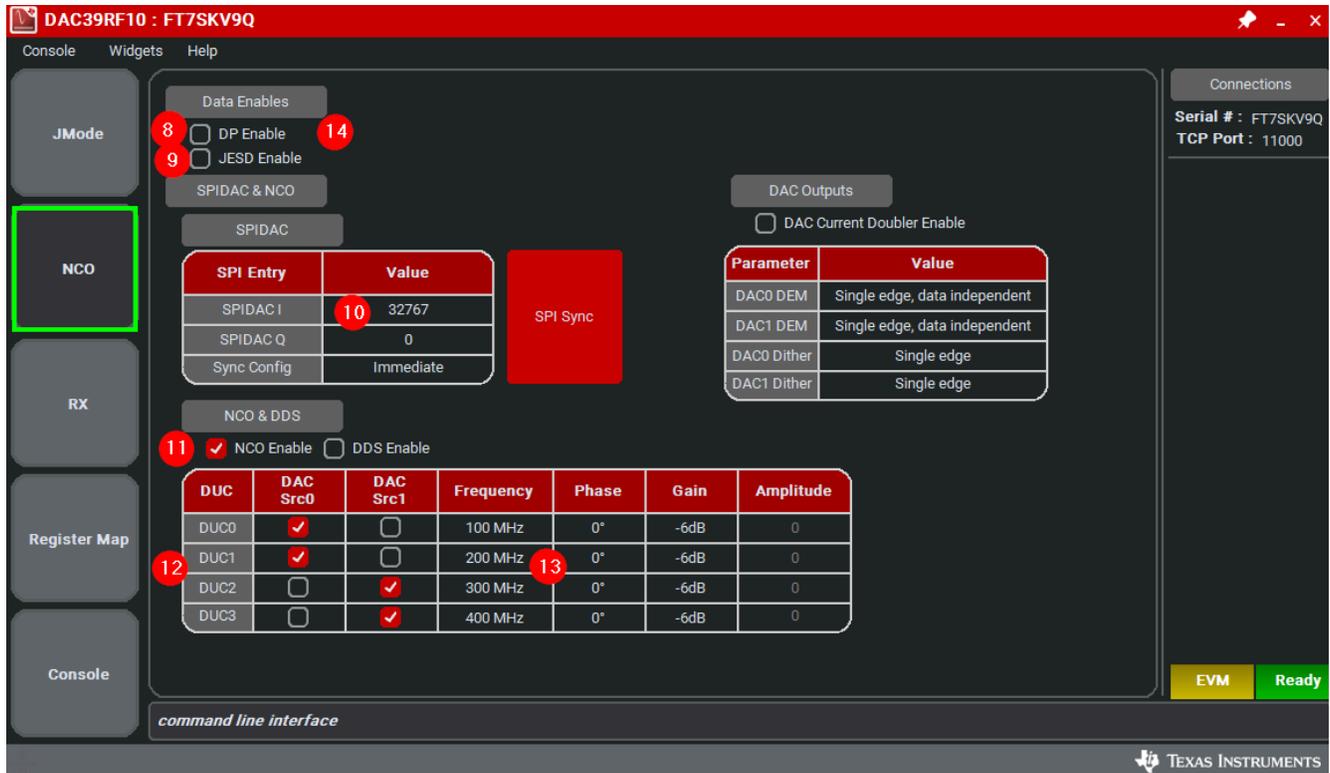


Figure 2-7. NCO Only Mode GUI Settings

Similar to SPI DAC mode, the DDS mode can be used as a lower power option. To enable DDS mode, the following steps are used.

1. Follow steps 1-9 from above.
2. Skip step 10.
3. For 11 step, check the NCO DDS Enable box.
4. Follow step 12.
5. Follow step 13.
6. For Amplitude (two DUCs routed to single DAC, amplitude reduced by 6dB from max value of 32767 to 16384), program 16384.
7. Follow step 14.
8. Both channels on the DAC have outputs.

2.2.11 Launch the HSDCpro Software and Load the FPGA Image to the TSW14J59EVM

1. Launch the HSDCpro 5.303 or later software.
2. Click **OK** to confirm the serial number of the TSW14J59EVM device. If multiple TSWxxxx boards are connected, then select the model and serial number for the one connected to the TRF1108-DAC39RFEVM.
3. For the *Device*, select **DAC** from the drop-down menu.

Note

If the pop-up window says *No Firmware*, then select a device to load firmware into the board and click **OK** to proceed to the next step.



Figure 2-8. Launching HSDCpro and Setup

4. Select the DAC39RF1x_JMODE0 device from the DAC select drop-down in the top left corner.
5. When prompted, click **Yes** to update the firmware (wait for firmware to download).

Note

If the user configures the EVM with options other than the default register values, then different instructions can be required for selecting the device in HSDC Pro. For more details, see [Section 2.5](#).



Figure 2-9. HSDCpro Setup

6. Enter the data rate as *10.24G* or the desired input data rate. The data rate value can be referenced from the DAC39RF10EVM GUI and is displayed on output parameter as shown in [Figure 2-3](#).
7. For DAC Option drop-down, select the *Offset Bin* option. The DAC39RF10EVM GUI always defaults to offset binary.
8. Navigate to lower left side of the HSDCpro GUI to I/Q Multitone Generator section. For # of tones, enter 1. For Tone Center, enter 1G (1GHz or desired frequency); # of samples can be left 65536.
9. Tone selection needs to be *Real*, since this is JMODE0; the DUC/ NCO is bypassed. If another JMODE was configured, such that DUC/NCO was used, then the Tone selection needs to be *Complex*.

- Click *Create Tones* button and then click *Send* in upper left side of HSDCpro GUI. If a pop-up window appears mentioning the SERDES RATE, then click *OK*. The DAC sends the programmed frequency to the outputs.

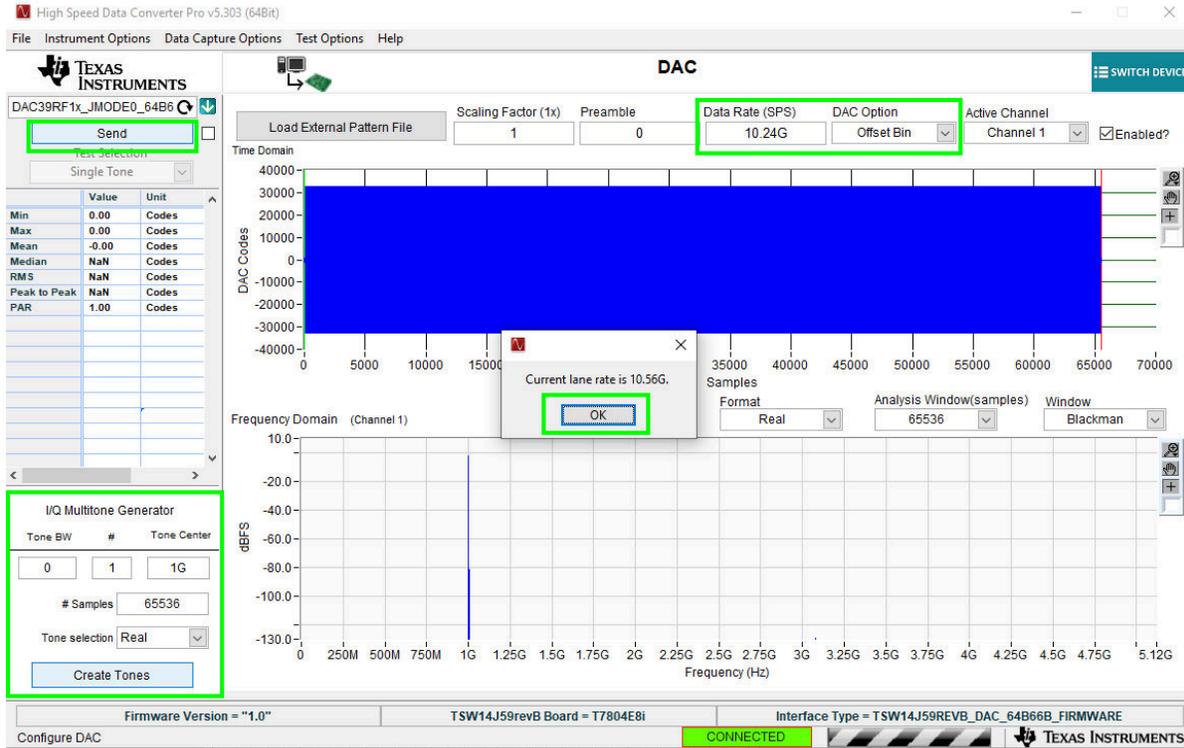


Figure 2-10. HSDCpro Generating the Tone and Sending to the DAC

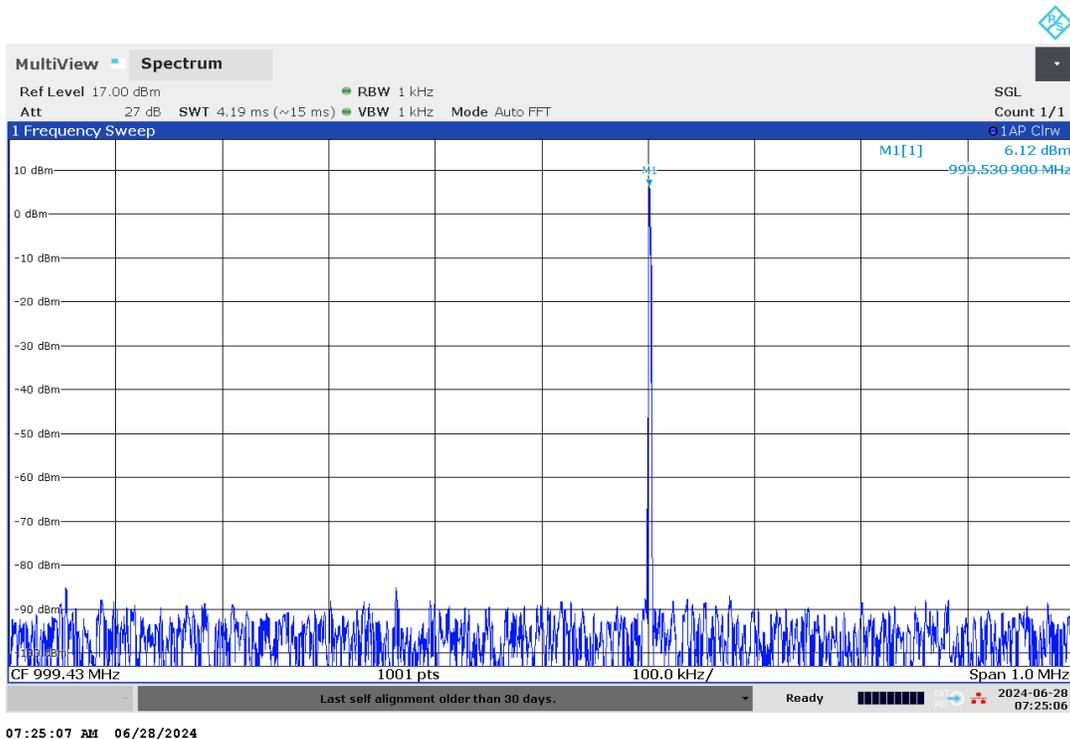


Figure 2-11. DAC Output Displayed on Spectrum Analyzer

2.3 Device Configuration

The DAC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the FTDI dongle. A GUI is provided to write instructions on the bus and program the registers of the DAC device.

For more information about the registers in the DAC device, see the [DAC39RF10, DAC39RFS10 10.24, 20.48-GSPS, 16-bit, Dual and Single Channel, Multi-Nyquist Digital-to-Analog Converter \(DAC\) with JESD204B, C Interface](#) data sheet.

2.3.1 Supported JESD204C Device Features

The DAC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J59EVM firmware, all JESD204C link features of the DAC device are not supported. [Table 2-3](#) lists the supported and non-supported features.

Table 2-3. Supported and Non-Supported Features of the JESD204C Device

JESD204C Feature	Supported by DAC Device	Supported by TSW14J59EVM
Number of lanes per link (L)	L = 1, 2, 3, 4, 6, 8, 12, 16 ⁽¹⁾	L = 1, 2, 3, 4, 6, 8, 12, 16 supported
Scrambling	Supported	Supported
Test patterns	PRBS7, PRBS9, PRBS15, PRBS31	Not Supported
Speed	Lane rates from 0.75 to 12.8 Gbps	Lane rates from 2 to 17.16 Gbps $f_{(\text{SAMPLE})}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

2.3.2 Tab Organization

Control of the DAC device features are available in the JMode, NCO and RX tabs.

2.3.3 Register Map and Console Control

The *Register Map* tab, illustrated in [Figure 2-12](#), allows configuration of the devices at the bit-field level. At any time, the controls in [Table 2-4](#) can be used to configure or read from the device.

The Console tab logs all the SPI reads and writes which are performed when various devices are programmed on the DAC EVM . The config files can saved and loaded from the console tab.

Table 2-4. Register Map and Console Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers <ul style="list-style-type: none"> Clicking on a register field allows individual bit manipulation in the register data cluster The value column shows the value of the register at the time the GUI was last updated The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the <i>Write Data</i> field
Write all button	Update all registers shown in the register map summary with the values shown in the <i>Register Map</i> summary
Read register button	Read from the register highlighted in the <i>Register Map</i> summary and display the results in the <i>Read Data</i> field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the <i>Register Map</i> summary and display the current state of the hardware
<i>Load Configuration</i> button	Load a configuration file from disk and register address/data values in the file
<i>Save Configuration</i> button	Save a configuration file to disk that contains the current state of the configuration registers
<i>Register Data</i> cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the <i>Block</i> drop-down box using the address and write data information

DAC39RF10 : FT7SKV9Q

Console Widgets Help

Register Name **Address** **Default** **Mode** **Size** **Value**

DAC39RF10						
CONFIG_A	0x0000	0x30	R/W	8	0x30	
DEVICE_CONFIG	0x0002	0x00	R/W	8	0x00	
CHIP_TYPE	0x0003	0x00	R	8	0x00	
CHIP_ID	0x0004	0x00	R	8	0x00	
CHIP_ID	0x0005	0x00	R	8	0x00	
CHIP_VERSION	0x0006	0x00	R	8	0x00	
VENDOR_ID	0x000C	0x00	R	8	0x00	
VENDOR_ID	0x000D	0x00	R	8	0x00	
SYSREF_CTRL	0x0080	0x40	R/W	8	0x40	
SYSREF_POS	0x0090	0x00	R	8	0x00	
SYSREF_POS	0x0091	0x00	R	8	0x00	
SYSREF_POS	0x0092	0x00	R	8	0x00	
SYSREF_ALIGN	0x00A0	0x00	R/W	8	0x00	
SYSREF_CFG	0x00A1	0x00	R/W	8	0x00	
JESD_EN	0x0100	0x00	R/W	8	0x00	
JMODE	0x0101	0x00	R/W	8	0x00	
JESD_M	0x0102	0x01	R/W	8	0x01	
JCTRL	0x0103	0x03	R/W	8	0x03	
SHMODE	0x0104	0x00	R/W	8	0x00	
KM1	0x0105	0x1F	R/W	8	0x1F	
RBD	0x0106	0x00	R/W	8	0x00	
JESD_STATUS	0x0107	0x00	R/W	8	0x00	
REFDIV	0x0108	0x30	R/W	8	0x30	
MPY	0x0109	0x14	R/W	8	0x14	

Register : CONFIG_A [0x0000]

Block: DAC39RF10

Register Address: 0x0000 Register Value: 0x30

Register Name: CONFIG_A

Current Register: Write All Block Registers: To Default

Read Read All

Register Description: CONFIG_A [0x0000]

Configuration A (default: 0x30)
[7] SOFT_RESET

Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing and will always read zero. After writing this bit, the part may take up to 150ns to reset. During this time, do not perform any SPI transactions.

Serial #: FT7SKV9Q
TCP Port: 11000

EVM Ready

command line interface

DAC39RF10 : FT7SKV9Q

Console Widgets Help

Load File Save File Clear Log

LOG OF REGISTER WRITES

```

LMK04828.write(0x140,0xFF)
LMK04828.write(0x11C,0x22)
LMK04828.write(0x11F,0x11)
LMK04828.write(0x11E,0xF0)
LMX1204.write(0x09,0x0010)
LMX1204.write(0x10,0x1200)
DAC39RF10.write(0x0000,0x80)
time.sleep(0.1)
DAC39RF10.write(0x0101,0x03)
DAC39RF10.write(0x0102,0x08)
DAC39RF10.write(0x0103,0x13)
DAC39RF10.write(0x0108,0x20)
DAC39RF10.write(0x0109,0x21)
DAC39RF10.write(0x010A,0x00)
DAC39RF10.write(0x010B,0x00)
DAC39RF10.write(0x0103,0x13)
DAC39RF10.write(0x0103,0x11)
DAC39RF10.write(0x01C2,0x01)
DAC39RF10.write(0x02E1,0x05)
DAC39RF10.write(0x02E3,0x00)
DAC39RF10.write(0x02E3,0x00)
DAC39RF10.write(0x02E3,0x11)
DAC39RF10.write(0x02E8,0x00)
DAC39RF10.write(0x0723,0x1F)
DAC39RF10.write(0x0724,0x0F)
DAC39RF10.write(0x0725,0x1F)
DAC39RF10.write(0x0726,0x0F)
DAC39RF10.write(0x072E,0x14)
DAC39RF10.write(0x072F,0x14)
DAC39RF10.write(0x0739,0x14)
DAC39RF10.write(0x0100,0x01)
DAC39RF10.write(0x02E0,0x01)

```

Serial #: FT7SKV9Q
TCP Port: 11000

EVM Ready

command line interface

Figure 2-12. Register Map Tab

2.4 Troubleshooting the TRF1108-DAC39RFEVM

Some troubleshooting procedures are shown in [Table 2-5](#).

Table 2-5. Troubleshooting

Issue	Troubleshoot
General problems	<ul style="list-style-type: none"> • Verify the test setup is similar to Figure 2-1. Repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J59EVM. Verify that the power switch is in the ON position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Make sure the board-to-board FMC+ connection is secure. • Press the <i>CPU_RESET</i> button on the TSW14J59EVM. Try clicking <i>Instrument Options</i> → <i>Reset Board</i> after changing the DAC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the DAC, LMX and LMK devices.
TSW14J59 LEDs are not correct	<ul style="list-style-type: none"> • Verify the settings of the configuration switches on the TSW14J59EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the DAC device internal registers are configured properly. • If LEDs are not blinking, then reprogram the DAC EVM devices. • Try pressing the <i>CPU_RESET</i> button, on the TSW14J59EVM. • Try clicking <i>SEND</i> button in HSDC Pro again.
Configuration GUI is not working properly	<ul style="list-style-type: none"> • Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a <i>USB serial device</i> is recognized when the EVM is connected to the PC. • Verify that the yellow EVM <i>Status</i> LED light in the lower right corner of the GUI is on. If the light is not on, then try restarting the GUI and reconfiguring the devices.
Configuration GUI is not able to connect to the EVM	<ul style="list-style-type: none"> • Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description <i>ADC12DJxx00RF</i>.
DAC output looks incorrect, distorted or there is no output	<ul style="list-style-type: none"> • Verify that the TSW14J59EVM is properly connected to the PC with a USB-C cable and that the board serial number is properly identified by the HSDC software. • Check that the proper DAC device mode is selected. The mode must match in HSDC Pro and the DAC GUI. • Check that the configuration parameters are properly configured. • Select <i>Instrument Options</i> → <i>Download Firmware</i> and download 'TSW14J59REVB_DAC_64B66B_FIRMWARE.bit'. Try to send again. • Verify J13, J17, J14, J18 are installed correctly.
Output power looks low	<ul style="list-style-type: none"> • Check that the spectrum analyzer is set to proper settings. • SMA connector is properly connect to the DAC output and Spectrum analyzer. • Verify J13, J17, J14, J18 are installed correctly.

2.5 Customizing the EVM for Optional Clocking Support

The TRF1108-DAC39RFEVM can be clocked using 3 different methods: LMX->DACCLK | LMX/LMK-> FPGA option, EXT->DACCLK | LMX/LMK-> FPGA option and EXT->DACCLK | LMK-> FPGA option.

2.5.1 LMX->DACCLK | LMX/LMK-> FPGA option (Default)

By default, the EVM is configured to use LMX->DACCLK | LMX/LMK->FPGA clock option. The user provides a single high frequency (8-10dBm) signal to an SMA labeled LMX CLKp. This signal is routed to LMX1204, which generates the buffered DACCLK signal, low frequency DAC SYSREF signal, FPGA reference clocks, and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 is used in clock distribution mode and provides several copies or divided down version of the FPGA reference clock and FPGA SYSREF signal.

The EVM can be configured to use LMX->DACCLK | LMX/LMK->FPGA clock option with the following steps:

1. Modify the hardware:
 - a. Remove C136 and C139, populate C141 and C142.
 - b. Remove C134 and C135, populate C138 and C140.
 - c. Remove C75 and C76, populate C73 and C74.

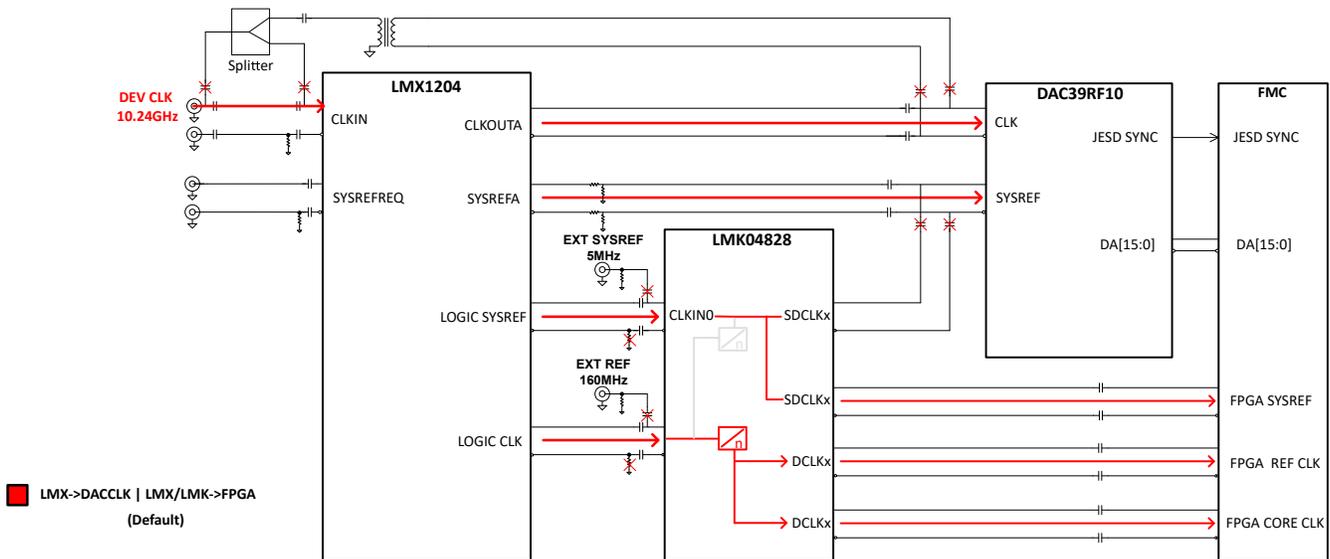


Figure 2-13. LMX->DACCLK | LMX/LMK->FPGA Clocking System Block Diagram

2.5.2 EXT->DACCLK | LMX/LMK-> FPGA Clocking Option

The TRF1108-DAC39RFEVM can be configured to use EXT->DACCLK | LMX/LMK-> FPGA Clocking option. Similar to above use case The user provide a single high frequency (10-15 dBm) signal to an SMA labeled LMX CLKp. This signal is routed though the splitter to Balun and LMX1204. The Balun converts the single ended signal into differential and is used to clock the DAC. The second output from the splitter is used by LMX1204 which generates the low frequency DAC SYSERF signal, FPGA reference clocks and FPGA SYSREF signal. The FPGA reference clocks and FPGA SYSREF signal are feed into the CLKIN1 and CLKIN0 of LMK04828. The LMK04828 and is used in clock distribution mode and provides several copies/divided down version of FPGA reference clock and FPGA SYSREF signal. The block diagram of clocking option is shown in [Figure 2-14](#).

The EVM can be configured to use onboard clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C75 and C76, populate C73 and C74

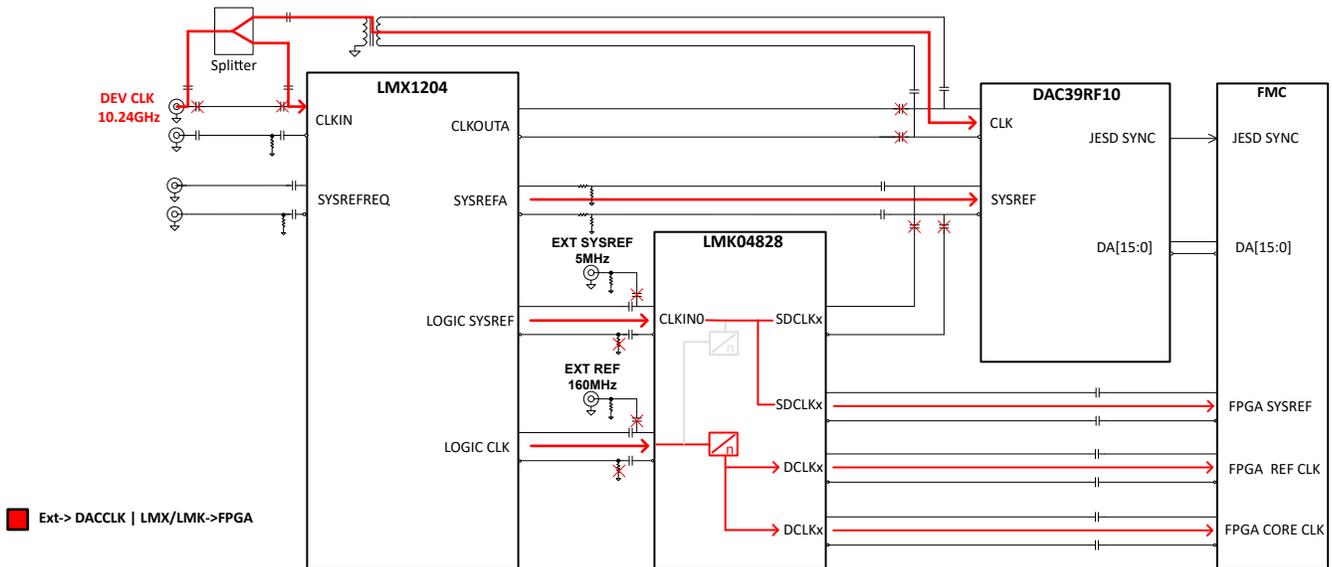


Figure 2-14. EXT->DACCLK | LMX/LMK-> FPGA Clocking System Block Diagram

2.5.3 EXT->DACCLK | LMK-> FPGA Clocking Option

The TRF1108-DAC39RFEVM can be configured to use EXT->DACCLK | LMK-> FPGA Clocking option. In this use case, the user provides a two clock signal; a high frequency (10-15dBm) signal to an SMA labeled LMX CLKp. This signal is routed through the splitter to Balun and LMX1204. The Balun converts the single-ended signal into differential and is used to clock the DAC. The second low frequency signal is CLKIN1 input of LMK04828. The LMK04828 is used to generate the low frequency DAC SYSREF signal, FPGA reference clocks, and FPGA SYSREF signal. The LMK04828 is used in clock distribution mode and provides several copies or a divided-down version of FPGA reference clock and FPGA SYSREF signal. The block diagram of external reference clocking options is shown in Figure 2-15.

The EVM can be configured to use external reference clocking option with the following steps:

- Remove C141 and C142, populate C136 and C139
- Remove C138 and C140, populate C134 and C135
- Remove C65 and R64, populate C64 and R66
- Remove C73 and C74, populate C75 and C76
- Remove C88 and R69, populate C83 and R71

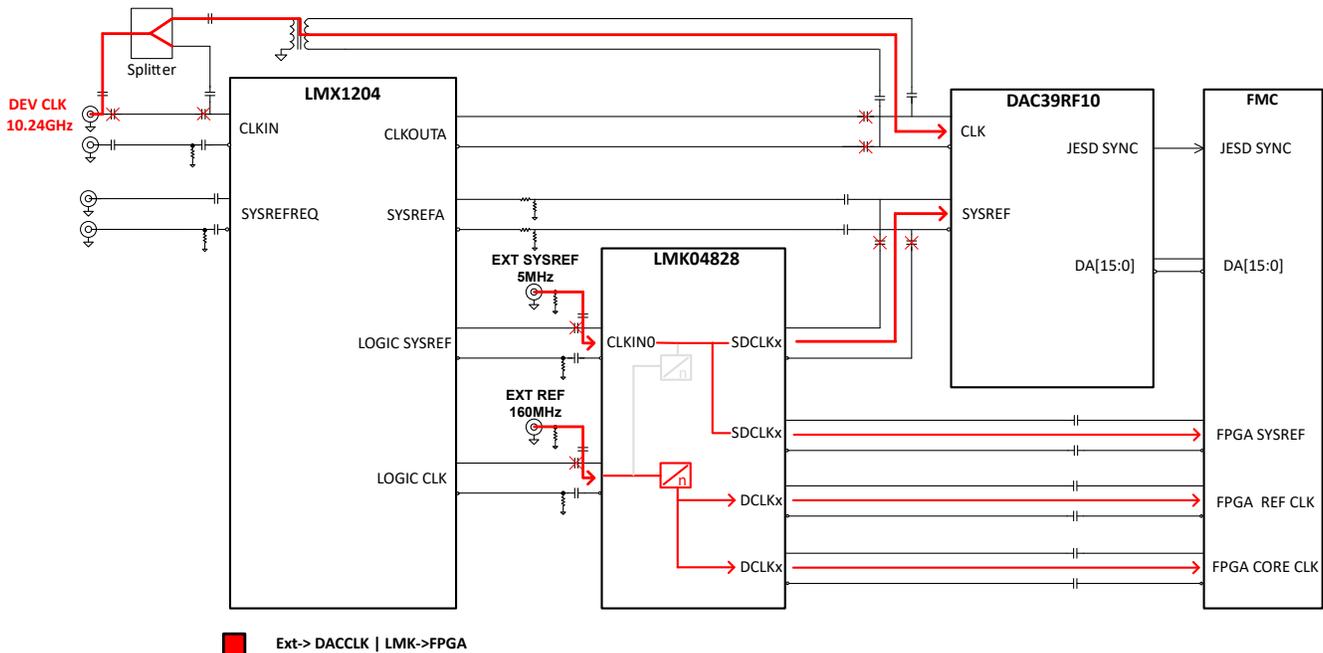


Figure 2-15. External Reference Clocking System Block Diagram

2.6 Signal Routing

The signal routing details for the TRF1108-DAC39RFEVM are shown in [Table 2-6](#).

Table 2-6. TRF1108-DAC39RFEVM Signal Routing

JESD204C Inputs	FMC(+) Pi	FMC(+) Signal Names ⁽¹⁾
Lane0	A38,A39	DP5_C2M_INV
Lane1	B36,B37	DP6_C2M_INV
Lane2	B32,B33	DP7_C2M_INV
Lane3	A34,A35	DP4_C2M_INV
Lane4	Y30,Y31	DP13_C2M_INV
Lane5	A30,A31	DP3_C2M_INV
Lane6	Z28,Z29	DP12_C2M_INV
Lane7	B28,B29	DP8_C2M_INV
Lane8	Y6,Y7	DP21_C2M_INV
Lane9	C2,C3	DP0_C2M_INV
Lane10	Z8,Z9	DP20_C2M_INV
Lane11	A22,A23	DP1_C2M_INV
Lane12	Z24,Z25	DP10_C2M_INV
Lane13	B25,B26	DP9_C2M_INV
Lane14	Y26,Y27	DP11_C2M_INV
Lane15	A26,A27	DP2_C2M_INV

(1) Red items with _INV in the signal name are inverted with respect to standard FMC polarity.

2.7 Jumpers and LEDs

The jumper settings are shown in [Table 2-7](#). The LED functionality is shown in [Table 2-8](#).

Table 2-7. Jumper Settings

Label	Description	Function
J12	Selects the source for SPI signals	Uninstalled (default): SPI signals to various device on the EVM are controlled by the FTDI dongle board. Installed: SPI signals from FMC+ connector are controlling the devices on the EVM (this feature is supported on the next rev of the board).
J13	Power down for TRF1108 on CHA	Installed (default): pulls the power-down pin on the TRF1108 to low, enabling the amplifier.
J14	Test pin for TRF1108 on CHA	Installed (default): pulls the test pin to low.
J16	External Supply connection for TRF1108 amplifiers	Uninstalled (default): connection to supply rails for TRF1108 amplifiers debugging purposes.
J17	Power down for TRF1108 on CHB	Installed (default): pulls the power-down pin on the TRF1108 to low, enabling the amplifier.
J18	Test pin for TRF1108 on CHB	Installed (default): pulls the test pin to low.

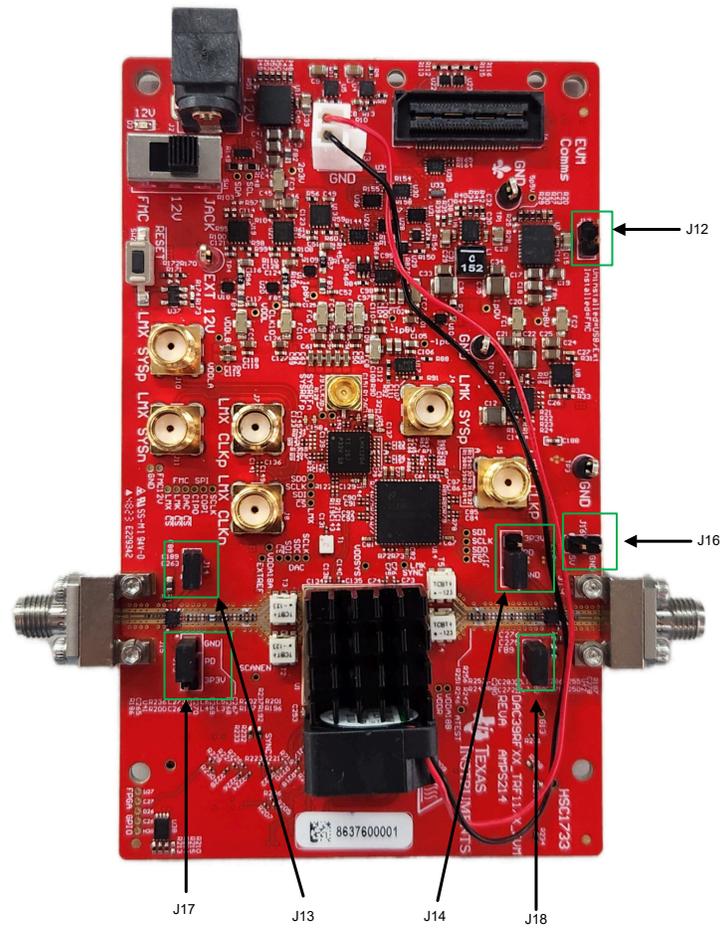


Figure 2-16. Jumper Locations

Table 2-8. LEDs

Label	Function
D3	12V power indicator

3 Hardware Design Files

3.1 Schematics

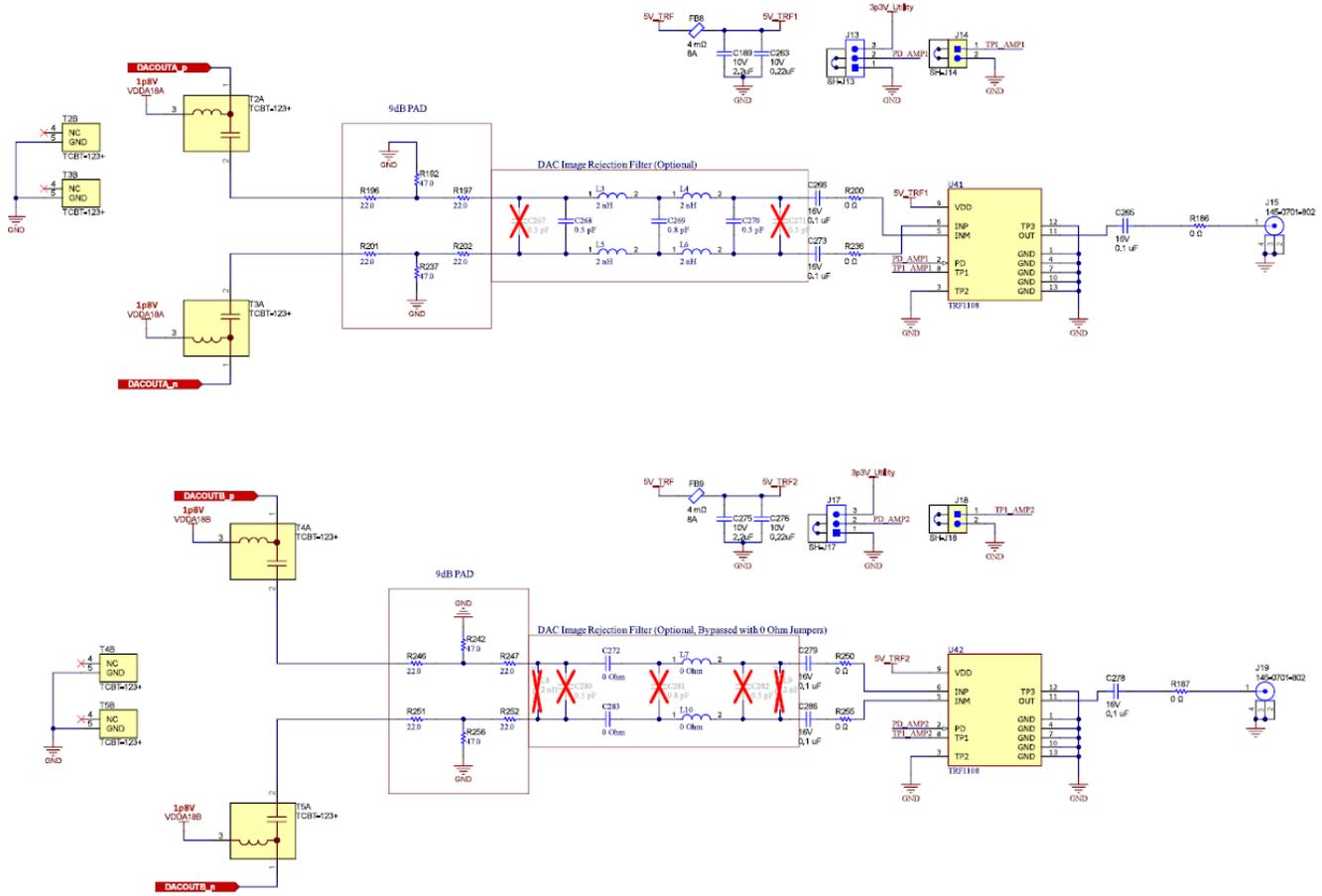


Figure 3-1. Analog Output Path Schematic

A 9dB attenuation pad is added between the inputs and the DAC. The 9dB pad helps with the flatness of the frequency response along with preventing saturation of the amplifiers.

3.2 PCB Layouts

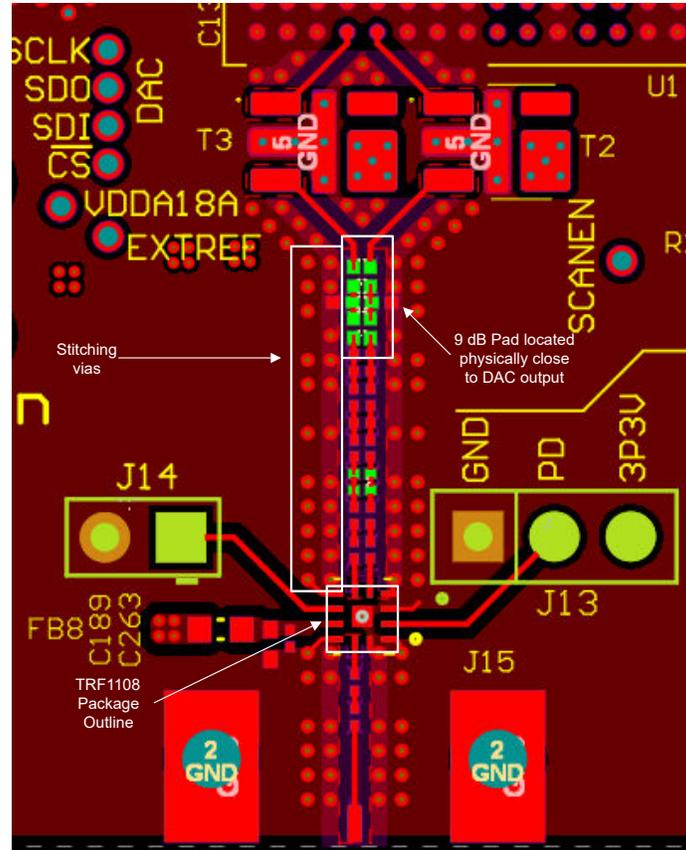


Figure 3-2. Layout Suggestions

Any high frequency board presents unique challenges for implementation. The DAC39RF10 presents a maximum sampling rate of 20.48 GSPS. Therefore, the first nyquist of this device is 10.24GHz. Care must be taken when laying out this design.

On the TRF1108-DAC39RFEVM, the analog front end is an example of this. First, the trace widths and distances to the top ground plane must be carefully chosen to present as 50Ohm transmission lines. Stitching vias are recommended at $<1/8$ th wavelength distance from each other to connect the top ground plane to the adjacent ground plane. The 9dB pad is also located as close to the DAC output as physically possible.

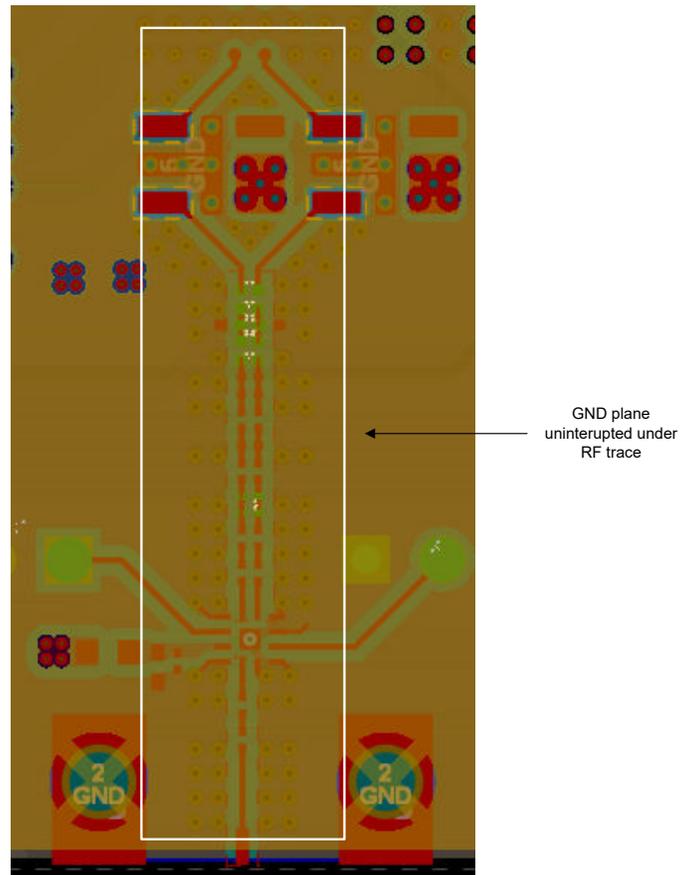


Figure 3-3. RF Ground Plane

The ground plane directly adjacent to the top plane is uninterrupted underneath the RF trace. This prevents excess inductance and thus incorrect impedance of the RF trace.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	Megtron6	4.90mil	3.34	
2	L2 GND1	CF-004	1.40mil		
	Dielectric 2	FR4-370HR	3.00mil	3.72	
3	L3 PWR1	CF-004	1.40mil		
	Dielectric 3	FR4-370HR	3.00mil	3.72	
4	L4 GND2	CF-004	1.40mil		
	Dielectric 4	FR4-370HR	3.00mil	3.86	
5	L5 PWR2	CF-004	1.40mil		
	Dielectric 5	FR4-370HR	3.00mil	3.72	
6	L6 GND3	CF-004	1.40mil		
	Dielectric 6	FR4-370HR	3.00mil	3.86	
7	L7 Ctrl Signal 1	CF-004	1.40mil		
	Dielectric 8	FR4-370HR	3.00mil	3.72	
	Dielectric 7	FR4-370HR	3.00mil	3.72	
8	L8 GND4	CF-004	1.40mil		
	Dielectric 9	FR4-370HR	6.00mil	3.86	
9	L9 GND5	CF-004	1.40mil		
	Dielectric 11	FR4-370HR	3.00mil	3.72	
	Dielectric 10	FR4-370HR	3.00mil	3.72	
10	L10 Ctrl Signal 2	CF-004	1.40mil		
	Dielectric 12	FR4-370HR	3.00mil	3.86	
11	L11 GND6	CF-004	1.40mil		
	Dielectric 13	FR4-370HR	3.00mil	3.72	
12	L12 PWR3	CF-004	1.40mil		
	Dielectric 14	FR4-370HR	3.00mil	3.86	
13	L13 GND7	CF-004	1.40mil		
	Dielectric 15	FR4-370HR	3.00mil	3.72	
14	L14 PWR4	CF-004	1.40mil		
	Dielectric 16	FR4-370HR	3.00mil	3.72	
15	L15 GND8	CF-004	1.40mil		
	Dielectric 17	Megtron6	4.90mil	3.34	
16	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				
Total board thickness:			81.00mil		

Figure 3-4. Layer Stackup

The layer stackup, especially dielectric between the RF and RF ground layer must be optimized for controlled dielectric constant. Here, the dielectric was chosen as Panasonic Megtron6, with a highly controlled dielectric constant of 3.6.

Additionally, the solder mask layer was omitted from on top of and directly adjacent to the RF trace. This is because this layer often includes uncontrolled properties and, thus is generally not recommended to be included directly on high frequency lines.

3.3 Bill of Materials (BOM)

Table 3-1. Bill of Materials

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
C1	1	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X7R, 0805	C0805C105K5RAC7800	Kemet	0805
C2, C3	2	1 uF	CAP CER 1UF 50V X7R 0805	C2012X7R1H105K125AB	TDK Corporation	0805
C4, C37, C48, C67, C68, C69, C70, C71, C72, C77, C78, C79, C80, C81, C82, C95, C96, C113, C122, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C262	34	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 10%, X5R, 0402	GRM155R61E104KA87D	MuRata	0402
C5, C6	2	0.001 uF	CAP CER 1000PF 50V X7R 0603	CGA3E2X7R1H102K080AA	TDK Corporation	0603
C7, C9, C15, C28, C29, C39, C174	7	10 uF	CAP CER 10UF 25V X5R 0805	KGM21AR51E106KU	KYOCERA AVX	0805
C8, C10, C26	3	4.7 uF	CAP CER 4.7UF 10V X5R 0402	C1005X5R1A475K050BE	TDK Corporation	0402
C11, C12, C35, C36	4	47 uF	CAP CER 47UF 16V X5R 1210	1210YD476KAT2A	KYOCERA AVX	1210
C13, C14, C27, C146	4	0.01 uF	CAP CER 10000PF 10V X7R 0402	KGM05AR71A103MH	KYOCERA AVX	0402
C16, C40, C175	3	2200pF	CAP CER 2200PF 25V X7R 0402	KGM05AR71E222JH	KYOCERA AVX	0402
C17, C18, C19, C20, C21, C22, C24, C25, C33, C34, C41, C42, C43, C44, C45, C46, C176, C177, C178, C179	20	22 uF	CAP CER 22UF 10V X7S 0805	C2012X7S1A226M125AC	TDK Corporation	0805
C23, C47, C180	3	0.022 uF	CAP CER 0.022UF 25V X7R 0402	CGA2B2X7R1E223M050BA	TDK Corporation	0402
C30, C31	2	0.1 uF	CAP CER 0.1UF 25V X5R 0402	KGM05AR51E104KH	KYOCERA AVX	0402

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
C32, C65, C66, C73, C74, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C131, C138, C140, C141, C142, C143, C144, C148, C149, C150, C151, C152, C153, C155, C156, C157, C173, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C240, C241, C242, C243, C244, C246, C247, C249, C251, C256, C257, C258, C259, C260, C261, C265, C266, C273, C278, C279, C286	102	0.1 uF	Broadband Capacitors	0201BB104KW160	Passive Plus	0201
C38, C98, C106	3	2.2 uF	CAP CER 2.2UF 10V X5R 0402	C1005X5R1A225K050BC	TDK Corporation	0402
C49, C114, C123	3	0.1 uF	CAP CER 0.1UF 6.3V X5R 0402	04026D104KAT4A	KYOCERA AVX	0402
C50, C55, C59, C62, C63, C115, C120	7	1µF	CAP FEEDTHRU 1UF 20% 6.3V 0603	NFM18PC105R0J3D	Murata Electronics	0603

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
C51, C97, C100, C104, C105, C108, C112, C116, C124, C147	10	10 uF	CAP CER 10UF 10V X5R 0603	0603ZD106KAT2A	KYOCERA AVX	0603
C52, C56, C117, C121, C125, C128	6	1 uF	CAP CER 1UF 25V X5R 0402	C1005X5R1E105K050BC	TDK Corporation	0402
C53, C57, C60, C101, C109, C118, C126	7	10 uF	CAP CER 10UF 25V X5R 0603	GRM188R61E106KA73J	Murata	0603
C54, C58, C61, C102, C110, C119, C127	7	0.1 uF	CAP CER 0.1UF 25V X7R 0402	GRT155R71E104KE01J	Murata	0402
C94	1	10 uF	CAP CER 10UF 10V X5R 0603	C1608X5R1A106K080AC	TDK Corporation	0603
C99, C103, C107, C111	4	1 uF	CAP CER 1UF 10V X5R 0201	GRM033R61A105ME44D	Murata Electronics	0201
C129, C132, C133, C137, C145, C252, C253, C254, C255	9	0.47uF	CAP FEEDTHRU 0.47UF 6.3V 0402	NFM15PC474R0J3D	Murata	0402
C154, C158	2	100pF	CAP CER SMD	KGM03AR71H101KH	KYOCERA AVX	0201
C181, C184, C186, C264	4	22uF	CAP, CERM, 22uF, 10V, +/- 20%, X5R, 0603	CL10A226MP8NUNE	Samsung Electro-Mechanics	0603
C182, C185, C187, C189, C274, C275	6	2.2uF	CAP, CERM, 2.2uF, 10V, +/- 10%, X7S, 0402	C1005X7S1A225K050BC	TDK	0402
C183, C188	2	0.01uF	CAP, CERM, 0.01uF, 16V, +/- 10%, X7R, 0402	C0402C103K4RACTU	Kemet	0402
C263, C276	2	0.22uF	CAP, CERM, 0.22uF, 10V, +/- 20%, X5R, 0201	LMK063BJ224MP-F	Taiyo Yuden	0201
C268, C270	2		02013J0R5PBSTR\500	02013J0R5PBSTR\500	AVX Interconnect / Elco	
C269	1		02015J0R8PBSTR	02015J0R8PBSTR	AVX Interconnect / Elco	
C272, C283	2		0 Ohm Jumper	P15979CT-ND	Panasonic Electronic Components	
D1	1	30V	Diode, Schottky, 30V, 1A, SOD-123	MBR130T1G	ON Semiconductor	SOD-123
D2	1	15V	Diode, TVS, Bi, 15V, 24.4Vc, SMB	SMBJ15CA-13-F	Diodes Incorporated	SMB
D3	1		LED GREEN CLEAR CHIP SMD	LTST-C191TGKT	Lite-On Inc.	-

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
FB1, FB2, FB6, FB7, FB8, FB9, FB10	7	-	8.5Ohms at 100MHz 1 Power Line Ferrite Bead 0603 (1608 Metric) 8A 4mOhm	BLE18PS080SN1D	Murata	0603
FB3, FB4, FB5	3	-	FERRITE BEAD 30 OHM 0603 1LN	BLM18PG300SN1D	Murata Electronics	0603
FC1, FC2, FC3, FC4, FC5, FC6, FC7, FC8, FC9, FC10, FC12, FC13	12	27uF	Feed through capacitor 27uF	NFM31PC276B0J3L	Murata	1206
H1, H2	2		MACHINE SCREW PAN PHILLIPS 4-40	PMSSS 440 0025 PH	B&F Fastener Supply	-
H3, H4	2		Hex Standoff Threaded #4-40 Stainless Steel 1.250" (31.75mm) 1 1/4	2069-440-SS	RAF Electronic Hardware	-
J1	1		Connector, 1.27mm, 40x10, Black, SMT	ASP-184330-01	Samtec	-
J2	1		Power Jack, mini, 2.1mm OD, R/A, TH	RAPC722X	Switchcraft	-
J3	1		Header, 2.54mm, 2x1, Vertical, TH	22232021	Molex	-
J4, J5, J7, J8, J10, J11	6		SMA Connector Jack, Female Socket 50Ohm Surface Mount, Through Hole Solder	132134-15	Amphenol RF	-
J6	1		FTDI Dongle EVM Mating connector and standoff holes	QSH-030-01-L-D-A	Samtec	-
J9	1		SMP Connector Plug, Male Pin 50Ohm Surface Mount Solder	853050232	Molex	-
J12, J14, J16, J18	4		Header, 100mil, 2x1, Gold, TH	PBC02SAAN	Sullins Connector Solutions	-
J13, J17	2		Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec	3x1 Header
J15, J19	2		50 Ohm JACK, SMT	145-0701-802	Cinch Connectivity	50 Ohm JACK, SMT
L1	1	1.5µH	FIXED IND 1.5UH 11.1A 14.3 MOHM	XGL4020-152MEC	COILCRAFT	XGL4020
L3, L4, L5, L6	4		Film type RF Inductor 2nH ±0.05nH 600mA 0.12Ω 0201 (0603). LQP03HQ2N0W02D	LQP03HQ2N0W02D	Murata Electronics, [NoParam]	
L7, L10	2		Film type RF Inductor 2nH ±0.05nH 600mA 0.12Ω 0201 (0603). LQP03HQ2N0W02D	P15979CT-ND		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady	-
Logo1	1		FDL	FDL	-	-

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
MP1	1		Heat Sink Passive BGA Straight Adhesive 9.3C/W Black Anodized	ATS-54170R-C1-R0	Advanced Thermal Solutions	-
MP2, MP4	2		CONN 22-30AWG CRIMP TIN	8500113	Molex	-
MP3	1		CONN RCPT HSG 2POS 2.54MM	22013027	Molex	-
MP5	1		Fan Tubeaxial 5VDC Square - 17mm L x 17mm H Sleeve 0.636 CFM (0.018m ³ /min) 2 Wire Leads	F17HA-05HC	Nidec Copal	-
MP6, MP7	2		MACHINE SCREW PAN PHILLIPS 2-56, 0.5"	PMSSS 256 0050 PH	B&F Fastener Supply	-
Q1	1	20V	MOSFET, N-CH, 20V, 10A, DQK0006C (WSON-6)	CSD15571Q2	Texas Instruments	DQK0006C
R1, R36, R57	3	2mΩ	RES SHUNT, 0603, 0.002 OHM, 1%,	CSS0603FT2L00	Stackpole Electronics Inc	0603
R2	1	1MΩ	RES SMD 1M OHM 1% 1/10W 0402	ERJ-2RKF1004X	Panasonic Electronic Components	0402
R3	1	45.3kΩ	RES SMD 45.3K OHM 1% 1/10W 0402	ERJ-2RKF4532X	Panasonic Electronic Components	0402
R5	1	2.2kΩ	RES SMD 2.2K OHM 1% 1/8W 0805	ERJ-6ENF2201V	Panasonic Electronic Components	0805
R6	1	0Ω	RES 0 OHM JUMPER 1206 SMD	RCA12060000ZSEA	Vishay Dale	1206
R8, R9, R11, R15, R17, R20, R25, R31, R34, R35, R48, R49, R84, R86, R88, R91, R111, R112, R114, R115, R150, R151, R156, R161, R163, R178, R183, R189, R213, R214, R215	31	4.7kΩ	RES SMD 4.7K OHM 5% 1/10W 0402	ERJ-2GEJ472X	Panasonic Electronic Components	0402
R10	1	2MΩ	RES SMD 2M OHM 5% 1/10W 0402	ERJ-2GEJ205X	Panasonic Electronic Components	0402
R12	1	3.6MΩ	RES SMD 3.6M OHM 5% 1/10W 0402	ERJ-2GEJ365X	Panasonic Electronic Components	0402
R13, R14	2	1.2MΩ	RES SMD 1.2M OHM 5% 1/10W 0402	ERJ-2GEJ125X	Panasonic Electronic Components	0402

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
R18, R37, R38, R54, R55, R93, R94, R101, R102, R107, R113, R116, R172, R173, R204	15	0Ω	RES SMD 0 OHM JUMPER 1/10W 0402	ERJ-2GE0R00X	Panasonic Electronic Components	0402
R19, R24, R46, R63, R65, R68, R70, R119, R120, R121, R133, R136, R142, R143, R144, R145, R147, R152, R153, R154, R155, R158, R160, R162, R164, R165, R166, R167, R169, R175, R186, R187, R200, R205, R206, R207, R209, R211, R212, R216, R217, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R236, R250, R255	54	0Ω	RES SMD 0 OHM JUMPER 1/20W 0201	ERJ-1GN0R00C	Panasonic Electronic Components	0201
R27, R29, R182	3	18.2kΩ	RES SMD 18.2K OHM 1% 1/10W 0402	ERJ-2RKF1822X	Panasonic Electronic Components	0402
R30, R41, R53, R180	4	4.87kΩ	RES SMD 4.87K OHM 1% 1/10W 0402	ERJ-2RKF4871X	Panasonic Electronic Components	0402
R32	1	30.9kΩ	RES SMD 30.9K OHM 1% 1/10W 0402	ERJ-2RKF3092X	Panasonic Electronic Components	0402
R33, R40, R44, R45, R47, R56, R82, R83, R95, R104	10	10kΩ	RES 10K OHM 1% 1/10W 0402	ERJ-H2RF1002X	Panasonic Electronic Components	0402
R42	1	17.4kΩ	RES SMD 17.4K OHM 1% 1/10W 0402	ERJ-2RKF1742X	Panasonic Electronic Components	0402
R50	1	9.31kΩ	RES SMD 9.31K OHM 1% 1/10W 0402	ERJ-2RKF9311X	Panasonic Electronic Components	0402

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
R52	1	52.3kΩ	RES SMD 52.3K OHM 1% 1/10W 0402	ERJ-2RKF5232X	Panasonic Electronic Components	0402
R59	1	88.7kΩ	RES SMD 88.7K OHM 1% 1/10W 0402	ERJ-2RKF8872X	Panasonic Electronic Components	0402
R60	1	12.4kΩ	RES SMD 12.4K OHM 1% 1/10W 0402	ERJ-2RKF1242X	Panasonic Electronic Components	0402
R61	1	12kΩ	RES 12K OHM 0.5% 1/10W 0402 SMD	ERJ-U2RD1202X	Panasonic Electronic Components	0402
R62, R67, R125, R126	4	49.9Ω	RES SMD 49.9 OHM 1% 1/20W 0201	ERJ-1GNF49R9C	Panasonic Electronic Components	0201
R64, R69, R123, R128	4	100Ω	RES SMD 100 OHM 1% 1/20W 0201	ERJ-1GNF1000C	Panasonic Electronic Components	0201
R72, R73, R74, R75, R76, R77, R78, R79, R80, R81	10	120Ω	RES SMD 120 OHM 1% 1/20W 0201	ERJ-1GNF1200C	Panasonic Electronic Components	0201
R85, R90	2	255kΩ	RES SMD 255K OHM 1% 1/10W 0402	ERJ-2RKF2553X	Panasonic Electronic Components	0402
R87, R92	2	499kΩ	RES SMD 499K OHM 1% 1/10W 0402	ERJ-2RKF4993X	Panasonic Electronic Components	0402
R96, R105	2	20mΩ	RES SHUNT, 0603, 0.02 OHM, 1%, 0	CSS0603FT20L0	Stackpole Electronics Inc	0603
R98, R108	2	115kΩ	RES SMD 115K OHM 1% 1/10W 0402	ERJ-2RKF1153X	Panasonic Electronic Components	0402
R99, R109	2	33kΩ	RES SMD 33K OHM 1% 1/10W 0402	ERJ-2RKF3302X	Panasonic Electronic Components	0402
R100, R110	2	6.65kΩ	RES SMD 6.65K OHM 1% 1/10W 0402	ERJ-2RKF6651X	Panasonic Electronic Components	0402
R148, R149	2	2.2kΩ	RES SMD 2.2K OHM 5% 1/10W 0603	ERJ-3GEYJ222V	Panasonic Electronic Components	0603
R170	1	100kΩ	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	Panasonic Electronic Components	0402
R176	1	1kΩ	RES SMD 1K OHM 1% 1/10W 0402	ERJ-2RKF1001X	Panasonic Electronic Components	0402

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
R177	1	3.6kΩ	RES SMD 3.6K OHM 1% 1/10W 0402	ERJ-2RKF3601X	Panasonic Electronic Components	0402
R179	1	28.7k	RES, 28.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040228K7FKED	Vishay-Dale	0402
R184	1	10.5k	RES, 10.5 k, 1%, 0.1 W, 0603	RC0603FR-0710K5L	Yageo	0603
R185	1	2.00k	RES, 2.00 k, 1%, 0.1 W, 0603	RC0603FR-072KL	Yageo	0603
R192, R237, R242, R256	4	47	RES, 47.0, 1%, 0.05 W, 0201	ERJ-U01F47R0C	Panasonic Electronic Components	0201
R196, R197, R201, R202, R246, R247, R251, R252	8	22	RES, 22.0, 1%, 0.05 W, 0201	ERJ-U01F22R0C	Panasonic Electronic Components	0201
R208, R232, R233, R234	4	100Ω	RES SMD 100 OHM 5% 1/10W 0402	ERJ-2GEJ101X	Panasonic Electronic Components	0402
SH-J13, SH-J14, SH-J17, SH-J18	4		Shunt, 2.54mm, Gold, Black	60900213421	Würth Elektronik	Shunt, 2.54mm, Black
SW1	1		Switch Slide SPDT 120V, 6A	1101M2S3CGE2	C&K Components	-
SW2	1		SWITCH TACTILE SPST-NO 0.05A 24V	FSMSM	TE Connectivity	-
T1	1		1:2 LTCC Transformer, 4700 - 12000MHZ, 50Ω	NCR2-123+	Mini-Circuits	-
T2, T3, T4, T5	4		Signal Conditioning BIAS TEE SURFACE MOUNT	TCBT-123+	Mini-Circuits	-
TP1, TP2, TP3	3		Test Point, Multipurpose, Black, TH	5011	Keystone	-
TP4	1		Test Point, Multipurpose, Red, TH	5010	Keystone	-
U1	1			DAC39RF10ACK	Texas Instruments	
U2	1		12V, 5A, 30mΩ eFuse with Adjustable +/-15% Accurate Current Limit, DRC0010J (VSON-10)	TPS259261DRC	Texas Instruments	VSON-10
U3, U10, U12, U18, U20	5		28V, 16-Bit, I2C Output Current, Voltage and Power Monitor With Alert in WCSP Package	INA231AIYFFR	Texas Instruments	WCSP
U4, U5	2		300mA, 18V, Ultra-Low IQ, Low-Dropout Linear Voltage Regulator With Power-Good	TPS7A2501DRV	Texas Instruments	WSON

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
U6	1		Regulators 2A, low-VIN (1.1V), low-noise, high-accuracy, ultra-low-dropout voltage regulator with power good	TPS7A8300ARGR	Texas Instruments	VQFN-20
U7, U11	2		3V to 17V, 2A/3A Low-Noise and Low-Ripple Buck Power Module with Integrated Ferrite Bead Filter Compensation	TPSM82913RDU	Texas Instruments	Module
U8	1		1A, high-PSRR, ultra-low-dropout voltage regulator with low-IQ and enable	TPS7A8001DRB	Texas Instruments	VSON-8
U9	1		4V to 18V Input, 6A Synchronous SWIFT™ Step-Down Converter with Internally Compensated Advanced Current Mode Control	TPS543620RPYR	Texas Instruments	VQFN-14
U13, U19, U21	3		1A, ultra-low noise, ultra-high PSRR, RF voltage regulator	TPS7A9401DSC	Texas Instruments	WSON-10
U14	1		Ultra low-noise JESD204B compliant clock jitter cleaner with integrated 2370 to 2630MHz VCO0	LMK04828BISQ/NOPB	Texas Instruments	WQGN
U15, U17	2		Low-Noise Positive- and Negative-Output Charge Pump With Integrated LDO	LM27762DSS	Texas Instruments	WSON-10
U16	1		Single Bus Inverting Buffer Gate	SN74AUP1G04DCK	Texas Instruments	SC70
U22, U23, U29, U32, U34	5		Single Bus Buffer Gate With 3-State Outputs	SN74AUP1G125DRL	Texas Instruments	SOT-5
U24	1		Signal Conditioning 50 ohm 2 terminal Power Splitter	PS1608GT2-R50-T1	Susumu	-
U25	1		High Frequency SYSREF Buffer/Multiplier/Divider	LMX1204RHAT	Texas Instruments	SOT-23
U26, U30, U35	3		Translation - Voltage Levels 4-bit dual-supply bus transceiver with 3-state outputs and independent direction control inputs	SN74AVC4T774RSV	Texas Instruments	UQFN-16
U27	1		5V low-leakage-current, 2: 1, 2-channel precision analog switch	TMUX1136DQA	Texas Instruments	USON-10
U28, U31, U36	3		Low-Voltage 4-Bit 1-of-2 FET Multiplexer/ Demultiplexe	SN74CBTLV3257RSV	Texas Instruments	UQFN

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
U33	1		Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation And 3-State Outputs	SN74AVC2T45YZPR	Texas Instruments	DSBGA-8
U37	1		Push-pull, supply voltage supervisor with manual reset	TPS3125J18DBV	Texas Instruments	SOT-23
U38	1		EEPROM 64K 8KX8 1.8V SER EE IND 1/4AWP RPO	24LC64FT-I/MNY	Microchip	TDFN-8
U39	1		3V to 17V, 2A Low Noise and Low Ripple Buck Converter Module with Integrated Ferrite Bead Filter Compensation	TPSM82912RDUR	Texas Instruments	B0QFN28
U40	1		2A High-Accuracy Low-Noise Low-Dropout (LDO) Voltage Regulator, DSK0010A (WSON-10)	TPS7A9201DSKR	Texas Instruments	DSK0010A
U41, U42	1		Very high performance, differential-to-single-ended (D2S) amplifier optimized for radio-frequency (RF) applications.	TRF1108RPVR	Texas Instruments	WQFN-FCRLF12
C64, C75, C76, C83, C130, C134, C135, C136, C139, C239, C245, C248, C250	0	0.1 uF	Broadband Capacitors	0201BB104KW160	Passive Plus	0201
C267, C271	0		02013J0R5PBSTR\500	02013J0R5PBSTR\500	AVX Interconnect / Elco	
C280, C282	0		02013J0R5PBSTR\500		AVX Interconnect / Elco	
C281	0		02015J0R8PBSTR	02015J0R8PBSTR	AVX Interconnect / Elco	
F1	0		FUSE BOARD MOUNT 2.5A 32VDC 1206	SF-1206FP250-2	Bourns Inc.	1206
FC11, FC14	0	27uF	Feed through capacitor 27uF	NFM31PC276B0J3L	Murata	1206
L8, L9	0		Film type RF Inductor 2nH ±0.05nH 600mA 0.12Ω 0201 (0603). LQP03HQ2N0W02D	LQP03HQ2N0W02D		
R4, R28, R39, R51, R58, R89, R97, R106, R181, R210	0	4.7kΩ	RES SMD 4.7K OHM 5% 1/10W 0402	ERJ-2GEJ472X	Panasonic Electronic Components	0402
R7	0	0Ω	RES 0 OHM JUMPER 1206 SMD	RCA12060000ZSEA	Vishay Dale	1206
R16	0	100kΩ	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	Panasonic Electronic Components	0402

Table 3-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer	Package Reference
R21, R22, R23, R26, R124, R146, R157, R159, R168, R218, R219, R220, R221	0	0Ω	RES SMD 0 OHM JUMPER 1/20W 0201	ERJ-1GN0R00C	Panasonic Electronic Components	0201
R43, R103, R171, R174	0	0Ω	RES SMD 0 OHM JUMPER 1/10W 0402	ERJ-2GE0R00X	Panasonic Electronic Components	0402
R66, R71, R129, R130, R131, R132, R138, R139, R140, R141	0	49.9Ω	RES SMD 49.9 OHM 1% 1/20W 0201	ERJ-1GNF49R9C	Panasonic Electronic Components	0201
R117, R118	0	66.5Ω	RES SMD 66.5 OHM 1% 1/20W 0201	ERJ-1GNF66R5C	Panasonic Electronic Components	0201
R122	0	100Ω	RES SMD 100 OHM 1% 1/20W 0201	ERJ-1GNF1000C	Panasonic Electronic Components	0201
R127, R135	0	82.5Ω	RES SMD 82.5 OHM 1% 1/20W 0201	ERJ-1GNF82R5C	Panasonic Electronic Components	0201
R134, R137	0	130Ω	RES SMD 130 OHM 1% 1/20W 0201	ERJ-1GNF1300C	Panasonic Electronic Components	0201

4 Additional Information

4.1 Trademarks

SWIFT™ is a trademark of Texas Instruments.

USB Type-C® and USB-C® are registered trademarks of USB Implementers Forum.

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Rohde & Schwarz® is a registered trademark of Rohde & Schwarz GmbH & Co.

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5 References

This section provides references to technical documents and user's guides.

5.1 Technical Reference Documents

- Texas Instruments, [DAC39RF10, DAC39RFS10 10.24, 20.48-GSPS, 16-bit, Dual and Single Channel, Multi-Nyquist Digital-to-Analog Converter \(DAC\) with JESD204B, C Interface](#), data sheet
- Texas Instruments, [TRF1108 DC to 12GHz Bandwidth, Differential to Single-Ended RF Amplifier](#), data sheet
- Texas Instruments, [TSW14J59EVM JESD204C Data Capture and Pattern Generator Card](#), user's guide
- Texas Instruments, [High-Speed Data Converter Pro GUI](#), user's guide (also available in the software help menu)
- Texas Instruments, [LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs](#), data sheet
- Texas Instruments, [LMX1204 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider](#), data sheet
- FTDI Chip, [FTDI USB to Serial Driver Installation Manual](#)

5.2 TSW14J59EVM Operation

For configuration and status information, refer to the [High-Speed Data Converter Pro GUI User's Guide](#).

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2024) to Revision A (January 2025)	Page
• Added a hot surface caution note.....	2

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
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WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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- 4 *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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