

# EVM User's Guide: DAC39RF12EVM

## DAC39RF12EVM Evaluation Module



### Description

The DAC39RF12EVM is an evaluation board for evaluating the DAC39RF10/DAC39RF12 family of digital-to-analog converters (DAC) from Texas Instruments. The DAC39RF10/DAC39RF12 is a family of single and dual channel DACs with 16-bit resolution. The devices can be used in non-interpolation modes (real) as well as interpolation modes (complex IQ). The maximum input rate is 24GSPS in a dual edge sampling mode with 8 bits of DAC resolution. 12GSPS real data is also supported with a single channel DAC. This evaluation board also includes the following features.

### Features

- Two balun-coupled output networks per DAC output allowing singled ended signal evaluation.
- A 3MHz to 6GHz low band balun for 1<sup>st</sup> Nyquist evaluation.
- A 1.8GHz to 18GHz high band balun for 2<sup>nd</sup>/3<sup>rd</sup> Nyquist evaluation.
- A LMK04828 clock distribution chip for distributing FPGA reference clocks as well as SYSREF for subclass 1 operation.
- A balun-coupled clock input network to test the DAC performance with an external low-noise clock source.
- An FMC+ with High-speed serial data connections for full JESD204C testing of all 16 lanes.
- A USB to serial chip to allow programming of the DAC/LMK with a simple USB connection.
- The ability to program the DAC/LMK from an FPGA using the FMC+ connector.<sup>1</sup>
- Device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FPGA using SPI through FMC+ connector

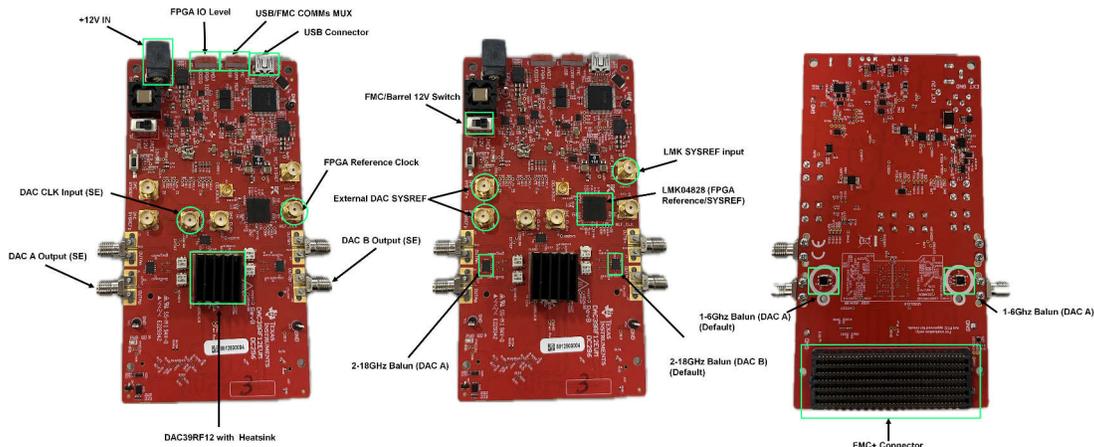


Figure 1-1. DAC39RF12EVM Key Components

The DAC39RF12EVM is paired with the TSW14J59EVM data capture and pattern generator card.<sup>2</sup>

<sup>1</sup> To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in [Section 2.3](#).

<sup>2</sup> If the DAC39RF12EVM is only used in DDS mode, then data capture EVM is not required.

# 1 Evaluation Module Overview

## 1.1 Introduction

The following user guide gives an in depth overview on using the DAC39RF12EVM evaluation board hardware as well as the software GUIs that are associated with the EVM to change, configure and evaluate the DAC in the various modes and features.

## 1.2 Kit Contents (Required Equipment)

The following equipment and documents are included in the DAC39RF12EVM kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

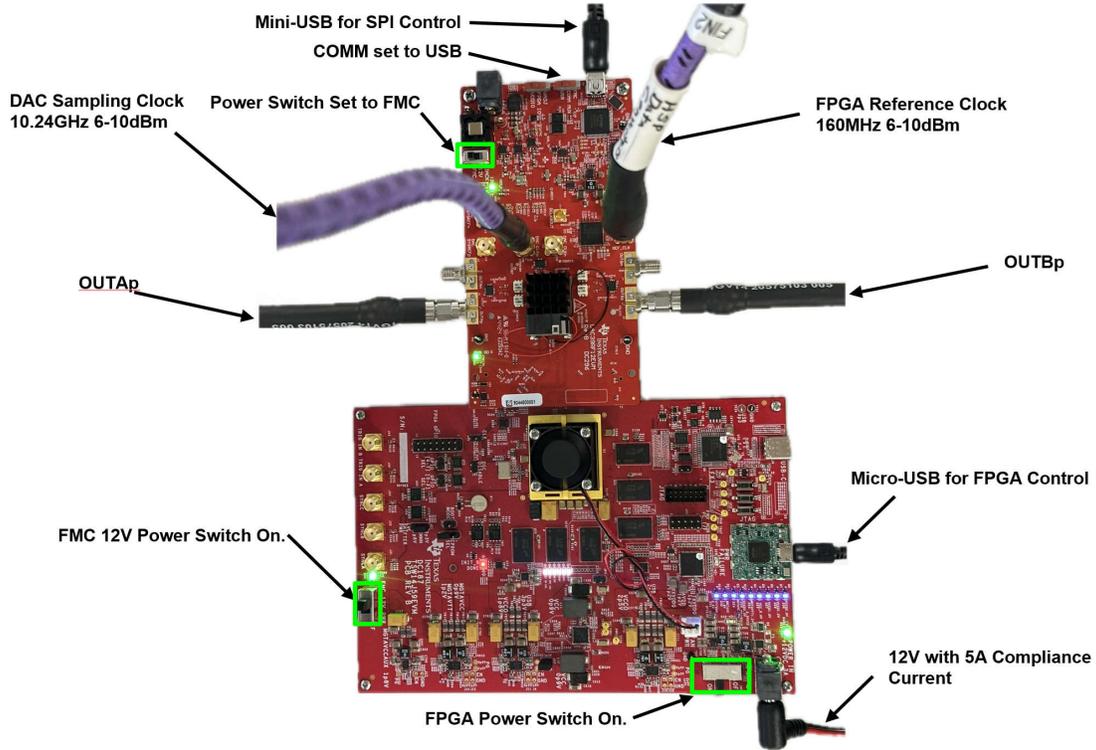
The following equipments are **not** included in the DAC39RF12EVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- PC computer running Microsoft® Windows® 10 or higher
- Low phase-noise signal generator for DEVCLK (Sampling clock).
- Additional signal generator for FPGA reference clock generation.
  - Both signal generators need to be 10MHz reference locked.
- Two low noise power supplies: 12V/5V (TSW14J59EVM) and 12V/3A (DAC39RF12EVM)
- Three SMA type low loss cables

## 2 Hardware

### 2.1 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.



**Figure 2-1. DAC39RF12EVM Test Setup**

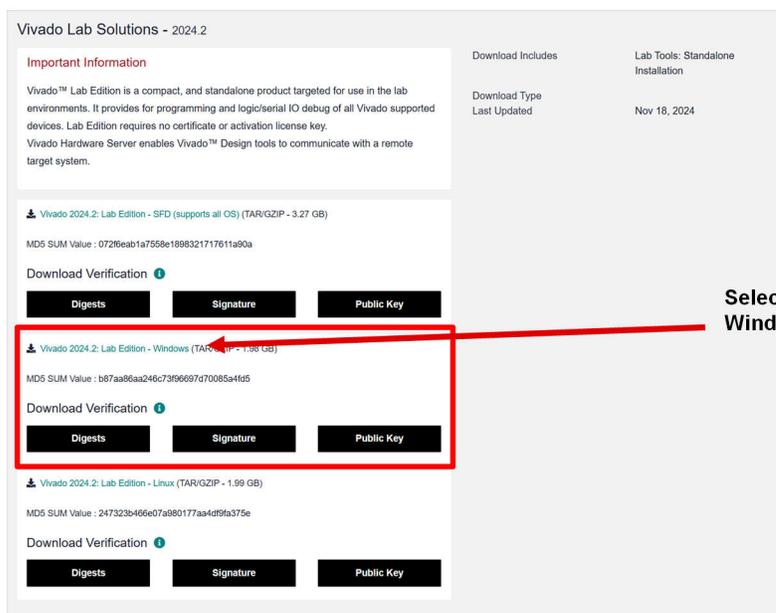
### 2.1.1 Installing the DAC39RF12EVM Configuration GUI Software

1. Download the DAC39RF12EVM Configuration GUI software from the EVM tool folder at [DAC39RF12EVM GUI](#).
  - a. NOTE: The GUI download includes the following:
    - i. DAC39RF12 EVM GUI
    - ii. J59 Commander
      1. DAC WaveGen
    - iii. J59 Server
2. Run the executable file (DAC39RF12EVM\_SW\_Package\_v3.1.2.exe).
3. Install Vivado Lab Tools: <https://www.xilinx.com/support/download.html>
  - a. Follow the next section for instructions on how to install the Xilinx tools and add environment variables path to the desktop PC.

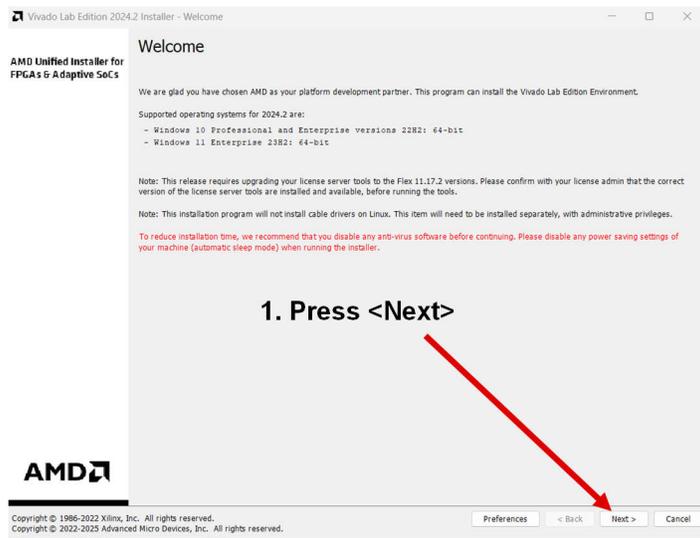
#### 2.1.1.1 Installing & Setting Up Vivado Lab Tools

For the DAC39RF12EVM, Vivado Lab Tools will need to be installed. Please follow the steps outlined in this section.

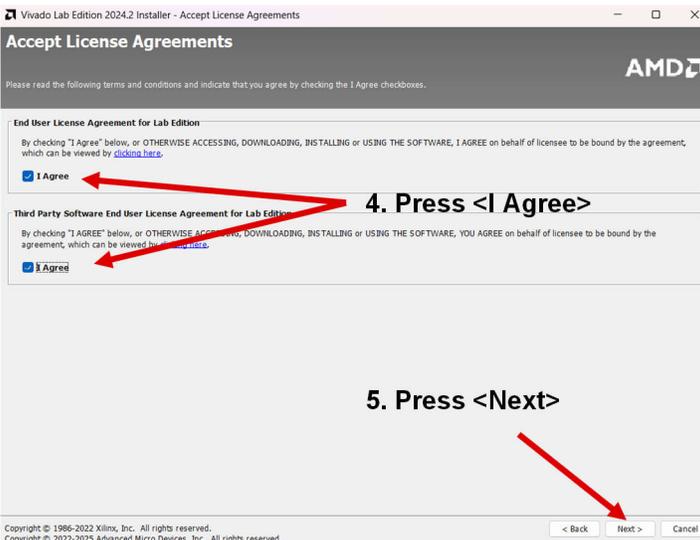
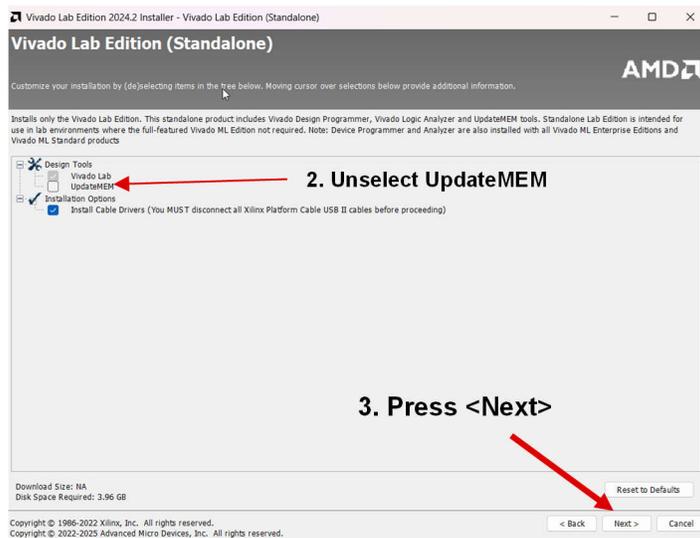
1. Create a User account for AMD and sign in.
  - a. Fill out the appropriate information before downloading.
  - b. When complete, press the download button.
2. The download file type will be a .tar file. In Windows you can open the .tar file and explore it.
3. Next, look inside the Vivado\_Lab\_Win\_2024.2\_1113\_1001 folder for <xsetup.exe>
  - a. Right click and execute it, windows will ask you to “Extract All”.
4. Once the files are extracted, open the folder and find “xsetup.exe”.
  - a. Right click on this file and install it. Windows may ask for permissions.
5. Follow the sequence of steps in the figures outlined below in order to finish the Xilinx Lab Tools installation.

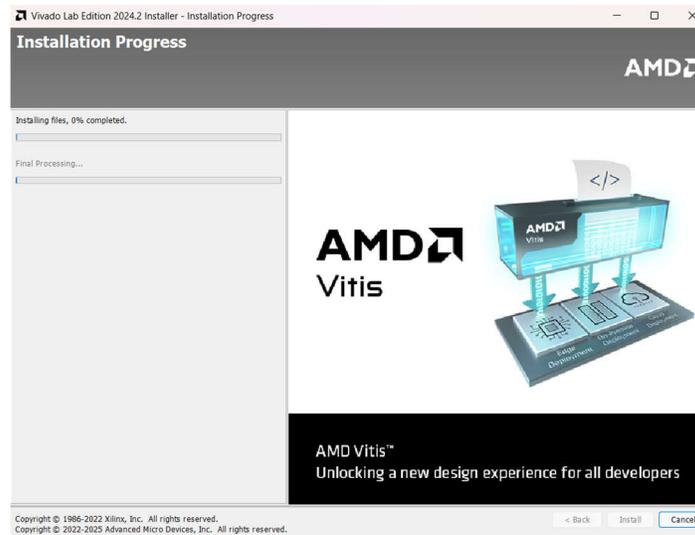
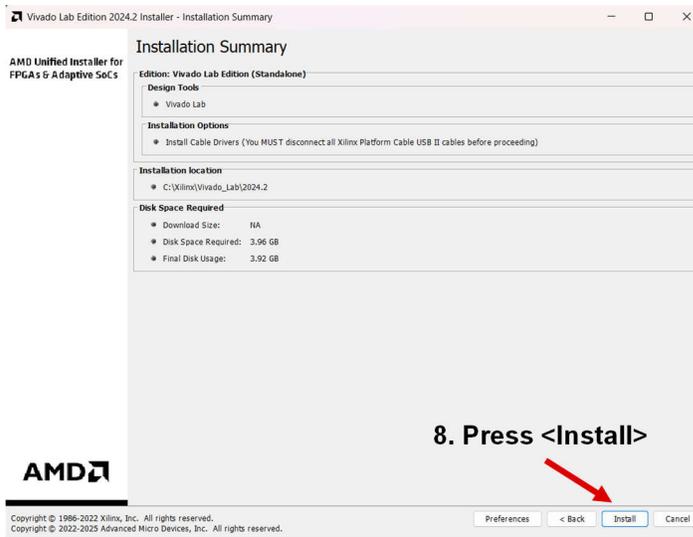
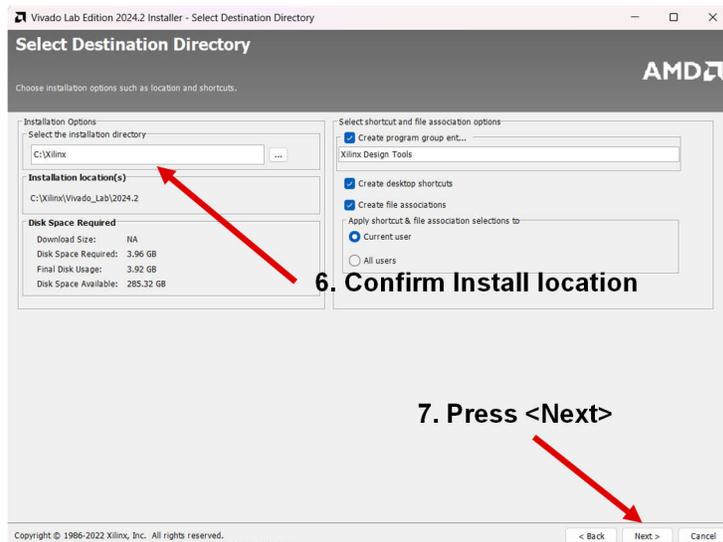


Select Vivado 2024.2 Lab Edition Windows (TAR/GZIP)



**Figure 2-2. Installing Vivado Lab Tools**





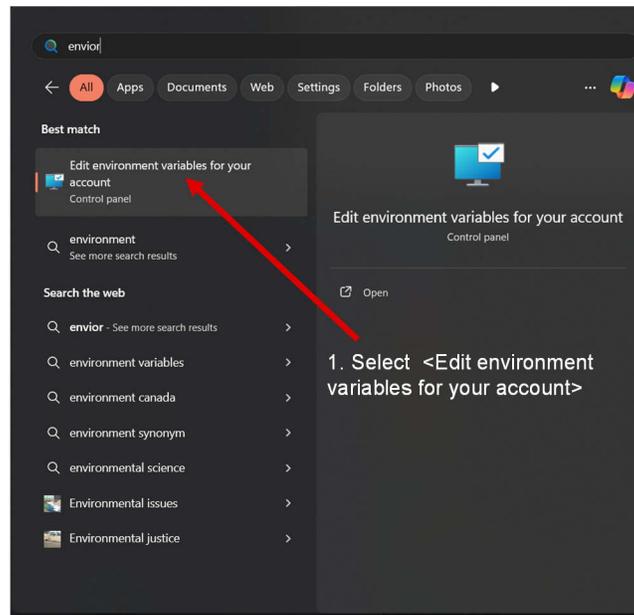
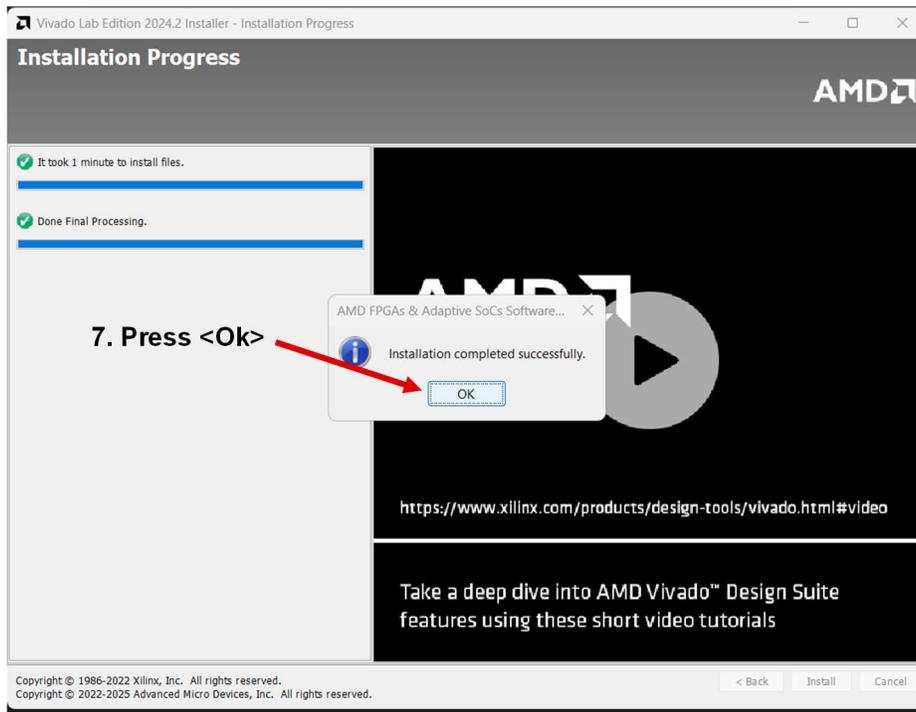
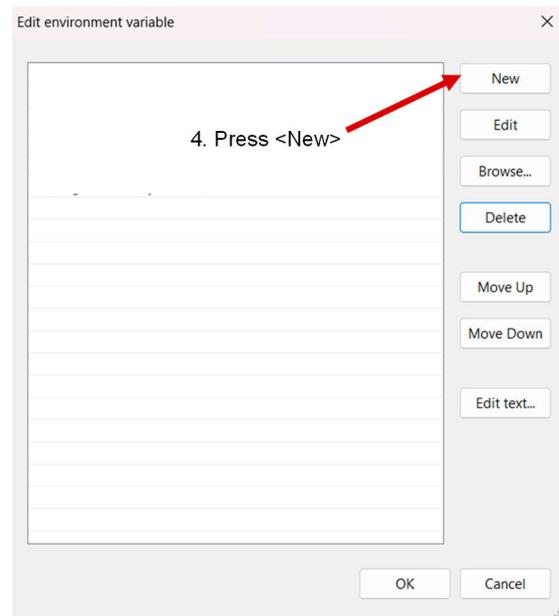
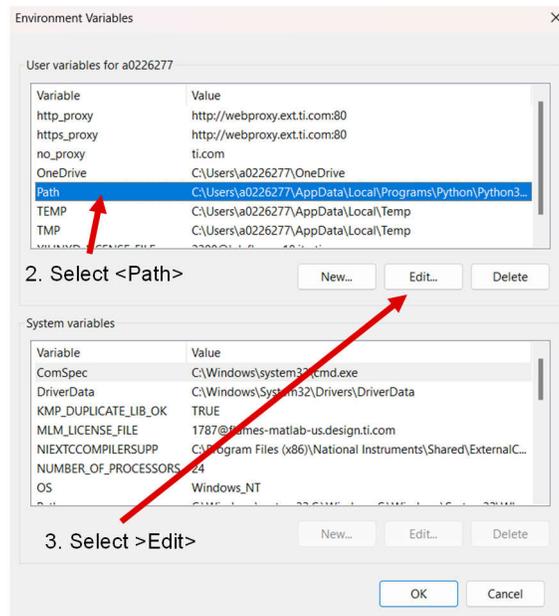
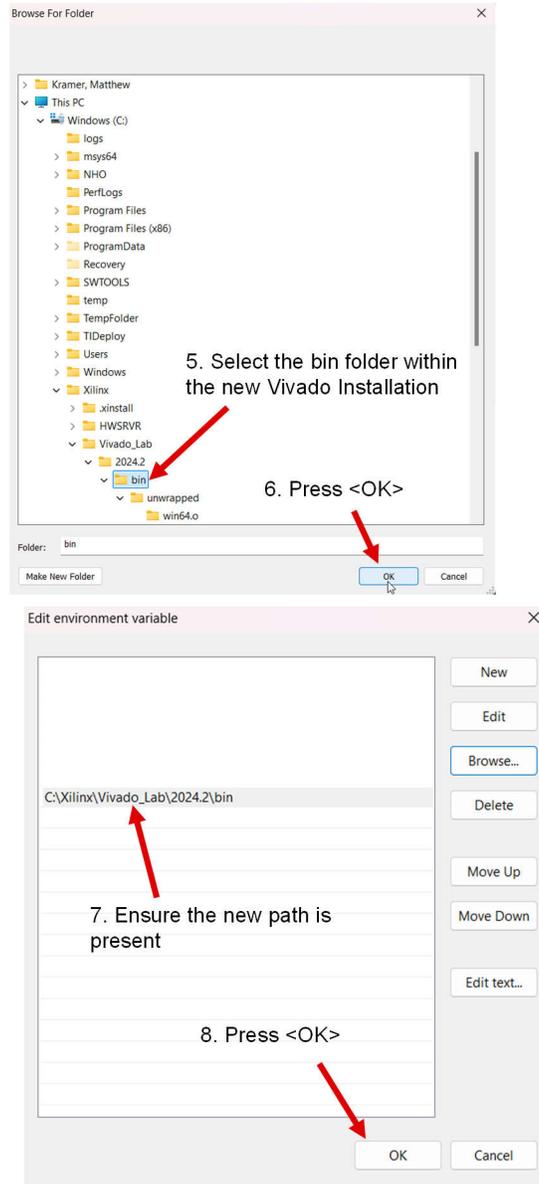


Figure 2-3. Adding Vivado Lab Tools to the Windows PATH





Once this is complete, the J59\_Server can be run.

### 2.1.2 Connect the DAC39RF12EVM and TSW14J59EVM

1. With the power off, connect the DAC39RF12EVM to the TSW14J59EVM through the FMC+ connector as shown in [DAC39RF12EVM Test Setup](#).

### 2.1.3 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12V DC (minimum 5A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the TSW14J59EVM power connector.
2. DAC39RF12EVM can be powered with 12V DC (minimum 3A) though the connector jack(J5) on the DAC39RF12EVM, or the EVM can be powered from the TSW14J59EVM via FMC+ connector. There is a switch (SW1) which can be used to select power from the barrel jack on the DAC EVM, or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the DAC39RF12EVM power supply is set to the opposite position (Jack) from which it should be drawing power. If using barrel jack option, connect the power cable to a 12V DC (minimum 3A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector. [Table 2-1](#) is used as a reference to power the DAC EVM.

**Table 2-1. Powering the DAC39RF12EVM**

DAC39RF12 Powered from	DAC39RF12 Power Switch position	TSW14J59EVM FMC switch position	Power supply needed
TSW14J59EVM via FMC+ connector	FMC	ON	12V 5A for TSW14J59EVM
External Supply with jack on DAC39RF12EVM	JACK	OFF	12V 3A for TSW14J59 and 12V 3A for DAC39RF12EVM

**CAUTION**

Make sure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage. Leave the power switches in the off position until directed later.

### 2.1.4 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the Aoutp (J1) SMA connector of the DAC39RF12EVM .

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#### Note

1. The FPGA REF clock frequency can be obtained from the DAC39RF12EVM GUI once the DAC39RF12EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown in [Figure 1-1](#).
  2. Make sure that the DEVCLK and Reference clock sources are frequency-locked using a common 10MHz reference to for functionality.
  3. Do not turn on the RF output of any signal generator at this time.
  4. In all of these examples the FPGA REF clock = 160MHz, the DAC sampling clock = 10.24GHz.
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### 2.1.5 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a Micro USB cable from the PC to the TSW14J59EVM.

### 2.1.6 Turn On the DAC39RF12EVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on the TSW14J59EVM must be set to the on position, and power switch on the DAC39RF12EVM must be set to FMC(default). If external power supply is used to power the DAC EVM. Then turn on the 12V power supply connected to the barrel jack on the DAC EVM and set the power switch position on DAC39RF12EVM to JACK position.  
The green Power Good LED(D5) on DAC EVM should turn on, indicating DAC EVM is getting power.
2. Connect the DAC EVM to the PC with the mini-USB cable to the EVM.

### 2.1.7 Turn On the Signal Generators

1. Turn on the output of the low phase noise RF signal generator and connect to DAC CLKp (J6) via the SMA cable. Set the signal generator to 10.24GHz at a +6dBm output level.
2. Turn on the output of the RF signal generator and connect to REF\_CLK (J8) via the SMA cable.
3. Set the signal generator to 160MHz at a +6dBm output level. Using another SMA cable, connect it to OUTAp (J1), the output of the DAC to a spectrum analyzer.

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#### Note

The max clock rate supported by DAC39RF12EVM is 12GHz

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### 2.1.8 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 0

Configuration example of DAC39RF12EVM in JMODE 0

1. JMODE 0 is considered bypass mode or real data mode, interpolate x1.
  - a. Configuration details:
    - i. 10.24GSPS
    - ii. 10.3125Gbps SERDES rate
    - iii. 16 lanes
    - iv. JESD\_M = 1
    - v. CHA & CHB outputs are equal
2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

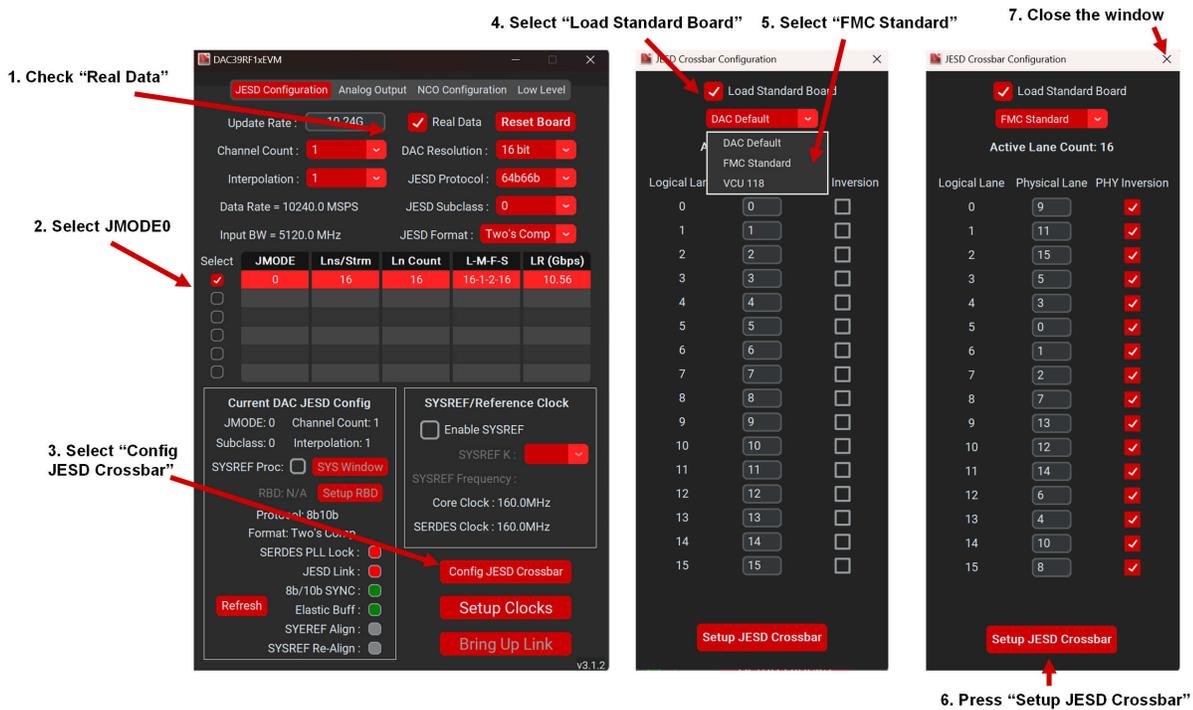


Figure 2-4. DAC39RF12EVM GUI Configuration, Part 1

1. Then launch/bring up the J59\_Server.exe. As shown in the figure.
2. Next, launch/bring up J59\_Commander. Set the interpolation to 1, then open the DAC Wavegen GUI.

Update Interpolation to 1

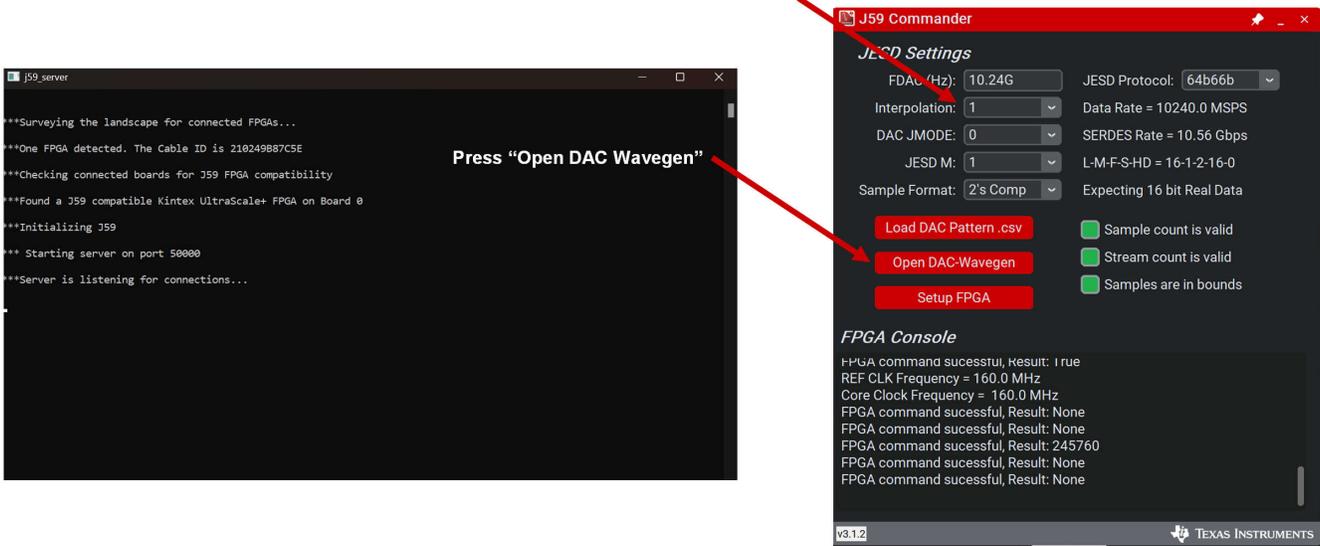


Figure 2-5. J59 Server.exe and J59 Commander, Step 2

1. In the DAC Wavegen GUI, setup the details as noted in figure Figure 2-6.

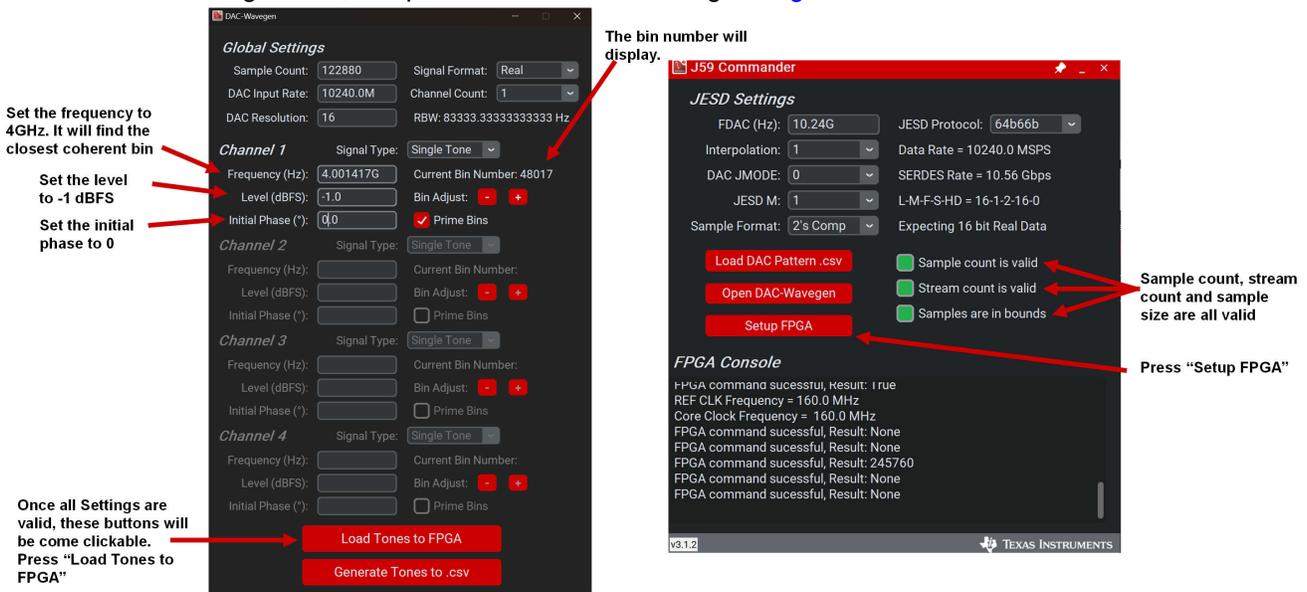


Figure 2-6. DAC Wavegen GUI & J59 Commander setup details, Step 3

2. Once the FPGA is setup, there should be the following output on the spectrum analyzer. Figure Figure 2-8.

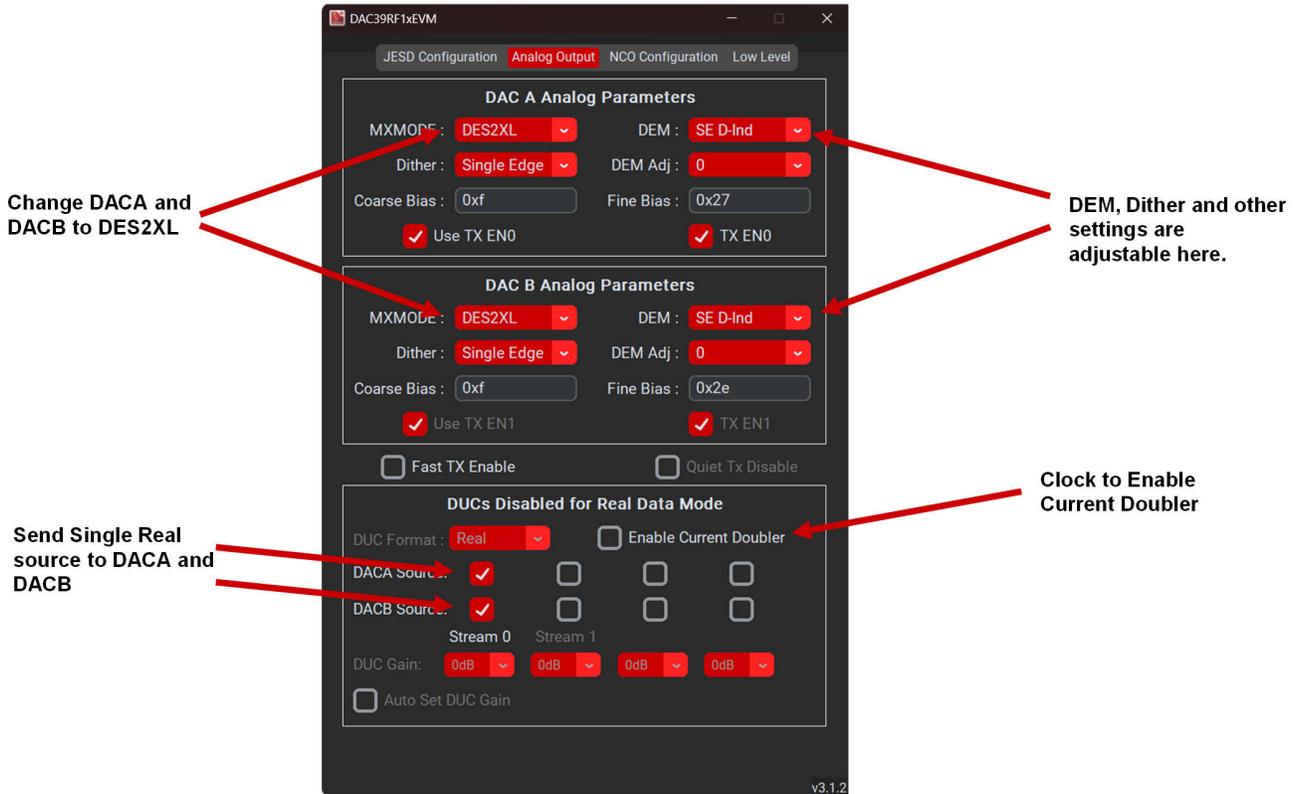


Figure 2-7. DAC39RF12EVM GUI Configuration Steps, Step 4

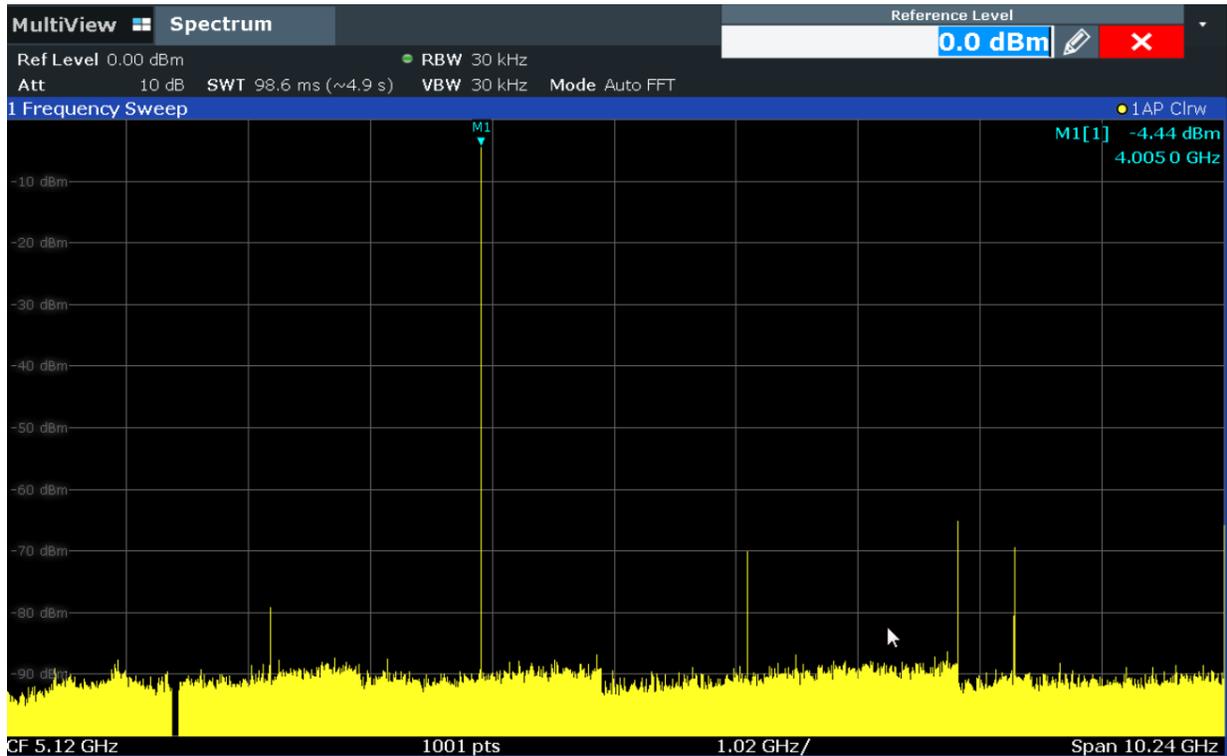


Figure 2-8. DAC39RF12EVM, CHA Output Spectrum in JMODE 0, DES2XL Mode

### 2.1.9 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 1

Configuration example of DAC39RF12EVM in JMODE 1

1. JMODE 1: complex data, interpolate x2.
  - a. Configuration details:
    - i. 10.24GSPS
    - ii. 10.3125Gbps SERDES rate
    - iii. 16 lanes
    - iv. JESD\_M = 2
    - v. CHA & CHB outputs are equal
2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

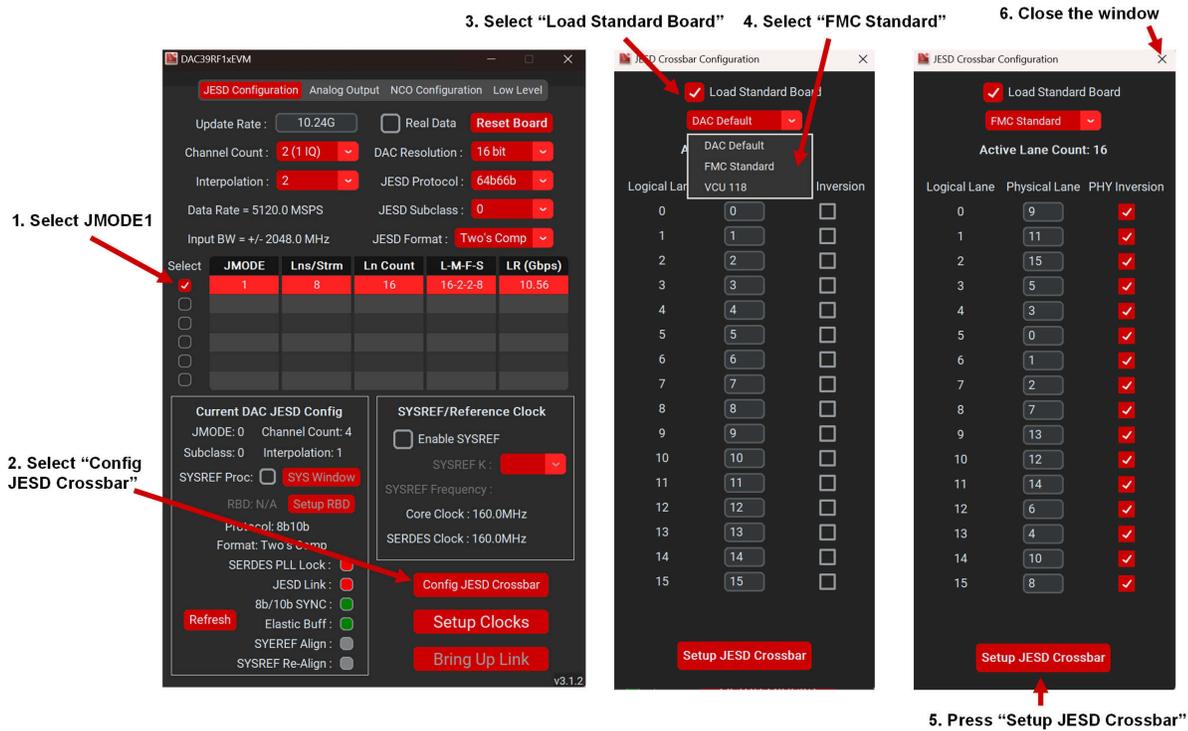
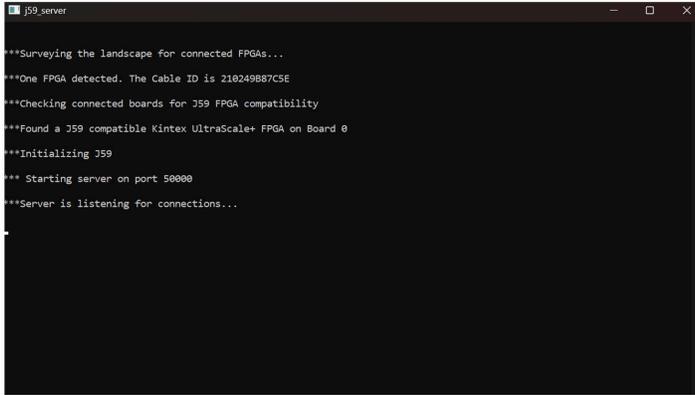
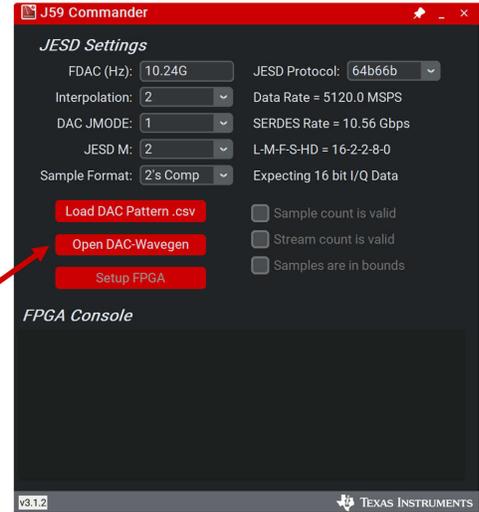


Figure 2-9. DAC39RF12EVM GUI Configuration, Step 1

1. Launch J59 Server



2. Launch J59 Commander



Press "Open DAC Wavegen"  
Then see next slide

Figure 2-10. J59 Server.exe and J59 Commander Setup, Step 2

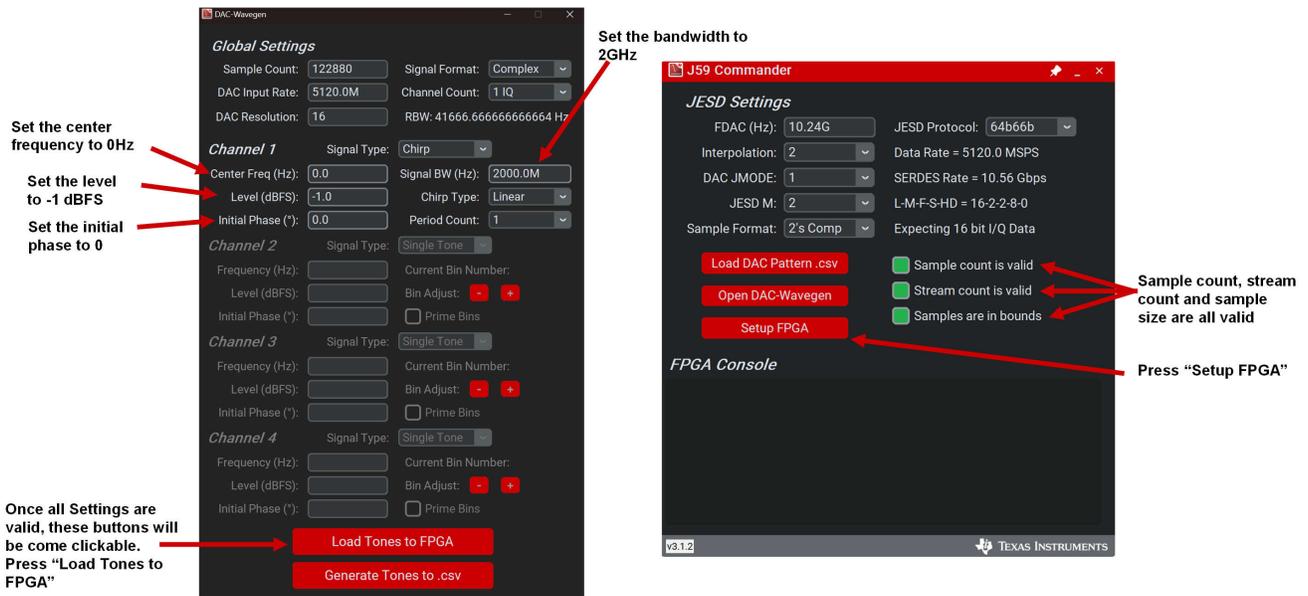


Figure 2-11. DAC Wavegen GUI & J59 Commander setup details, Step 3

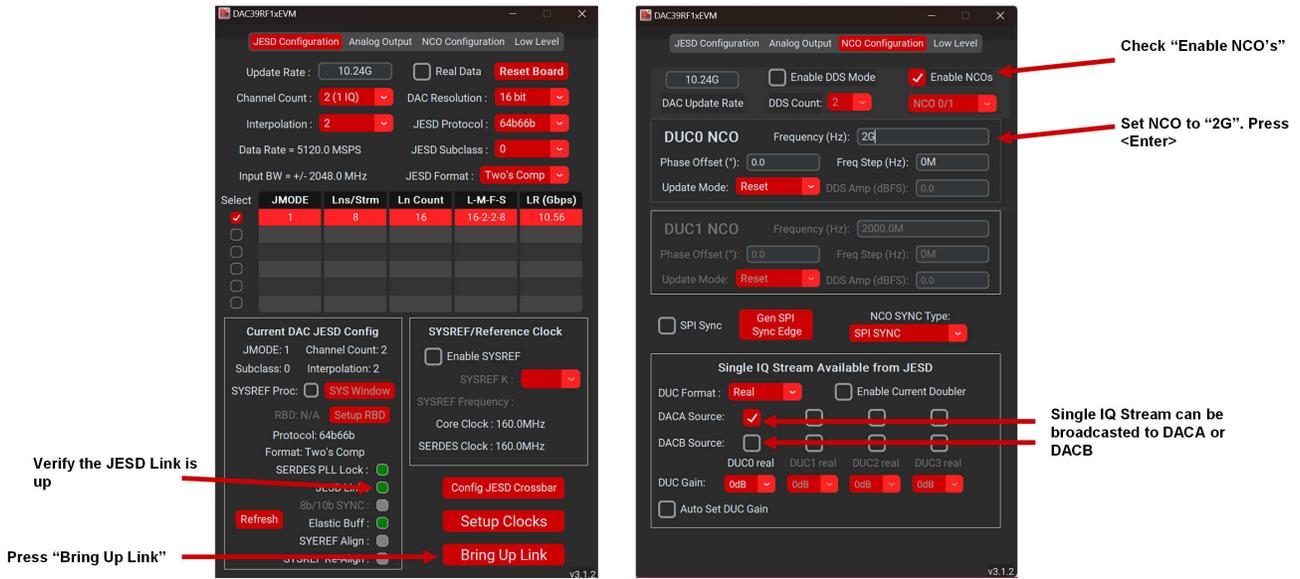


Figure 2-12. DAC39RF12EVM GUI Configuration Steps, Step 4: Moving the modulated waveform up in frequency.

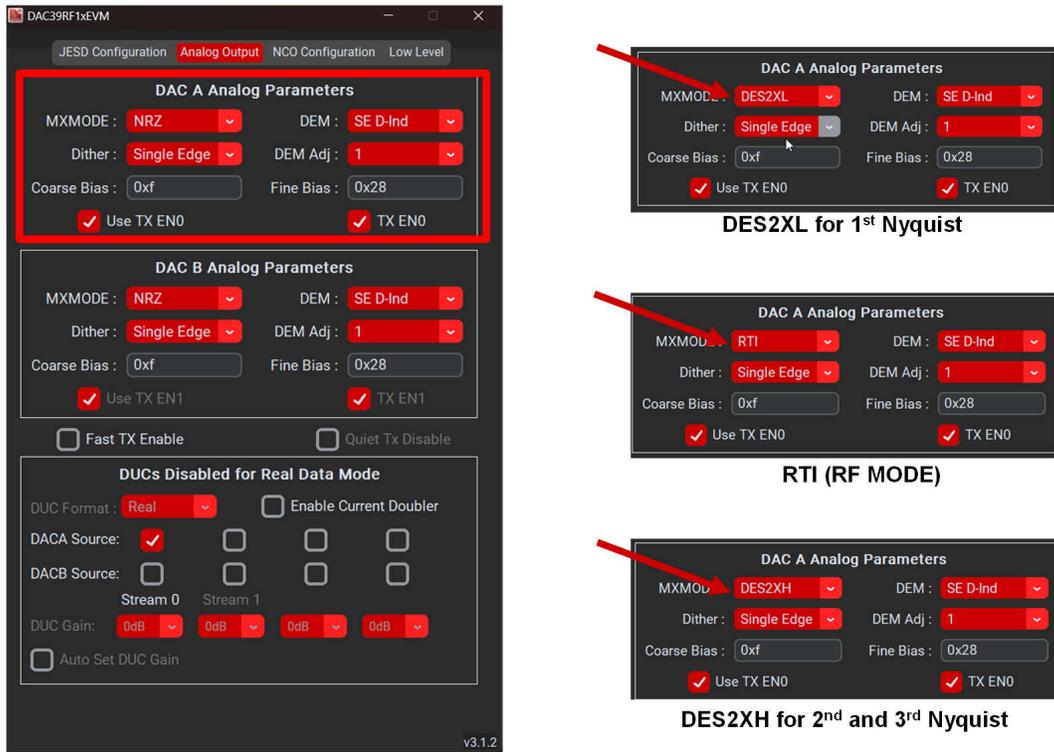
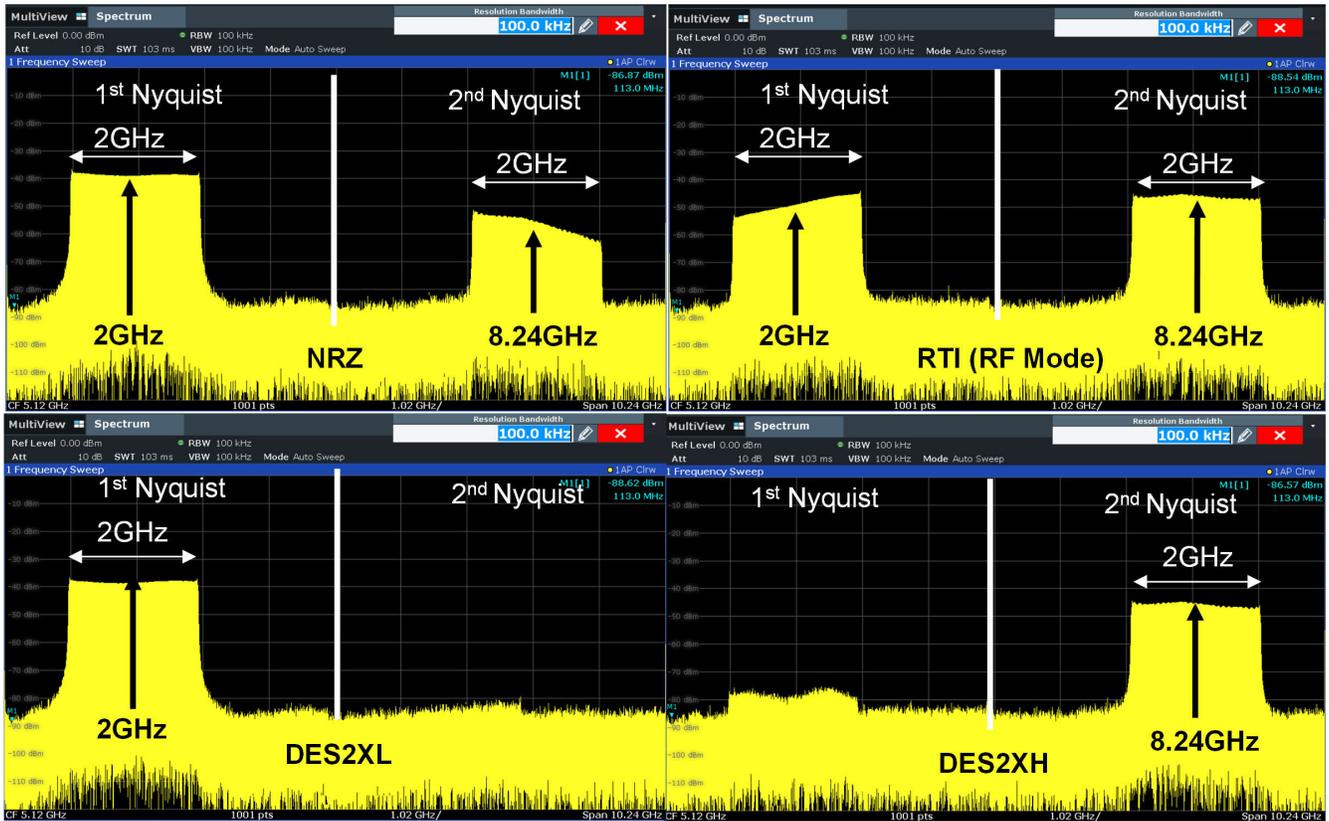


Figure 2-13. DAC39RF12EVM GUI Configuration Steps, Step 5

**Note**

The MXMODE of each DAC can be changed in real time. This can help with frequency planning.



**Figure 2-14. DAC39RF12EVM, CHA Output Spectrum in JMODE 1, showing the modulated waveform vs. The different output DAC modes.**

### 2.1.10 Launching the DAC39RF12EVM GUI and Programing the DAC EVM - JMODE 3

Configuration example of DAC39RF12EVM in JMODE 3

1. JMODE 3 is considered complex data, 4 complex streams, interpolate x8.
  - a. Configuration details:
    - i. 10.24GSPS
    - ii. 10.3125Gbps SERDES rate
    - iii. 16 lanes
    - iv. JESD\_M = 8
    - v. CHA & CHB outputs are equal
2. Simply follow the numerated steps in the subsequent figures, to launch the DAC GUI. Following the steps as shown to configure the EVM.

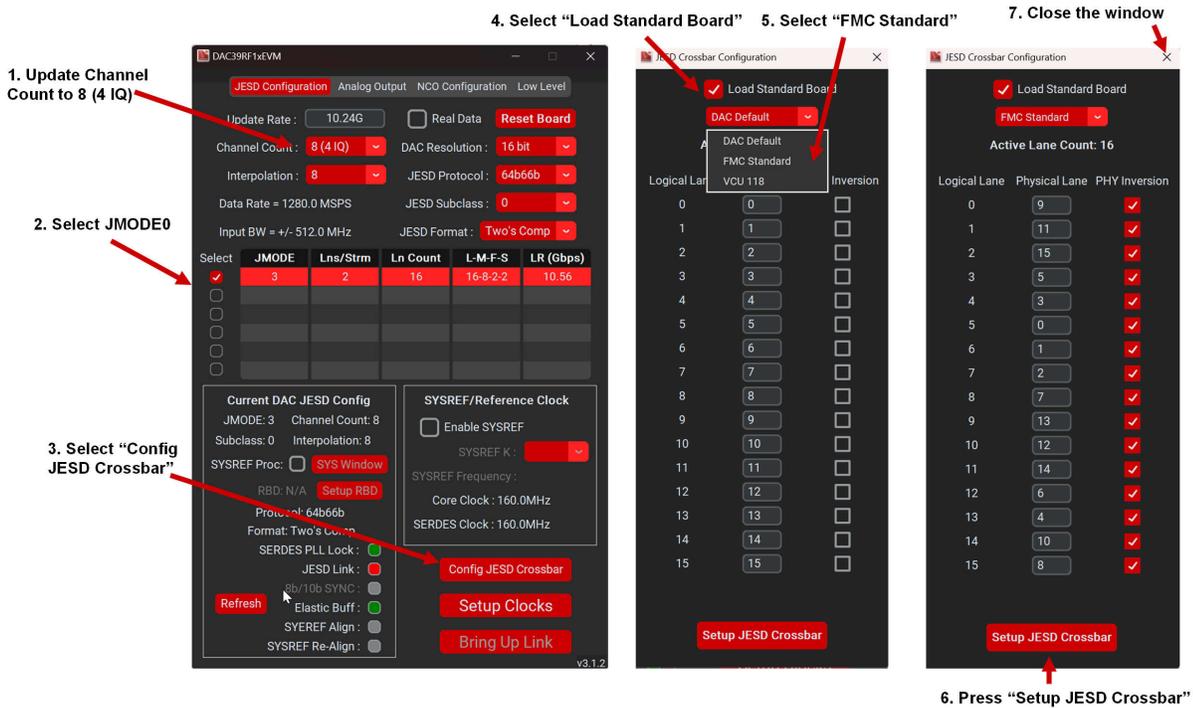


Figure 2-15. DAC39RF12EVM GUI Configuration, Step 1

Update Interpolation to 1

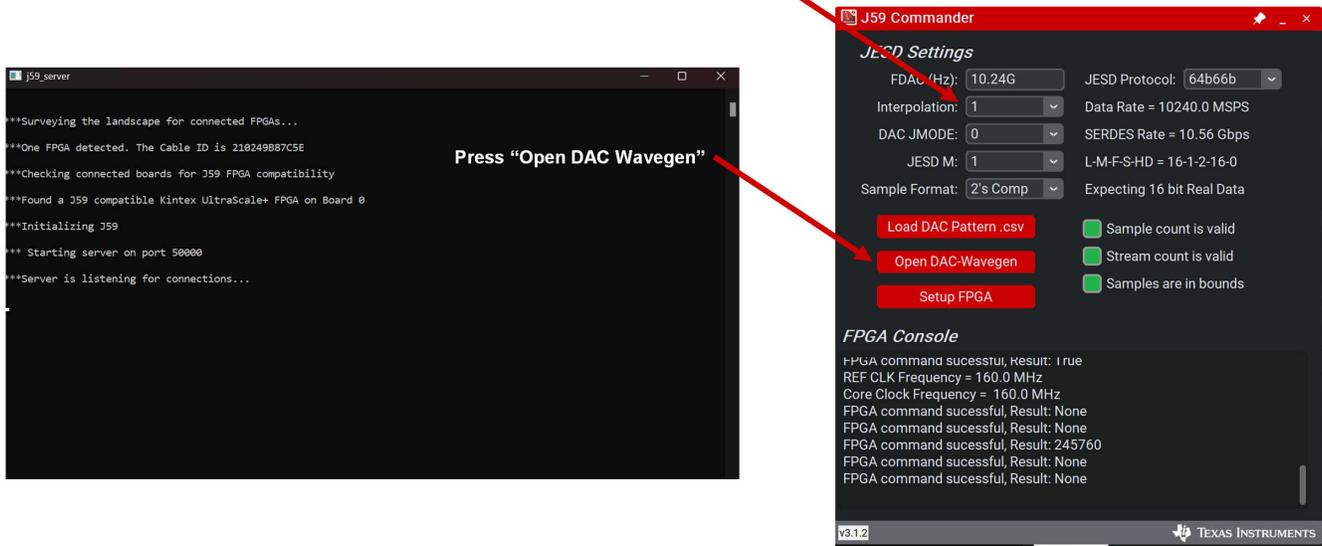


Figure 2-16. J59 Server.exe and J59 Commander Setup, Step 2

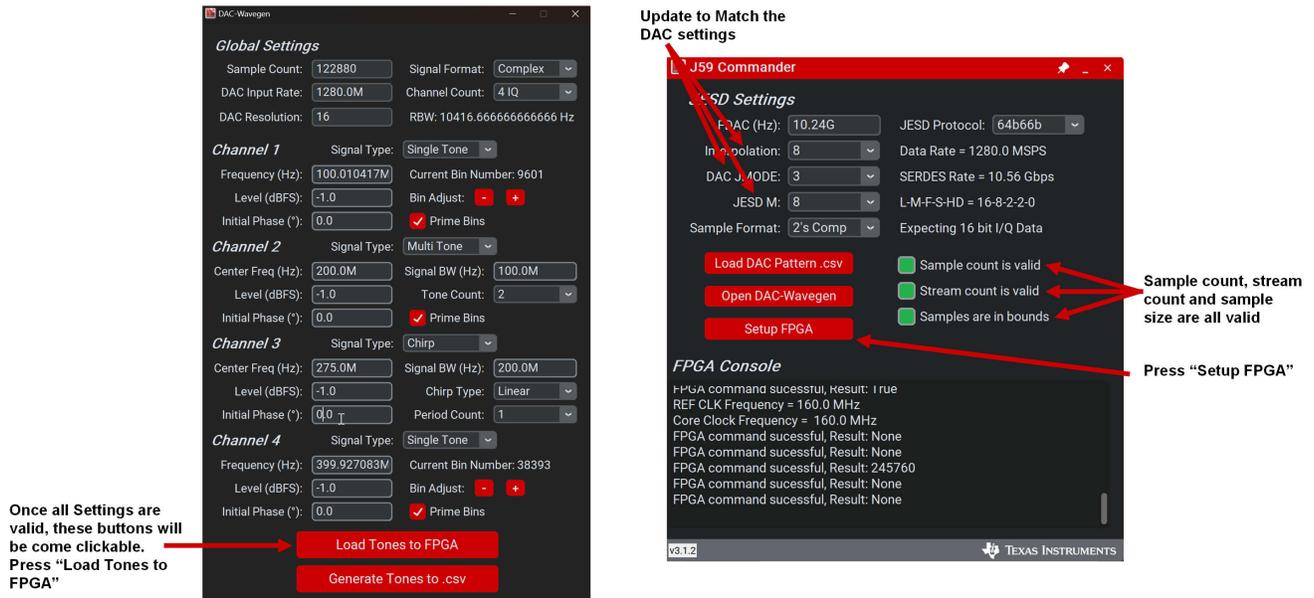


Figure 2-17. DAC Wavegen GUI & J59 Commander setup details, Step 3



Figure 2-18. DAC39RF12EVM GUI Configuration Steps, Step 4

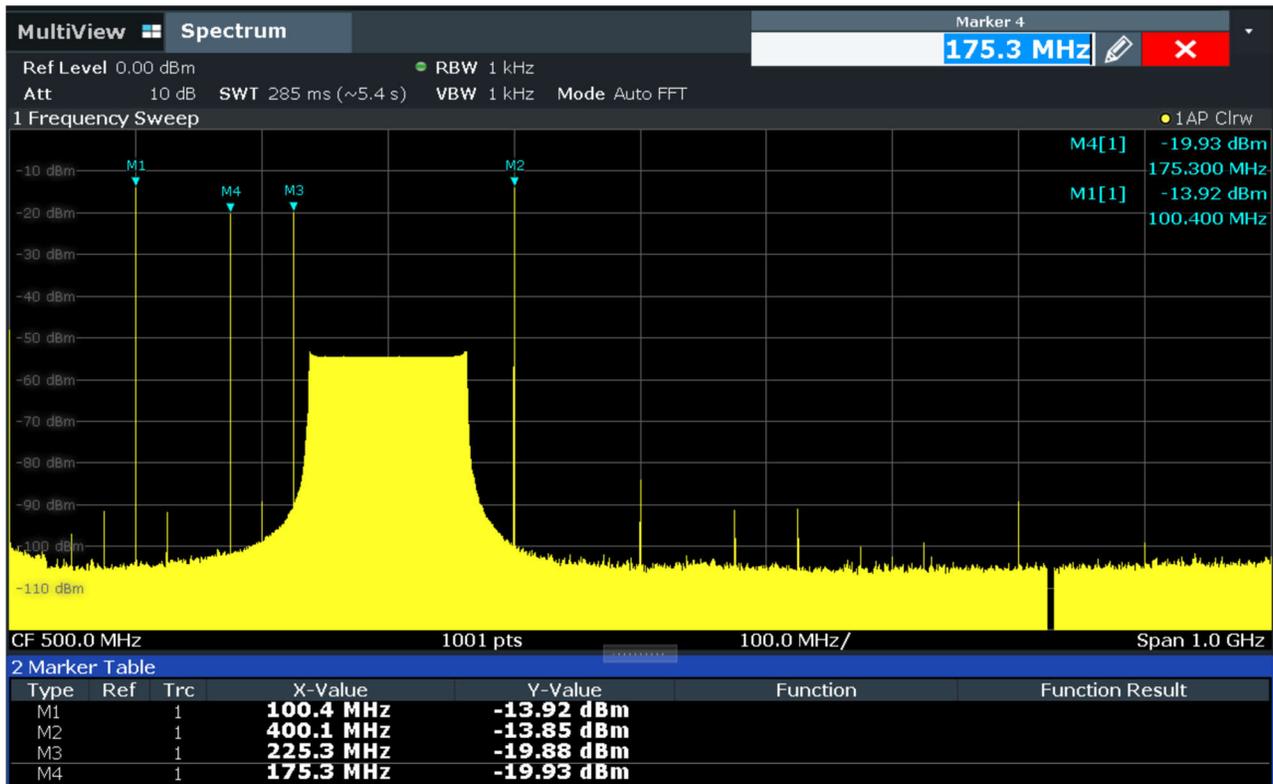


Figure 2-19. DAC39RF12EVM, CHA Output Spectrum in JMODE 3, Baseband Data

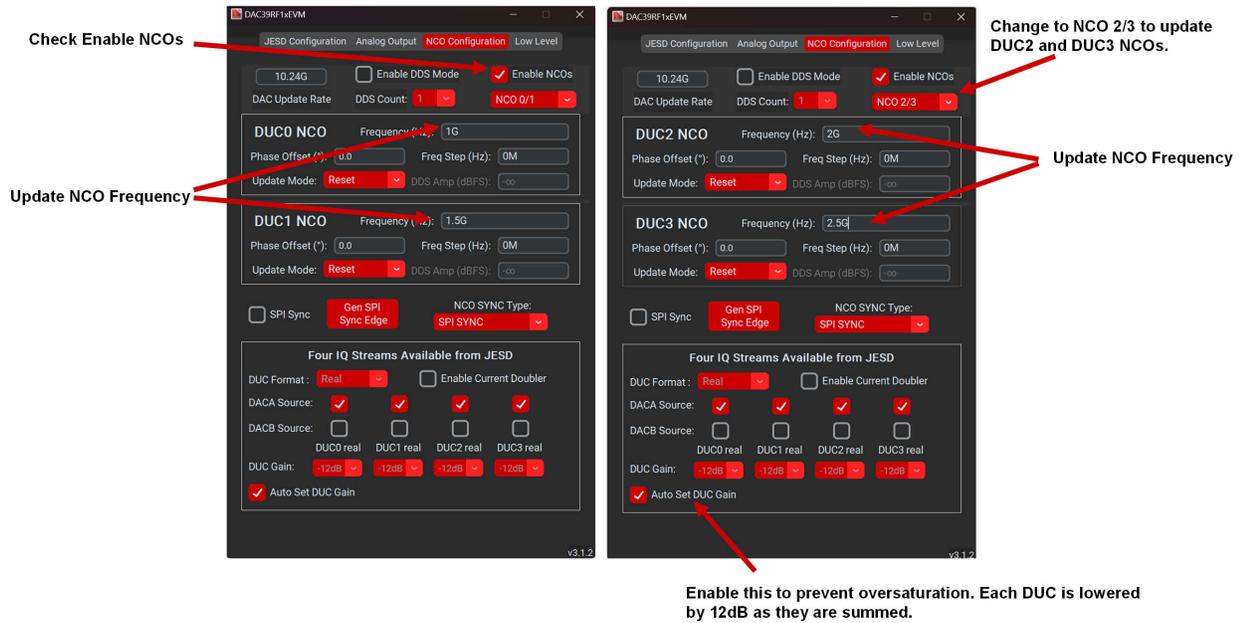


Figure 2-20. DAC39RF12EVM GUI Configuration Steps, Part 3, Enabling the NCO & Setting the frequency. Step 5

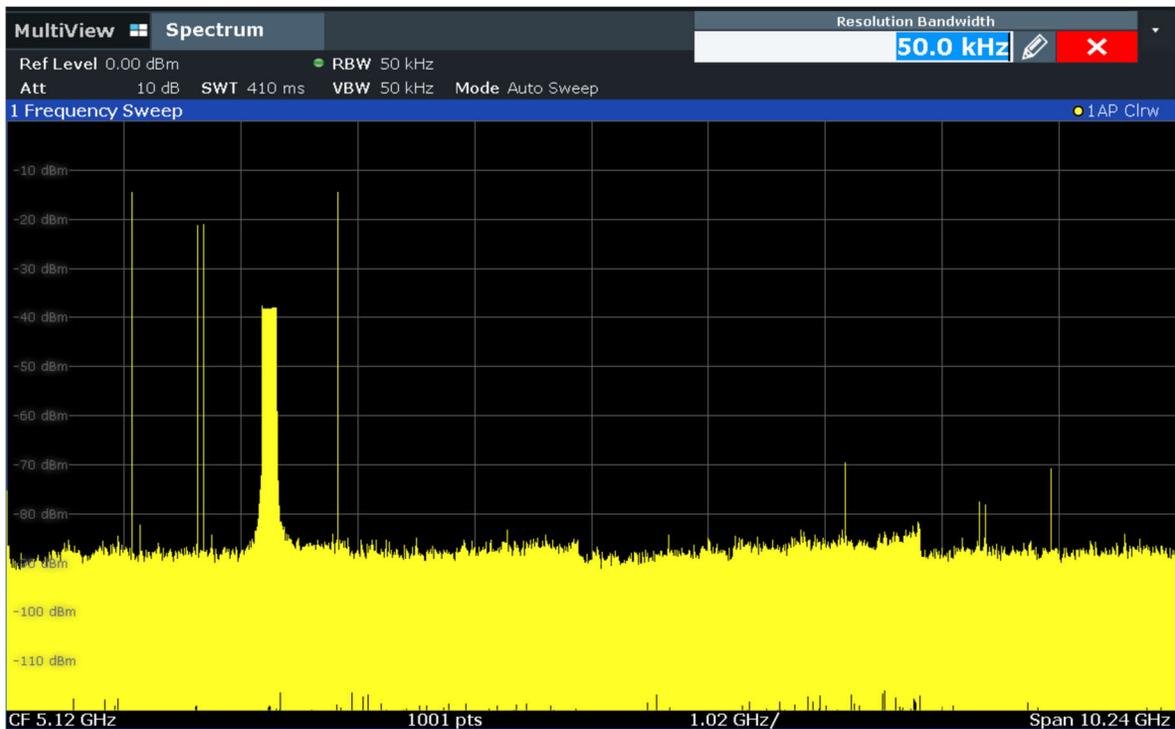


Figure 2-21. DAC39RF12EVM, CHA Output Spectrum in JMODE 3, NCO Enabled

Configuration example of DAC39RF12EVM in DDS Mode

1. Enable DDS Mode
  - a. Configuration details:
    - i. 10.24GSPS
    - ii. With DUC0 mapped to CHA & DUC1 mapped to CHB
2. Simply follow the numerated steps in the figure below after launching the DAC GUI.

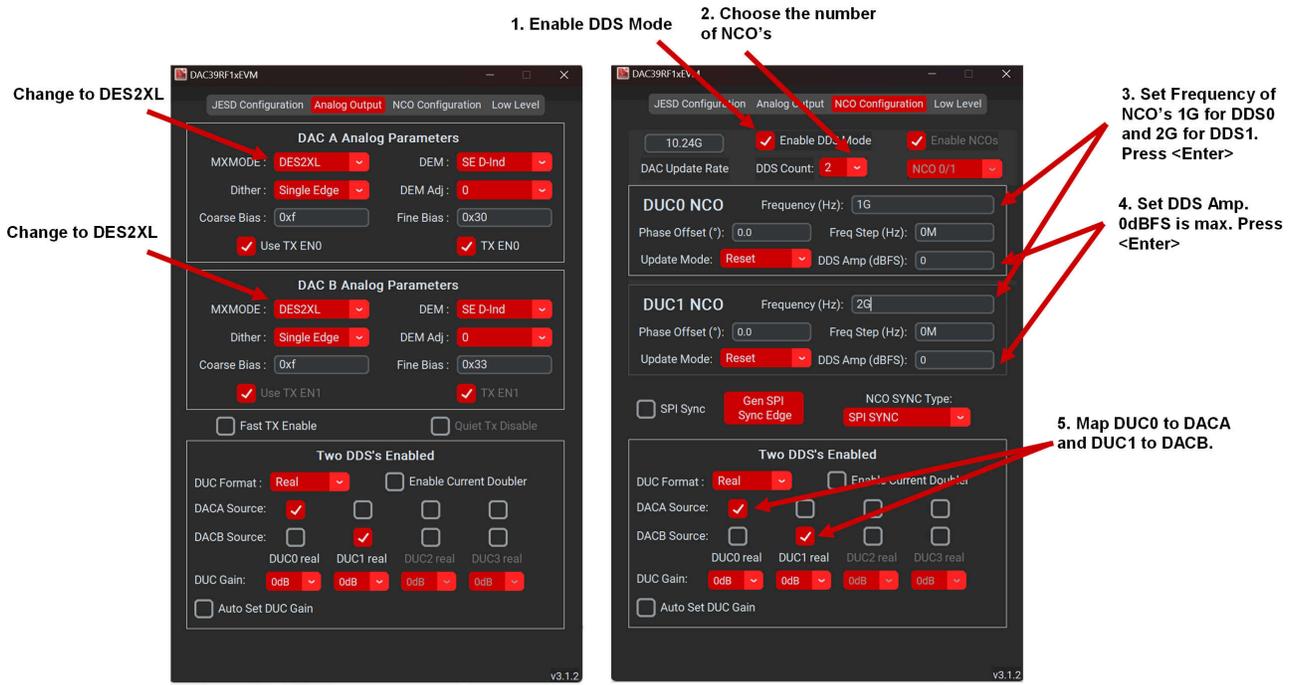


Figure 2-22. DAC39RF12EVM GUI Configuration for DDS Mode



DACA Generating a 1GHz tone in DDS mode. Note the reduced 2<sup>nd</sup> Nyquist image due to DES2XL output mode



DACB Generating a 2GHz tone in DDS mode. Note the reduced 2<sup>nd</sup> Nyquist image due to DES2XL output mode

Figure 2-23. DDS Mode Output Spectrum

## 2.2 Evaluation Board Details: Analog Outputs

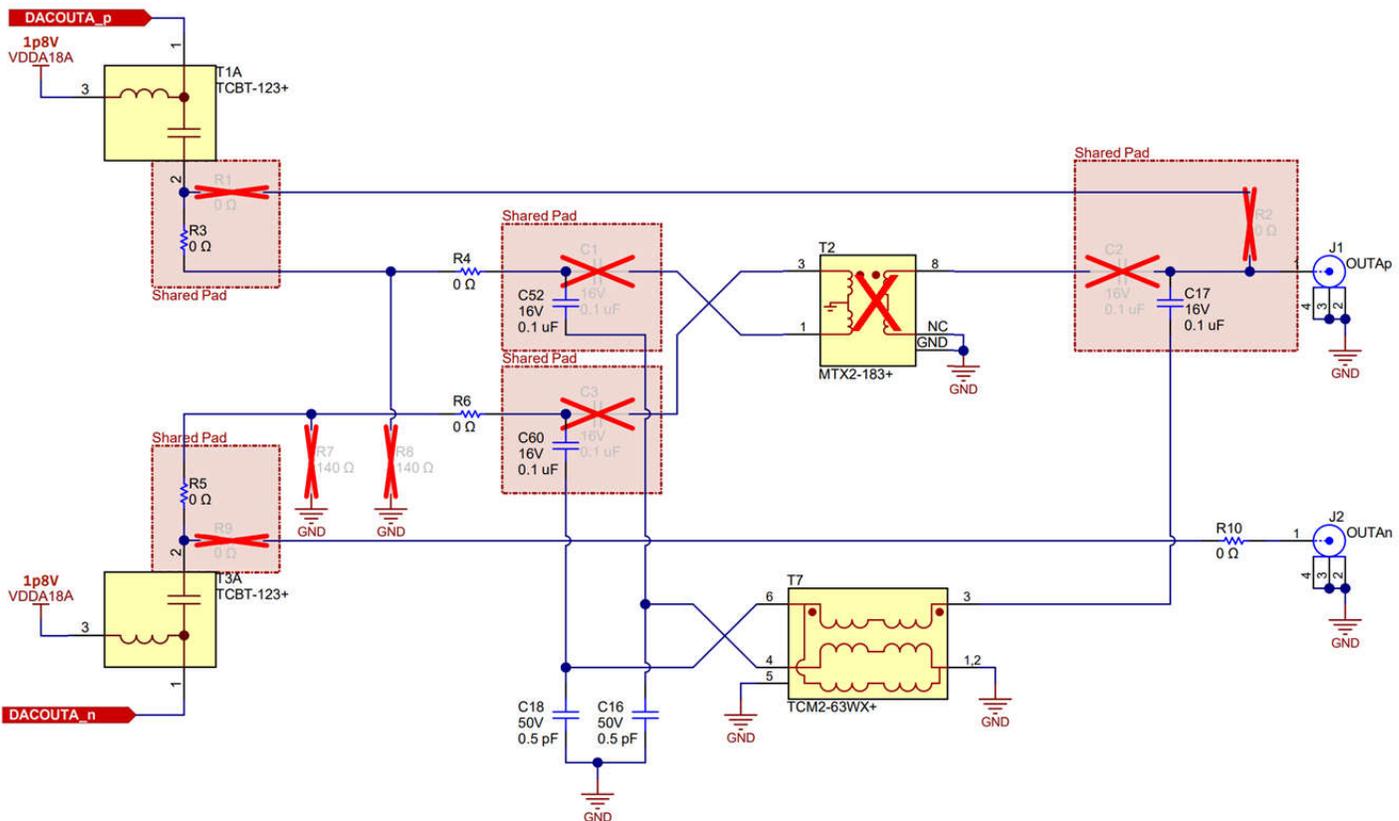
The analog output path can be configured for both a high frequency path (MTX2-183+ balun from Mini-Circuits), which is default on CHB. And low frequency path (TCM2-63WX+ balun from Mini-Circuits) which is default on CHA. To use either balun, some components must be changed to direct the output signal as appropriate. See [Table 2-2](#).

Each analog output path also has the ability to bypass both balun options entirely and allow the user to access the outputs differentially as well. To enable this feature, some components must be changed. See [Table 2-3](#).

**Table 2-2. Component Changes to Modify DAC EVM Output Paths**

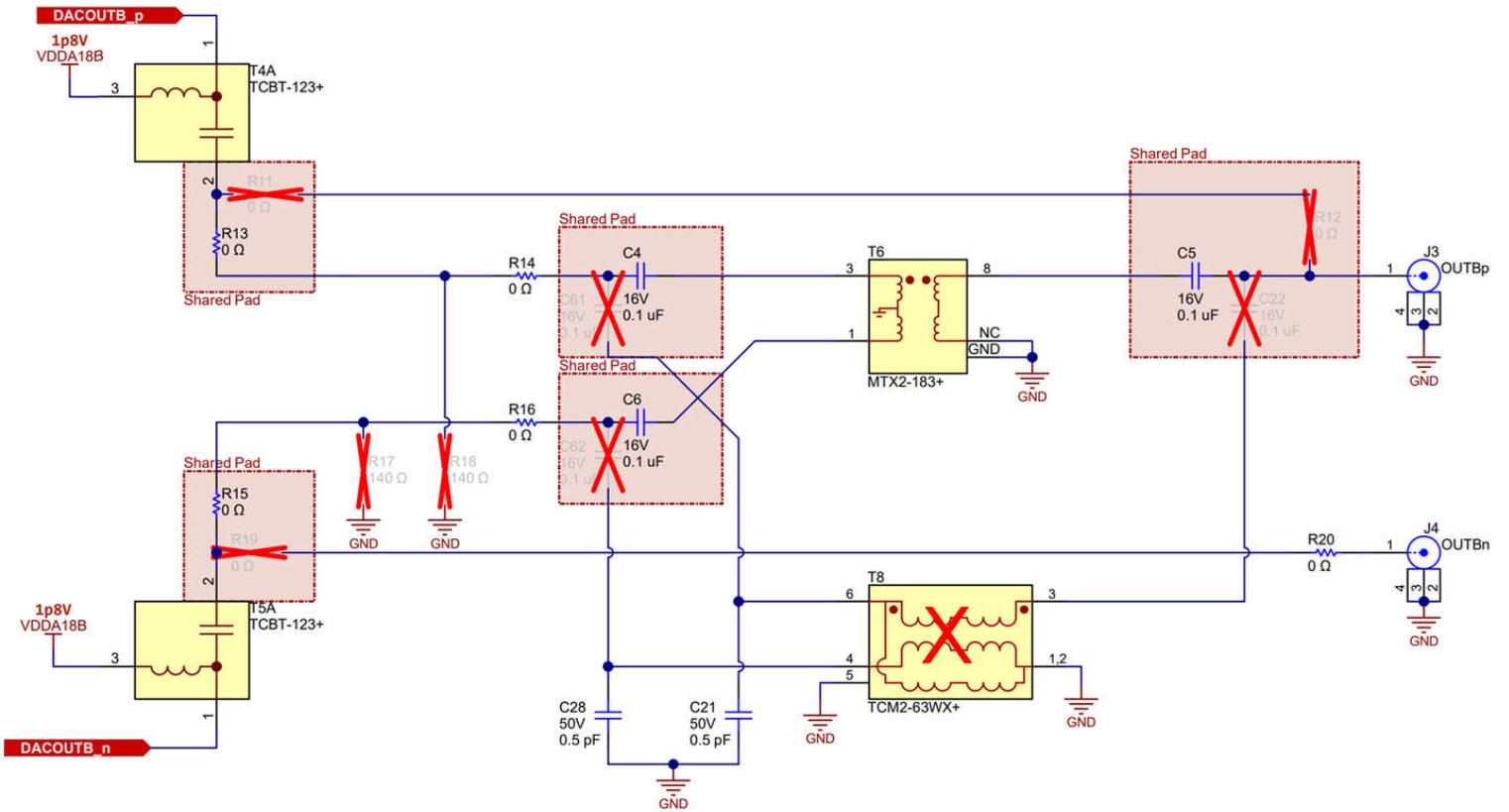
DAC Output Channel	Components to Remove	Components to Populate
CHA - Single-ended (MTX2-183+)	C52, C60, C17	C1, C2, C3 = 0.1μF
CHA - Differential (balun bypass)	R3, R5, C17	R1, R9, R2 = 0Ω
CHB - Single-ended (TCM2-63WX+)	C4, C6, C5	C61, C62, C22 = 0.1μF
CHB - Differential (balun bypass)	R13, R19, C5	R11, R15, R12 = 0Ω

Each analog output path has a wideband biasT on each output P/N pin to bias the outputs appropriately across the DAC supported bandwidth.



A. DAC Output stage. By default the TCM2-63WX+ balun is used for this channel. (30MHz to 6GHz)

**Figure 2-24. Analog Output Path - CHA**



A. DACB Output stage. By default the MTX2-183+ balun is used for this channel. (2MHz to 18GHz)

Figure 2-25. Analog Output Path - CHB

## 2.3 FMC Signal Routing

Table 2-3 provides the signal routing details for the DAC39RF12EVM.

All signal routing is handled by the DAC with the internal JESD crossbar feature.

This is also featured in the JESD crossbar dialogue box within the DAC39RF12EVM GUI.

**Table 2-3. Signal Routing**

DAC JESD Resource	Inverted	FMC Resource	FMC Pins	TSW14J59 FPGA Resource
Lane 9	Yes	DP0_C2M	C2, C3	Q224 MGTYTXN0
Lane 11	Yes	DP1_C2M	A22, A23	Q224 MGTYTXN1
Lane 15	Yes	DP2_C2M	A26, A27	Q224 MGTYTXN2
Lane 5	Yes	DP3_C2M	A30, A31	Q224 MGTYTXN3
Lane 3		DP4_C2M	A34, A35	Q225 MGTYTXN0
Lane 0	Yes	DP5_C2M	A38, A39	Q225 MGTYTXN1
Lane 1	Yes	DP6_C2M	B36, B37	Q225 MGTYTXN2
Lane 2	Yes	DP7_C2M	B32, B33	Q225 MGTYTXN3
Lane 7	Yes	DP8_C2M	B28, B29	Q226 MGTYTXN0
Lane 13	Yes	DP9_C2M	B24, B25	Q226 MGTYTXN1
Lane 12	Yes	DP10_C2M	Z24, Z25	Q226 MGTYTXN2
Lane 14	Yes	DP11_C2M	Y26, Y27	Q226 MGTYTXN3
Lane 6	Yes	DP12_C2M	Z28, Z29	Q227 MGTYTXN0
Lane 4	Yes	DP13_C2M	Y30, Y31	Q227 MGTYTXN1
Lane 10	Yes	DP20_C2M <sup>(1)</sup>	Z8, Z9	Q227 MGTYTXN2
Lane 8	Yes	DP21_C2M <sup>(1)</sup>	Y6, Y7	Q227 MGTYTXN3

(1) DP20\_C2M and DP21\_C2M can be rerouted to DP14\_C2M and DP15\_C2M to meet VITA compliance with other FPGA boards.

## 3 References

### 3.1 Trademarks

Microsoft® and Windows® are registered trademarks of Microsoft Corporation. All trademarks are the property of their respective owners.

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
  - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductor products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
  - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
  - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
  - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
  - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

### **WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

**NOTE:**

**EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.**

### 3 Regulatory Notices:

#### 3.1 United States

##### 3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

##### 3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### **FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### 3.2 Canada

##### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

#### 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_02.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page)

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#### 3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
    - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
    - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
    - 4.3 *Safety-Related Warnings and Restrictions:*
      - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
      - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
    - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
  5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
  6. *Disclaimers:*
    - 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
    - 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
  7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.
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8. *Limitations on Damages and Liability:*

8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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