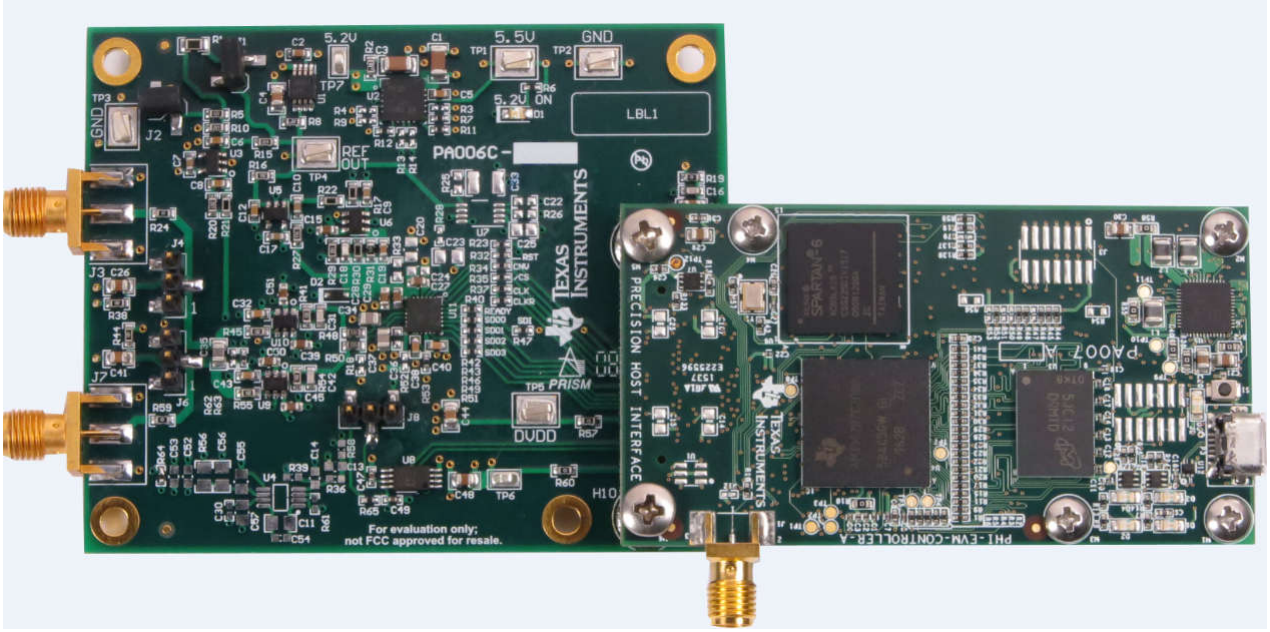
User's Guide

ADS9110EVM-PDK User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS9110 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS9110 , which is an 18-bit, 2-MSPS, fully-differential input, successive approximation register (SAR) analog-to-digital converter (ADC) that featuresan enhanced serial multiSPI® digital interface an enhanced serial multiSPI® digital interface. The EVM-PDK eases the evaluation of the ADS9110 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.



The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS9110	SBAS629
OPA625	SBOS688
OPA376	SBOS406
OPA378	SBOS417
REF5050	SBOS410
TPS7A4700	SBVS204

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1 Evaluation Module Overview

The ADS9110EVM-PDK is a platform for evaluating the performance of the ADS9110 SAR ADC, which is a fully-differential input, 18-bit, 2-MSPS device. The evaluation kit includes the ADS9110EVM board and the *Precision Host Interface* (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS9110EVM board includes the ADS9110 SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS9110
- Supplies power to all active circuitry on the ADS9110EVM board

Along with the ADS9110EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS9110EVM-PDK Features

The ADS9110EVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS9110 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS9110 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, Windows 8, 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS9110EVM Features

The ADS9110EVM includes the following features:

- Onboard low-noise and low distortion ADC input drivers optimized to meet ADC performance
- Onboard precision 5.0V voltage reference filtered and followed by a low-noise, low-offset and low-impedance buffer. The reference driver circuit is optimized for 1-LSB voltage regulation under maximum loading conditions at full device throughput of 2 MSPS.
- Jumper-selectable 0V and 2.5V input common-mode options allow unipolar and bipolar inputs
- Onboard ultralow noise low-dropout (LDO) regulator for excellent 5.2V single-supply regulation of all operation amplifiers and voltage reference

2 Analog Interface

As an analog interface, the evaluation board uses operational amplifiers in a variety of configurations to drive the ADS9110 input signal and reference inputs. This section covers driver details including jumper configuration for different input signal common modes and board connectors for a differential signal source.

2.1 Connectors for Differential Signal Source

The ADS9110EVM is designed for easy interfacing to an external analog differential source via a subminiature version A (SMA) connector or 100-mil headers. J7 and J3 are SMA connectors that allow analog source connectivity through coaxial cables. Also, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to the J4:2 and J6:2 pins.

Note

The input does not support single-ended signals. The external source must be differential or balanced keeping the negative and positive inputs to the board symmetric such that Vs(+) = –Vs(–) at any given time.

Table 2-1. J7 and J3 SMA Connectors Description

Pin Number	Signal	Description
J3	Vs(–)	Negative differential board input, 1kΩ input impedance
J7	Vs(+)	Positive differential board input, 1kΩ input impedance

Table 2-2. J4 and J6 Headers Description

Pin Number	Signal	Description
J4:3	TEST 0.23V	Do not use: diagnostic use only
J4:2	Vs(–)	Negative differential board input, 1kΩ input impedance
J4:1	AGND	Analog ground
J6:3	AGND	Analog ground
J6:2	Vs(+)	Positive differential board input, 1kΩ input impedance
J6:1	TEST 4.77V	Do not use: diagnostic use only

2.2 ADC Differential Input Signal Driver

The differential signal inputs of the ADS9110 are not dynamically high impedance. SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed that effectively make the ADC inputs dynamically low impedance. Thus, the evaluation board has low impedance on board drivers that maintain ADC performance with maximum loading at the full device throughput of 2-MSPS for signal.

2.2.1 Input Signal Path

Figure 2-1 shows the signal path for the differential signal applied at the board inputs. The board input impedance is 1kΩ with 10nF differential filtering that keeps noise in external cabling common. The overall signal path bandwidth is limited to 160kHz by the anti-aliasing filter formed from a 1kΩ resistor and 1nF capacitor at the amplifier feedback. Finally, the two OPA625 operational amplifiers drive the ADS9110 differential inputs with 2.2Ω impedance up to 7MHz that properly drives the low dynamic impedance of the ADC inputs at 2-MSPS.

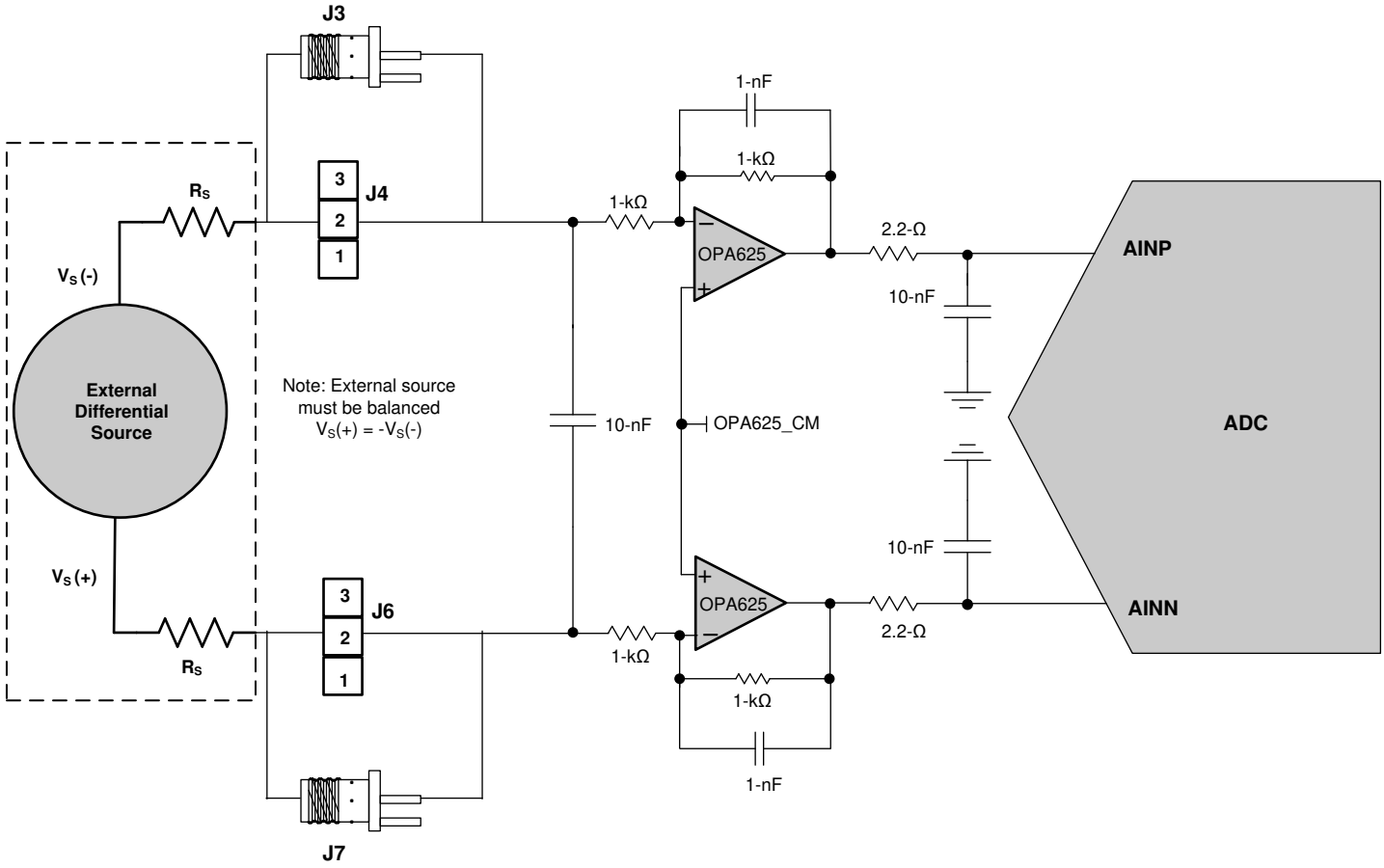

Figure 2-1. OPA625 Differential Input Driving Path

2.2.2 Input Common-Mode Jumper Configuration

The ADS9110EVM board accommodates three external source common-mode options: 0V, 2.5V, and floating with jumpers J1 and J2; see Figure 2-2 and Table 2-3.

J2 selects the OPA625 common-mode as 2.5V (J2:OPEN) or 1.25V (J2:CLOSED). J1 increases the OPA625 common-mode by almost 100mV to avoid amplifier output saturation with full-scale external source signal amplitude. R1 is installed as 280kΩ, allowing full-scale external source signals for external source impedance (R_S) between 0Ω and 32Ω, with 0V common mode. R1 must be changed to compensate for larger external source impedance (R_S) values or for 2.5V external source common-mode, as explained in Section 2.2.3.

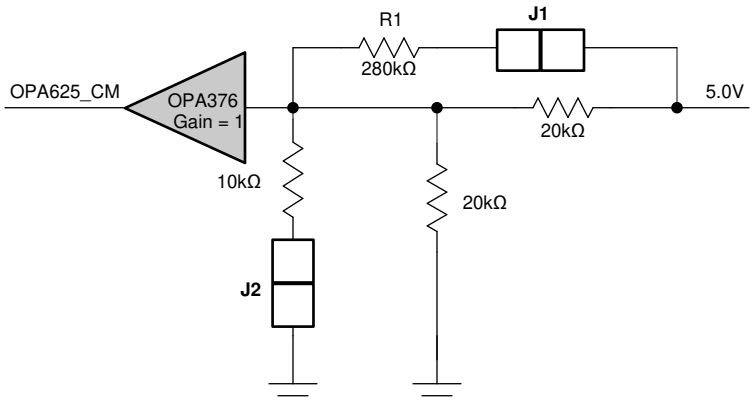

Figure 2-2. Common-Mode Selection Jumpers

Table 2-3. J1 and J2 Configuration per Input Common-Mode

J1 Setting (R1 Comp)	J2 Setting	External Signal Common-Mode	Differential Source Type
CLOSED	CLOSED	0V	Bipolar: If R1 = 280kΩ, R_S range is 0Ω to 32Ω
CLOSED	OPEN	2.5V	Unipolar: must change R1 to match R_S
CLOSED	OPEN	Floating	AC-coupled bipolar: If R1 = 280kΩ, no R_S restriction

2.2.3 R1 Setting vs Source Impedance

The external source impedance (R_S) adds up to the 1kΩ of the input resistor, thereby moving the output common-mode of the OPA625 amplifiers. To compensate for this change in output common-mode, R1 can be modified according to the particular external source impedance value used with the evaluation board to allow full-scale input range without saturating the OPA625 amplifiers.

The board is shipped with R1 as 280kΩ that allows an external source impedance (R_S) range between 0Ω to 32Ω for a 0V common-mode configuration (J1: closed and J2: closed). For floating or ac-coupled signals, the input common-mode is set by the OPA625 amplifiers themselves and R1 must remain at 280kΩ for any given source impedance. The ADC common-mode for 0V input common-mode setting is calculated using Equation 1.

$$\mathrm{ADC\_V_{CM}} = \frac{5 \times (10\mathrm{k\Omega}//20\mathrm{k\Omega})}{(10\mathrm{k\Omega}//20\mathrm{k\Omega}) + (\mathrm{R_1}//20\mathrm{k\Omega})} \times \left(1 + \frac{1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) \quad (1)$$

In the case of unipolar input signals with a 2.5V common-mode, the ADC common-mode is calculated using Equation 2.

$$\mathrm{ADC\_V_{CM}} = \frac{5 \times 20\mathrm{k\Omega}}{20\mathrm{k\Omega} + (\mathrm{R_1}// 20\mathrm{k\Omega})} \times \left(1 + \frac{1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) - \left(\frac{2.5 \times 1\mathrm{k\Omega}}{1\mathrm{k\Omega} + \mathrm{R_S}}\right) \quad (2)$$

For Equation 1 and Equation 2, the value of R1 must be calculated to satisfy Equation 3:

$$2.5\ \mathrm{V} \leq \mathrm{ADC\_V_{CM}} \leq 2.6\ \mathrm{V} \quad (3)$$

2.3 Onboard ADC Reference

The EVM does not include a provision for driving the reference input of the ADS9110 from an external source. The reference input signal path is entirely self-contained on the ADS9110EVM and consists of the REF5050, a 5.0V precision voltage reference. The output of the REF5050 is filtered and buffered by a reference driver formed from two amplifiers: the OPA625 and OPA378. This reference driver offers zero-offset, low-noise and is optimized for a 1-LSB voltage regulation under maximum loading conditions at full device throughput of 2-MSPS. The schematic for the reference driver circuit is shown in Figure 2-3.

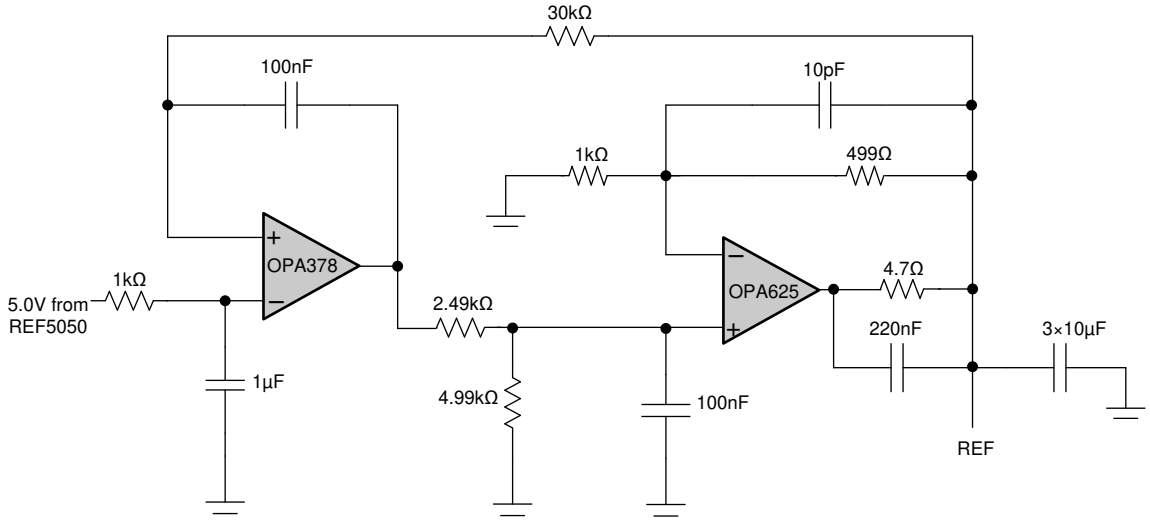

Figure 2-3. Onboard Reference Signal Path

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS9110 ADC (over SPI or multiSPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS9110EVM-PDK platform. Once the hardware is initialized, the EEPROM is no longer used.

3.1 multiSPI® for ADC Digital IO

The ADS9110EVM-PDK supports all the interface modes as detailed in the ADS9110 18-Bit, 2-MSPS, 15-mW, SAR ADC With Enhanced Performance Features data sheet . In addition to the standard SPI modes, (with single-, dual-, and quad-SDO lanes), the multiSPI modes support single- and dual-data output rates and the four possible clock source settings as well. The PHI is capable of operating at a 1.8-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer.

The EEPROM on the ADS9110EVM use a 3.3V power supply generated directly by the PHI. The ADC and analog input drive circuits are powered by the TPS7A4700 onboard the EVM, which is a low-noise linear regulator that uses the 5.5V supply out of a switching regulator on the PHI to generate a much cleaner 5.2V output. The 1.8 V supply to the digital section of the ADC is provided directly by an LDO on the PHI.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and the loads to minimize inductance along the load current path.

5 ADS9110EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS9110EVM-PDK.

5.1 Default Jumper Settings

Jumper settings are determined by common mode and source impedance of the external source that provides a differential signal to the board. Remove shunts from J4 and J6 and set J2 and J1 according to the external source as described in Section 2.

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS9110 and run the GUI installer to install the EVM GUI software on the user's computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message can appear or the *installer.exe* file can be deleted.

Accept the license agreements and follow the on-screen instructions to complete the installation.

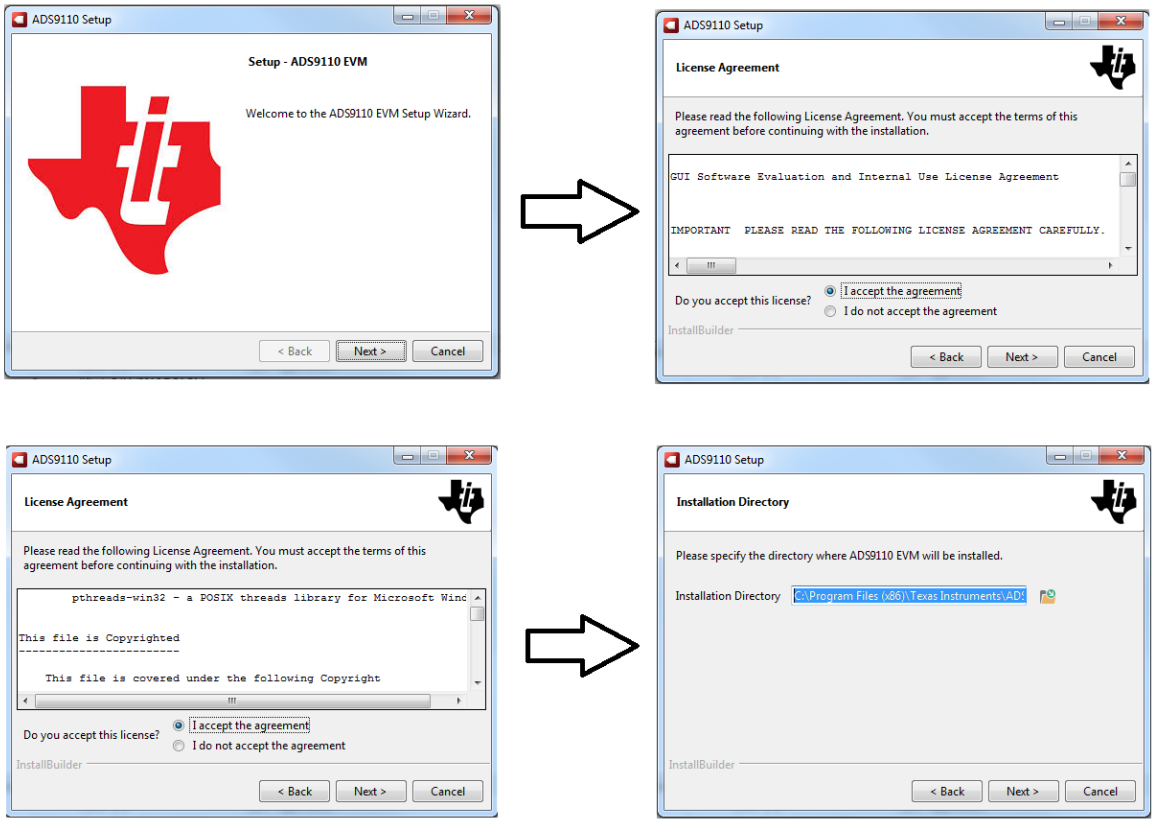

Figure 5-1. ADS9110 Software Installation Prompts

As a part of the ADS9110EVM GUI installation, a prompt with a *Device Driver Installation* appears on the screen. Click *Next* to proceed.

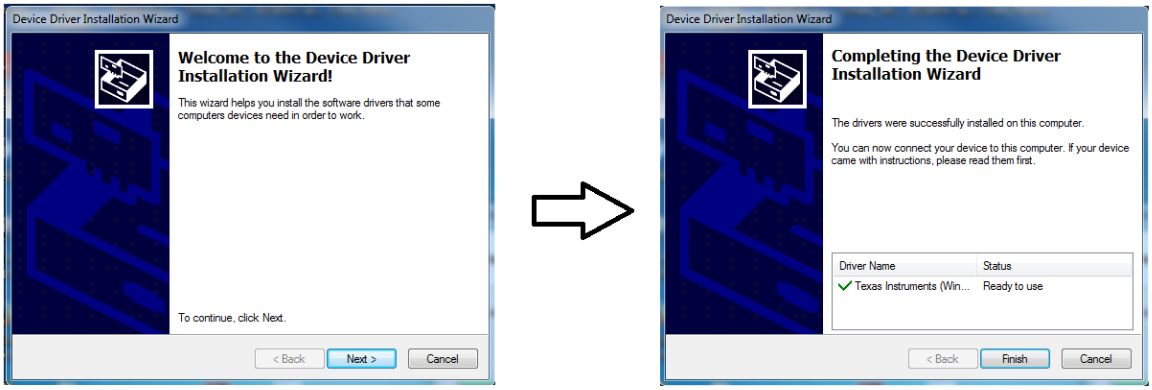

Figure 5-2. Device Driver Installation Wizard Prompts

Note

A notice can appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS9110EVM-PDK requires *LabVIEW™ Run-Time Engine* and can prompt for the installation of this software, if not already installed.

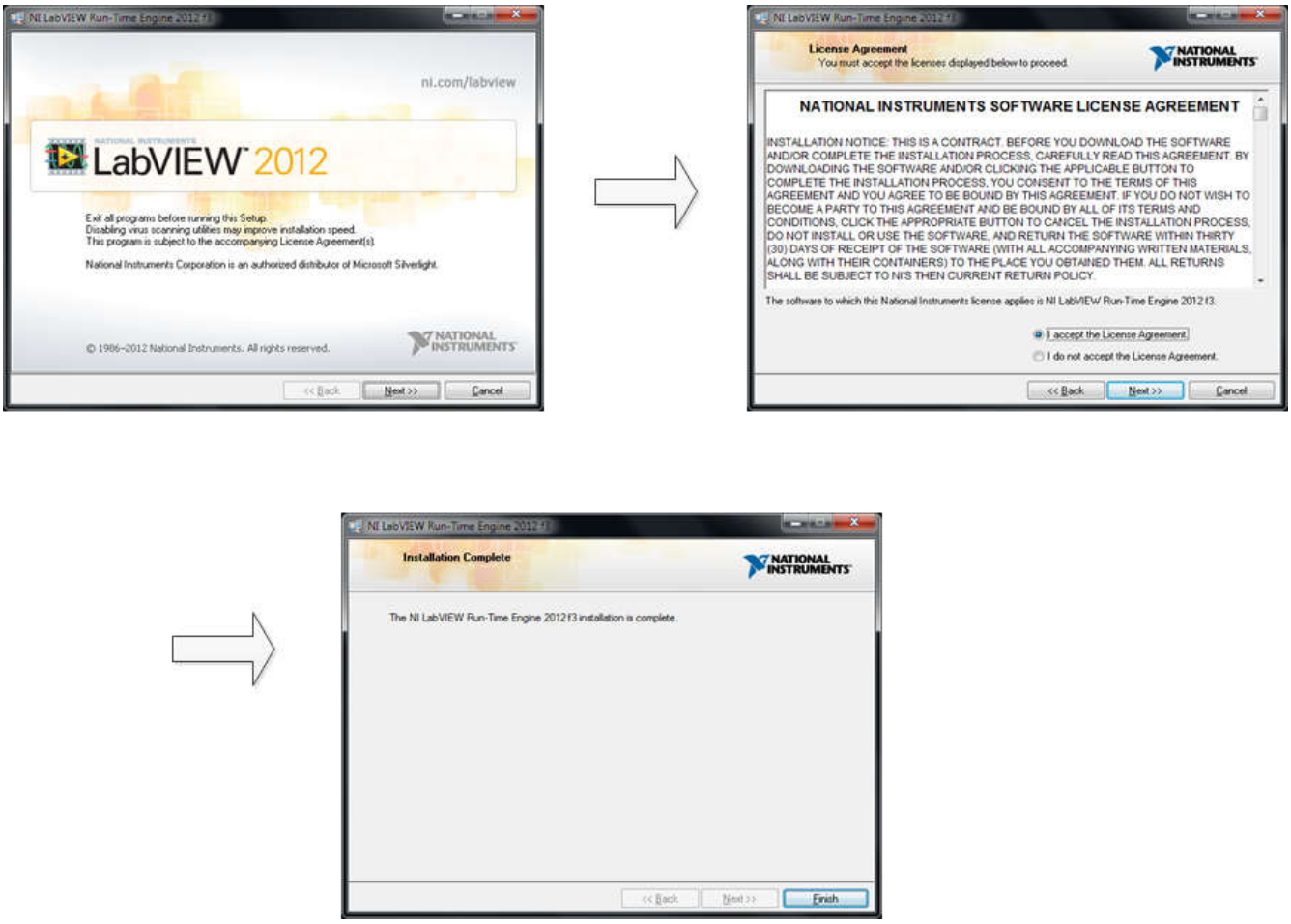

Figure 5-3. LabVIEW Run-Time Engine Installation

After these installations, verify that C:\Program Files (x86)\Texas Instruments\ADS9110EVM is as shown in Figure 5-4.

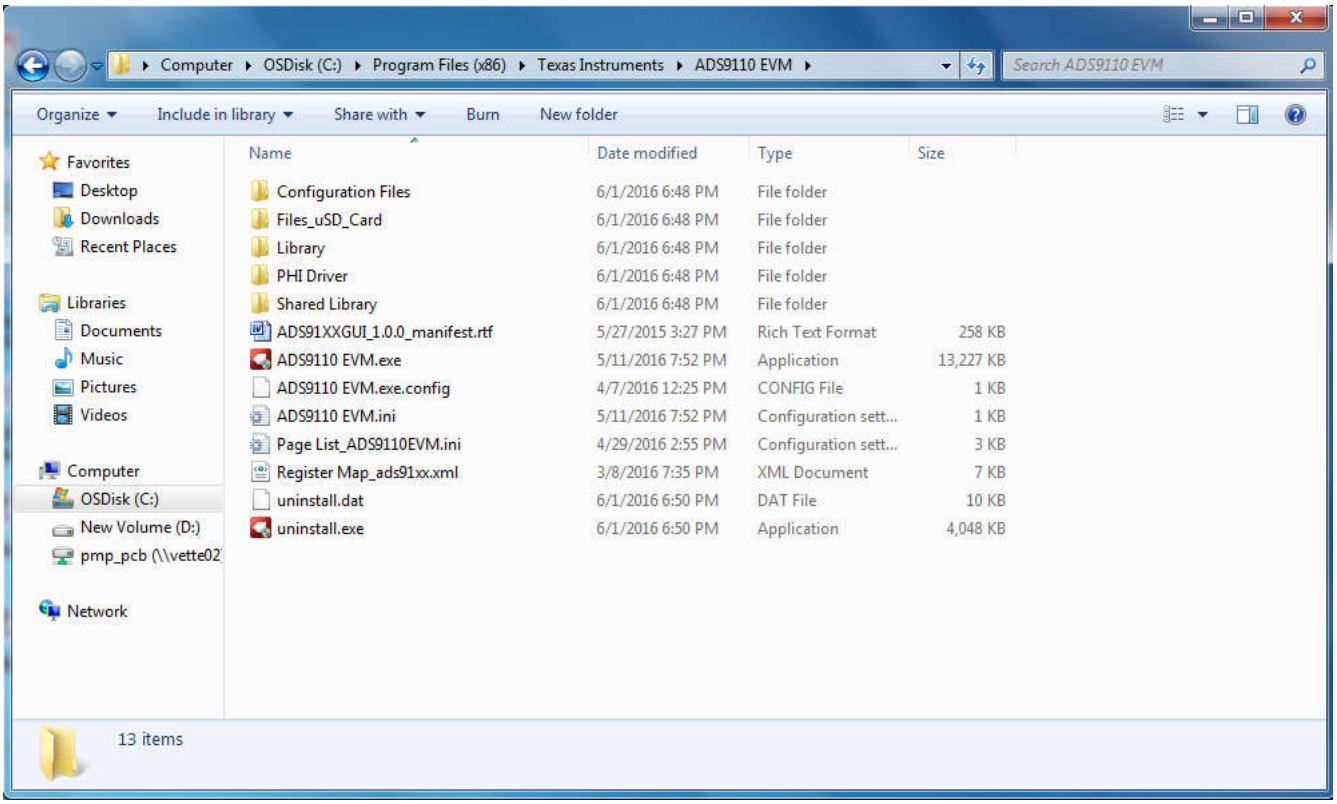

Figure 5-4. ADS9110EVM-PDK Folder Post-Installation

6 ADS9110EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS9110EVM-PDK to the computer and evaluating the performance of the ADS9110:

1. Connect the ADS9110EVM to the PHI. Install the two screws as indicated in Figure 6-1.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. The resulting LED indicators are shown in Figure 6-1.

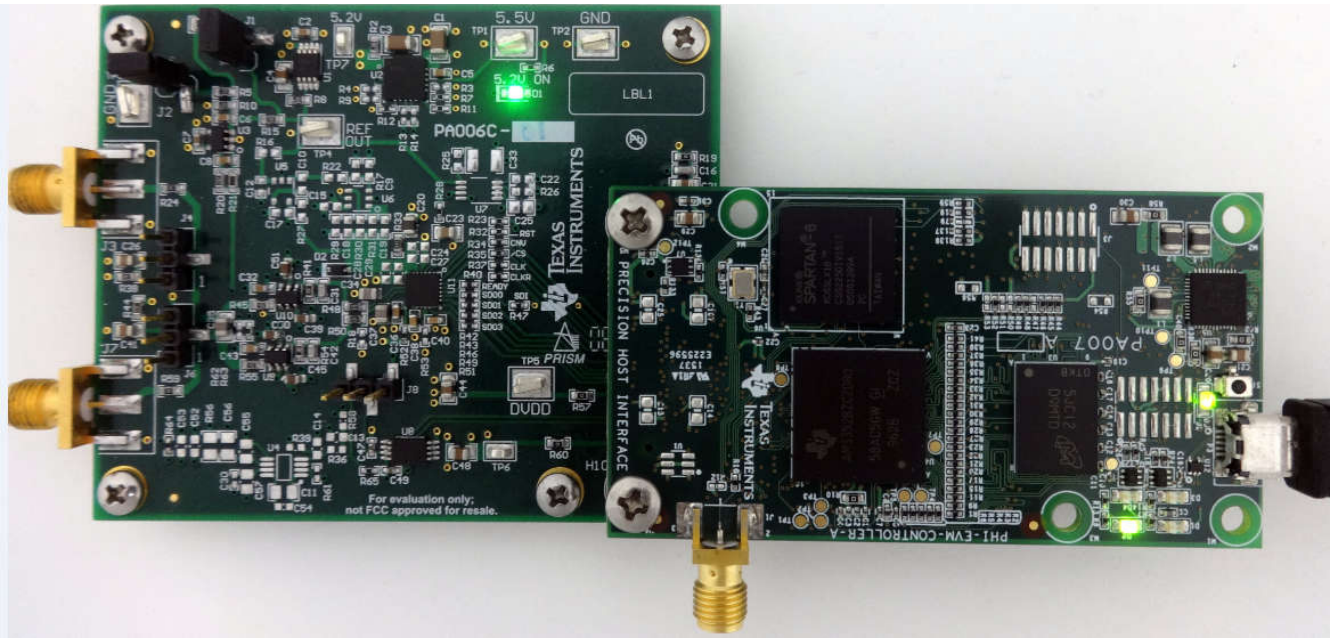

Figure 6-1. EVM-PDK Hardware Setup and LED Indicators

3. Launch the ADS9110EVM GUI software.

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the ADS9110 including interface modes, sampling rate, and number of samples to be captured.

Figure 6-2 identifies the input parameters of the GUI (as well as the default values) through which the various functions of the ADS9110 can be exercised. These settings are global because the settings persist across the GUI tools listed in the top left pane (or from one page to another).

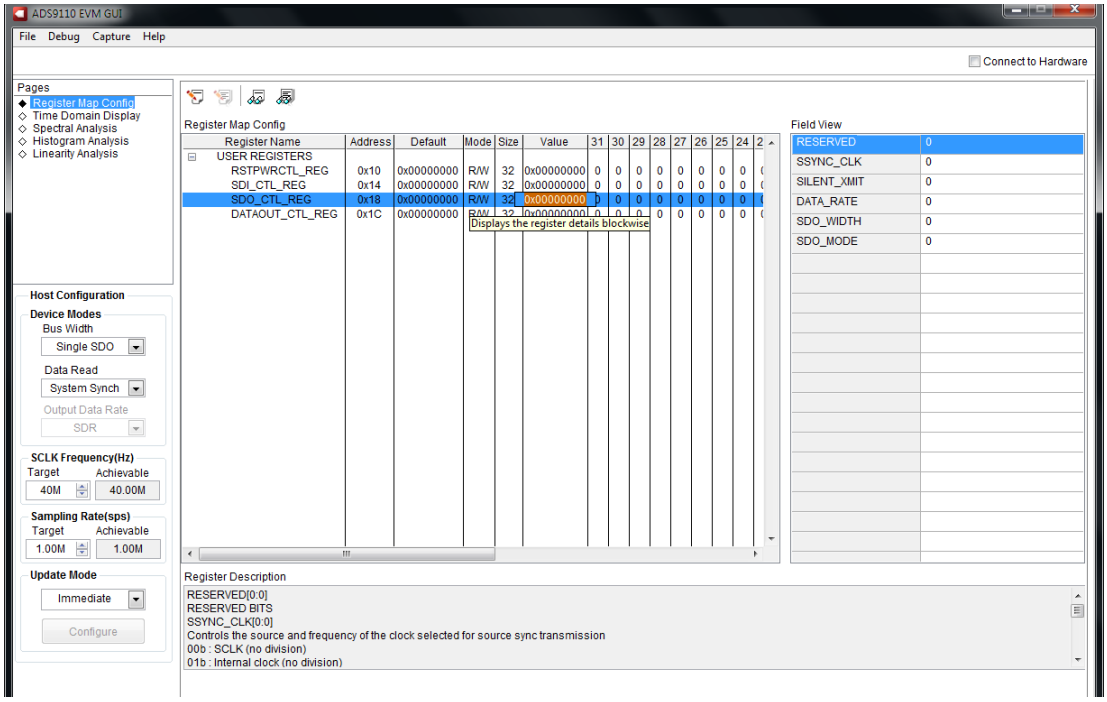

Figure 6-2. EVM GUI Global Input Parameters

The host configuration options in this pane allow the user to choose from various SPI and multiSPI host interface options available on the ADS9110. The host always communicates with the ADS9110 using the standard SPI protocol over the single SDI lane, irrespective of the mode selected for data capture.

The drop-down boxes under the Interface Configuration sub-menu allow the user to select the data capture protocol. The SDO Width drop-down allows selection between Single-, Dual- and Quad-SDO lanes. The SDO Mode drop-down allows selection between Standard SPI and multiSPI modes.

In SPI mode, the SDI Mode drop-down allows selection between the four SPI protocol combinations for CPOL and CPHA.

In multiSPI mode, the Clock Source drop-down menu allows selection between Source and System Synchronous modes; the Data Rate drop-down menu allows selection between SDR and DDR modes. Detailed descriptions of each of these modes is available in the ADS9110 18-Bit, 2MSPS, 15mW, SAR ADC With Enhanced Performance Features data sheet). The selected data capture protocol is summarized in the Protocol Selected indicator box.

The user can select *SCLK Frequency* and *Sampling Rate* on this paneand is dependent of the protocol selected. The GUI allows the user to enter the targeted values for these two parameters and the GUI computes the best values that can be achieved, considering the timing constraints of the selected device protocol.

The user can specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings and the achievable frequency can differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the Target Sampling Rate argument (also in Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK

frequencyand selected *Device Mode* and the closest match achievable is displayed. This pane, therefore, allows the user to try various settings available on the ADS9110 in an iterative fashion until the user converges to the best settings for the corresponding test scenario.

The final option in this pane is the selection for the Update Mode. The default value is *Immediate*, indicating that the interface settings selection made by the user is applied to configure both the host and the ADS9110 instantly. *Manual* indicates that the selection made is made only when the user finalizes the choices and is ready to configure the device.

The **Device Reset** button functions as a Master RESET to both the ADS9110EVM and the GUI. When the button is pressed, the ADC RESETs to the RESET configuration explained in the ADS9110 18-Bit, 2MSPS, 15mW, SAR ADC With Enhanced Performance Features data sheet). The GUI also updates the Interface Configuration settings and the Register Map to reflect the device RESET state.

6.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS9110. This tool can be selected by clicking on the Register Map Config radio button at the Pages section of the left pane, as indicated in Figure 6-3. On power-up, the values on this page correspond to the Host Configuration Settings that enable ADC sampling at the maximum sampling rate specified for the ADC. The register values can be edited by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately. The effect of changes in the register value reflect on the ADS9110 device on ADS9110EVM-PDK based on the Update Mode selection, as described in Section 6.1.

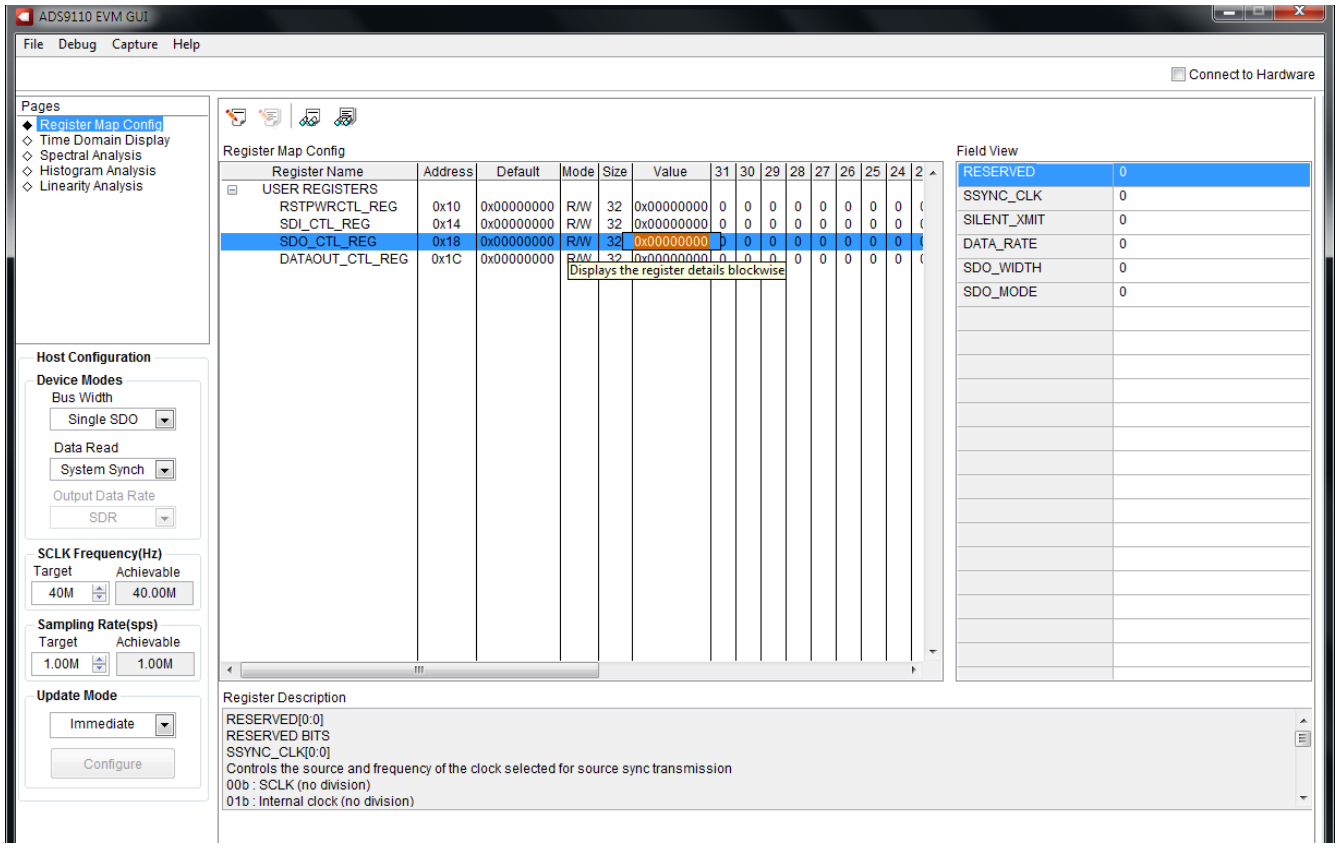

Figure 6-3. Register Map Configuration

Section 6.3 through Section 6.6 describe the data collection and analysis features of the ADS9110EVM-PDK GUI.

6.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS9110, as per the current interface mode settings using the **Capture** button as indicated in Figure 6-4. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections, triggers calculations to be performed on the same set of data.

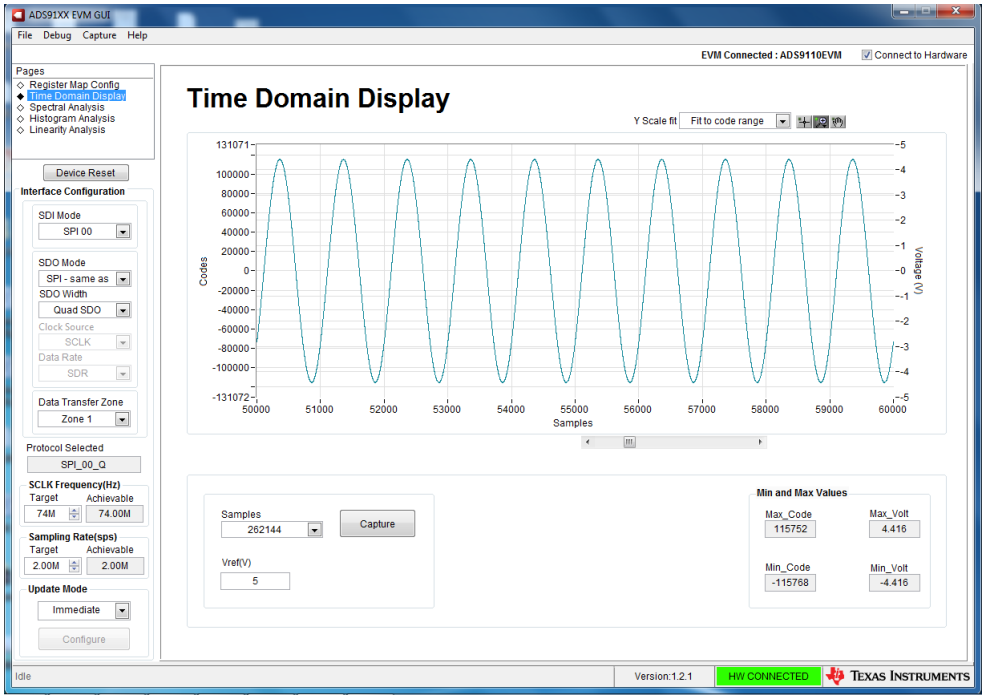

Figure 6-4. Time Domain Display Tool Options

6.4 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS9110 SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in dc inputs.

For dynamic performance evaluation, the external differential single-ended source must have better specifications than the ADC to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 6-1.

Table 6-1. External Source Requirements for Evaluation of the ADS9110

Specification Description	Specification Value
Signal frequency	2kHz
External source type	Balanced differential
External source common-mode	0V or floating (see Section 2.2.2 for jumper settings)
External source impedance (R_S)	10Ω–30Ω
External source differential impedance ($R_{S\_DIFF} = 2 \times R_S$)	20Ω–60Ω
Source differential signal (V_{PP} Amplitude for –0.1 dBFS)	$(2 \times R_S \times 4.45 \times 10^{-3}) + 8.9V$ or $(R_{S\_DIFF} \times 4.45 \times 10^{-3}) + 8.9V$
Maximum noise	$10\mu V_{RMS}$
Maximum SNR	110 dB
Maximum THD	–130 dB

For 2kHz SNR and ENOB evaluation at a maximum throughput of 2 MSPS, the number of samples must be 32768 or 65536. More samples brings the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations. On the contrary, for THD and SFDR evaluation, a much larger number of samples must be used to reduce the noise floor below –140 dBc to analyze noise-free harmonics and spurs in the order of –120dBc. Such analysis requires at least 262144 samples.

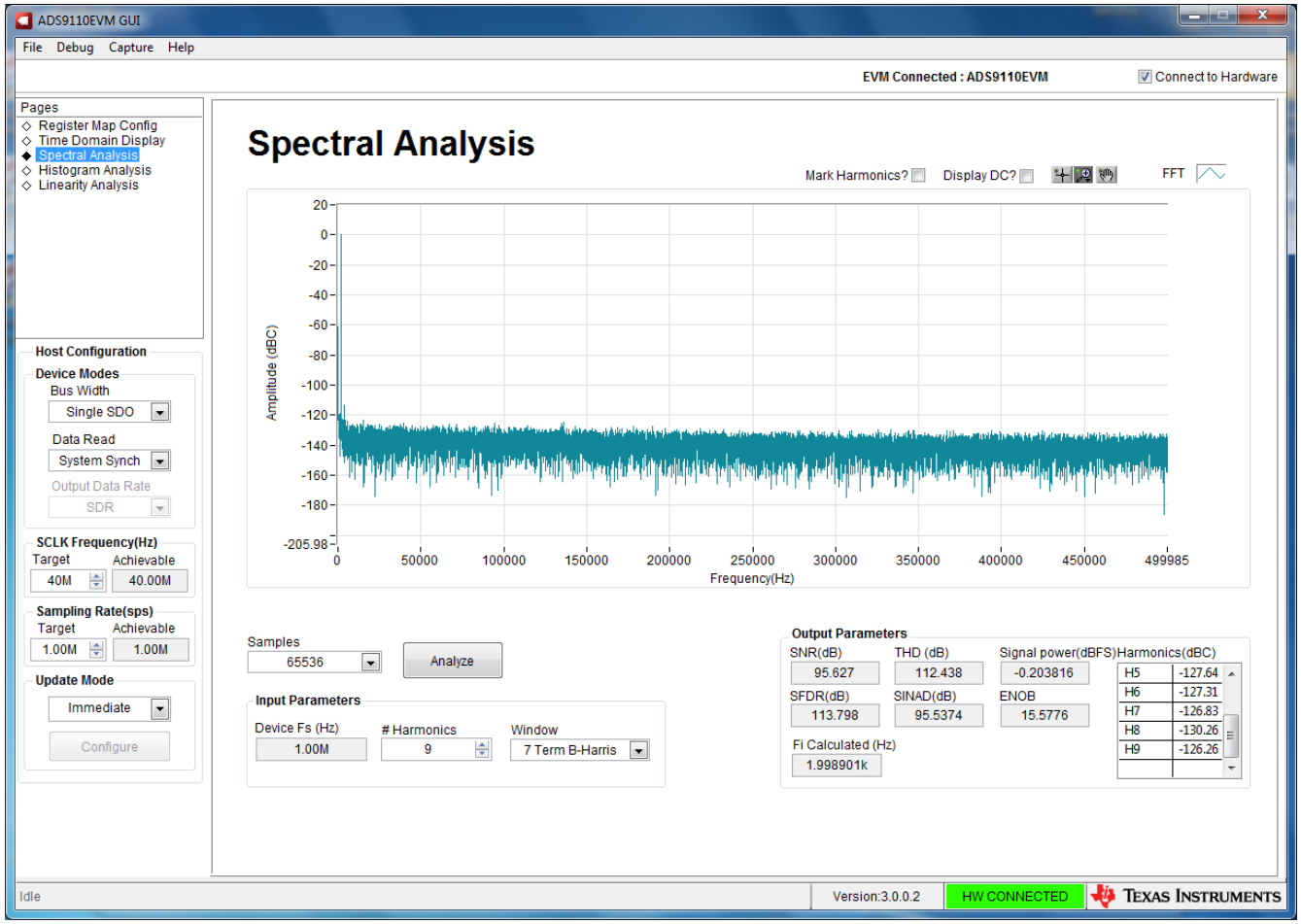

Figure 6-5. Spectral Analysis Tool

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

6.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking the *Capture* button, as shown in Figure 6-6:

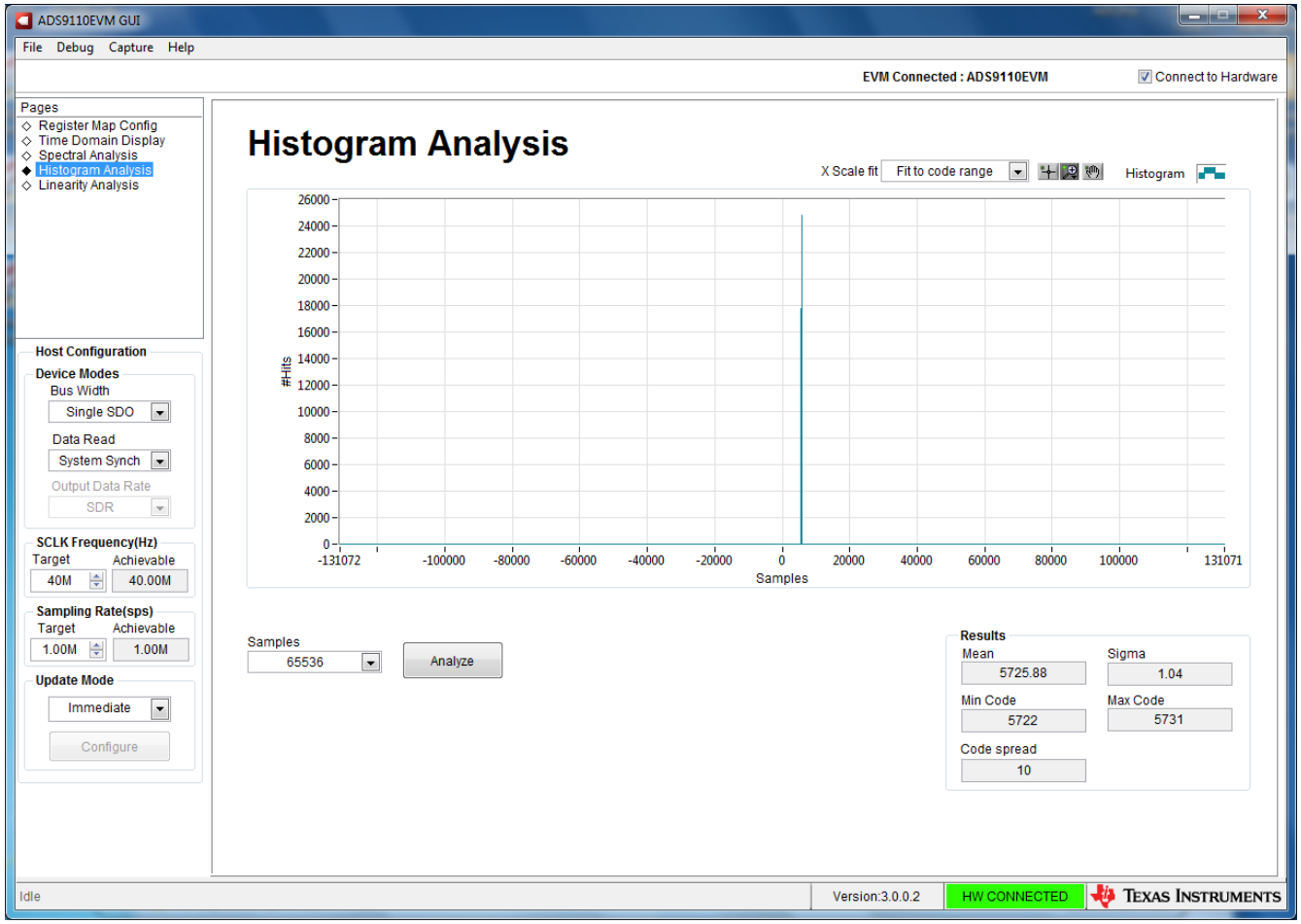

Figure 6-6. Histogram Analysis Tool

6.6 Linearity Analysis Tool

The linearity analysis tool measures and generates the DNL and INL plots over code for the specific ADS9110 installed in the evaluation board. A 2kHz sinusoidal input signal is required, which is slightly saturated (35mV outside the full-scale range at each input or 0.13dBFS) with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 6-2.

Table 6-2. External Source Requirements for ADS9110 Evaluation

Specification Description	Specification Value
Signal frequency	2kHz
External source type	Balanced differential
External source common mode	0V or floating (see Section 2.2.2 for jumper settings)
External source impedance (R_S)	10Ω–30Ω
External source differential impedance ($R_{S\_DIFF} = 2 \times R_S$)	20Ω–60Ω
Source differential signal (V_{PP} amplitude for –0.1 dBFS)	$(2 \times R_S \times 4.57 \times 10^{-3}) + 9.14V$ or $(R_{S\_DIFF} \times 4.57 \times 10^{-3}) + 9.14V$
Maximum noise	$30\mu V_{RMS}$
Maximum SNR	100dB
Maximum THD	–130 dB

The number-of-hits setting depends on the external noise source. For a 110dB SNR external source with approximately 10µVrms of noise, the total number of hits must be 512. For a source with 100dB SNR, the recommended number of hits is 1024.

Note

This analysis can take a couple of minutes to run and the evaluation board must remain undisturbed during the complete duration of the analysis.

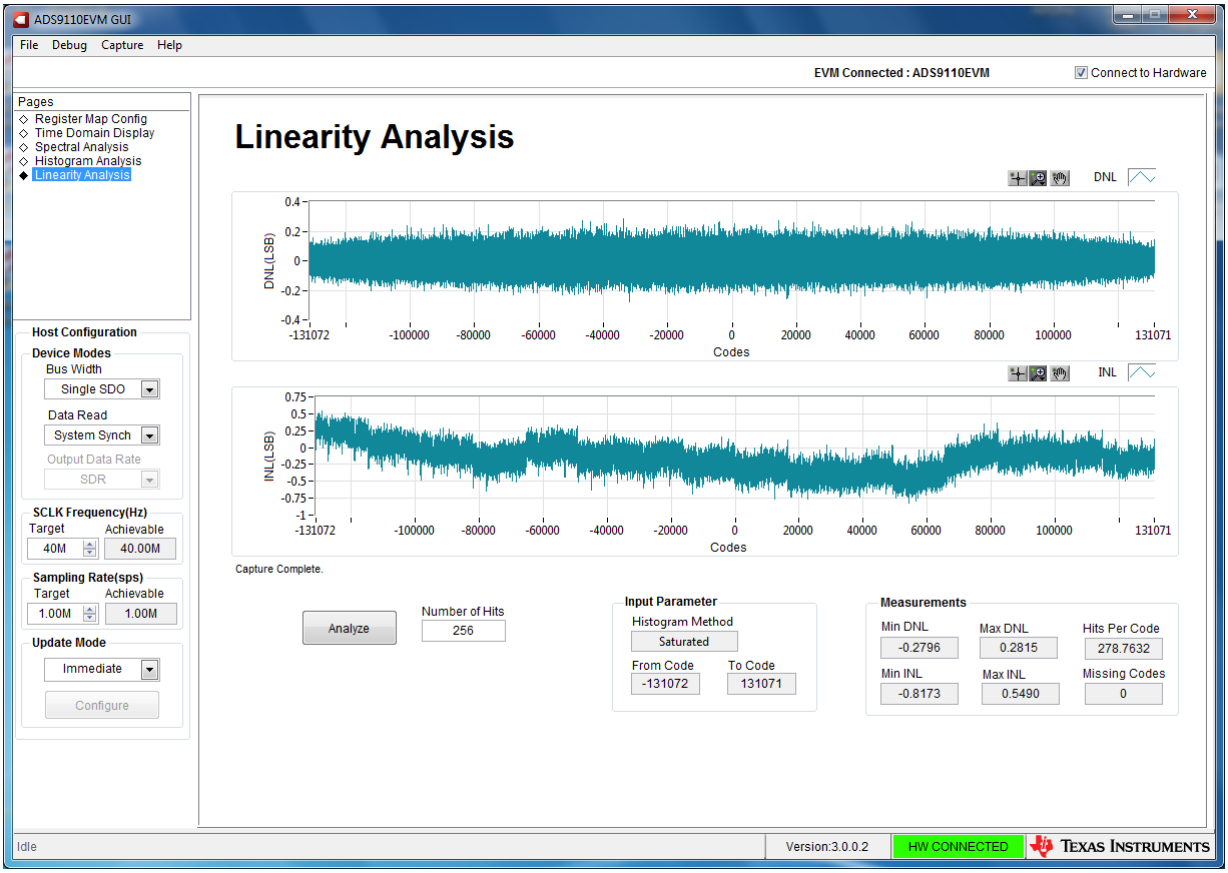

Figure 6-7. Linearity Analysis Tool

7 Hardware Design Files

This section contains the ADS9110EVM bill of materials, PCB layout, and the EVM schematics.

7.1 Schematics

The EVM schematics are shown below.

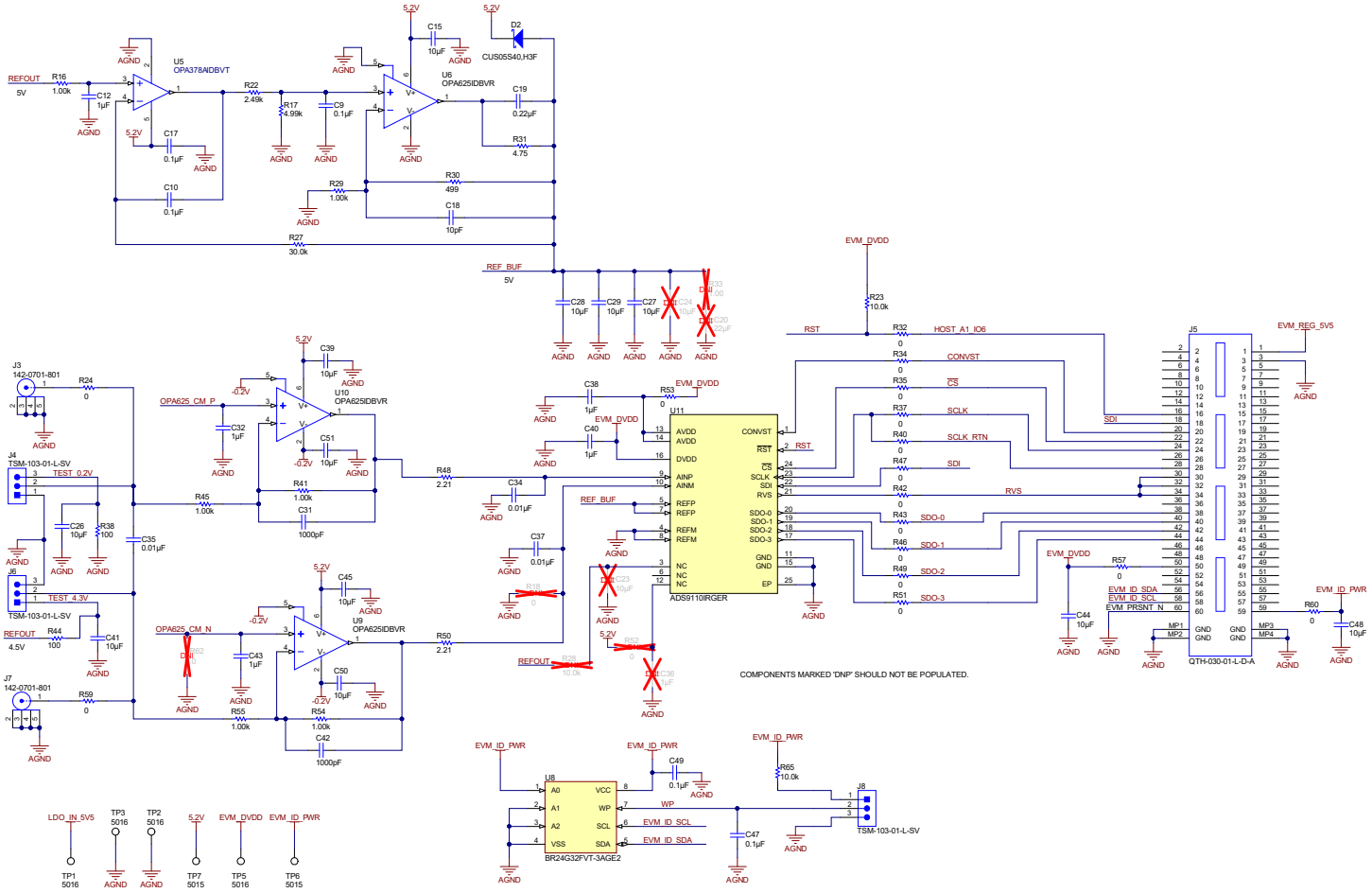

Figure 7-1. Schematic Diagram (Page 1) of the ADS9110EVM PCB

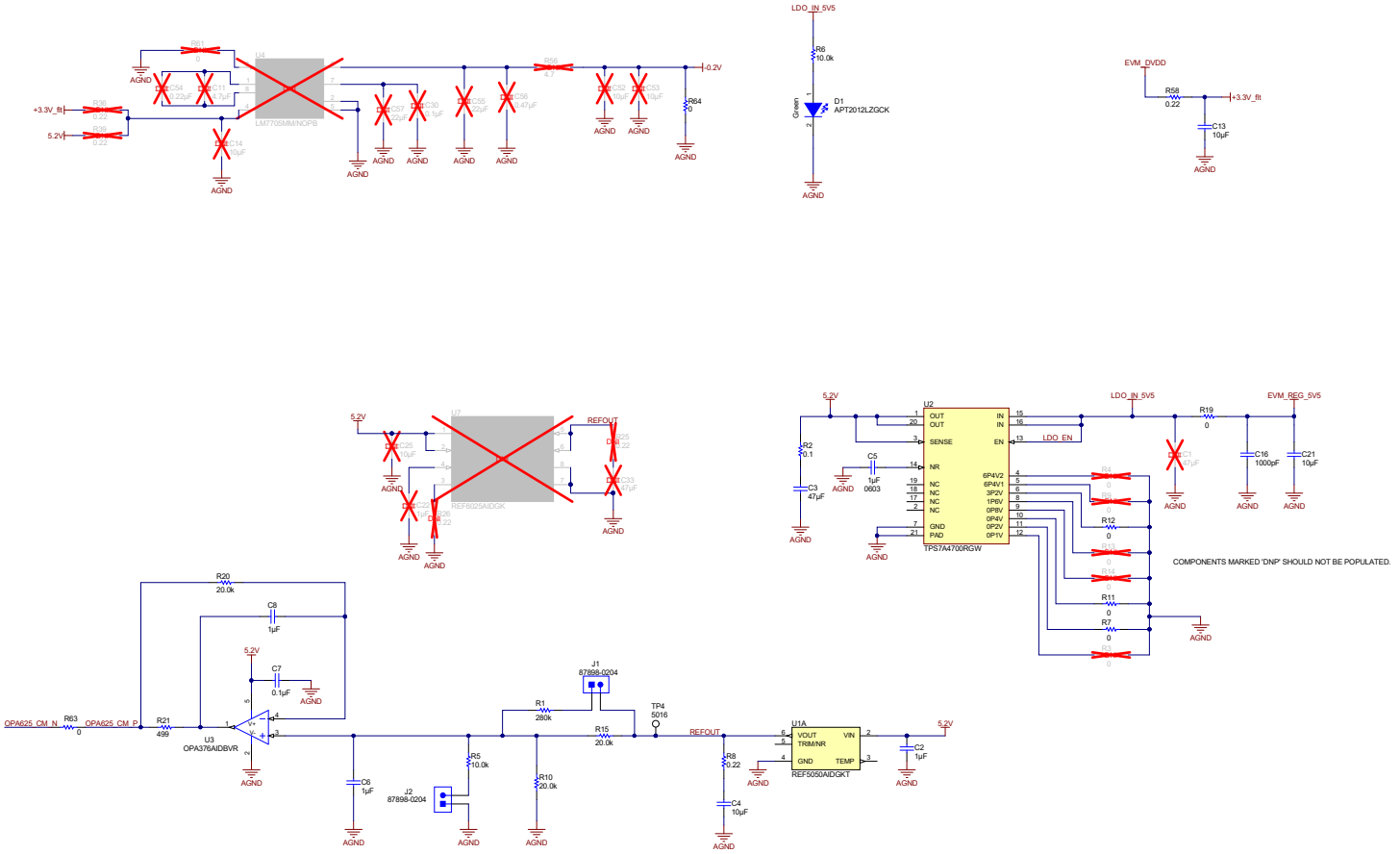

Figure 7-2. Schematic Diagram (Page 2) of the ADS9110EVM PCB

7.2 PCB Layout

Figure 7-3 through Figure 7-6 illustrate the EVM PCB layout.

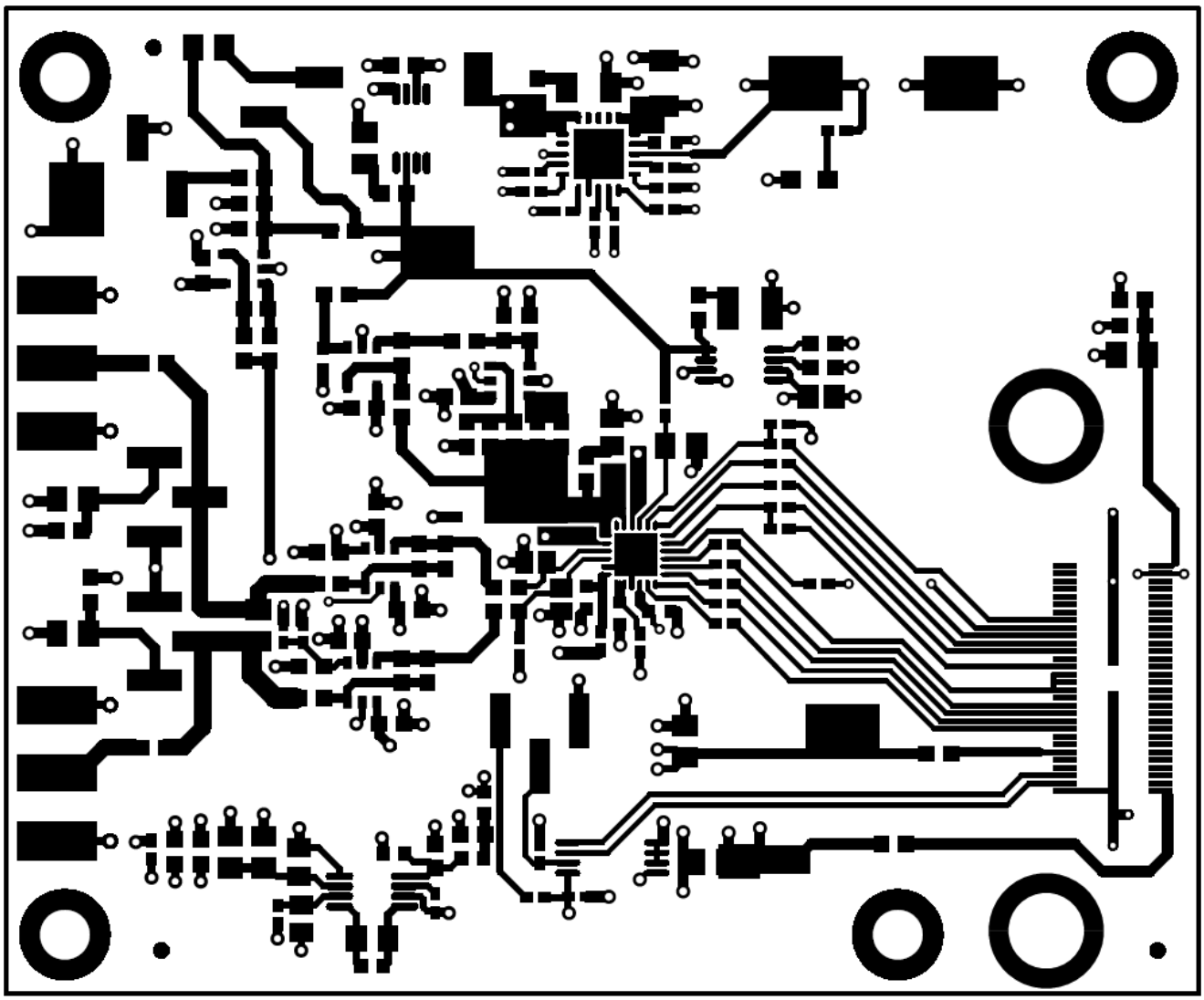

Figure 7-3. ADS9110EVM PCB Layer 1: Top Layer

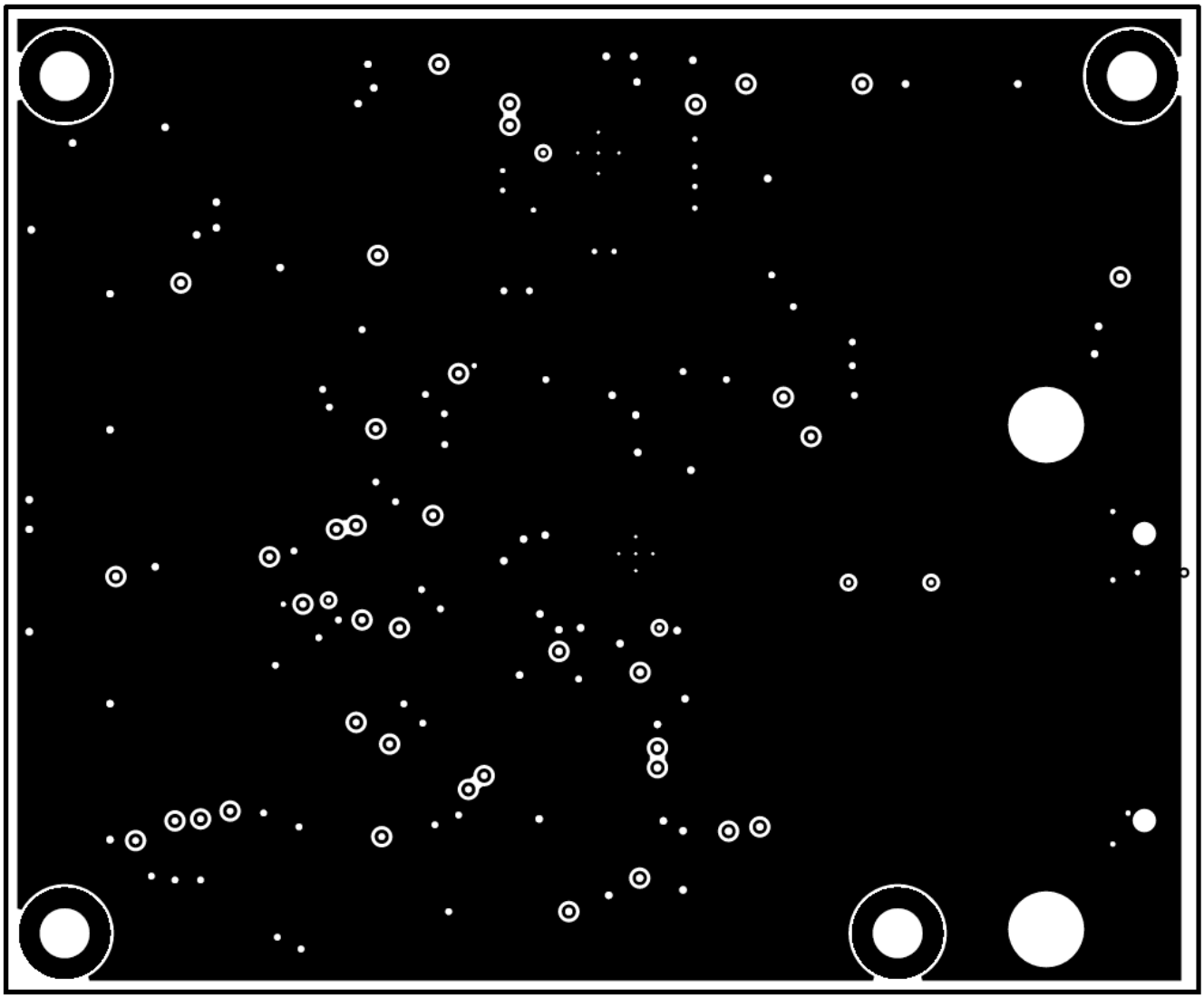

Figure 7-4. ADS9110EVM PCB Layer 2: GND Plane

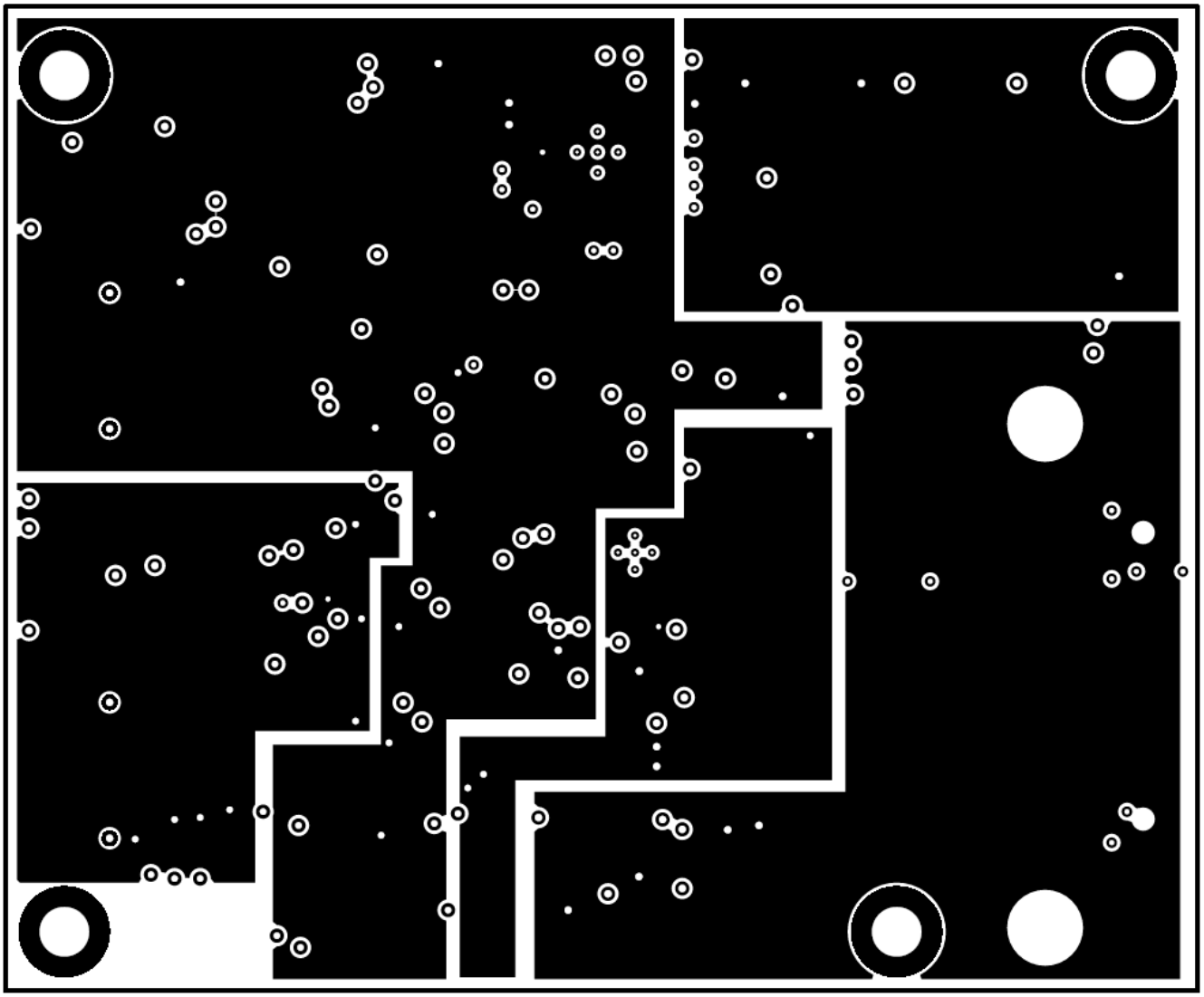

Figure 7-5. ADS9110EVM PCB Layer 3: Power Planes

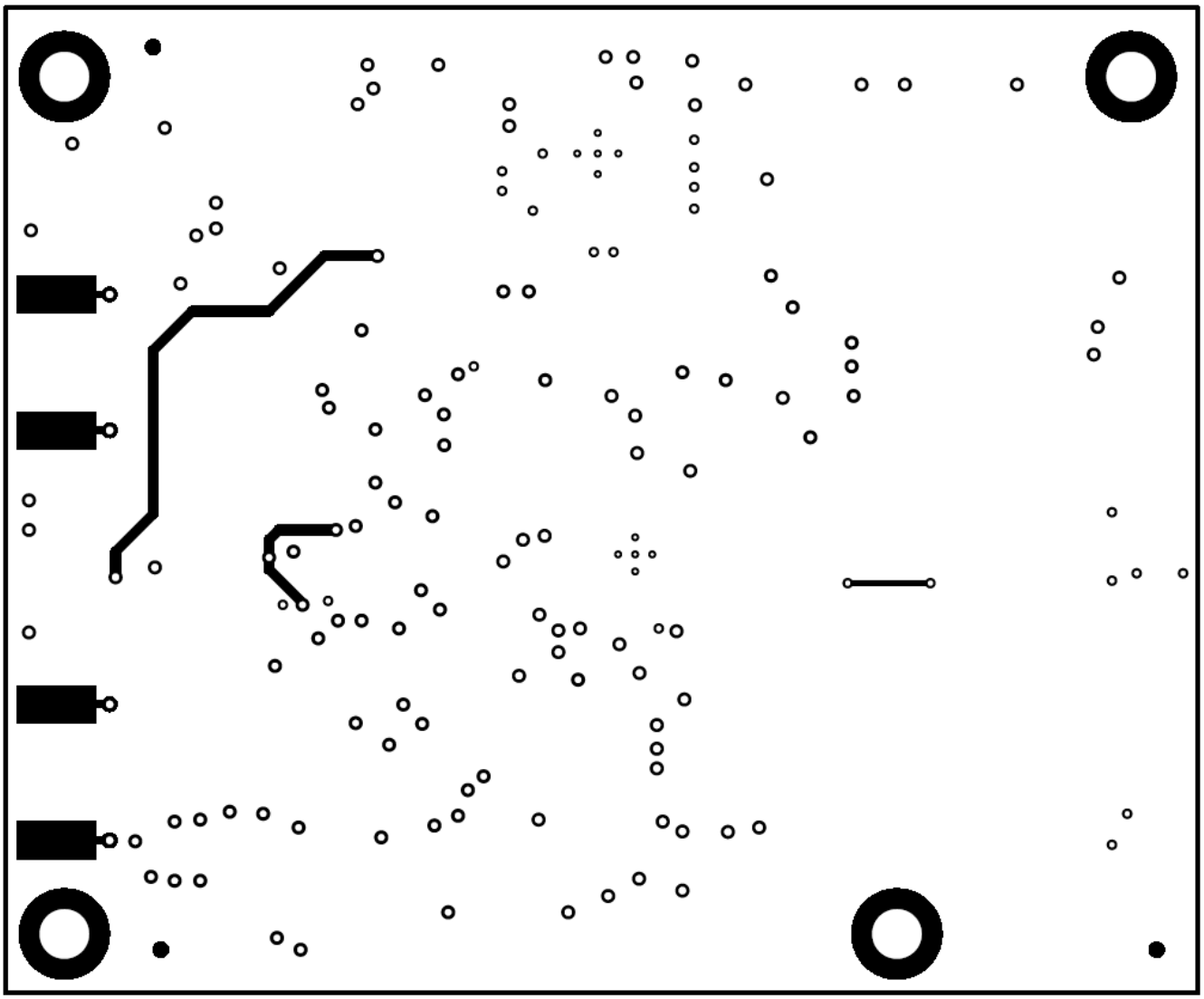

Figure 7-6. ADS9110EVM PCB Layer 4: Bottom Layer

7.3 Bill of Materials

Table 7-1 lists the ADS9110EVM BOM.

Table 7-1. ADS9110EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C3	2	47uF	CAP, CERM, 47µF, 25V, +/- 20%, X5R, 1206	1206	C3216X5R1E476M160AC	TDK
C2, C5, C6, C8, C12, C32, C38, C40, C43	9	1uF	CAP, CERM, 1µF, 25V, +/- 10%, X7R, 0603	0603	GRM188R71E105KA12D	MuRata
C4, C21, C26, C41, C44, C48	6	10uF	CAP, CERM, 10µF, 10V, +/- 10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata
C7, C9, C10, C17	4	0.1uF	CAP, CERM, 0.1µF, 25V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C13, C15, C27, C28, C29, C39, C45, C50, C51	9	10uF	CAP, CERM, 10µF, 10V, +/- 10%, X7T, 0603	0603	ZRB18AD71A106KE01L	MuRata
C16, C31, C42	3	1000pF	CAP, CERM, 1000pF, 50V, +/- 1%, C0G/NP0, 0603	0603	GRM1885C1H102FA01J	MuRata
C18	1	10pF	CAP, CERM, 10pF, 50V, +/- 1%, C0G/NP0, 0603	0603	C0603C100F5GAC7867	Kemet
C19	1	0.22uF	CAP, CERM, 0.22µF, 25V, +/- 5%, X7R, 0603	0603	C0603C224J3RAC7867	Kemet
C34, C35, C37	3	0.01uF	CAP, CERM, 0.01µF, 100V, +/- 1%, C0G/NP0, 0805	0805	C0805C103F1GACTU	Kemet
C47, C49	2	0.1uF	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata
D1	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D2	1	40V	Diode, Schottky, 40V, 0.5A, SOD-323	SOD-323	CUS05S40,H3F	Toshiba
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40		PMSSS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		3/16 Hex Female Standoff		1891	Keystone
H9, H10	2		ROUND STANDOFF M3 STEEL 5MM		9774050360R	Wurth Elektronik
H14, H15	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
J1, J2	2		Header, 2.54mm, 2x1, Gold, R/A, SMT		87898-0204	Molex
J3, J7	2		Connector, End launch SMA, 50 ohm, SMT		142-0701-801	Johnson
J4, J6, J8	3		Header, 100mil, 3x1, Gold, SMT		TSM-103-01-L-SV	Samtec
J5	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT		QTH-030-01-L-D-A	Samtec
R1	1	280k	RES, 280 k, 0.1%, 0.125 W, 0805	0805	RG2012P-2803-B-T5	Susumu Co Ltd
R2	1	0.1	RES, 0.1, 1%, 0.1 W, 0603	0603	ERJ-3RSFR10V	Panasonic
R5	1	10.0k	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-103-B-T5	Susumu Co Ltd
R6, R23, R65	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R7, R11, R12, R32, R34, R35, R37, R40, R42, R43, R46, R47, R49, R51, R53, R63, R64	17	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R8, R58	2	0.22	RES, 0.22, 1%, 0.1 W, 0603	0603	ERJ-3RQFR22V	Panasonic
R10, R15, R20	3	20.0k	RES, 20.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-203-B-T5	Susumu Co Ltd
R16, R29, R41, R45, R54, R55	6	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RG1608P-102-B-T5	Susumu Co Ltd

Table 7-1. ADS9110EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R17	1	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603	RG1608P-4991-B-T5	Susumu Co Ltd
R19, R24, R57, R59, R60	5	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
R21, R30	2	499	RES, 499, 0.1%, 0.1 W, 0603	0603	RG1608P-4990-B-T5	Susumu Co Ltd
R22	1	2.49k	RES, 2.49 k, 0.1%, 0.1 W, 0603	0603	RG1608P-2491-B-T5	Susumu Co Ltd
R27	1	30.0k	RES, 30.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-303-B-T5	Susumu Co Ltd
R31	1	4.75	RES, 4.75, 1%, 0.1 W, 0603	0603	CRCW06034R75FKEA	Vishay-Dale
R38, R44	2	100	RES, 100, 0.1%, 0.1 W, 0603	0603	RG1608P-101-B-T5	Susumu Co Ltd
R48, R50	2	2.21	RES, 2.21, 1%, 0.1 W, 0603	0603	CRCW06032R21FKEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3		Shunt, 100mil, Gold plated, Black		881545-2	TE Connectivity
TP1, TP2, TP3, TP4, TP5	5	SMT	Test Point, Compact, SMT		5016	Keystone
TP6, TP7	2	SMT	Test Point, Miniature, SMT		5015	Keystone
U1	1		Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin VSSOP (DGK), Green (RoHS & no Sb/Br)	DGK0008A	REF5050AIDGKT	Texas Instruments
U2	1		36V, 1A, 4.17µVRMS, RF LDO Voltage Regulator, RGW0020A	RGW0020A	TPS7A4700RGW	Texas Instruments
U3	1		Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim Series, DBV0005A	DBV0005A	OPA376AIDBVR	Texas Instruments
U5	1		Low-Noise, 900kHz, RRIO, Precision Operational Amplifier, Zerø-Drift Series, 2.2 to 5.5V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)	DBV0005A	OPA378AIDBVT	Texas Instruments
U6, U9, U10	3		High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers, DBV0006A	DBV0006A	OPA625IDBVR	Texas Instruments
U8	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U11	1		18-Bit, 2-MSPS, 20-mW, SAR ADC with Enhanced Serial Interface, RGE0024H	RGE0024H	ADS9110IRGER	Texas Instruments
C11	0	4.7uF	CAP, CERM, 4.7µF, 16V, +/- 10%, X5R, 0805	0805	EMK212BJ475KG-T	Taiyo Yuden
C14, C24, C52, C53	0	10uF	CAP, CERM, 10µF, 10V, +/- 10%, X7T, 0603	0603	ZRB18AD71A106KE01L	MuRata
C20, C55, C57	0	22uF	CAP, CERM, 22µF, 10V, +/- 20%, X7S, 0805	0805	C2012X7S1A226M125AC	TDK
C22	0	1uF	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
C23	0	10uF	CAP, CERM, 10µF, 10V, +/- 10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata
C25	0	10uF	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata
C30	0	0.1uF	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata
C33	0	47uF	CAP, CERM, 47µF, 10V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C36	0	1uF	CAP, CERM, 1µF, 25V, +/- 10%, X7R, 0603	0603	GRM188R71E105KA12D	MuRata
C54	0	0.22uF	CAP, CERM, 0.22µF, 25V, +/- 5%, X7R, 0603	0603	C0603C224J3RAC7867	Kemet
C56	0	0.47uF	CAP, CERM, 0.47µF, 35V, +/- 10%, X5R, 0805	0805	GMK212BJ474KG-T	Taiyo Yuden

Table 7-1. ADS9110EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H12	0		CABLE USB A MALE-B MICRO MALE 1M (Kit Item)	USB Cable	102-1092-BL-00100	CNC Tech
R3, R4, R9, R13, R14, R18, R52, R61, R62	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R25, R26	0	0.22	RES, 0.22 ohm, 1%, 0.1W, 0603	0603	ERJ-3RQFR22V	Panasonic
R28	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R33	0	1.00	RES, 1.00, 1%, 0.1 W, 0603	0603	RC0603FR-071RL	Yageo America
R36, R39	0	0.22	RES, 0.22, 1%, 0.1 W, 0603	0603	ERJ-3RQFR22V	Panasonic
R56	0	4.7	RES, 4.7, 5%, 0.125 W, 0805	0805	ERJ-6GEYJ4R7V	Panasonic
U4	0		Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free	MUA08A	LM7705MM/NOPB	Texas Instruments
U7	0		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A	DGK0008A	REF6025AIDGK	Texas Instruments

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 7, 2015 to January 30, 2025 (from Revision * (October 2015) to Revision A (July 2025))	Page
• Updated schematics	24
• Updated *Bill of Materials* table	30

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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