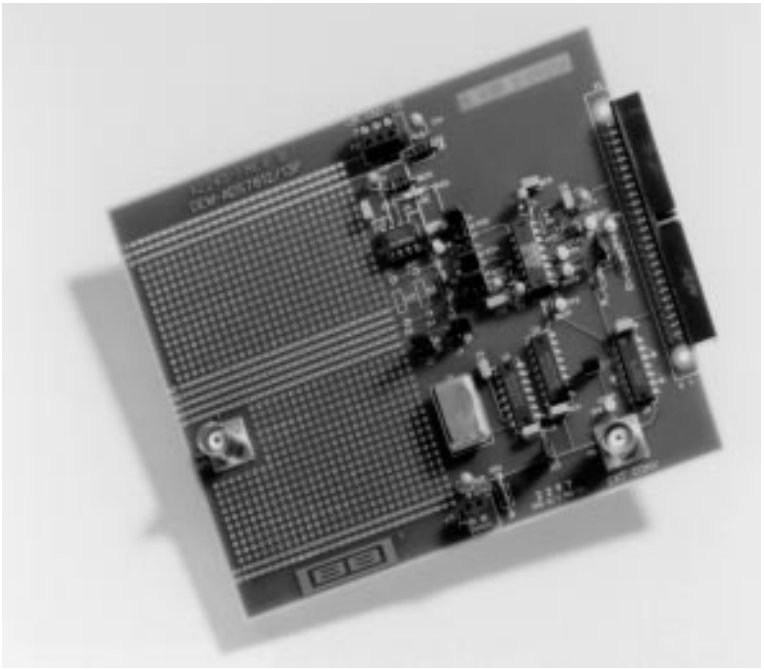
BURR-BROWN®

DEM-ADS7812/13P
EVALUATION FIXTURE



FEATURES

- COMPUTER INTERFACE
- STAND-ALONE CAPABILITY
- BREADBOARD AREAS
- INPUT RANGE EASILY CONFIGURED FOR APPLICATION

APPLICATIONS

- TRANSDUCER INTERFACE
- MULTIPLEXED DAS

DESCRIPTION

The DEM-ADS7812/13P evaluation fixture is designed for quick evaluation of Burr-Brown's ADS7812 and ADS7813. Breadboard areas are provided with optional bipolar power supply connections to assist in the evaluation of various driver amplifiers or multiplexed input circuits to the input of the analog-to-digital converter. Additionally, the demonstration fixture has flexibility in its clocking circuit to allow for various fixed conversion rates. To further enhance the clocking network, an external off board clock can be connected through the BNC connector, P5. The DEM-ADS7812/13P has been designed to accommodate stand-alone operation.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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GETTING STARTED

The user must provide power to the analog input portion of the board as well as power to the DUT and digital network. P3 should be powered with ±15V which provides power to U1. P4 should be powered with +5V, which provides power to the DUT (X1), and digital network, U2, U3, U4, U5, and U6. The ground connection of both power connectors are tied together with the ground plane of the board. The factory set position of the jumpers are shown below.

J1 = not installed
J2 = A
J3, J4, J8, J12, J14 = open
J5 = A
J6 = C
J7 = B
J10, J13 = installed
J9, J15 = short

DEM-ADS7812/13P BOARD DESCRIPTION

All of the jumper functions for the DEM-ADS7812/13P are shown in Table I. These jumpers affect the circuit's analog front end, clocking circuit, and the shut down enhancement circuit.

JUMPER NAME	JUMPER FUNCTION
J1, J2	Used to configure the input analog source to the driver amplifier (U1). See Table III.
J3, J4	Solderable power supply options for the driver amplifier, U1.
J5, J6, J7	Used to configure the analog input range of the A/D converter (DUT). See Table II.
J8, J9, J14, J15	Solderable connection options to enhance the shut down capability of the A/D converter (DUT).
J10, J13	Used to configure the clock generation circuit. See Table IV.
J12	Determines serial clock source for serial I/O.

TABLE I. Description of Jumpers on DEM-ADS7812/13P Demonstration Fixture.

ANALOG INPUT CONFIGURATIONS

Input Range: J5, J6, J7—The input range of the A/D converter is configured using J5, J6, and J7. In general, all positions that are labeled "A" will connect the corresponding input pin of the A/D converter to the analog input. All positions that are labeled "B" of jumpers J5, J6, and J7 will connect the corresponding input pin of the A/D converter to "GND". Finally, all positions that are labeled "C" will connect the corresponding input pin of the A/D converter to "BUF". A quick look-up table for the more common analog input ranges is shown in Table II. A complete list is given in Table IV of either the ADS7812 or the ADS7813 data sheet.

Analog Input Driver Amplifier : J1, J2, J3, J4—J1 and J2 can be used to configure the on board amplifier in an inverting or non-inverting gain. The values of R_3, R_4, R_5, and C_{17} are interchangeable by using the sockets provided, E1 through E8. J3 and J4 are jumpers that can be shorted with solder to allow for alternative power supply configurations for the amplifier. All of these jumpers and components allow for a variety of configurations for the front-end analog driving amplifier.

ANALOG INPUT RANGE	CONNECT $R_{1\,IN}$ TO	CONNECT $R_{2\,IN}$ TO	CONNECT $R_{3\,IN}$ TO	A/D INPUT IMPEDANCE (Ω)
±10V	J5-A (V_{IN})	J6-C (BUF)	J7-B (GND)	45.7k
0.3125 to 2.8125V	J5-A (V_{IN})	J6-A (V_{IN})	J7-A (V_{IN})	> 10M
±5V	J5-B (GND)	J6-C (BUF)	J7-A (V_{IN})	26.7k
0V to 10V	J5-C (BUF)	J6-B (GND)	J7-A (V_{IN})	26.7k
0V to 4V	J5-C (BUF)	J6-A (V_{IN})	J7-B (GND)	21.3k
±3.33V	J5-A (V_{IN})	J6-C (BUF)	J7-A (V_{IN})	21.3k
0.5V to 4.5V	J5-B (GND)	J6-A (V_{IN})	J7-B (GND)	21.3k

TABLE II. These are the Jumper Settings (J5, J6 and J7) for the Most Common Input Ranges to the ADS7812 and ADS7813. Note that all jumper configurations on the DEM-ADS7812/13P board are acceptable. Refer to Table IV of the ADS7812 or ADS7813 product data sheets for more details concerning other input range options. Configured for CIB testing.

The combination of J1, J2, R_3, R_4, and C_{17} are used to configure the front-end amplifier, U1. Figure 1 shows the analog gain options available for this board. The various configurations for this input stage are summarized in Table III. R_5 is used to isolate the output of the amplifier from the input of the A/D converter. The factory setting for R_5 is 0Ω, however, an appropriate value for R_5 could also be 50Ω.

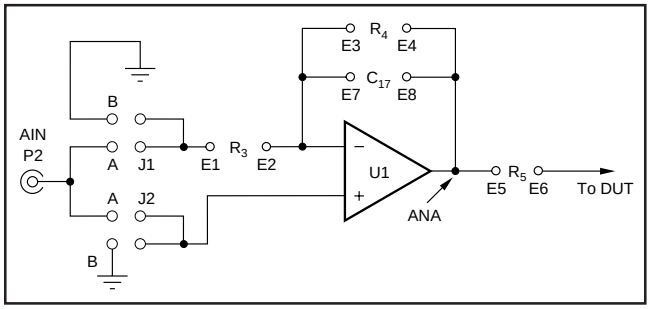

FIGURE 1. The Analog Input Section of the DEM-ADS7812/13P Demonstration Fixture.

	J1	J2	ANALOG GAIN (V/V)
Inverting Configuration	A	B	ANA/AIN = $-R_3/R_4$
Non-inverting Configuration	B	A	ANA/AIN = $1 + R_3/R_4$

TABLE III. The Gain of the Amplifier, U1, can be Configured Negative or Positive with the Above Jumper Settings. R_3, R_4, R_5 and C_{17} can be easily changed by using the low-profile sockets, labeled as E1 - E8.

An input signal can be connected to the circuit using the coax connector, P2 (AIN). The breadboard is also connected to AIN. Additionally, the breadboard ANA bus bypasses the operational amplifier, U1, completely to allow for custom driver circuits to be built on the breadboard.

The power supply to the amplifier, U1, is supplied from a different connector (P3) than the power supply (P4) to the A/D converter, X1 (DUT). This is done to allow for maximum flexibility. In addition, an alternative operational amplifier power supply connection is possible using J3 and J4. These two jumpers, as with J14, J15, J8 and J9 (discussed later) are solder options. In the case with J3 and J4 the amplifier's positive power supply can easily be attached to pins 7 and 8 by connecting the solder switch, J3. The negative supply can be connected to both pins 4 and 5 of the amplifier is desired by connecting the solder switch, J4. This option is useful if the operation amplifier in the U1 socket has an alternative power supply connection with the positive supply connected to pins 7 and 8 and the negative supply connected to pins 4 and 5.

DIGITAL OUTPUT CONFIGURATIONS

Clock Network : J13, J10, P5—The convert command to the A/D converter is provided through one of two paths. The first path is from the EXT CONV connector, (P5) and the second path is from the clock generator network; U2, U3, and U4. The jumper configuration is shown in Table IV. The on board clock generator network divides a 16MHz oscillator signal (U2) to 40kHz at J10. 40kHz is the recommended maximum throughput rate for the ADS7812 and ADS7813. Slower clock signals can be generated by changing the oscillator chip, U2 or by using an external clock source through P5. The AND gate, implemented with U5, insures that the timing between $\overline{BUSY}$ and $\overline{CONV}$ (t_4, per product data sheet) is not violated.

CLOCK OPTION	J10	J13
External Clock (P5)	No Jumper	No Jumper
On Board Clock	Connected	Connected

TABLE IV. Jumper Configuration of Clock Options on the DEM-ADS7812/13P Demonstration Fixture.

External Digital Interface—All critical digital lines are connected to the 25 x 2 pin connector, P1 (see Table V). This connector is designed to interface to Burr-Brown's Computer Interface Board, DEM-CIB. The DEM-CIB and accompanying Windows compatible program allow the performance of the ADS7812 and ADS7813 to be evaluated directly from a PC. If an off board clock provides the synchronous clock for serial I/O, then jumper J12 should be installed (see Table VI).

Additionally, the user of the DEM-ADS7812/13P can use the board in a stand-alone mode, using P1 as the interface connection to a user designed interface.

POWER SAVING FEATURE

The ADS7812 and ADS7813 has a power-down mode that is activated by taking $\overline{CONV}$ LOW and the PWRD HIGH. This will power down all of the analog circuitry including the reference. While in the power-down mode, the capacitors connected to CAP and REF, C_3, C_4, and C_{16}, will begin to discharge. When the power-down mode is exited, these capacitors must be allowed to recharge and settle to a 16-bit level. When the P-Channel, HEXFET Power MOSFET, U6, (IRF7604) is included in the circuit (available on request), the power up time can be significantly reduced. This function is enabled and disabled according to the settings specified in Table VII.

P1 PIN NUMBER	PIN DESCRIPTION
All Even Pins	Ground
39	Power-down mode pin, to X1 (DUT) pin 15
31	$\overline{BUSY}$, connected to X1 (DUT) pin 14
29	$\overline{CS}$ (Chip Select), connected to X1 (DUT) pin 13
25	EXT/$\overline{INT}$ (External or internal DATACLK pin. Selects the source of the synchronous clock for serial data), connected to X1 (DUT) pin 11
23	DATA (Serial data out), connected to X1 (DUT) pin 10
21	DATACLK, connected to X1 (DUT) pin 9
7	CONV (or system clock)

TABLE V. External Digital Interface Connector, P1 Pin Description.

J12	DESCRIPTION
Not installed	DUT EXT/$\overline{INT}$ is LOW. Synchronous clock for serial data is derived from DUT internal conversion clock.
Installed	DUT EXT/$\overline{INT}$ is HIGH. Synchronous clock for serial data is derived from P1-21 external connector.

TABLE VI. Serial Clock Source and the Setting for J12.

DESIRED OPERATION	J8	J9	J14	J15
Unenhanced Power-Down Mode	No Connect	Connected with Solder Switch	No Connect	Connected With Solder Switch
Enhanced Power-Down Mode	Connected with Solder Switch	No Connect	Connected with Solder Switch	No Connect

TABLE VII. Jumper Solder Instructions for Standard Power-Down Operation (unenhanced) and Accelerated Power-Down Operation (enhanced) for the ADS7812 and ADS7813. "No connect" implies there is no solder switch connecting both pads of the jumper. "Connected with solder switch" requires that the user apply enough solder to short both pads of the jumper.

PART IDENTIFIER	QUANTITY	PART NUMBER	DESCRIPTION
X1	1	ADS7813PB	DUT, Low Power, Serial 16-Bit Sampling A/D Converter, Burr-Brown
U1	1	OPA627BP	Precision High-Speed DiFET® Op Amp, Burr-Brown
U6	1	IRF7604	P-Channel, HEXFET Power MOSFET, International Rectifier (Available on Request from Factory)
U5	1	74HC08N(1)	Quad 2-Input, AND Gate, TI
U3	1	74AC11074N(1)	Dual D-Type Flip Flop, TI
U2	1	CTX116-ND(1)	16MHz Oscillator, Digi-Key (CTS)
U4	1	74LS390N(1)	Dual Decade Counter, 4-Bit, TI
R_3	1	RN55C75R0F(1)	Resistor, 75Ω, 0.125Ω, 1%, Metal-film
R_5	1	0.0QBK-ND(1)	Resistor, 0Ω, Yageo (Digi-Key part number)
R_4		—	None Installed
C_{17}		—	None Installed
R_1	1	RN55C1003F(1)	Resistor, 100kΩ, 0.125Ω, 1%, Metal-film
R_2	1	RN55C1002F(1)	Resistor, 10kΩ, 0.125Ω, 1%, Metal-film
C_3, C_7	2	T350A105K035AS(1)	Cap, 1µF, 35V, 10%, Tantalum, Diped/Radial
C_5, C_8, C_{16}	3	CK05BX103K(1)	Cap, 0.01µF, X7R, 100V, 10%, Ceramic
C_1, C_2, C_9 - C_{12}	6	CK05BX104K(1)	Cap, 0.1µF, 50V, 10%, Ceramic X7R, Kemet
C_4, C_5, C_{13} - C_{15}	5	T350B225K025AS(1)	Cap, 2.2µF, 25V, 10%, Tantalum, Dipped/Radial Kemet
P1	1	IDH-50LP-SR3-TG(1)	Robinson Nugent, Right Angle, 25 x 2
P2, P5	2	KC-79-274-M06(1)	Connector BNC, PCB Mount, King
P4	1	31165102(1)	2-Pin Term Block, 3.5mm Centers, RIACON Electronics
P3	1	31165103(1)	3-Pin Term Block, 3.5mm Centers, RIACON Electronics
J5 - J7	3	TSW-103-07-T-D(1)	Jumper, SAMTEC, 2 x 3 Terminal Strip
J1 - J2	2	TSW-102-07-T-D(1)	Jumper, SAMTEC, 2 x 2 Terminal Strip
J10, J12, J13	3	TSW-101-07-T-D(1)	Jumper, SAMTEC, 2 x 1 Terminal Strip
TP1 - TP6, TP8	7	HD411-2	Test Point, 0.125 Pad, 0.093 Drill, USECO 1280B
X1 Socket	1	AG-516-11-DES	DUT Socket, 16-Pin DIP, Augat
U1 Socket	1	AG-508-11-DES	Op Amp Socket, 8-pin DIP, Augat
U2 Socket	1	1107741	Aries, 14-pin Oscillator Socket
E1 - E8	8	AMP50863-5	“E” Point 0.062 Drill, Resistor Sockets, Augat, Hotlite Socket .0
RB1, RB2, RB3, RB4, RB5	5	90F1533	Rubber Feet, Newark
J1, J2, J5 - J7, J10, J12, J13 Tops	8	SNT-100-BK-T-H	Jumper Tops, Samtec
CR3	1	SA5.0AGICT-ND(1)	5.0V Transient Voltage Suppressor, DO-204AC, Digi-Key
CR1, CR2	2	SA15AGICT-ND(1)	15V Transient Voltage Suppressor, DO-204AC, Digi-Key
Bare PC Board	1	A2245	DEM-ADS7812/13P, Burr-Brown
Sample	1	ADS7812P	DUT, Low Power Serial 14-Bit Sampling A/D Converter, Burr-Brown.

NOTE: (1) Substitutions Allowed.

TABLE VIII. Parts List for the DEM-ADS7812/13P.

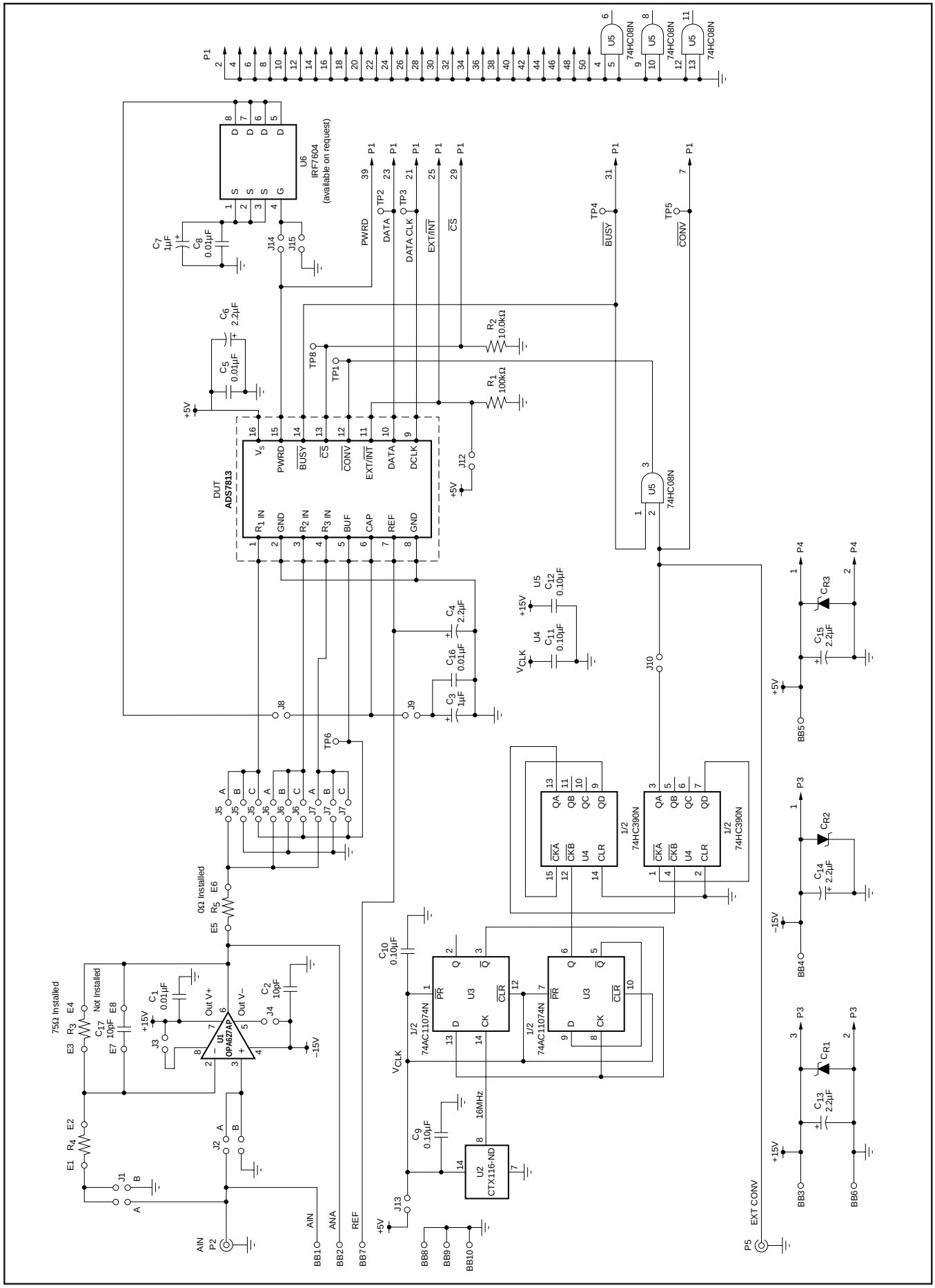

FIGURE 2. Circuit Diagram of the DEM-ADS7812/13P Demonstration Fixture.

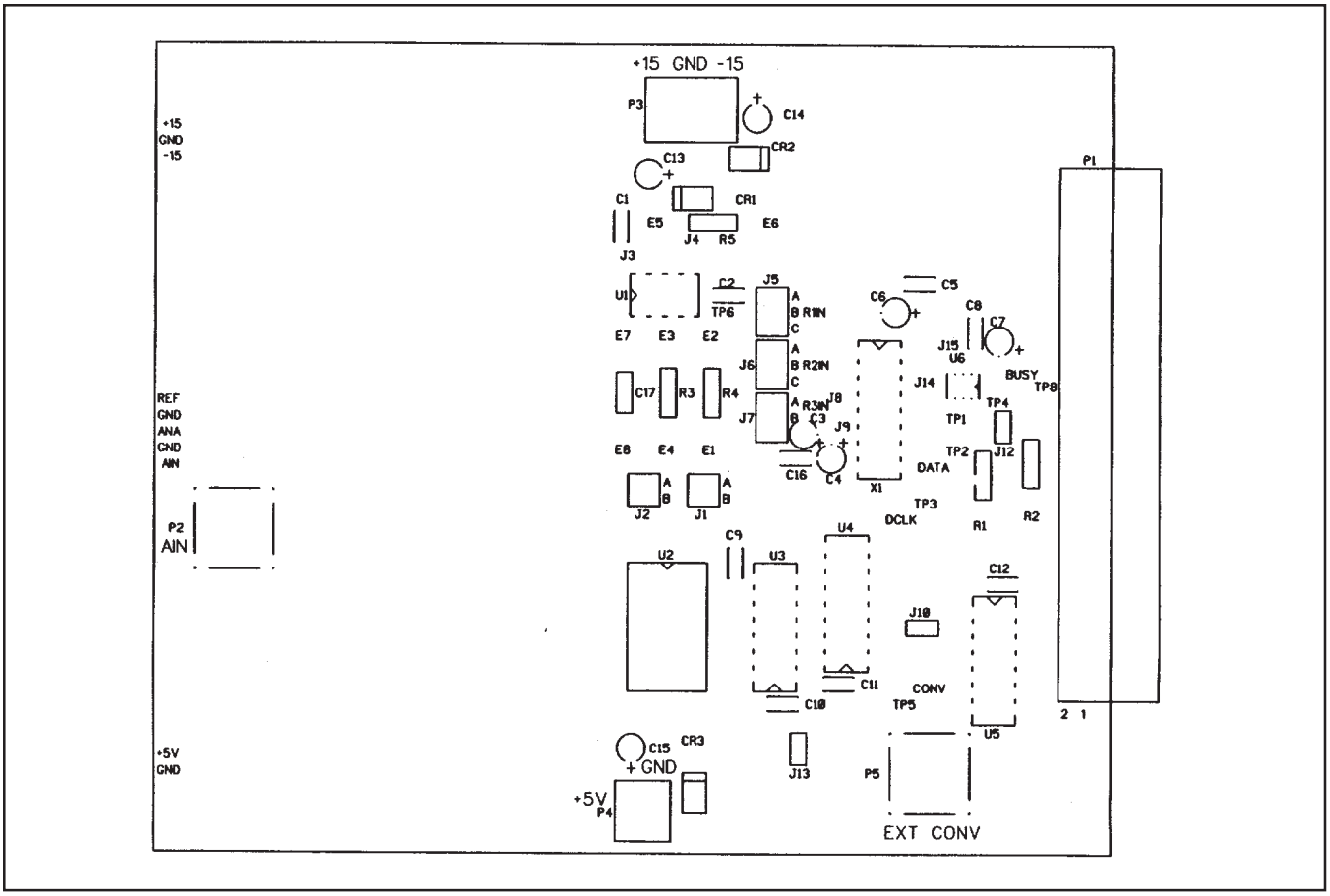

FIGURE 3. Silkscreen of the DEM-ADS7812/13P Demonstration Board.

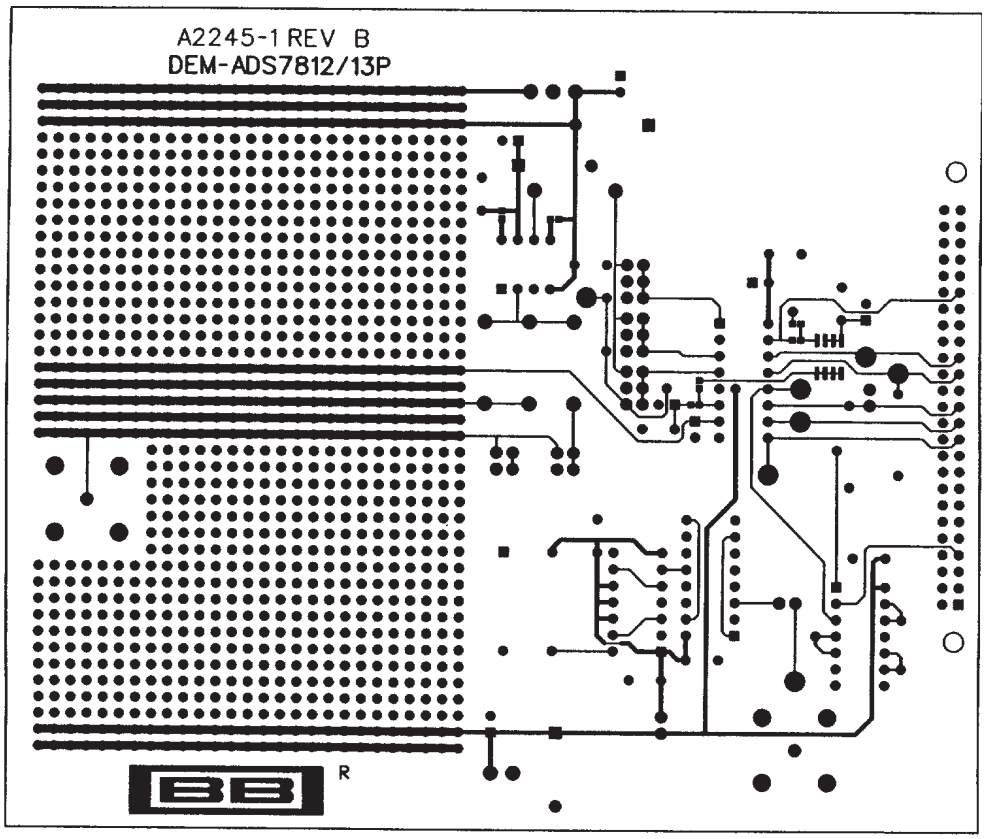

FIGURE 4. Component Side of the DEM-ADS7812/13P Demonstration Board.

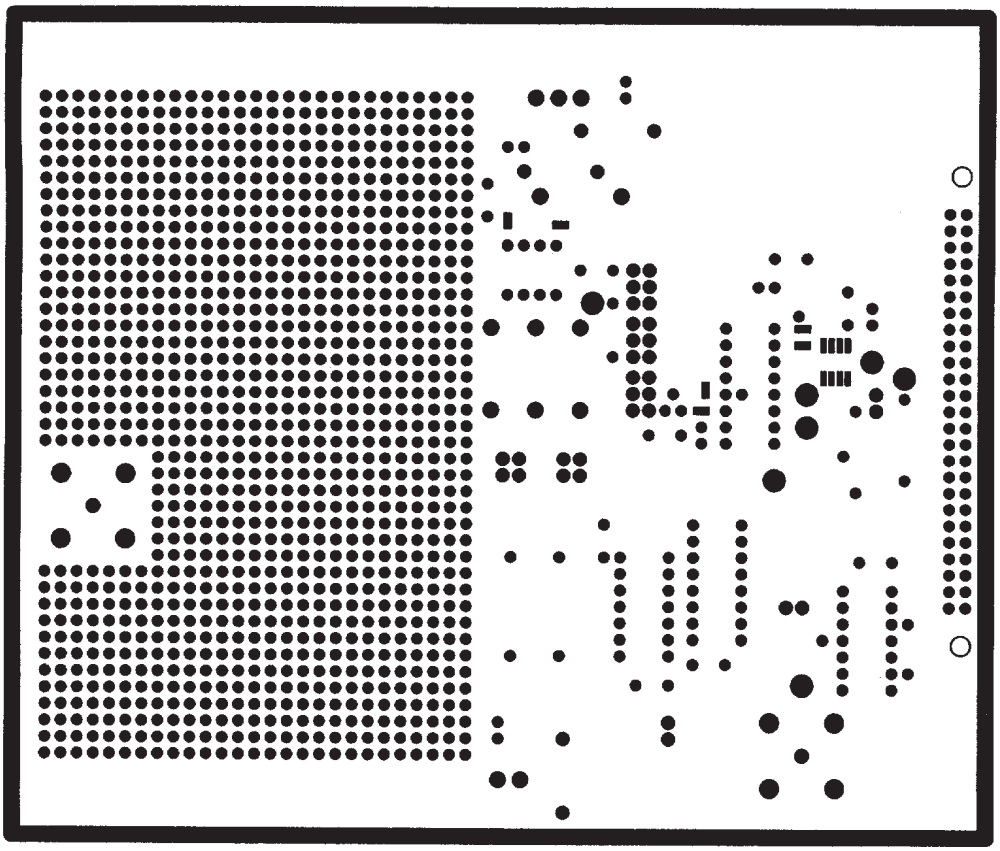

FIGURE 5. Top Soldermask of the DEM-ADS7812/13P Demonstration Board.

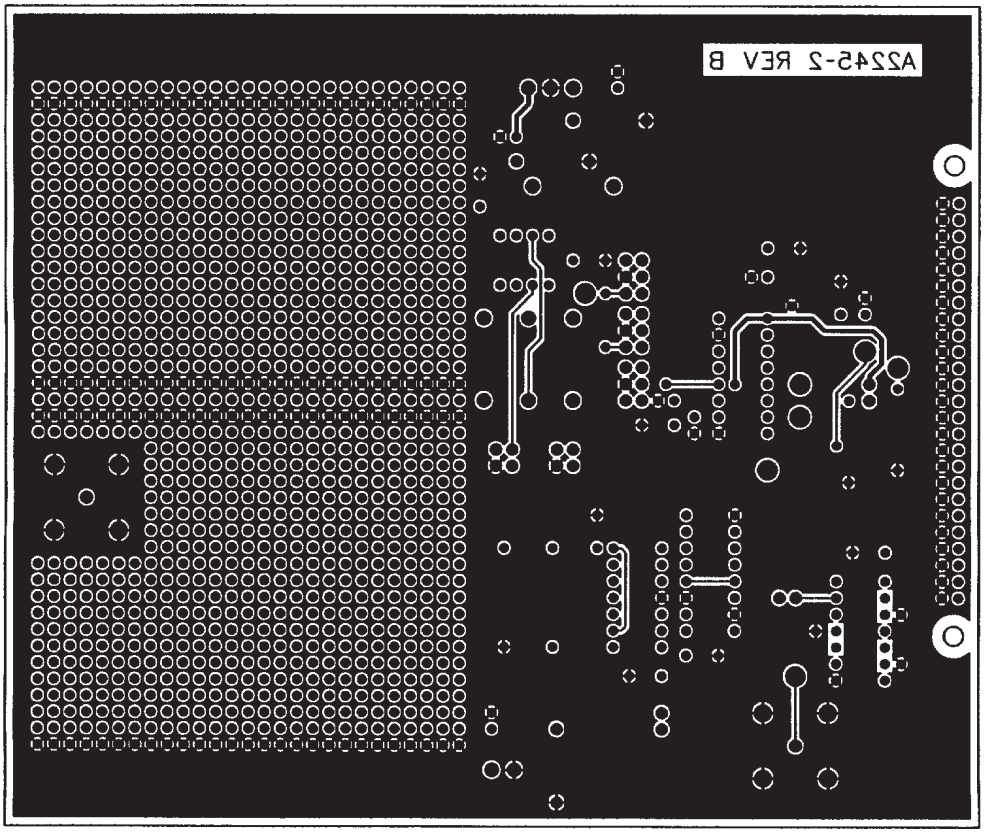

FIGURE 6. Ground Plane of the DEM-ADS7812/13P Demonstration Board.

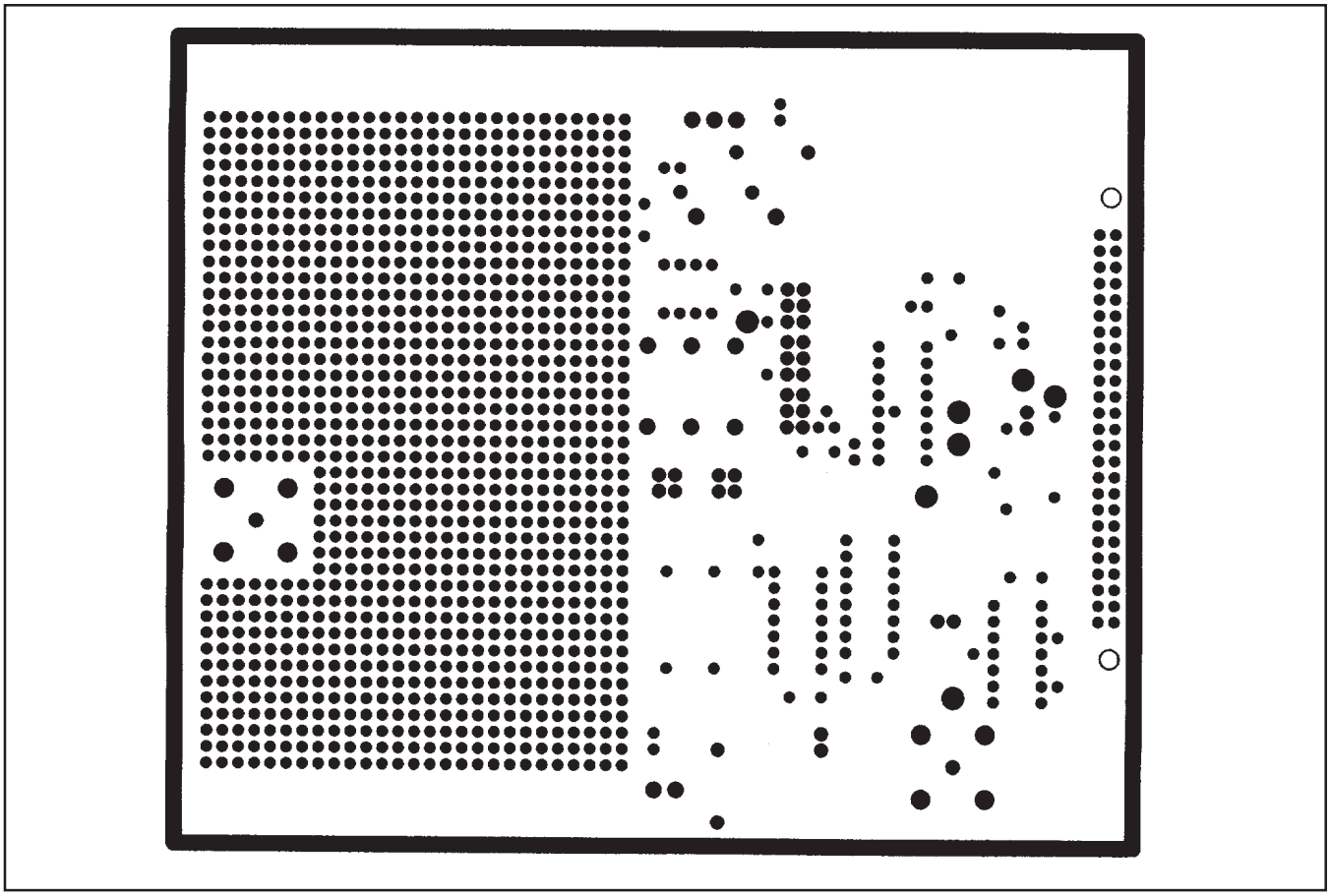

FIGURE 7. Bottom Soldermask of the DEM-ADS7812/13P Demonstration Board.

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