Application Note

The Fine Art of Passive Matching a High-Speed A/D Converter Analog Input Frontend

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ABSTRACT

Understanding the mechanisms involved in designing high speed analog-to-digital converter frontends, is sometimes like an art all in its own. Simply plopping a balun down and drawing two trace lines from the balun's secondary outputs to the ADC's inputs is not something that is recommended in any high-speed analog receiver frontend design. Baluns are notorious for being parasitic sensitive on bandwidth (BW), along with other nuisances. Here in this paper, we reveal a few ways to get the most out of your passive analog input design using a balun. The added benefit, is that you do not need a costly balun nor a costly attenuation pad between the two devices to achieve the BW you are looking for. So sit back, grab a beverage, as we unveil the fine art of tuning for BW and distortion.

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Trademarks

1 The Art of Choosing the Correct Balun or Transformer

Before opening the CAD SW program to start on your PCB layout, we assume you have already decided on both the ADC you plan to use and the BW intended for your application. Now you need to decide, if the passive frontend is right for your design. Assuming again, you do not need to DC couple, that is, sample the DC frequency bin. Because a balun does not require an additional power supply, the benefits of using a balun include lower overall power consumption, and smaller board space requirements. Additionally, with no extra supply to contend with, a balun does not add noise to the overall RF signal chain that leads up to the ADC. This, in turn, means no degradation in SNR (signal-to-noise ratio) or NSD (noise spectral density) can occur.

Once established, a balun must be chosen, and the choices are numerous. When choosing a balun, the suggestion is to first look at your BW requirements. Choose a balun that has a bit more bandwidth than what is required so that the balun acts more like a window than a door. This is especially important at those higher frequency applications. See Figure 1-1. Shown are two different baluns used in the same application with the ADC3669, 16-bit, dual channel ADC. Even though both baluns are rated for the same BW, they can ultimately respond differently due to the combination of the ADC's varying input impedance due to the ADC's internal sample network, as well as the PCB trace parasitics. Notice that with no *match* applied with either balun, the BW falls quite rapidly, as noted in the two points described previously.

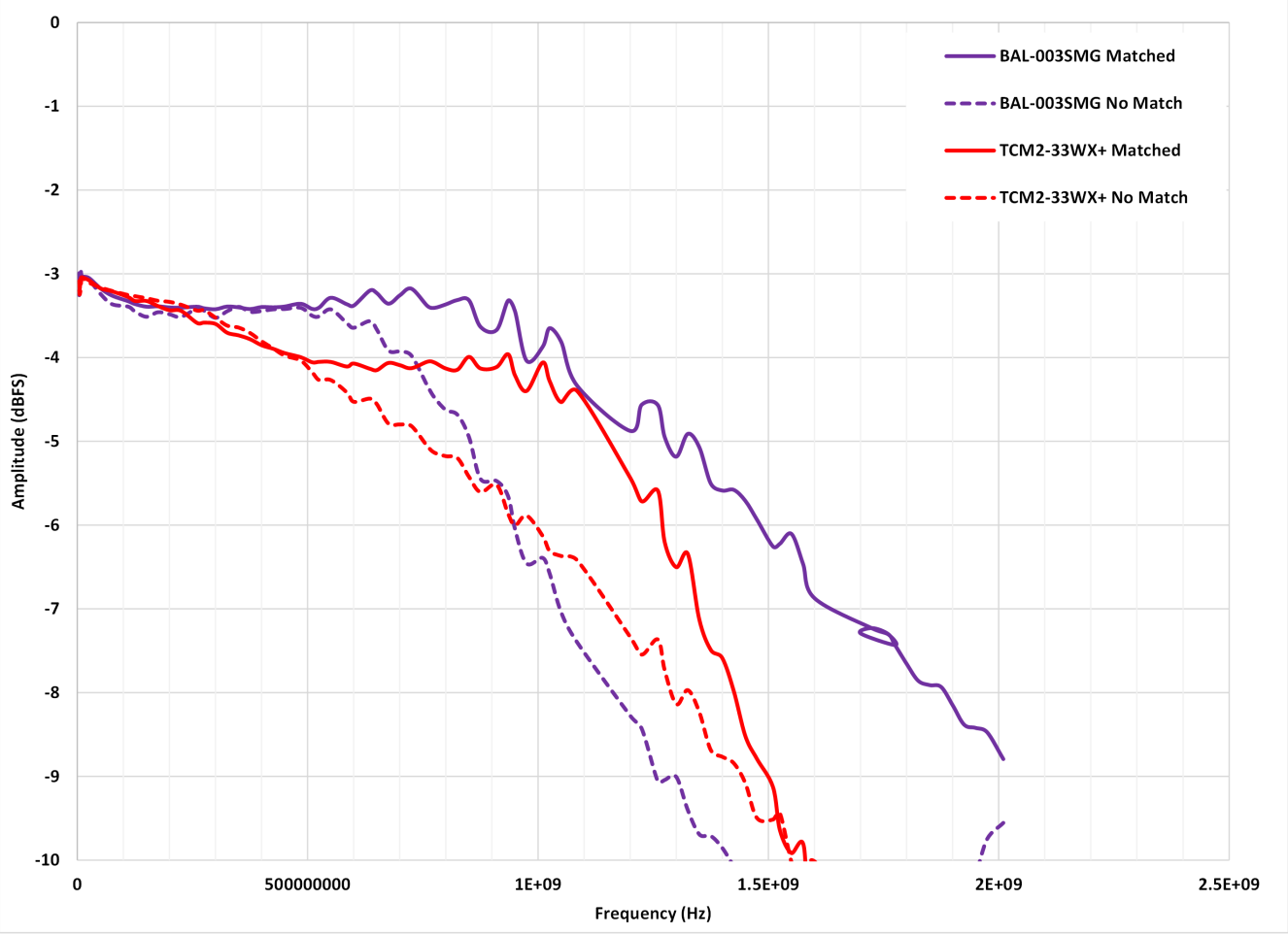

Figure 1-1. ADC3669 and Balun BW Comparison: Match (solid lines) vs. No Match (dashed lines)

A few other nuggets to think about during the balun down-selection process and before you go off and start simulating. Take a close look at the balun's PCB footprint and layout recommendation in the data sheet, there is a reason why it is the way it is. The recommendation is to follow these recommendations exactly, unless you want to inadvertently make the balun respond differently. The balun was characterized using this footprint both for the data sheet collection and measuring the s-parameters, and can only perform up to spec under these

circumstances. Which leads me to another thought, sometimes our balun vendors use the balun test board to measure the s-parameters, and do not de-embed the connectors nor the traces on the test board. So BW beware!

Lastly, start to understand the balun's phase imbalance over your specific BW. The poorer the balun's inherent phase imbalance the worse even order distortion (HD2 or second harmonic distortion) the ADC can manifest. If HD2 is important to your frequency planning application, it is recommended to pick a balun with good phase imbalance. There is really no good guide on this, as each ADC can also have the sensitivity to phase differences across its useable frequency range. Typically choosing a balun that has ≤5degrees of phase imbalance over your application operating BW can be a good start. This can add little to the aggregate even order distortion already existing in your RF signal chain lineup. For more information on balun phase imbalance and its impact to even order distortion, see the reference link. Figure 1-2 shows the difference between the same two matched baluns scenarios again, and impact it has on even order distortion using the ADC3669. Notice the HD3, odd order distortion, or third harmonic response is relatively the same across frequency and has no impacted differences.

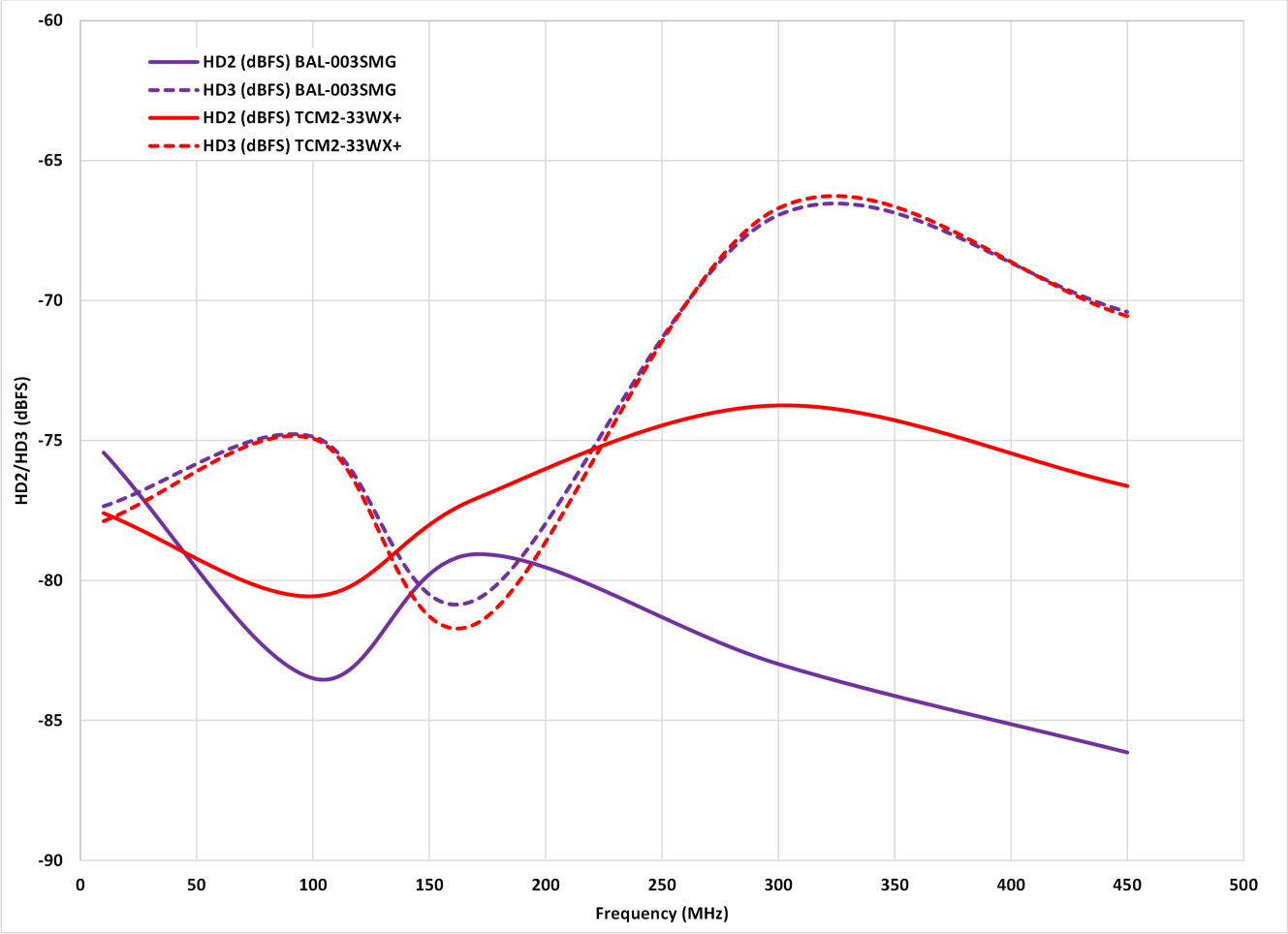

Figure 1-2. ADC3669 HD2/HD3 Comparison between Two Baluns: High Cost vs. Lower Cost

2 The Art of Choosing the Correct Balun Matching Network

Over the years, we have seen many attempts to simulate and get the balun match perfected. After weeks to months of simulation and trying to understand some level of PCB parasitic, the match does not quite work out when the PCB design is fabricated. The recommendation is to start the design process differently, use the following topology as shown in Figure 2-1. This can give you a great *sandbox* to play in using any components you wish to complete the match. Wonder if all of this effort and tradeoffs are actually worth it, the suggestion is to refer back to Figure 1-1. The following section describes each component to know the need or function within the input matching network to the ADC.

C1/C2: typically a 0.1uF, blocks DC from being fed into the balun or transformer. Some balun designs lead to ground and or DC can aggravate the balun's function leading to poor performance. So, that is what they are for, put them in.

R1: allows for back termination near the outputs of the balun after the DC blocking capacitors, not always needed, if your trace lengths are long enough you can need this component. Assuming no perfect match across the band of interest is something that cannot be achieved, you can need to back terminate to handle any standing waves that can accumulate as the imperfect match rolls back and forth across your frequency range.

R2/R3/R4: This allows for various matching techniques to be employed. These three components are the heart of the match and can take the form in several combinations to solve the balun or ADC matching conundrum. For widest band matches these three components generally are configured as a matching pad. This helps to dissolve the standing waves between the balun and ADC providing for a "stiff" 50ohm impedance that is generally needed by both devices. Though these are represented as resistors, these components can take the form of capacitors and or inductors as well.

C3: this capacitor, typically a 0.1uF, ties the center point of the R3s together and allows for an AC current path. This is also a good idea because when over-ranging the ADC's input full scale, this allows for this AC current to go somewhere…you are welcome. Side note: this capacitor can also be located at R5 instead.

R5: allows back termination, on the opposite side near the ADC's inputs, and is again not always necessary. This provides the same function as R1 but from the opposite perspective to help resolve standing waves that can accumulate. Typically, the need for R1 and or R5 are required when trace connections are 300mils in length or more.

R6: these are your kickback components. These are typically in the form of resistors but in some cases inductors or low-Q ferrite beads can help snub any residual charge kickback that comes back onto the analog input network from the internal sampling circuit in the ADC. These component placeholders are essential when using unbuffered ADCs.

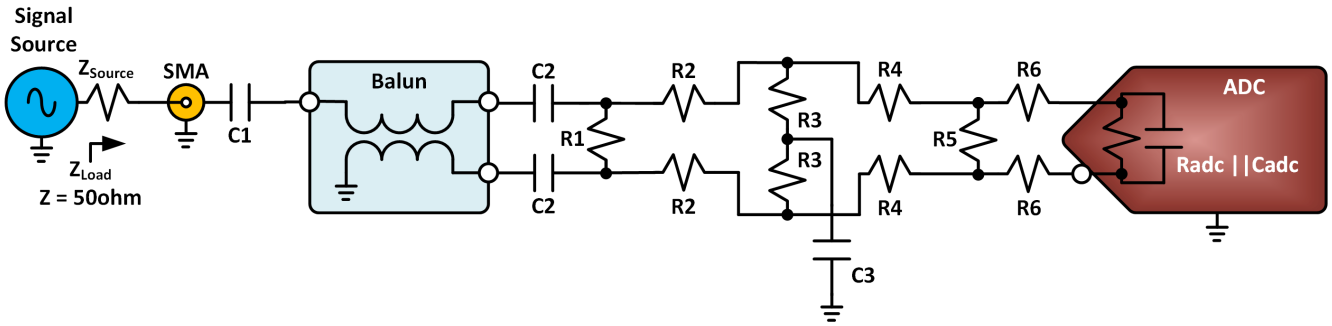

Figure 2-1. Generalize Passive Network Component Placeholders

Again, be weary if you just plan to run two traces from the output of the balun to the inputs of the ADC. Even if you collect s-parameters, simulate, and prove the output out to your colleagues, this can prove to be costly unless you have previous experience with the balun and ADC combo.

3 Example Art Using the ADC3669

Now for an example using a low cost balun and the ADC3669, 16-bit, dual channel ADC, for a wideband frontend match design of 1.5GHz of analog sampling BW.

In this case, we plan to use the TCM2-33WX+ from Mini-Circuits (MC). This balun has 3GHz of BW and a low insertion loss as compared to higher cost baluns that are easier to match with. This MC balun also has a very good phase imbalance, <5degrees, when compared to the other lower cost brethren across the same frequency range. For more details, see link to the MC balun data sheet.

Using the generalized circuit above, the components needed are not purely resistive to define the match. In this case, we can use an R-C-L (R2-R3-R6) approach which proved beneficial in our case, see Figure 3-1.

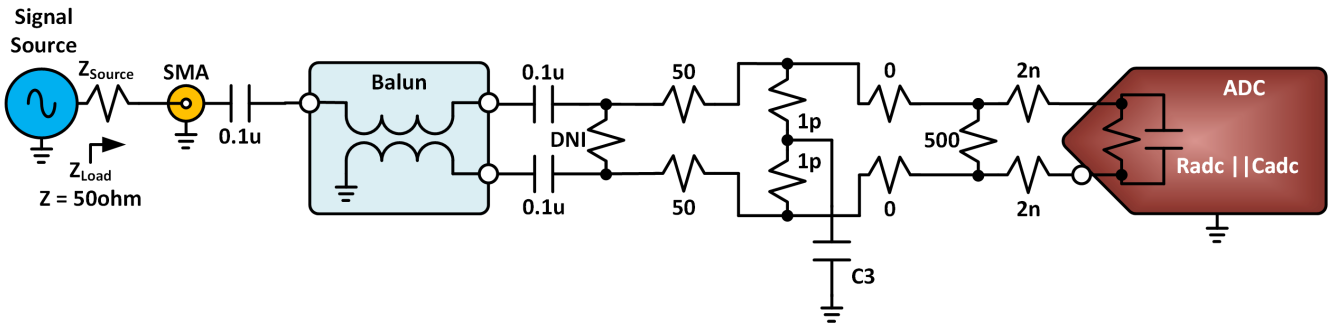

Figure 3-1. Finalized Passive Network Match

Here is where the fine art comes in. How do you approach this balun matching design conundrum? Do I model or simulate this? Some modeling can be done to help give guidance. But to be frank, PCB parasitics still come into play and unless you are a world-class warlord simulating expert, that has unlocked the key to backing out PCB parasitics subtleties, the typical approach is test a few different iterations on your board.

A good starting point is the following, grab both sets of S-parameters, if available, for the balun and ADC and use your favorite simulation SW. Be cautious on vendor s-parameters as noted above. Next, use the matching network format as given in Figure 2-1. Then, use the R2-R3-R4 matching approach for one of the following:

1. Use an attenuation pad approach, something like 8.6-140-8.6 ohms for R2-R3-R4 respectively, can give you a 3dB pad. For more on this approach, see the link.
2. Use an R-C-L approach for R2-R3-R4 respectively. Keep in mind this approach helps to resonate away the ADC's internal parasitic capacitance or "C" using an inductor or "L" as the last component. This can flatten out the BW, allowing the balun to do the rated BW job. However, this approach does take a bit if iteration to get this correct.

As stated above, the goal here was to not use a lossy attenuation pad. Therefore, to give more context to the R-C-L approach, see Figure 3-2, Figure 3-3, and Figure 3-4 as varying the L, C and R respectively in the network (Figure 3-1) and the role in defining the ultimate BW and network match.

Figure 3-2 shows how changing the value of L around has an influence on the BW while keeping all other component values the same. Notice as L is increased in value the BW is slowly reduced. This means the L value is having an adverse reactive effect on the internal C parasitic of the ADC.

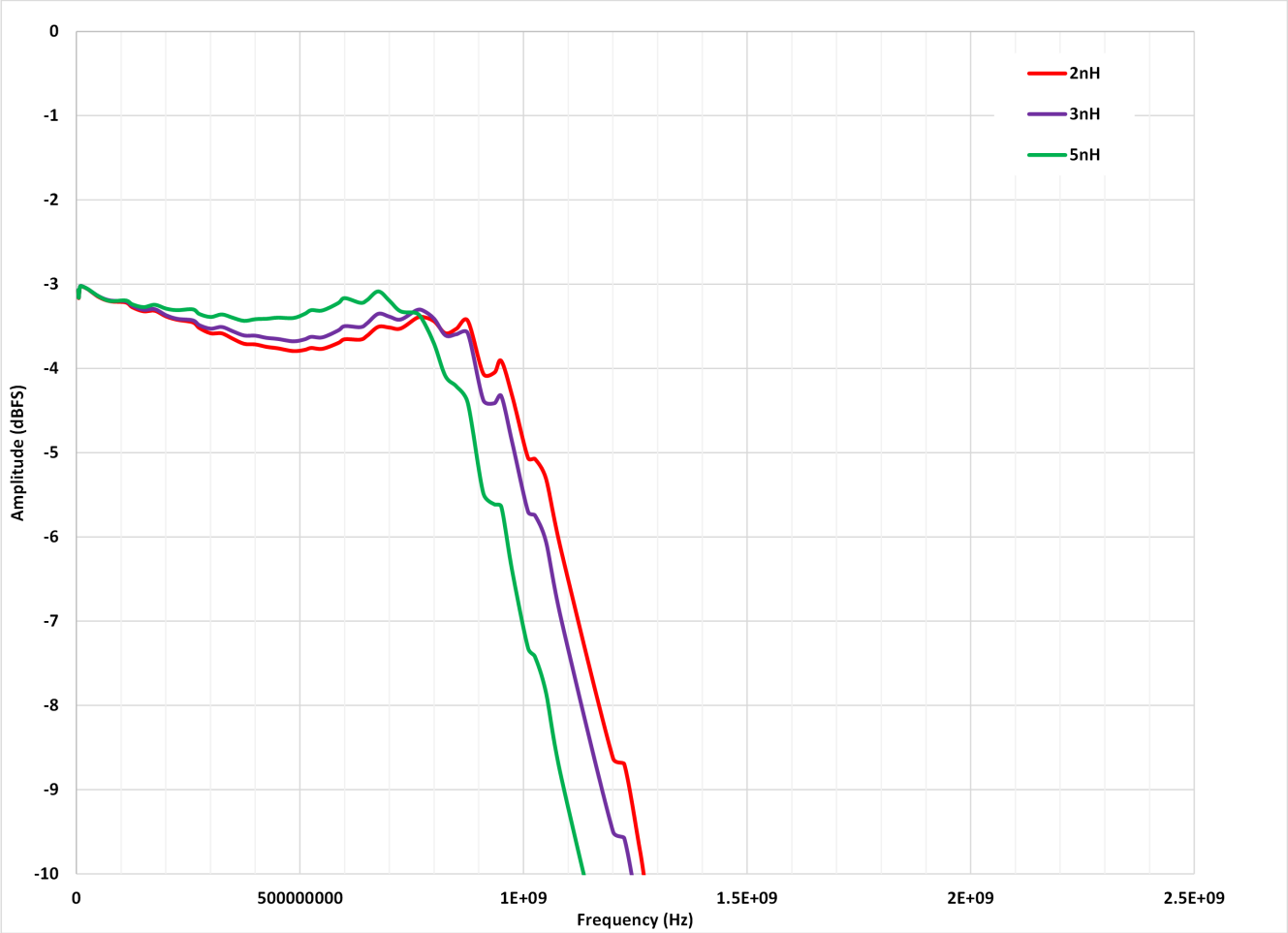

Figure 3-2. Passband Flatness Response with Various Inductance (“L”) Values at R4

In this next experiment, Figure 3-3 shows how moving the value of C around has it influence on the BW while keeping all other component values the same. Notice as C is reduced in value the BW is slowly improving at the cost of flatness of the BW. This means the C value is having a reactive effect on the balun’s return loss over frequency. These capacitors help preserve the balun’s BW vs. frequency.

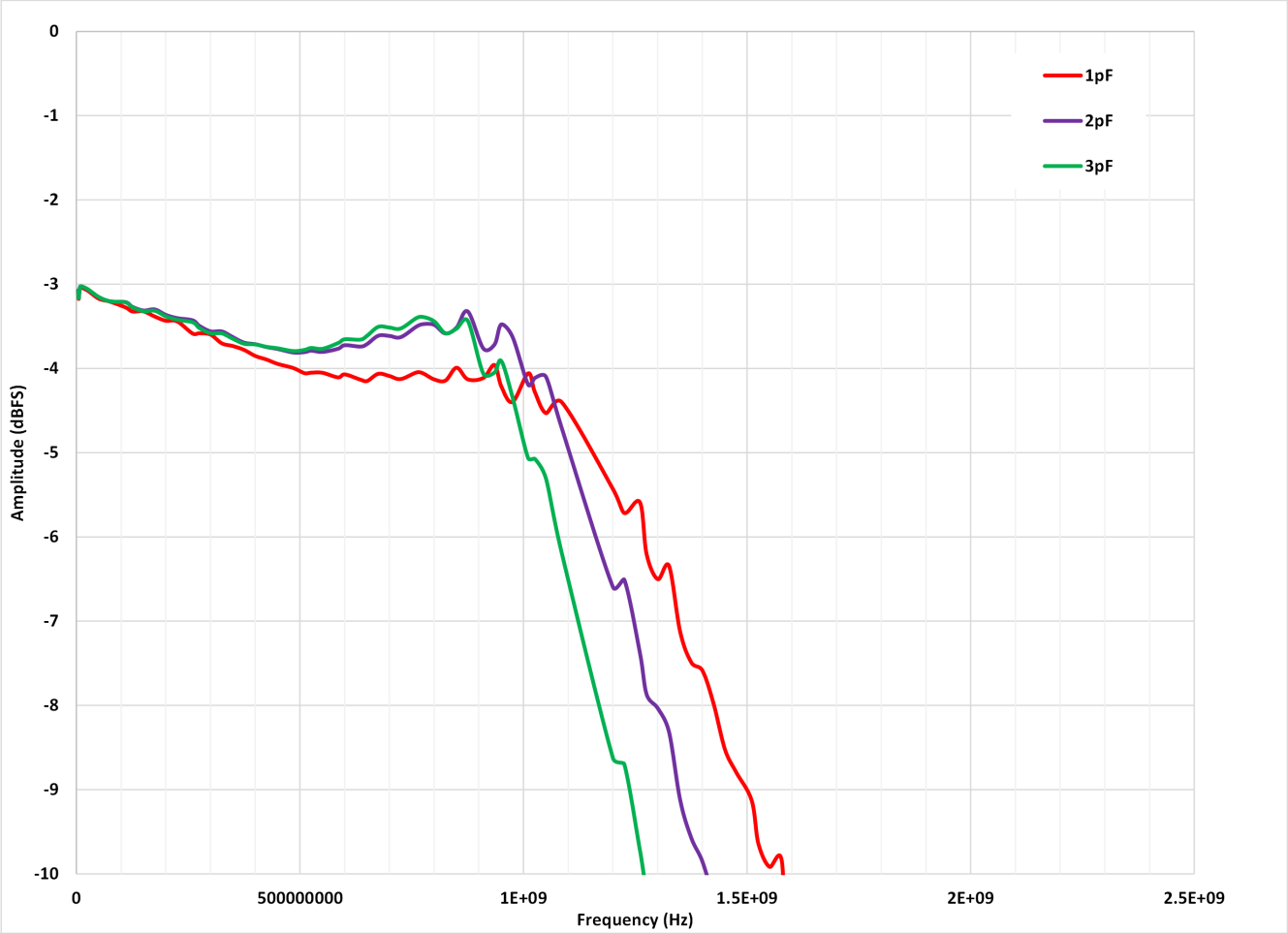

Figure 3-3. Passband Flatness Response with various Capacitance (“C”) Values at R3

In this final experiment, Figure 3-4 shows how moving the value of R around has the influence on the BW while keeping all other component values the same. Notice as R is increased in value the BW is slowly improving at the cost of flatness or peaking in the BW response. The effect of R’s value is almost the same as the effect of L, therefore preserving the impedance requirements that both the balun and ADC want to have in conjunction with each other.

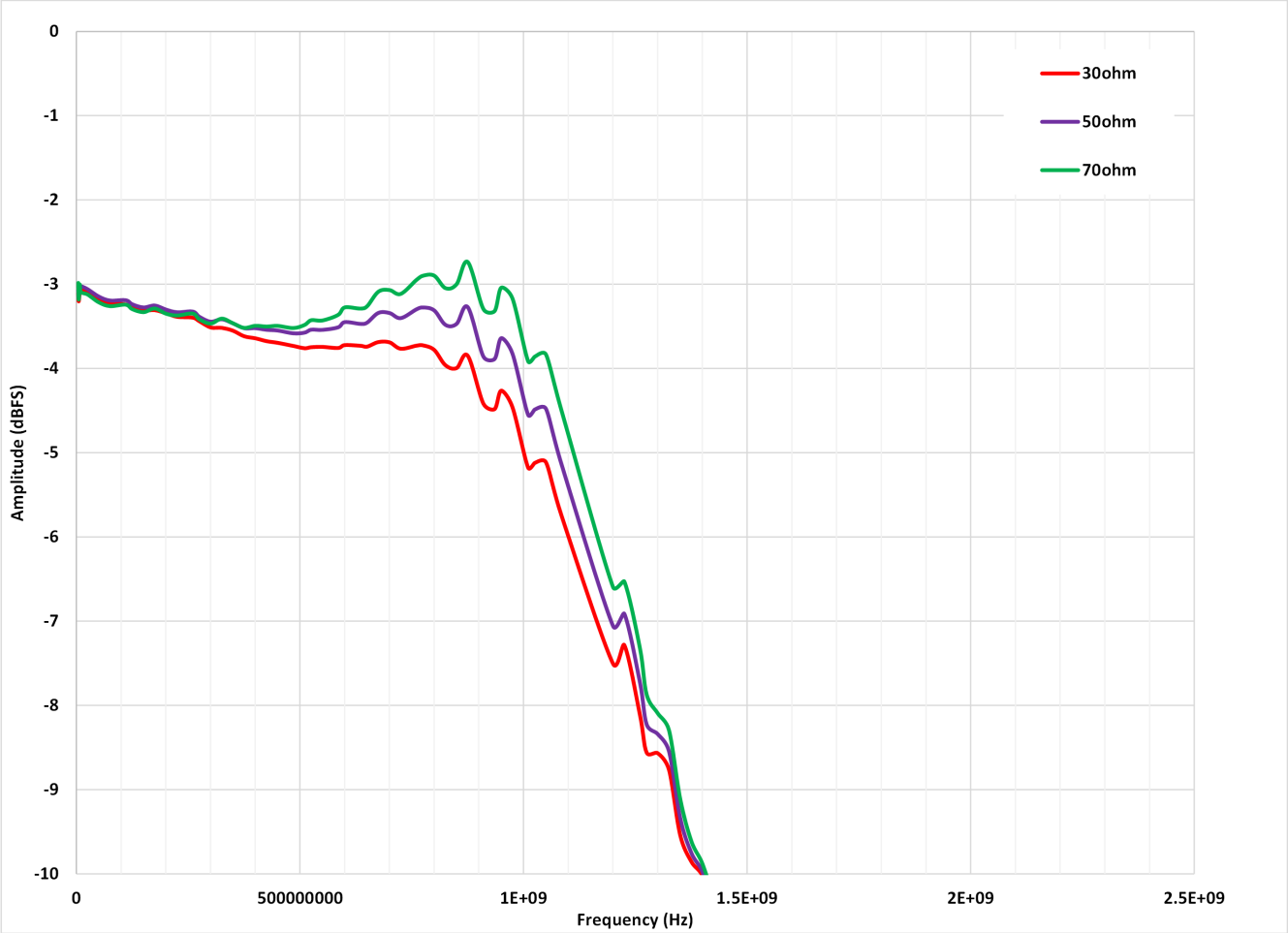

Figure 3-4. Passband Flatness Response with various Resistance (“R”) Values at R2

Ultimately, the R-C-L approach can be simulated as well, to give you a good starting point using the *tune* feature in your favorite simulation package. This does allow you to see the same *roles* each component plays in the network match. Settling on some good starting values can help define which direction to go when iterating and perfecting the match as needed for your application.

Next, during the matching design effort as iterations are made, the recommendation is from time to time to do an AC performance sweep across the application BW of the converter. This can give you insight as to how the performance is coming along dynamically and makes sure nothing has gone wrong with the ADC.

Figure 3-5 describes the ultimate AC performance (SNR and SFDR) measured across the bandwidth of the ADC3669 using this method to match the input network out to 1.5GHz.

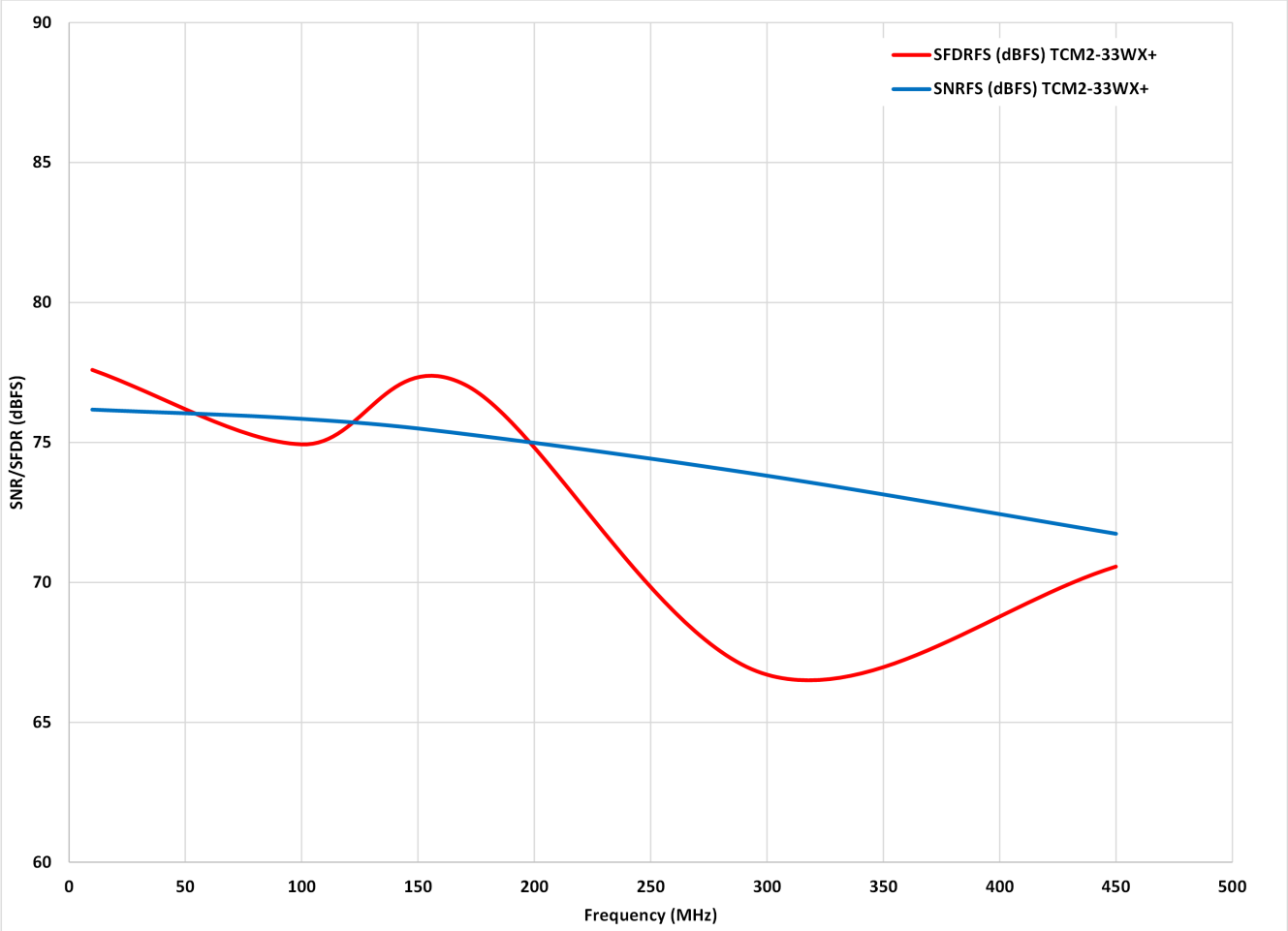

Figure 3-5. Final Matched Network AC Performance (SNR/SFDR) vs. Frequency

Before closing, there is one more match method, a narrow band approach, for those that only need a portion of the BW that the ADC can deliver. If we expand on the listing above, we can call this number 3 or…

- 3. Use a narrow band approach, effectively use the same example network described in Figure 2-1. But instead, use R5 to resonate out the ADC's internal sampling network parasitic capacitance or "C" by placing an inductor or "L" in shunt at R5. This is done by simply taking the frequency center point of the BW in the ADC's S-parameters. Assuming the s-parameter S1P file is in the form of real/imaginary, then you can equate this C value to an L value. Here is an example:

Using the s-parameter file, find the center frequency in the file based on the filter's design center frequency. In this case the 4pF was found at 110MHz center frequency for the narrow band filter design.

In the first step, find the reactive impedance at 4pF and 110MHz:

$$X_C = \frac{1}{(2 \times \pi \times f \times C)} = \frac{1}{(2 \times \pi \times 110M \times 4\text{p})} = 361.7\Omega \quad (1)$$

Next, Equate Xc to XL, as shown in the following equation:

$$X_C = X_L = (2 \times \pi \times \text{f} \times \text{L}) \quad (2)$$

Now solve for L:

$$L = \frac{X_C}{(2 \times \pi \times \text{f})} = \frac{361.7}{(2 \times \pi \times 110\text{M})} = 523nH \quad (3)$$

As shown previously, by equating the two reactive impedance, L is found and can *resonate out* the value of the ADC's internal C value, or in this case, 4pF. This sets the starting point for the value of L to be used. The value can be iterated from there to adjust the frequency a bit if need be to optimize the center point of your narrow bandwidth match.

4 Summary

To summarize, multi-GHz matching networks can be difficult and are not always straight forward. Hopefully this document provides good guidance on where to start as well as some of the pitfalls that can be encountered along the way. Make sure to choose a balun or transformer that is has some BW overage for your particular application. If HD2 is important to your frequency application, make sure to choose a balun with 5degrees or less in phase imbalance. Using the simplified input network above can provide all the initial placeholders that can be required in most matching efforts when using a balun or amplifier and ADC. In the end, you do not need every component listed, but initially these are nice to have, as you cannot capture all board layout and PCB parasitics in simulation. Lastly, understand the iterative tradeoffs that can have an effect on your BW performance. Keep in mind, some of these trades can also affect the linearity performance of the ADC as well. Although there is a lot to digest here, this paper provides the basics steps when approaching a balun and ADC matching network design in the GHz region, which can prevent your next matching effort from being BW hampered.

5 References

- Texas Instruments, *Unraveling the practical mysteries behind RF converter front ends*, seminar.
- Texas Instruments, *ADC3668, ADC3669 Dual-Channel, 16-Bit 250MSPS and 500MSPS Analog-to-Digital Converter (ADC)*, data sheet.

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