Application Note

Impact of Slew Rate on Noise

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ABSTRACT

The input clock slew rate can have a significant impact on the phase noise and signal to noise ratio for PLLs (phased locked loops), buffers, and data converters The best performance is obtained when the input clock slew rate is sufficiently high. This paper explores why this is the case and quantifies how phase noise is related to slew rate, power, and frequency using both a theoretical approached, as well as, measured results.

Table of Contents

Trademarks

1 Flicker Noise, Noise Floor, and Total Noise

When modeling the input stage of clock buffers, PLLs, and data converters, the total noise can be decomposed into flicker noise and noise floor.

1.1 Flicker Noise

The flicker noise (also called 1/f noise) results from an inherent device noise that is correlated from one clock cycle to the next. The characteristic behaviors of this noise are that it scales 20dB/decade with the output (carrier) frequency and decreases 10dB/decade with offset frequency.

$$\mathrm{PN}_{\mathrm{Flicker}}(\mathrm{f}, \mathrm{offset}) \propto 20 \times \log(\mathrm{f}) - 10 \times \log(\mathrm{offset}) \quad (1)$$

1.2 Noise Floor

The noise floor results from inherent device noise that is not correlated from one clock cycle to the next. The characteristic behaviors of this noise are that the noise is flat over offset frequency and scales 10dB/decade with the output frequency.

$$\mathrm{PN}_{\mathrm{NoiseFloor}}(\mathrm{f}) \propto 10 \times \log(\mathrm{f}) \quad (2)$$

1.3 Total Noise

The total noise can be found by adding the flicker noise and noise floor together.

$$\mathrm{PN}_{\mathrm{Total}}(\mathrm{f}, \mathrm{offset}) = 10 \cdot \log[10\text{^}(\mathrm{PN}_{\mathrm{Flicker}}(\mathrm{f}, \mathrm{offset})/10) + 10\text{^}(\mathrm{PN}_{\mathrm{NoiseFloor}}(\mathrm{f})/10)] \quad (3)$$

Note that as the flicker noise and noise floor scale differently with the output frequency, the shape of the total phase noise also changes with carrier frequency. Figure 1-1 shows a sample calculation of the total noise.

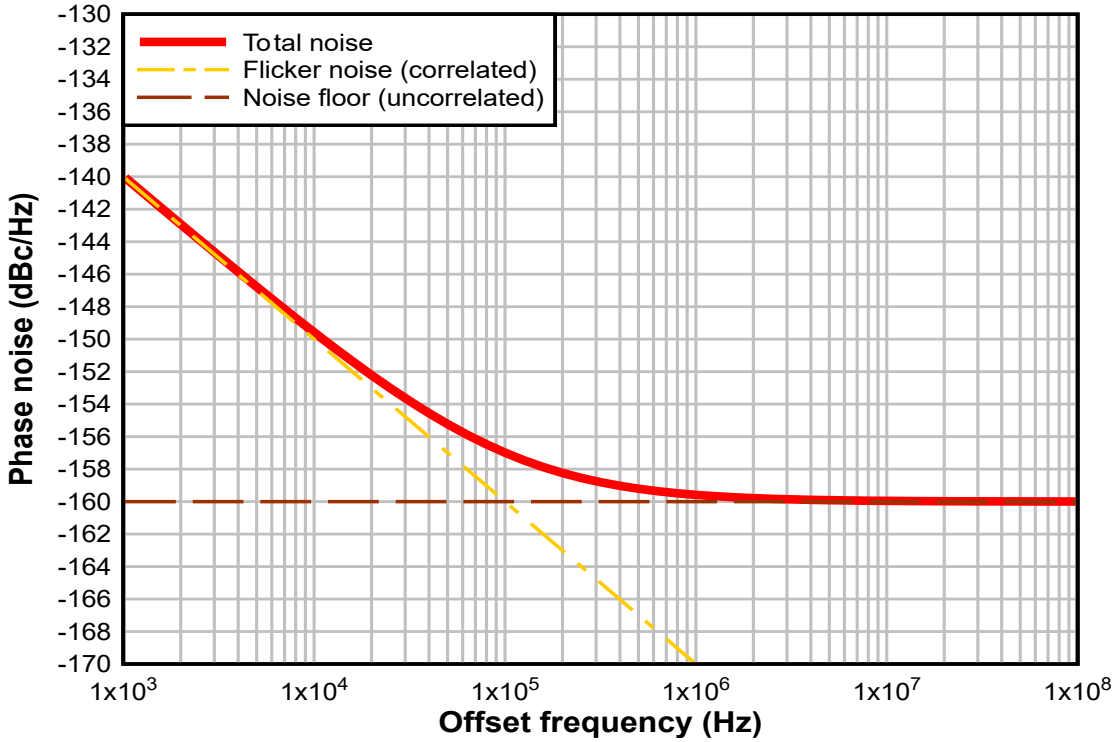

Figure 1-1. Calculation of Total Noise From Flicker Noise and Noise Floor

2 Finding the Slew Rate

2.1 Finding the Slew Rate With an Oscilloscope

The slew rate (SR) can be measured by finding a range near the middle level of the signal and taking the change in voltage (ΔV) divided by the change over a given time (Δt).

$$SR = \frac{dV}{dt} \approx \frac{\Delta V}{\Delta t} \tag{4}$$

This method works well if one the signal looks linear when the signal crosses through the threshold voltage and there is an oscilloscope with sufficient bandwidth to make the measurement.

2.2 Calculating the Slew Rate From Power and Frequency

In the case of the signal being a sine wave, the relationship between slew rate (SR), frequency (f), and power (p) and these calculations are in Section Appendix A: Relating Slew Rate, Power, and Frequency and the key relationship is as follows:

$$SR = \frac{2\pi \cdot f \times 10^{\frac{p}{20}}}{\sqrt{10}} \tag{5}$$

This equation implies that doubling the frequency doubles the slew rate and increasing the power by 6dB also doubles the slew rate and is shown in Figure 2-1.

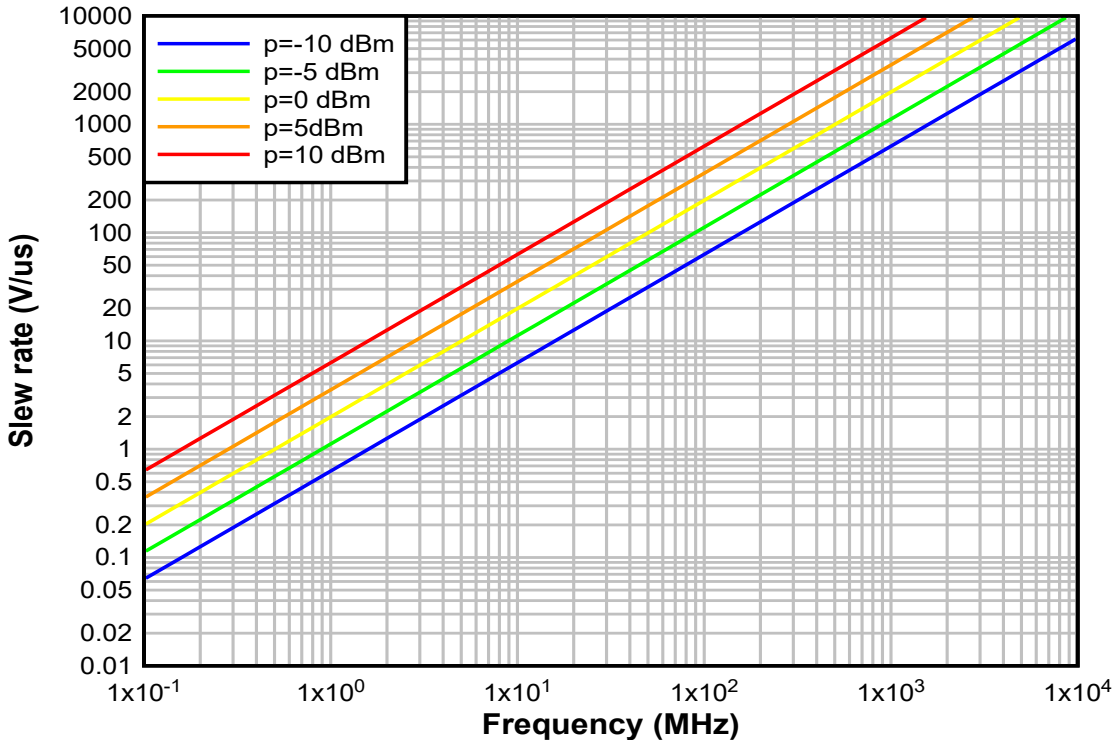

Figure 2-1. Relationship Between Power, Slew Rate, and Frequency for a Sine Wave

3 Impact of Slew Rate on Phase Noise

3.1 Modeling of Input Clock Slew Rate, Inherent Device Noise, and Output Jitter

Understanding the impact of slew rate on phase noise starts with modeling this on a simple buffer as shown in Figure 3-1. This understanding can then be expanded to understand the impact of input clock slew rate for PLLs, data converters, and clock buffers because they all contain an input buffer. The noise modeling starts with the assumption that the input clock has no noise and has some known slew rate. The inherent device noise can be modeled as an rms voltage that adds to the input clock to create an internal resultant signal. The signal then goes through a comparator that squares it up to produce the output signal.

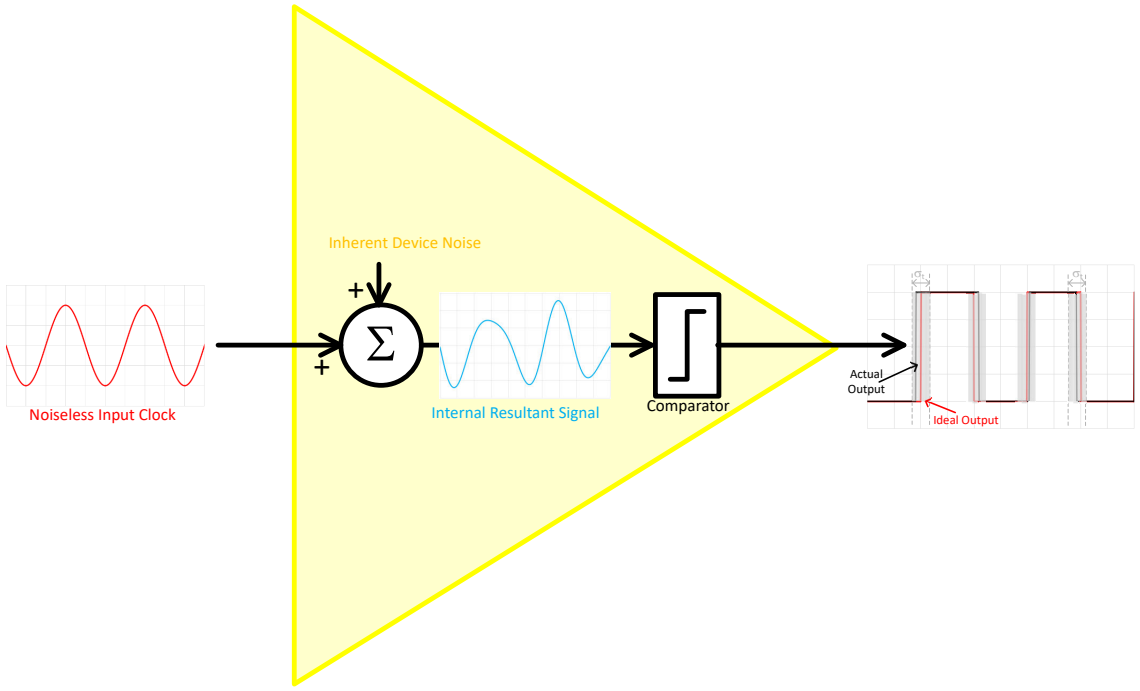

Figure 3-1. Modeling Impact of Slew Rate on Output Jitter

3.2 Slew Rate Impact on Flicker Noise and Noise Floor

The inherent device noise (RMS Voltage Noise) can be thought of as a constant and the jitter results from this can be lower for higher slew rates as implied by the following equation:

$$\text{RMS Jitter} = \frac{\text{RMS Voltage Noise}}{\text{Slew Rate}} \tag{6}$$

If noise of the input buffer dominates and increasing the slew rate (while holding frequency constant) improves significantly, then the phase noise is said to be slew rate limited. At some point, the phase noise from other parts of the device dominate and the phase noise is said to be not slew rate limited. At this point, increasing the slew rate brings diminishing returns, such as only 0.1dB for doubling the slew rate.

Table 3-1 shows fundamental trends for flicker noise and noise floor as a function of output frequency and slew rate. The total phase noise is the sum of the slew rate limited and non-slew rate limited phase noise sources. Derivations for this table are in Section Appendix B: Relating Slew Rate, Frequency, Jitter, and Phase Noise.

Table 3-1. Impact of Slew Rate and Carrier Frequency on Flicker Noise and Noise Floor

Noise type	Slew rate limited	Not slew rate limited
Flicker noise	$\mathrm{PN} \propto 20 \times \log(\mathrm{f}) - 20 \times \log(\mathrm{SR})$ (7)	$\mathrm{PN} \propto 20 \times \log(\mathrm{f})$ (8)
Noise floor	$\mathrm{PN} \propto 10 \times \log(\mathrm{f}) - 20 \times \log(\mathrm{SR})$ (9)	$\mathrm{PN} \propto 10 \times \log(\mathrm{f})$ (10)

In the case of a sine wave or clipped sine wave, the slew rate is proportional to the frequency. Applying this assumption to Table 3-1 gives Table 3-2. One observation is that when the frequency is higher, the device tends to not be slew rate limited and the flicker noise increases with frequency at a faster rate than the noise floor. For this reason, flicker noise becomes a much larger consideration at high frequencies (>10GHz) for buffers.

Table 3-2. Flicker Noise and Noise Floor Trends for a Sine Wave

Noise Type	Slew Rate Limited	Not Slew Rate Limited
Flicker Noise	$\mathrm{PN} = \mathrm{constant}$ (11)	$\mathrm{PN} \propto 20 \times \log(\mathrm{f})$ (12)
Noise Floor	$\mathrm{PN} \propto -10 \times \log(\mathrm{f})$ (13)	$\mathrm{PN} \propto 10 \times \log(\mathrm{f})$ (14)

Data for Table 3-3 data was taken from a graph in the Texas Instruments LMK00301 which demonstrates the behavior of a slew rate limited noise floor. As predicted, quadrupling the frequency while holding the slew rate constant results in about a 6dB degradation of the noise floor. Doubling the slew rate while keeping the frequency constant results in a 6dB improvement in the noise floor.

Table 3-3. LMK00301 Noise Floor as a Function of Slew Rate and Frequency

Slew rate (V/µs)	f=156.26MHz	f=625MHz
1	-148	-143.5
1.5	-152	-145.5
2	-154.5	-149
2.5	-156	-150.5

Figure 3-2 gives a hypothetical example that illustrates general trends for input buffer noise assuming a noiseless sine wave input clock of constant amplitude. The flicker noise starts out as constant versus clock frequency because the fact that the noise is slew rate limited counterbalances the general tendency to increase in frequency. After about 100MHz, the flicker noise increases due to not being slew rate limited. The noise floor is slew rate limited at lower frequencies and therefore actually improves for a while as the frequency is increased. Around 40MHz, the slew rate is sufficient and then the noise floor starts to degrade with frequency.

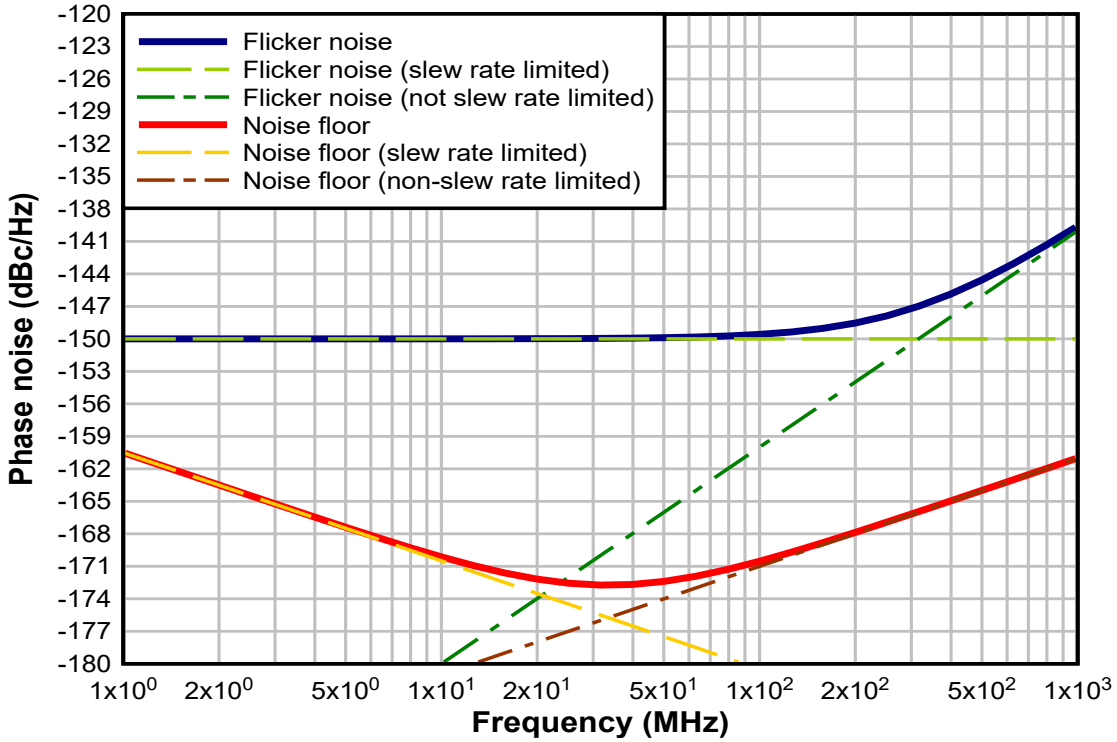

Figure 3-2. Flicker Noise and Noise Floor Trends With Frequency

Figure 3-3 shows the noise floor data taken from the Texas Instruments LMX1214 high frequency divider buffer and demonstrates the general *bowl shaped* trend for noise floor similar to Figure 3-2.

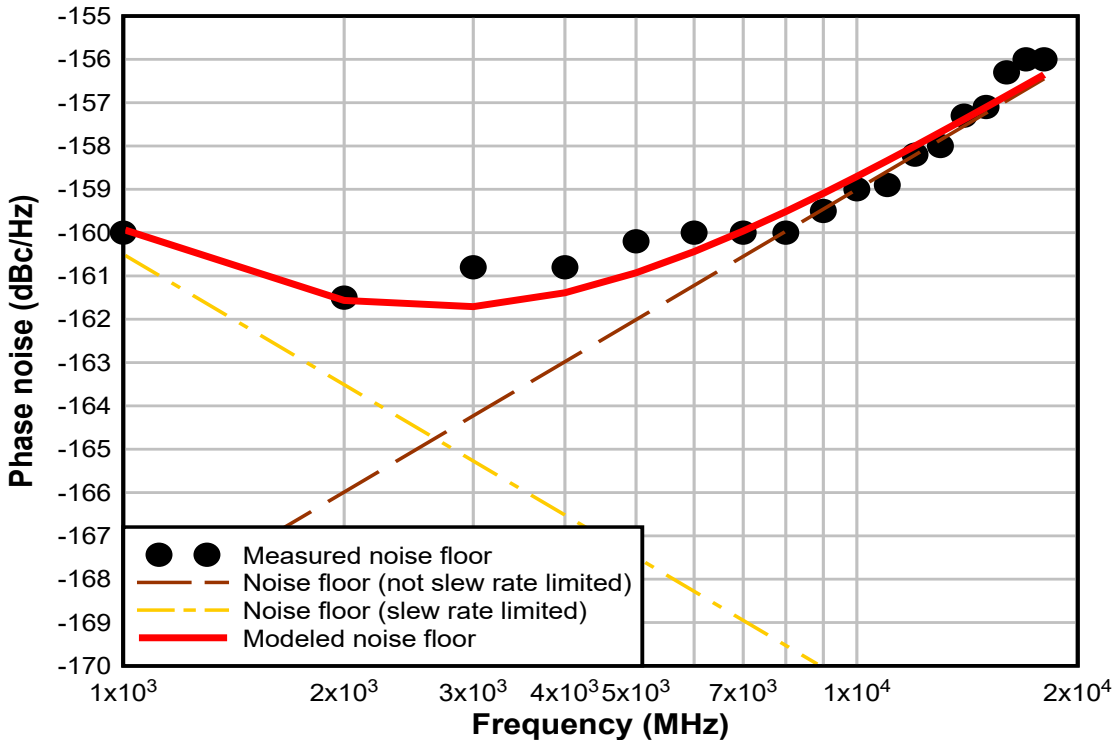

Figure 3-3. LMX1214 Noise Floor Trends vs. Frequency

Table 3-4 can be derived by assuming that frequency is constant, power is changing, and applying Equation 5 taking Table 3-1. This illustrates that both the flicker noise and noise floor are impacted in the same way by input power for this case. Figure 3-4 illustrates this in terms of a phase noise degradation.

Table 3-4. Flicker Noise and Noise Floor Assuming Slew Rate is Proportional to Frequency

Noise Type	Slew Rate Limited	Not Slew Rate Limited
Flicker noise	$PN \propto -p$ (15)	$\mathrm{PN} = \mathrm{constant}$ (16)
Noise floor	$PN \propto -p$ (17)	$\mathrm{PN} = \mathrm{constant}$ (18)

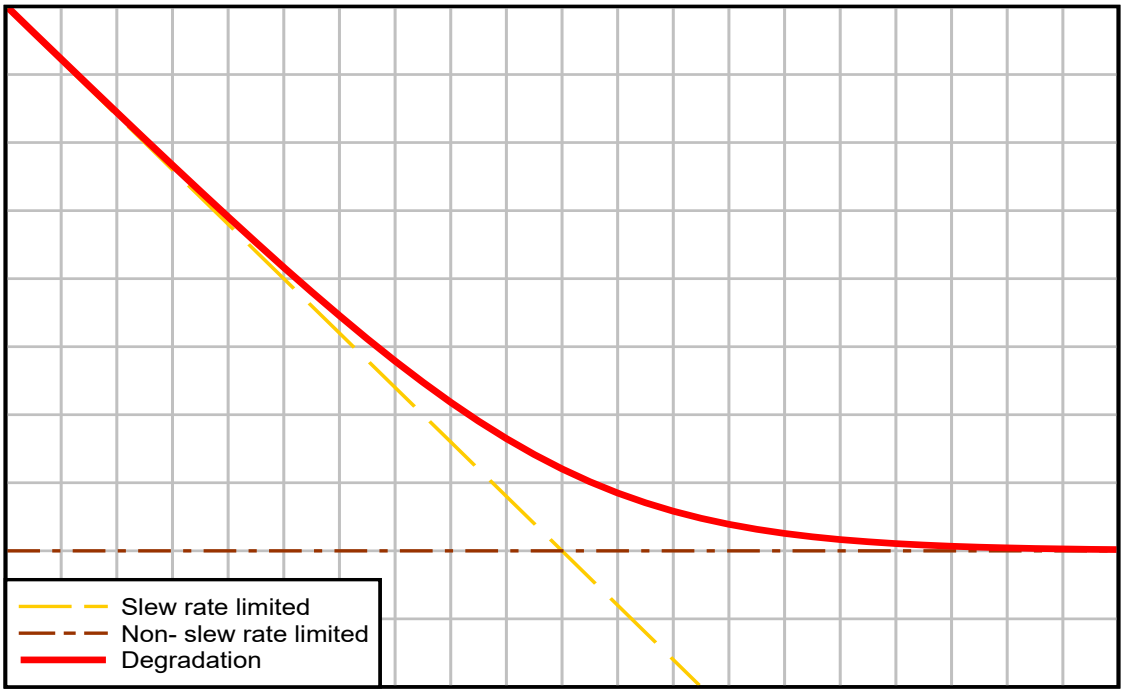

Figure 3-4. Phase Noise Degradation as a Function of Slew Rate

4 Application of Slew Rate Rules to PLL Synthesizers

4.1 PLL Flicker Noise

A PLL can have an input buffer that can limit the phase noise in some cases. The close in 1/f noise behaves very much like a buffer with the exception that the noise is multiplied up by a factor of 20×log(N), where N is the feedback divider value. The flicker noise is typically normalized to 1GHz carrier frequency and 10kHz offset, although there are other ways to create a metric. Figure 4-1 shows the PLL flicker noise degradation as a function if input power for the Texas Instruments LMX2615-SP PLL using a constant 100MHz input frequency. Note that this behaves very similar to a buffer.

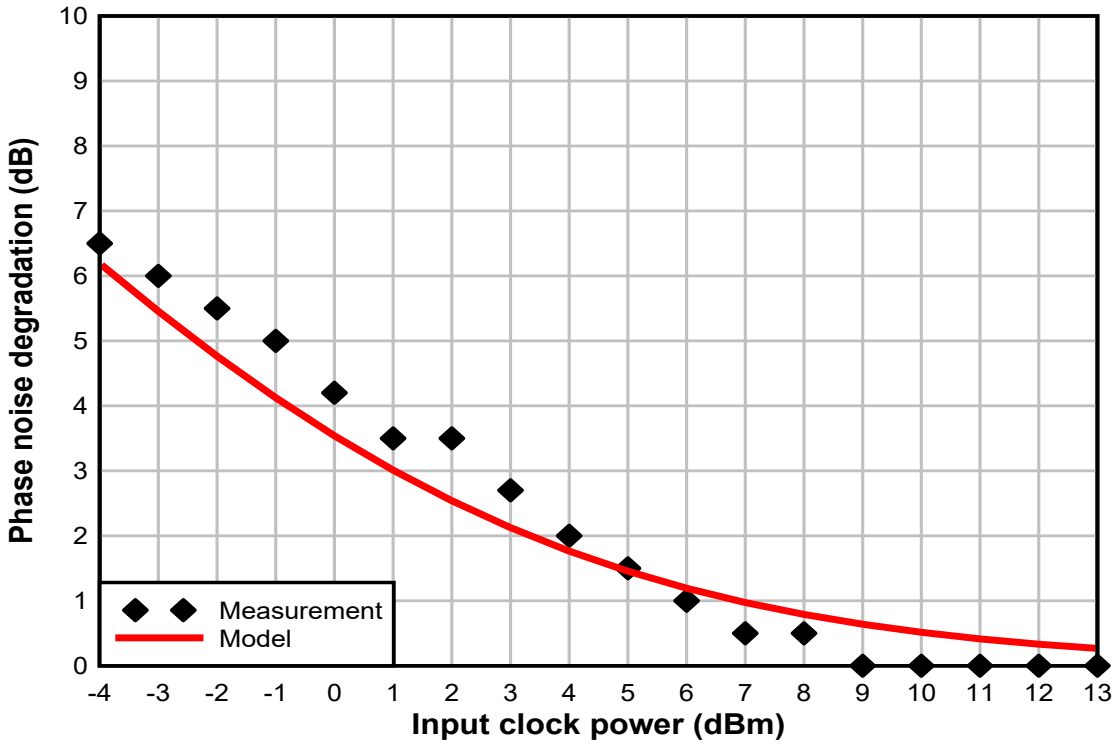

Figure 4-1. Impact of Clock Input Power on Flicker Noise for LMX2615-SP PLL

The model assumes for low input power, the trend is 1dB degradation per 1dB reduction in output power. Around 3dB input power, a knee is reached where the slew rate limited noise and non-slew rate limited noise are equally contributing to the total noise.

4.2 PLL Figure of Merit

For the noise floor, PLLs often characterize this in terms of figure of merit (FOM). This is a useful metric as the metric allows one to characterize the PLL noise floor with a single number. The noise floor can be calculated from the PLL figure of merit using feedback divider value (N) and phase detector frequency (f_{PD}).

$$\text{PN Noise Floor} = \text{FOM} + 20 \times \log(\text{N}) + 10 \times \log(f_{PD}) \quad (19)$$

Figure 4-2 shows the impact of input power on the PLL figure of merit

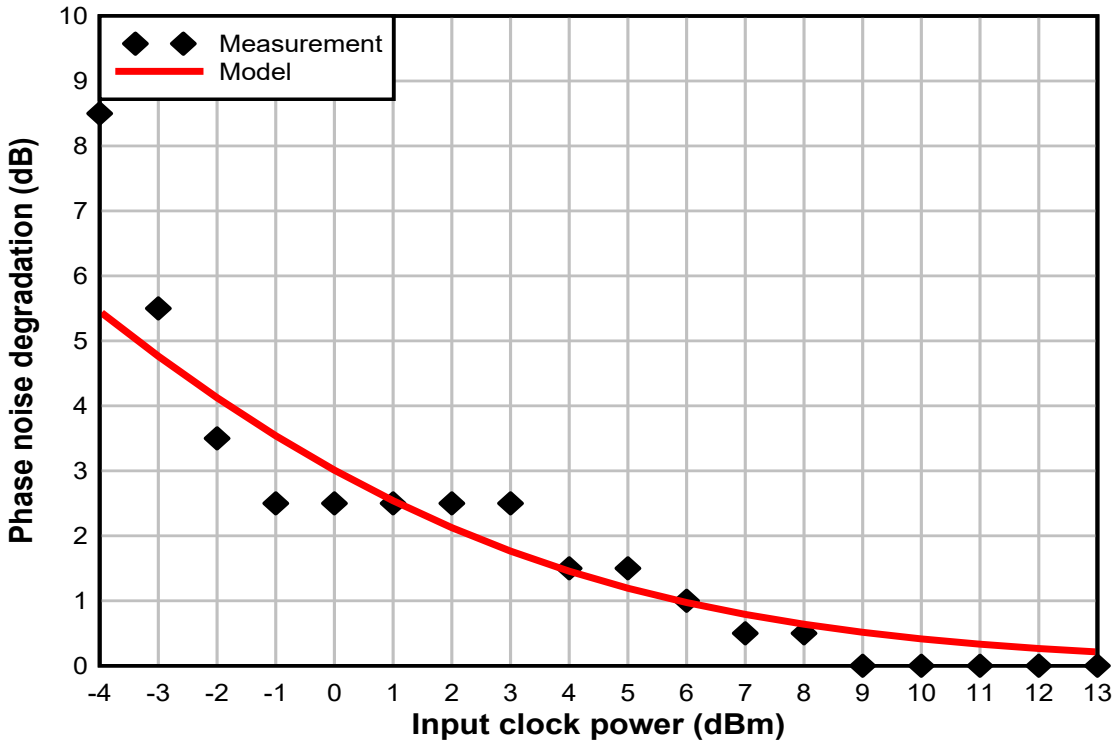

Figure 4-2. Impact of Clock Input Power for PLL Figure of Merit for LMX2615-SP PLL

Not shown is the impact of using a constant input power, but changing the input frequency. For a PLL, the R divider can divide the input clock frequency down and in doing so, phase noise is improved. When changing the input frequency and dividing the frequency down, this also divides down the internal buffer input noise as well. So in many cases, doubling the input clock frequency and doubling the R divider can improve the phase noise of a PLL.

4.3 Other Areas in PLLs Where Slew Rate has an Impact on Performance

Input clock slew rate can impact PLL fractional spurs. The reason for this is that is fractional spur energy from the fractional circuitry can couple to the input path of the PLL. This behaves in a very similar way as the inherent device noise in Figure 3-1. The resulting jitter is multiplied by 20×log(N). In the case where the input clock slew rate is low enough for the spur to be slew rate limited, increasing the input power by 1dB can improve the spur by 1dB. However, increasing the clock slew rate too much creates a stronger signal on the input and this can couple and mix. So for this reason, a high slew rate, but low frequency input, like LVDS, is designed for PLL spurs.

Slew rate also impact PLL R and N divider sensitivity. Sensitivity is the minimum power required for the counter to correctly function and where the output frequency is measured to be within 1Hz of the value needing to be. The inputs to these counters have an internal voltage noise and therefore sensitivity curves often have the *bowl shape* as shown for the noise floor as in Figure 2-1.

4.4 Improving PLL Slew Rate for Better Performance

Sometimes, one is stuck with a low input clock frequency, which is not designed for PLLs. In this case, if choosing a buffer strategically, then the buffer can improve the PLL phase noise. The Texas Instruments LMK1C1102 CMOS buffer has excellent noise floor and is very good at squaring up signals. Sine to Square Wave Conversion using Clock Buffers shows how this buffer can be used to improve the phase noise of the LMX2820, even for signal levels at the maximum allowable input power of +10dBm. This is very true for 10MHz and still true to just a small extent at even 100MHz input frequency.

5 Application of Slew Rate Rules to Data Converters

For data converters, one key metric is the signal to noise ratio, SNR. The signal to noise ratio is a combination of a fixed jitter (dependent on thermal noise, resolution, and other frequency-independent factors) and a SNR due to jitter.

$$\mathrm{SNR} = -10 \times \log\left[\left(10\text{^}\left(-\mathrm{SNR}_{\mathrm{Jitter}}/10\right)\right) + \left(10\text{^}\left(-\mathrm{SNR}_{\mathrm{Fixed}}/10\right)\right)\right] \quad (20)$$

The SNR due to jitter can be calculated as follows (Section Appendix C: Equations for Data Converters):

$$SNR_{Jitter} = -20 \times log[2\pi \times f \times \sigma] \quad (21)$$

Furthermore, the jitter (not including sampled signal) is a combination of the clock jitter and the aperture jitter.

$$\sigma_t = \sqrt{\sigma_{\mathrm{Clock}}{}^2 + \sigma_{\mathrm{Aperture}}{}^2} \quad (22)$$

Finally, in Section Appendix C: Equations for Data Converters, it is shown that the SNR for a slew rate limited case improves 1dB per 1dB with the clock power. Figure 5-1 puts these equations to actual measurements which are described in more depth in *Practical Clocking Considerations That Give Your Next High-Speed Converter Design an Edge*. In this case, a input clock of fixed 25MHz frequency, but variable amplitude was used to clock an analog to digital converter for both a 5MHz and 30MHz sampled signal. The slew rate limited trend lines show a dB/1dB trend and a separation between the 5MHz and 30MHz trend lines is 20×log(30MHz/5MHz) = 15.6dB. At lower amplitudes (like -15dBm), the performance is slew rate limited and we also see this same 15.6dB separation between the measurements for the 5MHz and 30MHz clocks. At higher input amplitudes, some other factors dominate that are not impacted by the slew rate. The result of this is there is not the full 15.6dB difference in the curves, but is actually closer to about 5dB at higher input power levels.

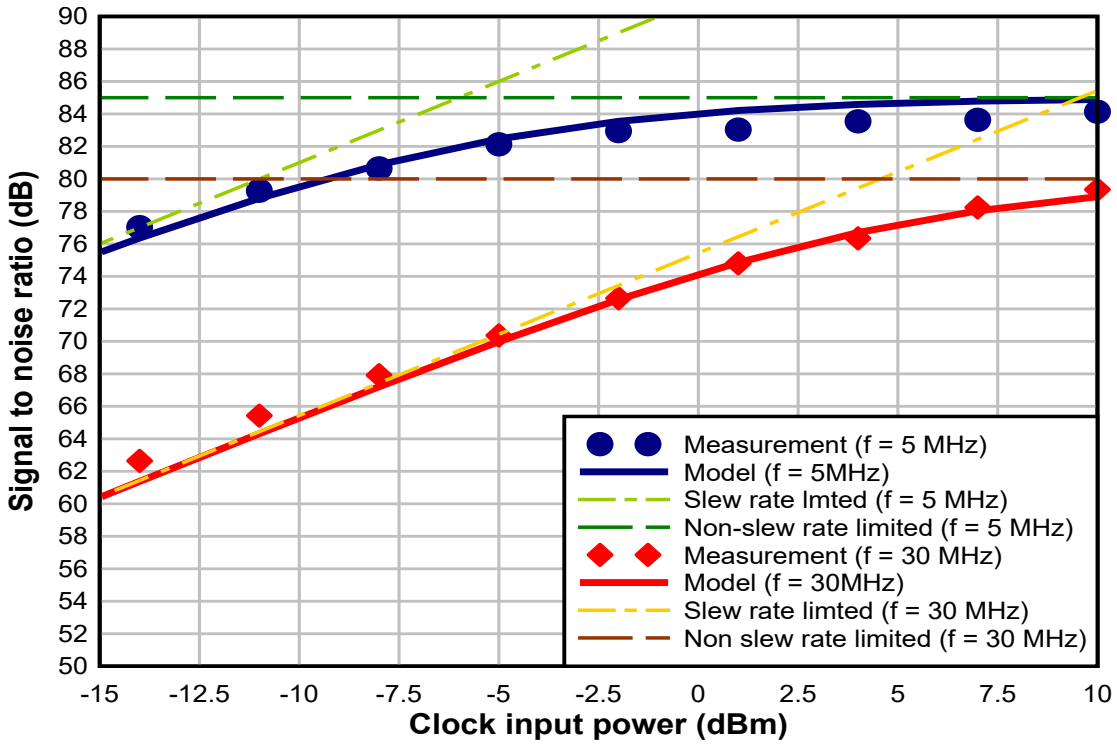

Figure 5-1. Data Converter SNR vs Input Clock Power for Rohde and Schwarz SMA100B Signal Generator

To illustrate the impact of jitter on the sampled signal, the experiment was repeated with a signal generator with higher noise as shown in Figure 5-2. For both of these figures, the slew rate limited case for both sampling frequencies is degraded by 3dB by using the noisier signal generator. For the non-slew rate limited case,

the signal generator makes 2dB difference for a 5MHz sampling frequency and 8dB difference for a 30MHz sampling frequency. For both figures, one can infer the portion of SNR that is fixed and the portion that is due to jitter as shown in Table 5-1. The method for doing this is presented in Section Appendix D: Calculations for Data Converter Example. In addition to the clock jitter and aperture jitter as mentioned in Equation 34, this jitter also includes that of the sampled signal.

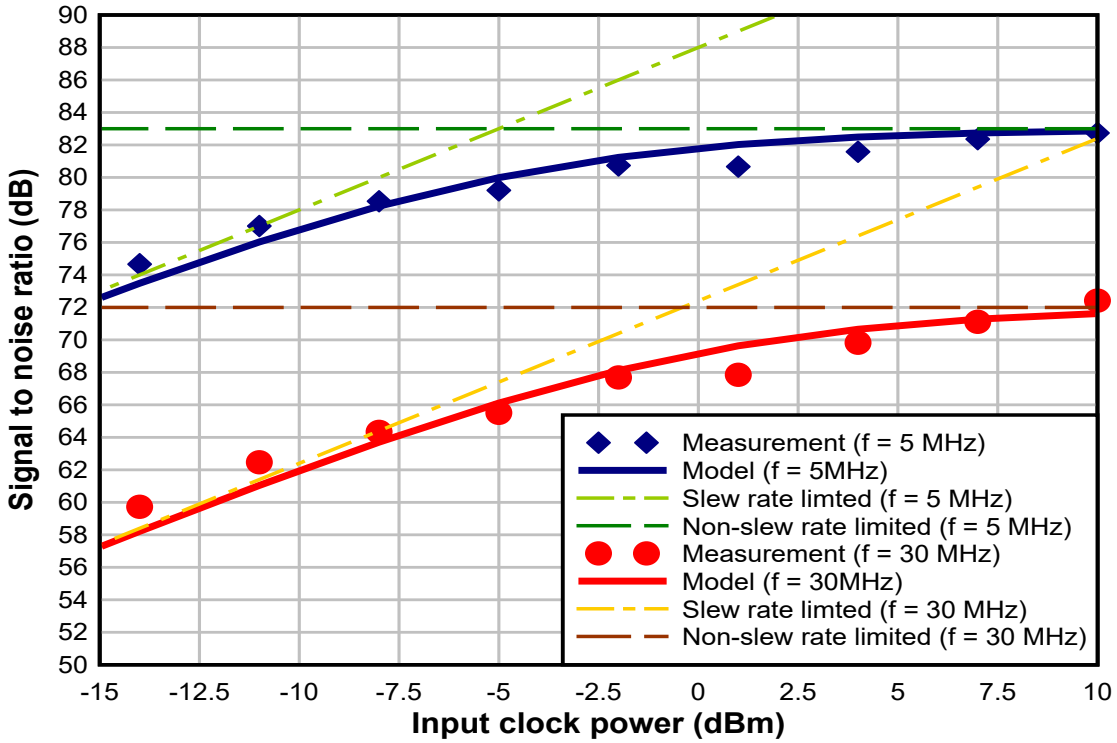

Figure 5-2. Data Converter SNR vs Input Clock Power for Agilent 4438C Signal Generator

Table 5-1. Calculation of Inferred Jitter

Signal Generator	Jitter	f	SNR	SNR_{Jitter}	SNR_{Fixed}
Rohde & Schwarz SMA100B	440.91 fs	5MHz	85	97.092	85.277
		30MHz	80	81.529	
Agilent 4438C	1296.71 fs	5MHz	83	87.800	84.747
		30MHz	72	87.800	

From the data sheet for the ADC3683, the aperture jitter is stated to be 180 fs. The jitter stated in Table 5-1 is the combination of the clock jitter and aperture jitter. In this case, the clock jitter is dominating over the aperture jitter.

6 Summary

The impact of the input clock slew rate has been discussed in this paper. As clock slew rate relates to frequency and power, general trends for phase noise and jitter were modeled and compared to actual measured data. By understanding these trends, the system can be better optimized for the best performance.

7 References

1. Texas Instruments, *Practical Clocking Considerations That Give Your Next High-Speed Converter Design an Edge*, application note.
2. Texas Instruments, *Sine to Square Wave Conversion using Clock Buffers*, application note.

Appendix A: Relating Slew Rate, Power, and Frequency

As a sine wave is a very common input clock, a sine wave is useful to derive the slew rate for this signal. Consider a sine wave of the form:

$$v(t) = A \times \sin(2\pi \times f \times t) \tag{23}$$

The slew rate (SR) can be found by taking the first derivative and evaluating this at the zero crossing.

$$SR = \frac{dv}{dt}\Big|_{t=0} = 2\pi \times f \times A \times \cos(2\pi \times f \times t)\Big|_{t=0} = 2\pi \times f \times A \tag{24}$$

Peak to Peak voltage is simply 2×A and RMS voltage is A/✓2 . It therefore follows the power is:

$$P_{dBm} = 10 \times \log\left\{\frac{\left(\frac{A^2}{2 \times 50\Omega}\right)}{0.001}\right\} = 10 \times \log\left(10 \times A^2\right) \tag{25}$$

Power (in dBm) can be related by power by combining Equation 24 and Equation 25.

$$P = 10 \times \log\left(10 \times A^2\right) = 10 \times \log\left(10 \times \left(\frac{SR}{2\pi \times f}\right)^2\right) \tag{26}$$

This can be arranged to receive the final result

$$SR = \frac{2\pi \times f \times 10^{\frac{P}{20}}}{\sqrt{10}} \tag{27}$$

Appendix B: Relating Slew Rate, Frequency, Jitter, and Phase Noise

Consider the case of a perfectly clean input clock with slew rate SR into a buffer. For the buffer, there is some internal voltage noise which we consider to be constant. In symbolic terms, this can be stated that with slew rate (SR) and rms jitter (and voltage jitter (which is:

$$\sigma_v = \sigma_t \times \mathrm{SR} \tag{28}$$

In this case, the unknown is the jitter that results from the voltage noise.

$$\sigma_t = \frac{\sigma_v}{\mathrm{SR}} \tag{29}$$

Now equation Equation 29 is just for one rising edge of the signal. In actuality, at every rising edge there is a different jitter. In this case, the number of cycles depends on the measurement time (t).

$$\mathrm{n} = \frac{\mathrm{t}}{\mathrm{f}} \tag{30}$$

Now variance relates to noise power. So consider measuring the power over the timer interval ***t*** . If the jitter in equation Equation 29 is correlated from one period to the next, then it appears as 1/f noise, also known as flicker noise. As jitter is the standard deviation of the time error, if one takes the average of n cycles, this average can be calculated.

$$\sigma_{\mathrm{flicker}} = \frac{\mathrm{n} \times \sigma_{\mathrm{t}}}{\mathrm{t}} = \sigma_{\mathrm{t}} \times \mathrm{f} \tag{31}$$

If the jitter in equation Equation 29 is not correlated from one period to the next, then it appears as noise floor. As jitter is the standard deviation of the time error, if one takes the average of n cycles, this average can be calculated.

$$\sigma_{\mathrm{floor}} = \frac{\sqrt{\mathrm{n} \times \sigma_{\mathrm{t}}}}{\mathrm{n}} = \sigma_{\mathrm{t}} \times \sqrt{\mathrm{f}} \tag{32}$$

Recall that jitter and phase noise are related.

$$\sigma = \frac{\sqrt{2 \times \int_{\mathrm{a}}^{\mathrm{b}} \mathrm{L(w)} \times \mathrm{dw}}}{2\pi \times \mathrm{f}} \tag{33}$$

For the integral, we are only interested in the phase noise as it changes with frequency and slew rate, so we are not concerned with the integration limits and we roll this up into a constant.

$$\sigma = \frac{\sqrt{2 \times 10^{PN/10} \times \int_a^b L(w) \times dw}}{2\pi \times \mathrm{f}} = \frac{constant \times \sqrt{10^{PN/10}}}{\mathrm{f}} \tag{34}$$

Equation Equation 34 can be arranged as follows.

$$\mathrm{PN} = 20 \times \log(\sigma) + \mathrm{constant} \tag{35}$$

In the case of flicker noise, combine Equation 31 and Equation 35 to get:

$$\mathrm{PN}_{\mathrm{flicker}} = 20 \times \log(\sigma_{\mathrm{t}} \times \mathrm{f}) + \mathrm{constant} \tag{36}$$

This can be rearranged to get the rule for 1/f noise.

$$\mathrm{PN}_{\mathrm{flicker}} \propto 20 \times \log(\sigma_{\mathrm{t}}) + 20 \times \log(\mathrm{f}) \tag{37}$$

This result can be combined with Equation 29 to obtain:

$$PN_{flicker} \propto 20 \times \log\left(\frac{\sigma_V}{SR}\right) + 20 \times \log\left(f\right) \quad (38)$$

As the voltage noise, is a constant, Equation 38 can be rearranged to get the fundamental relationship between flicker noise, slew rate, and frequency.

$$PN_{flicker} \propto 20 \times \log(f) - 20 \times \log(SR) \quad (39)$$

In the case of noise floor, we combine with Equation 32 with Equation 35 to get:

$$PN_{floor} = 20 \times \log(\sigma_t) + 20 \times \log(\sigma_t \times \sqrt{f}) + constant \quad (40)$$

This can be rearranged to get the rule for noise floor.

$$PN_{floor} \propto 20 \times \log(\sigma_t) + 10 \times \log(f) \quad (41)$$

Now combine this result with Equation 29 to get:

$$PN_{floor} \propto 20 \times \log\left(\frac{\sigma_V}{SR}\right) + 10 \times \log\left(f\right) \quad (42)$$

As the voltage noise, is a constant, Equation 41 can be rearranged to get the final result.

$$PN_{floor} \propto 10 \times \log(f) - 20 \times \log(SR) \quad (43)$$

Appendix C: Equations for Data Converters

1 Relating Sampled Signal Slew Rate to SNR

Consider a clock input to the system of the form:

$$v(t) = A \times \sin(2\pi \times f \times t) \tag{44}$$

The slew rate is therefore:

$$SR = \frac{dv}{dt}\Big|_{t=0} = 2\pi \times f \times A \times \cos(0) = 2\pi \times f \times A \tag{45}$$

The RMS voltage error can be found by multiplying the jitter by the slew rate.

$$\sigma_v = \sigma_t \times SR = \sigma_t \times 2\pi \times f \times A \tag{46}$$

The signal to ratio can now be found.

$$SNR_{Jitter} = 10 \times \log\left[\frac{A^2/R}{(\sigma_t \times 2\pi \times f \times A)^2/R}\right] = -20 \times \log[\sigma_t \times 2\pi \times f] \tag{47}$$

2 Justification That SNR Decreases 1dB per 1dB With Input Power for Slew Rate Limited Case

Start with the assumption that the clock jitter dominates and the slew rate limited. Table 3-1 shows that the phase noise is related to 20×log(SR). Equation 5 shows that a 6dB increase in clock power doubles the slew rate. Equation 33 relates phase noise to jitter. So therefore a 6dB increase in input power improves the phase noise by 6dB. This in turn reduces the jitter by a factor of 2. Equation 47 shows that this leads to a 6dB improvement in SNR. So to generalize this rule for a slew rate limited SNR for a data converter.

$$SNR \propto \text{Clock Input Power} \tag{48}$$

Appendix D: Calculations for Data Converter Example

Rearrange Equation 20 to get the following:

$$10^{-\mathrm{SNR}/10} = 10^{-\mathrm{SNR_{Fixed}}/10} + 10^{-\mathrm{SNR_{Jitter}}/10} \tag{49}$$

Also, realize Equation 21 implies that if f increases from 5 to 30MHz, then $\mathrm{SNR_{Jitter}}$ decreases by 20 × log(6) . Now define SNR1 as the SNR with 5MHz signal and SNR2 as the SNR with 30MHz signal.

$$10^{-\mathrm{SNR1}/10} = 10^{-\mathrm{SNR_{Fixed}}/10} + 10^{-\mathrm{SNR_{Jitter}}/10} \tag{50}$$

$$10^{-\mathrm{SNR2}/10} = 10^{-\mathrm{SNR_{Fixed}}/10} + 10^{-\frac{\mathrm{SNR_{Jitter}} - 20 \times \log(6)}{10}} = 10^{-\mathrm{SNR_{Fixed}}/10} + 36 \times 10^{-\frac{\mathrm{SNR_{Jitter}}}{10}} \tag{51}$$

Equation 50 and Equation 51 are a system of two equations and two unknowns. Subtract Equation 50 from Equation 51 and solve for $\mathrm{SNR_{Jitter}}$. Realize that for the 30MHz case, is lower.

$$\mathrm{SNR_{Jitter}} = 10 \times \log\left(\frac{10^{-\frac{\mathrm{SNR2}}{10}} - 10^{-\frac{\mathrm{SNR1}}{10}}}{35}\right) \tag{52}$$

Once $\mathrm{SNR_{Jitter}}$ is known, $\mathrm{SNR_{Fixed}}$ can be found.

$$\mathrm{SNR_{Fixed}} = 10 \times \log\left(10^{-\frac{\mathrm{SNR1}}{10}} - 10^{-\frac{\mathrm{SNR_{Jitter}}}{10}}\right) \tag{53}$$

Furthermore, we can rearrange Equation 47 to calculate the jitter as perceived by the data converter.

$$\sigma = \frac{10^{-\mathrm{SNR_{Jitter}}/20}}{2\pi \times \mathrm{f}} \tag{54}$$

Figure 5-1 and Figure 5-2 were used to get the SNR values for the on slew rate limited case to generate Table 5-1 was calculating using Equation 52, Equation 53, and Equation 54.

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