

Anti-Alias Filter Design for a 100kHz Bandwidth Data Acquisition Signal Chain



Maggie Lee, Michael Levin

ABSTRACT

Data acquisition systems are used in many industries, from automotive test to aerospace and defense. The front-end of a data acquisition system presents key challenges as the system must have sufficient bandwidth to capture the input signal without introducing frequency response distortion, phase shift, or attenuation that can compromise the signal's integrity. This application note discusses the design of an anti-aliasing filter for a 100kHz data acquisition signal chain.

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1 Introduction

Data acquisition systems (DAQs) have a wide range of applications, from acceleration and velocity measurements in vehicle brake testing, to strain measurements in structural health monitoring.

Some of the sensors used in DAQ systems can have a specified measurement bandwidth in their data sheets. For example, a typical MEMS accelerometer used in vibration monitoring can have a frequency response from DC (0Hz) to 10kHz. However, outside of the measurement bandwidth, a sensor can have a resonance frequency, which is where the sensor is most sensitive, which can distort the measurement. The MEMS accelerometer previously mentioned can have a resonance frequency around 60kHz. Any stray signal close to 60kHz can be amplified, creating an error in the measurement. To fix this error, an anti-aliasing filter can be used to filter out the unwanted frequencies. Note that resonance frequency from sensors is only one example of noise which can be present in a testing environment.

This report focuses on a signal chain designed for bandwidths up to 100kHz using the [PGA855](#), [THS4551](#), and [ADS127L21](#) as shown in [Figure 1-1](#). The evaluation board for [ADS127L21](#) has an anti-aliasing filter with THS4551 present on the board, however, the bandwidth and tolerance are not designed for higher frequencies. Adjustments were made to increase the filter bandwidth and were verified through simulation and hardware measurements.

The ADS127L21 is a 24-bit, high-speed, wide-bandwidth, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The ADS127L21 offers excellent ac and dc performance, along with multiple internal digital filter options including a fully programmable finite impulse response (FIR) and infinite impulse response (IIR) filter, making the device useful for a wide variety of data acquisition applications. THS4551 is a differential amplifier used to drive ADS127L21. ADS127L21 is designed for exceptional dc accuracy, low noise, and robust capacitive load driving, making ADS127L21 designed for data acquisition systems where high precision is required along with excellent signal-to-noise ratio (SNR).

The PGA855 is the input amplifier. The PGA855 is a precision, high-bandwidth programmable gain instrumentation amplifier. The PGA855 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain-selection pins. The output common-mode voltage can be independently set using the VOVM pin. The device features super-beta input transistors from Texas Instruments, which provide ultra-low input offset voltage, offset drift, input bias current, input voltage noise, and current noise.

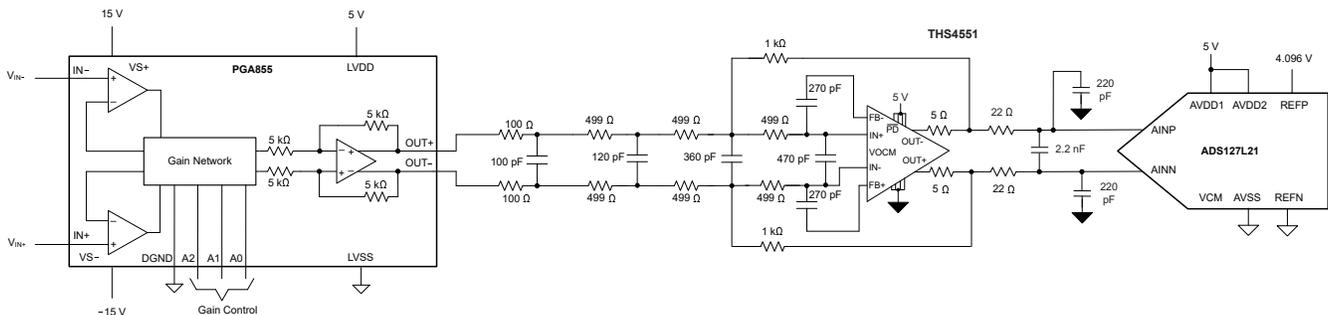


Figure 1-1. Data Acquisition Signal Chain

2 Anti-Aliasing Filter Design

The schematic shown in [Figure 2-1](#) is a 3rd order low pass filter on [ADS127L21EVM-PDK](#). With the passive components shown, the filter can have a bandwidth around 260kHz. By changing those components shown in red, the cutoff is pushed to over 370kHz. The tolerance of the capacitor and resistors can affect the filter's bandwidth, since the cutoff frequency is determined by the passive components. Changing the capacitors and resistors to 1% and 0.1% tolerances respectively, makes the filter more consistent over natural variations in the components' physical values. A filter design tool can be used to determine the resistor and capacitor values based on the filter's requirements. Texas Instruments' [Filter Design Tool](#) can be used to design single-ended filters. See [Design Methodology for MFB Filters in ADC Interface Applications](#) for more details on designing a multiple feedback filter.

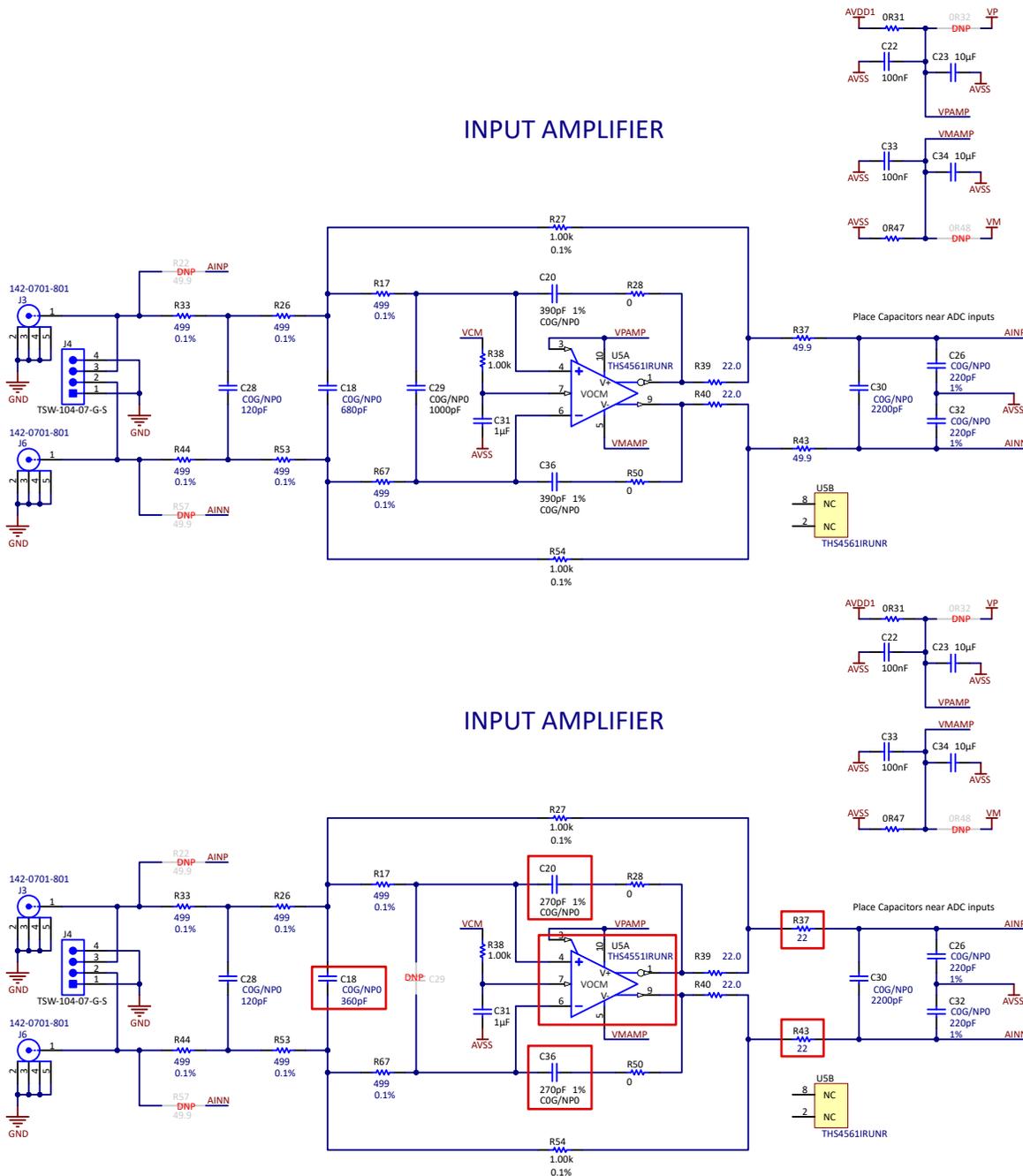


Figure 2-1. Anti-Alias Filter

2.1 Simulation

Monte-Carlo simulations can be used to generate a statistical estimate of typical variations from component tolerances. The Monte-Carlo Simulations shown in [Figure 2-2](#) demonstrate the expected spectral response of the AAF on [ADS127L21EVM-PDK](#). The mean and sigma displayed in the blue box supports the calculated expectations of the cutoff and the large swing of cutoffs spanning about 13kHz.

Monte-Carlo 100 runs of AAF as installed on the ADS127L21

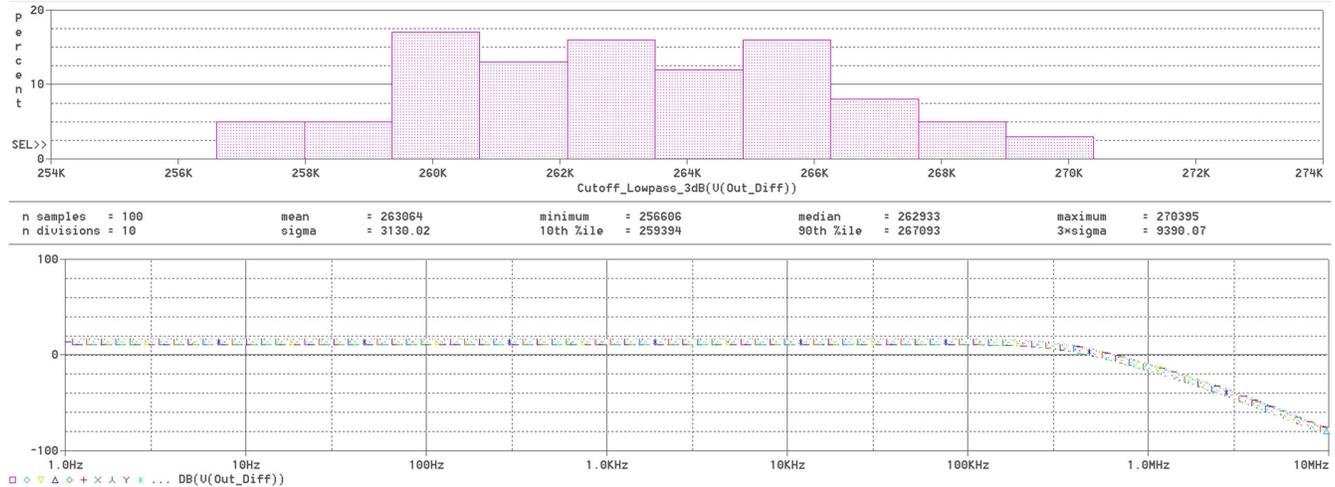


Figure 2-2. Monte-Carl Simulation With the Original AAF

In contrast, the same simulation with the new anti-aliasing filter gives a result shown in [Figure 2-3](#). The same mean bandwidth is more than 100kHz larger with a sigma three times tighter than that seen in [Figure 2-2](#).

Monte-Carlo 100 runs of AAF as installed on the ADS127L21

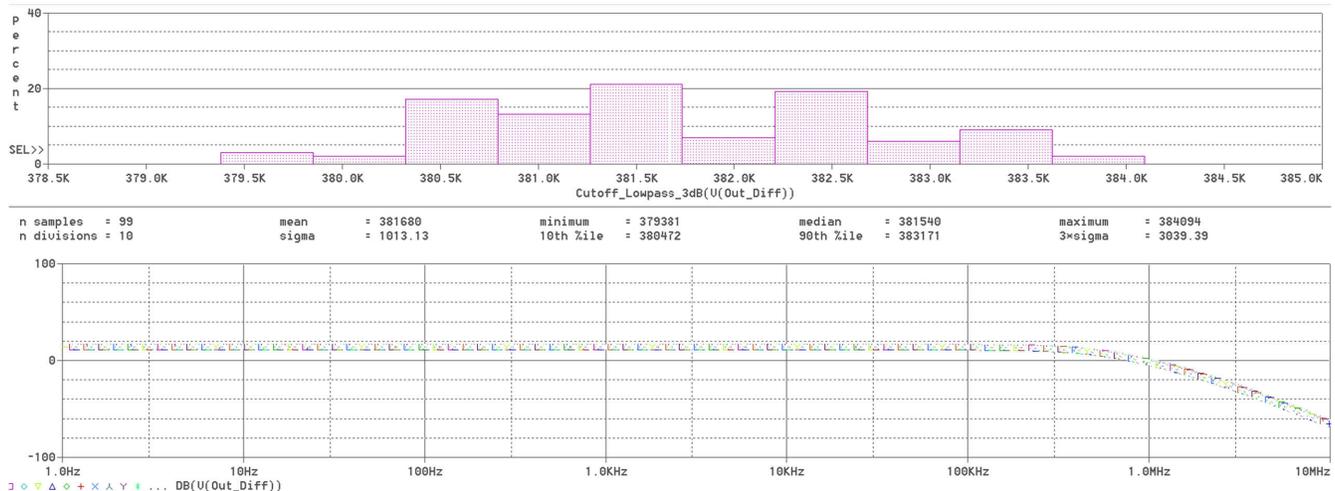


Figure 2-3. Monte-Carlo Simulation with the New AAF

Phase is another important metric since a consistent time delay between the input and output of the AAF can be accounted for by the computer. If the variations are inconsistent, voltages can be collected on unexpected clock cycles which can cause issues when processing data. For example, when taking power measurements with a power analyzer, if the phase is not accounted for when measuring the current and voltage, the calculated power can be inaccurate. In the same filter simulation, the phase can be seen in [Figure 2-4](#) with a somewhat constant slope between 0Hz and 100kHz.

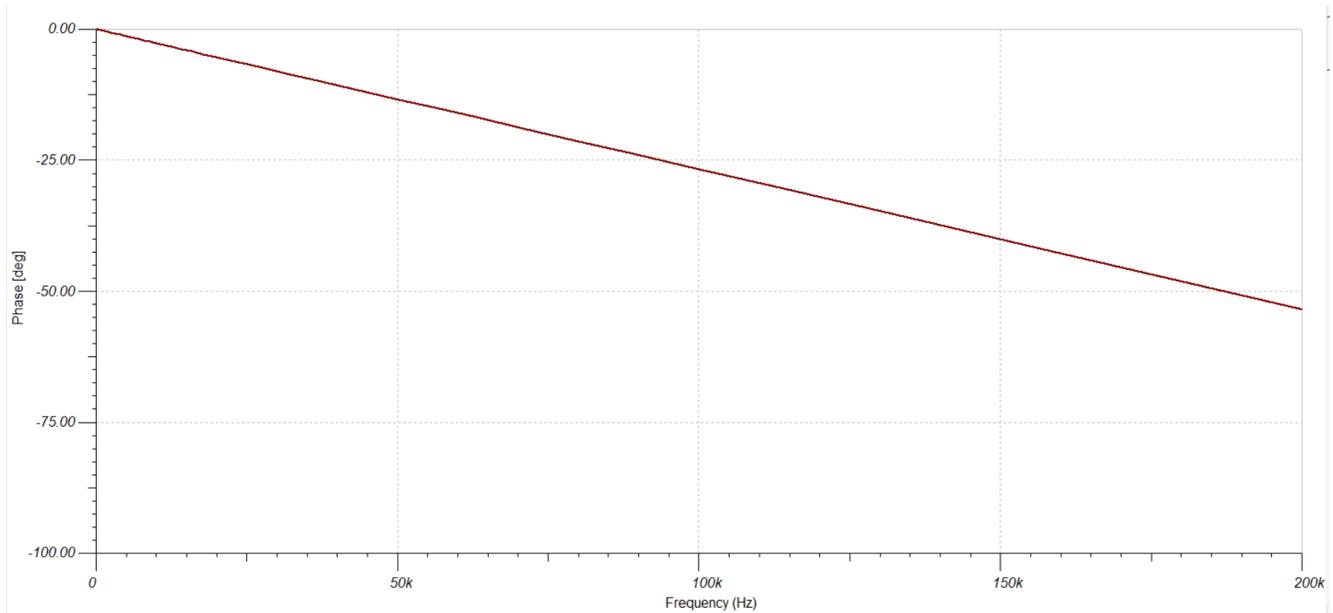


Figure 2-4. AAF Phase after Modifications

Group delay can be calculated from phase or measured directly. The linear phase leads to a very flat group delay. The simulation in [Figure 2-5](#) shows that the group delay is very flat from DC to 100kHz.

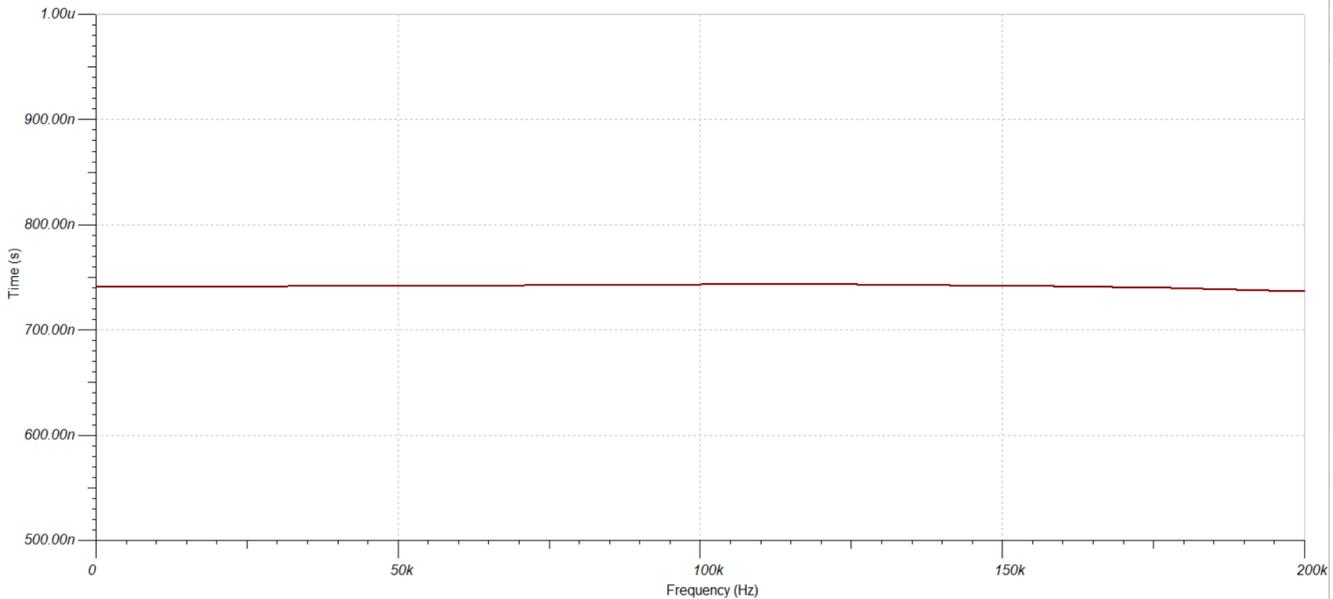


Figure 2-5. Simulation of the AAF Group Delay after Modification

The ADS127L21 has four speed modes and a programmable digital filter with data rates up to 512kSPS using the wideband filter and up to 1365kSPS using the low-latency filter, offering trade-offs between latency, bandwidth, resolution, and power consumption. In max-speed mode, ADS127L21 can have a modulator clock frequency of 16.384MHz. The filter must have good attenuation at the modulator frequency. The stopband attenuation at the modulator clock frequency minus the filter bandwidth (16.2MHz) is -112dB in simulation, as seen in [Figure 2-7](#). The digital filter can attenuate all signals between the digital filter bandwidth, up to the modulator frequency.

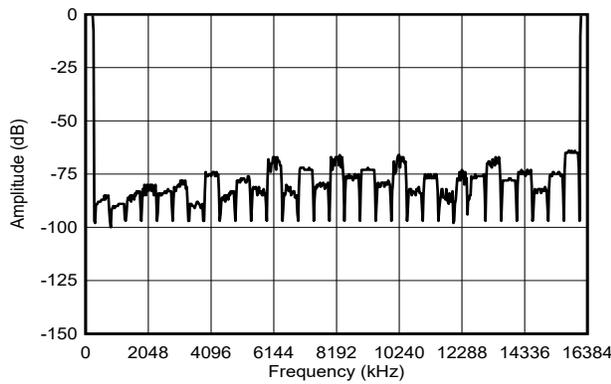


Figure 2-6. Wideband Filter Stop-Band Attenuation (OSR 32, fCLK 32.768MHz)

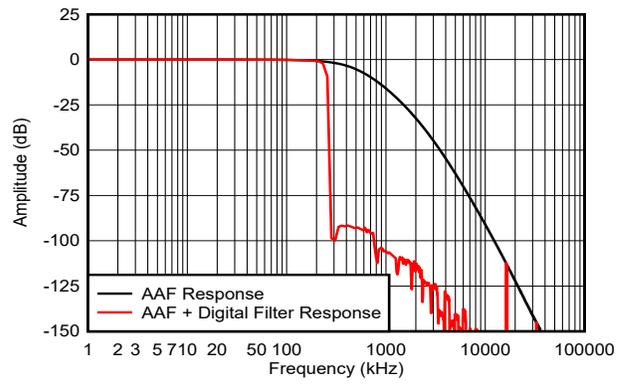


Figure 2-7. Combined Anti-Alias Filter and Digital Filter Response

2.2 Hardware Testing

The actual circuit can be tested to verify the simulations using [ADS127L21EVM-PDK](#) and [PGA855EVM](#) with the modifications described in [Figure 2-1](#).

The anti-aliasing filter can be tested with a low-distortion sine wave generator, while using the [ADS127L21EVM-PDK-GUI](#) is used to collect data.

The results shown in [Figure 2-8](#) and [Figure 2-9](#) are sound responses across varying frequencies and PGA855 gains. [Figure 2-9](#) shows that harmonic noise gets worse at higher frequencies, only jumping back down when the signal is close to the cutoff. As for SNR, the noise floor is comparable across gains at 100kHz and 200kHz but at frequencies at 100kHz and below, the high gain signals are noisier than unity or low gain signals. This makes sense since the input signal before high gain filters need to be small to reach the same output at the PGA855.

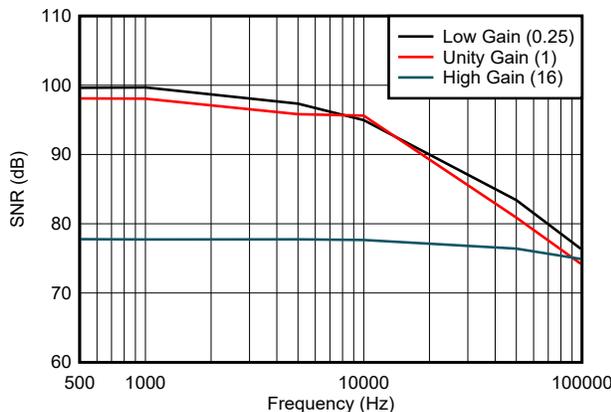


Figure 2-8. SNR

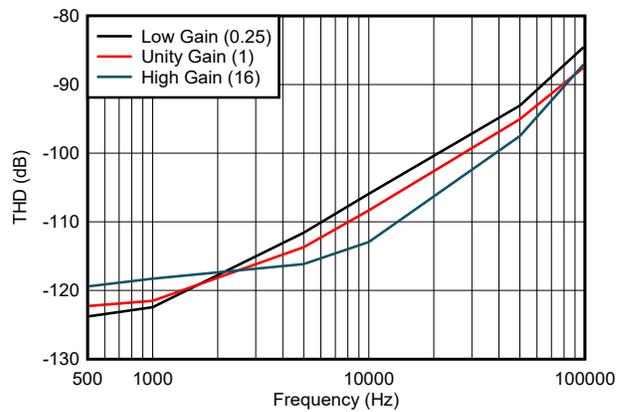


Figure 2-9. THD

Magnitude is an extremely important measurement to confirm the new cut off frequency which was predicted by the simulations. This can be seen best in the graph seen in [Figure 2-10](#). This shows not only a similar shape as the one seen in the [Figure 2-3](#), but a cut off frequency well beyond the target frequencies.

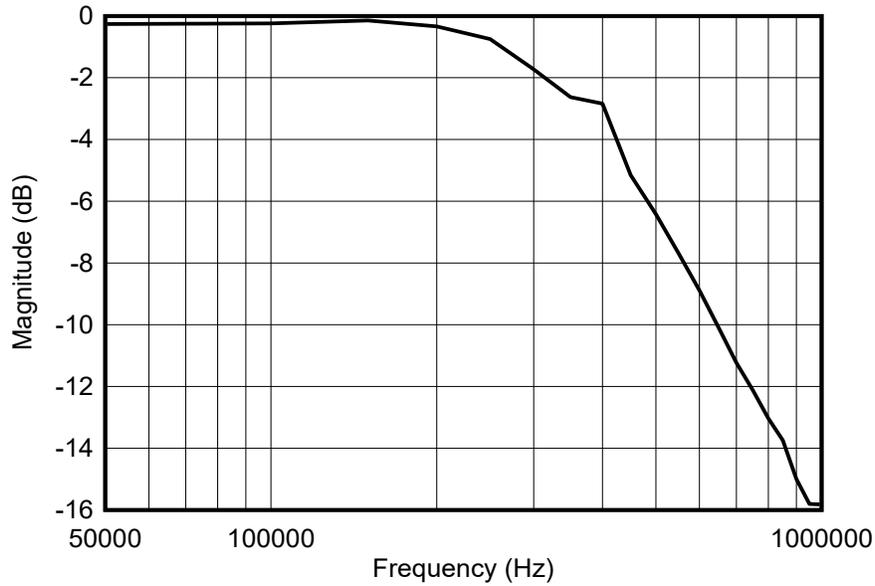


Figure 2-10. Anti-Alias Filter Magnitude

The group delay was calculated from phase measurements across the bandwidth. [Figure 2-11](#) shows that the group delay remains low across the entire bandwidth (the group delay was simulated on a microsecond scale, while it was measured on a nanosecond scale). This is consistent with the simulation in [Figure 2-5](#), which showed that the change in delay across the entire signal chain was around 10ns from DC to 100kHz. A consistent delay allows the computer to consistently anticipate when the proper data can be received between the input and output of the DAQ system.

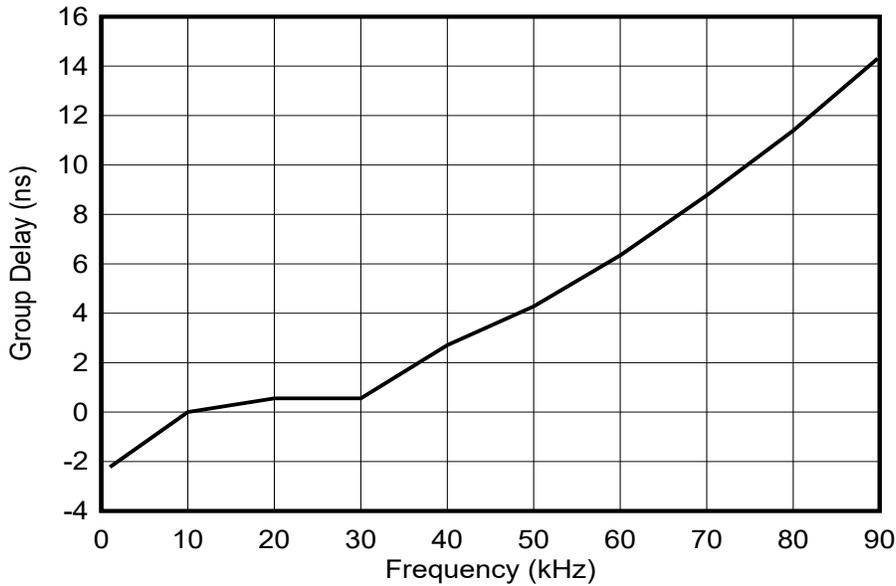


Figure 2-11. Group Delay of the Signal Chain (Normalized to 10kHz)

3 Summary

An anti-aliasing filter can be an important component in a data acquisition signal chain. The filter must be carefully designed to meet the bandwidth requirements of the DAQ input. An anti-aliasing filter can easily be simulated making the design process easier and allowing the designer to tune parameters as desired.

4 References

1. Texas Instruments, [Using SPICE Monte Carlo Tool for Statistical Error Analysis](#), video.
2. Texas Instruments, [Design Methodology for MFB Filters in ADC Interface Applications](#), application note.
3. Texas Instruments, [Data Acquisition](#).
4. Texas Instruments, [Filter Design Tool](#).

5 Revision History

Changes from Revision * (December 2024) to Revision A (February 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Wideband Filter Stop-Band Attenuation</i> and <i>Combined Anti-Alias Filter and Digital Filter Response</i> images.....	4

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