Analog Engineer's Circuit

Noninverting Circuit for High-to-Low Voltage Level Translation To Drive ADC

Art Kay

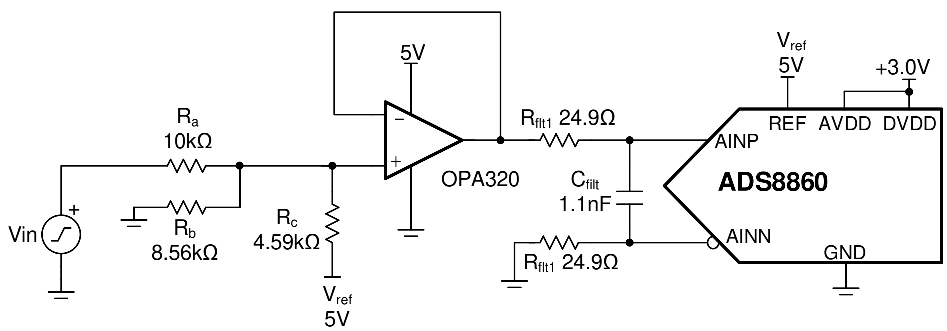
Input	ADC Input	Digital Output ADS8860
–10V	0.2V	$0A3D_H$ or 2621_d
10V	4.8V	$F5C3_H$ or 62915_d

Power Supplies

Vref	AVDD	DVDD
5V	3.0V	3.0V

Design Description

This circuit document describes how to translate a high-voltage signal (for example, ±10V) to a low voltage ADC input (for example, 0V to 5V). This circuit does not require any high-voltage supply to operate, but rather uses a voltage divider and level shift to translate the input signal. This circuit shows the OPA320 op amp and ADS8860 SAR ADC, but the topology applies to many different ADCs. This design can be used in a wide range of applications where a high-voltage input needs to be translated such as *analog input modules* for PLCs, *analytical lab instrumentation,* and *factory automation and control.*



Specifications

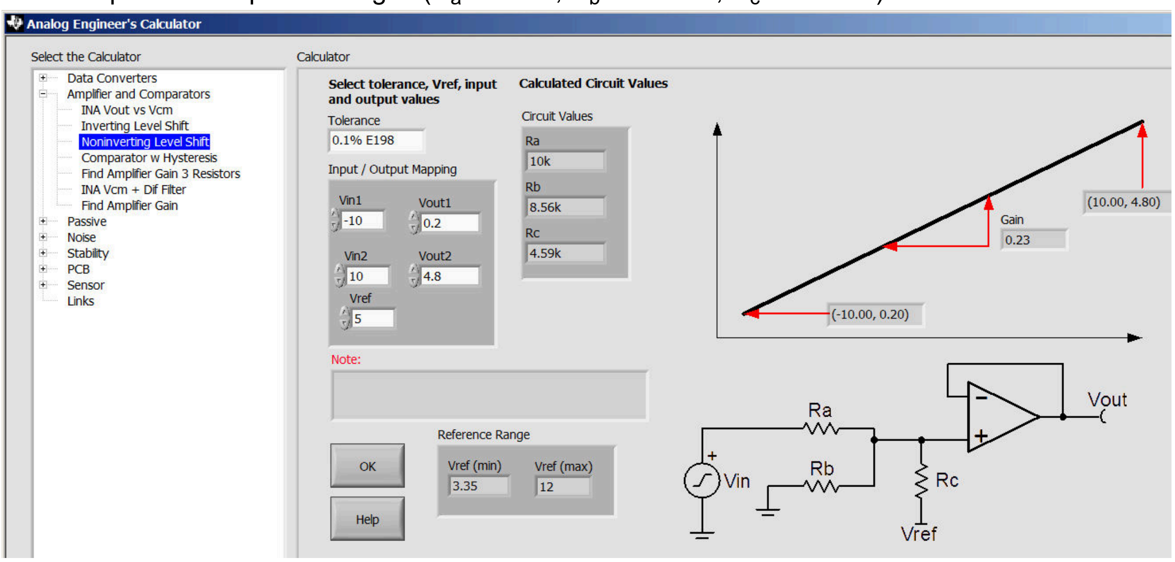
Specification	Goal	Calculated	Simulated
Bandwidth	> 1MHz	2.9MHz	4.06MHz
Noise	< 1/2LSB = 38.1µV	$23.56\mu V_{RMS}$	$21.04N\mu V_{RMS}$
Transient settling error	< 1/2 LSB = 38.1µV		35µV

Design Notes

1. Select a C0G type capacitor for Cfilt to minimize distortion.
2. Use 0.1% 20ppm/°C film resistors or better to minimize gain error and drift.
3. The input impedance of this circuit is $R_{in} = R_a + R_b||R_c$. For a high-impedance input, use a high-voltage amplifier buffer (for example, Vcc = +15V and Vee = –15V). Alternatively, increase the input impedance by multiplying R_a, R_b, and R_c by the same factor. However, increasing the resistance on all the resistors impacts the system noise.

Component Selection

1. The first step is to select the amplifier input and output range. In this example, the input range is –10V to +10V. The amplifier output range is set according to the ADC input and the amplifier linear output range. The ADC input range in this example is set by the reference voltage and is 5V. The amplifier supply is set to 5V to match the ADC input range. The output of the amplifier cannot swing to the power supply rails because of output swing limitations (that is, linear range for OPA320 0.1V < V_{OUT} < 4.9V). For this example, an output swing of 0.2V to 4.8V is selected for the input signal of –10V to 10V. The output range could have been set as 0.1V to 4.9V to match the linear range, but in this example design margin is added to account for power supply variation.
2. Use the *Analog Engineer's Calculator* in the next step to select component values. Enter the input and output voltages and reference voltage (–10V < V_{IN} < +10V, and 0.2V < V_{OUT} < 4.8V). The range of acceptable reference voltages is given at the bottom of the tool (3.35V to 12V, in this example). A reference of 5V is selected as this reference voltage is available elsewhere in the circuit. The tool outputs the 0.1% resistors required to map the voltages (R_a = 10kΩ, R_b = 8.56kΩ, R_c = 4.59kΩ).



3. The following equations show the transfer function for the non-inverting level-shift topology. It is possible to use these equations to solve for the different component values rather than the calculator. To do this, choose a reference value and fix the value of R_a to 10kΩ. Once this is done, solve for R_b and R_c for two different values of output signal. The algebra for this problem is a little complex, so the calculator is the suggested method. Use the equations to verify the transfer function as the equation following shows.

$$V_O = \frac{(R_b \,||\, R_c)}{R_a + (R_b \,||\, R_c)} \cdot V_{IN} + \frac{(R_a \,||\, R_b)}{R_c + (R_a \,||\, R_b)} \cdot V_{ref}$$

where

- $$R_b \,||\, R_c = \frac{R_b \cdot R_c}{R_b + R_c} \text{ and } R_a \,||\, R_b = \frac{R_a \cdot R_b}{R_b + R_c}$$

Using the values from the calculator:

R_a = 10kΩ, R_b = 8.56kΩ, R_c = 4.59kΩ

V_O = 0.23005V × V_{IN} + 2.506V

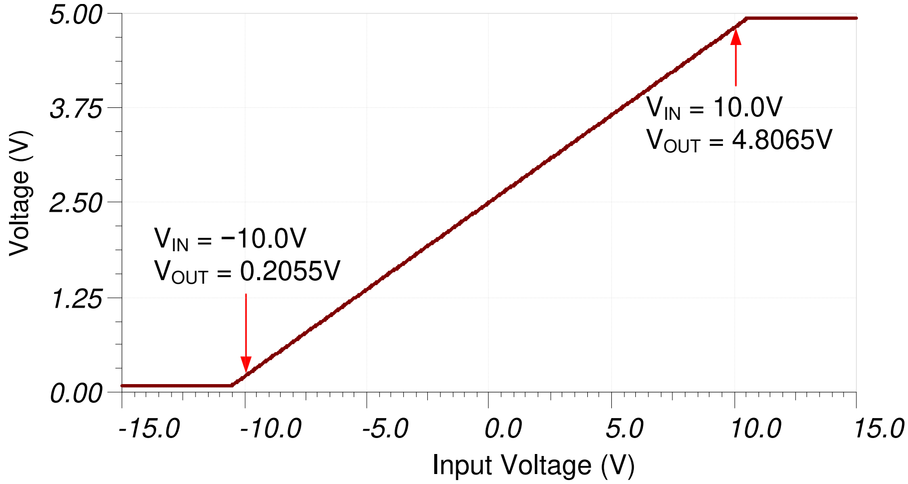
V_O(–10V) = 0.2055V

V_O(+10V) = 4.8065V

4. Find Rfilt and Cfilt to allow for settling at 1Msps. The *Refine the Rfilt and Cfilt Values on ADC drive* video from the *TI Precision Labs - ADCs* video series shows the algorithm for selecting Rfilt and Cfilt. The final value of 24.9Ω and 1.1nF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

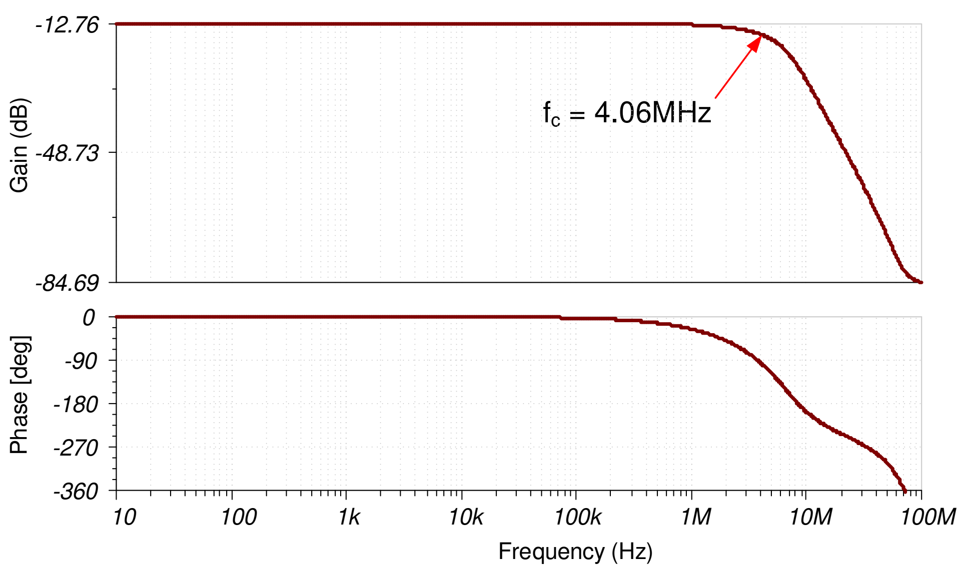
The following graph shows the linear output response for a –10V to 10V input. In this case, the amplifier output is approximately 0.2V for a –10V input and 4.8V for a +10V input. This design was scaled so that the output range avoids the nonlinear power supply rails by 0.2V. See the TI Precision Labs - ADCs *Determining a SAR ADC's Linear Range when using operational amplifiers* video for detailed theory on this subject.



AC Transfer Characteristics

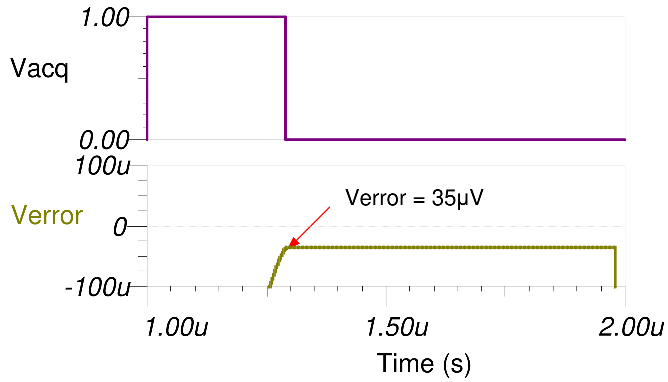
The bandwidth is limited by the RC charge bucket circuit. The calculated and simulated bandwidth compare well (calculated f_c = 2.9MHz, simulated f_c = 4.06MHz). The small discrepancy in the bandwidth is due to gain peaking on the OPA320 device.

$$f_c = \frac{1}{2\pi \cdot (2 \cdot 24.9\Omega) \cdot (1.1\text{nF})} = 2.9\text{MHz}$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a +10-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. See the *Final SAR ADC Drive Simulations* video for detailed theory on this subject.



Noise Simulation

The following noise calculation takes into account the thermal noise of the resistor network, the amplifier noise, and the bandwidth limit from the RC filter. The calculated total noise is 23.5µV_{RMS} and the simulated total noise is 21.04µV_{RMS}. See the *Op Amp Noise Calculation* video for detailed theory on amplifier noise calculations, and the *Calculating the total noise for ADC Systems* video for data converter noise.

Noise equivalent input resistor network:

$$R_{eq} = \frac{1}{\frac{1}{R_a} + \frac{1}{R_b} + \frac{1}{R_c}} = \frac{1}{\frac{1}{10\,k\Omega} + \frac{1}{8.56\,k\Omega} + \frac{1}{4.59\,k\Omega}} = 2.3\,k\Omega$$

Resistor network noise:

$$e_{nReq} = \sqrt{4kTR} = \sqrt{4 \cdot (1.381 \cdot 10^{-23}) \cdot (273 + 25) \cdot 2.3\,k\Omega} = 6.164\,\frac{nV}{\sqrt{Hz}}$$

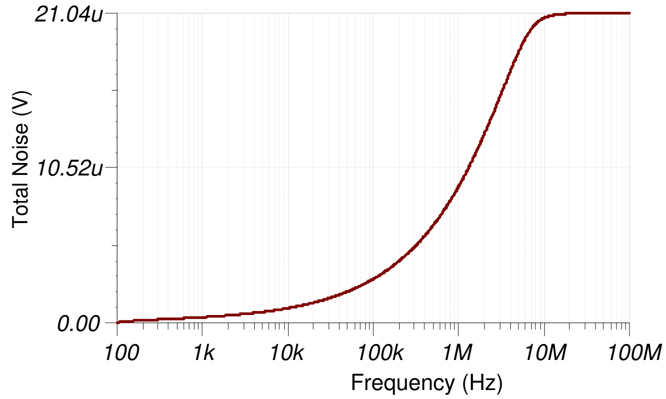
OPS320 noise density:

$$e_{nOPA320} = 7\,\frac{nV}{\sqrt{Hz}}$$

Total noise:

$$e_{nTOT} = \sqrt{e_{nOPA320}^2 + e_{nReq}^2} \cdot \sqrt{K_n \cdot f_c}$$

$$e_{nTOT} = \sqrt{\left(7\,\frac{nV}{\sqrt{Hz}}\right)^2 + \left(6.164\,\frac{nV}{\sqrt{Hz}}\right)^2} \cdot \sqrt{1.57 \cdot 4.06\,MHz} = 23.56\,\mu V_{RMS}$$



Design Featured Devices and Alternative Parts

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1-Msps sample rate, single-ended input, Vref input range 2.5V to 5.0V	16-bit, 1MSPS, 1-channel SAR ADC with single-ended input, SPI and daisy chain	Precision ADCs
OPA320	20-MHz bandwidth, rail-to-rail with zero crossover distortion, V_{OS}(MAX) = 150µV, V_{OS}(DriftMAX) = 5µV/°C, e_n = 7nV/$\sqrt{Hz}$	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	Operational amplifiers (op amps)

Link to Key Files

Texas Instruments, SBAC250 sources files, software support

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