Application Report
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Impact of Power-Supply Noise on Phase Noise Performance of RF DACs

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ABSTRACT

This application report examines the impact of power-supply noise on an on-chip sampling clock, and consequently, on the output performance of a radio-frequency (RF) digital-to-analog converter (DAC). Through theoretical analysis and practical measurement using TI's RF DAC devices, the DAC38RF8x and DAC38RF9x, this article gives the quantized requirement for the power supply, and provides an efficient and direct guide for DAC applications.

Contents

List of Figures

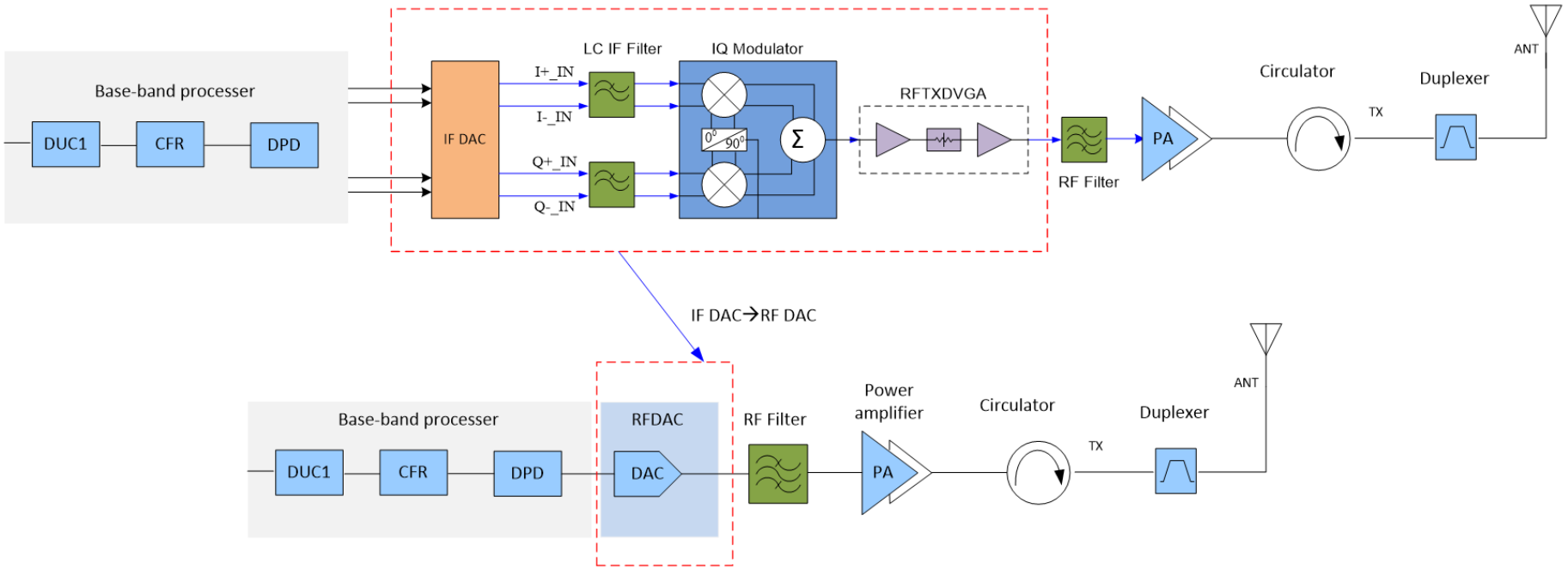
List of Tables

Trademarks

1 Introduction

The digital-to-analog converter (DAC) is a key device component in modern wireless communication products, and DAC performance dominates the entire transmit signal path in the radio remote unit (RRU). Along with the development of advanced IC technology, RF-sampling DACs can directly sample at the RF frequency. Figure 1 shows how compared to an intermediate-frequency (IF) sampling DAC, an RF DAC gives the system designer a better integration solution with fewer components, and achieves a software-defined radio to give the designer more flexibility. RF DACs are gaining wide popularity in fourth generation (4G) wireless systems, such as the macro FDD and TDD systems.

Figure 1. IF DAC Solution Versus RF DAC Integrated Solution



2 Theoretical Analysis

In this section, we discuss how the quality of power supply affects the phased-locked loop (PLL) output phase noise through basic PLL theory analysis.

Figure 2 shows a typical block diagram of the PLL, and the PLL transfer function.

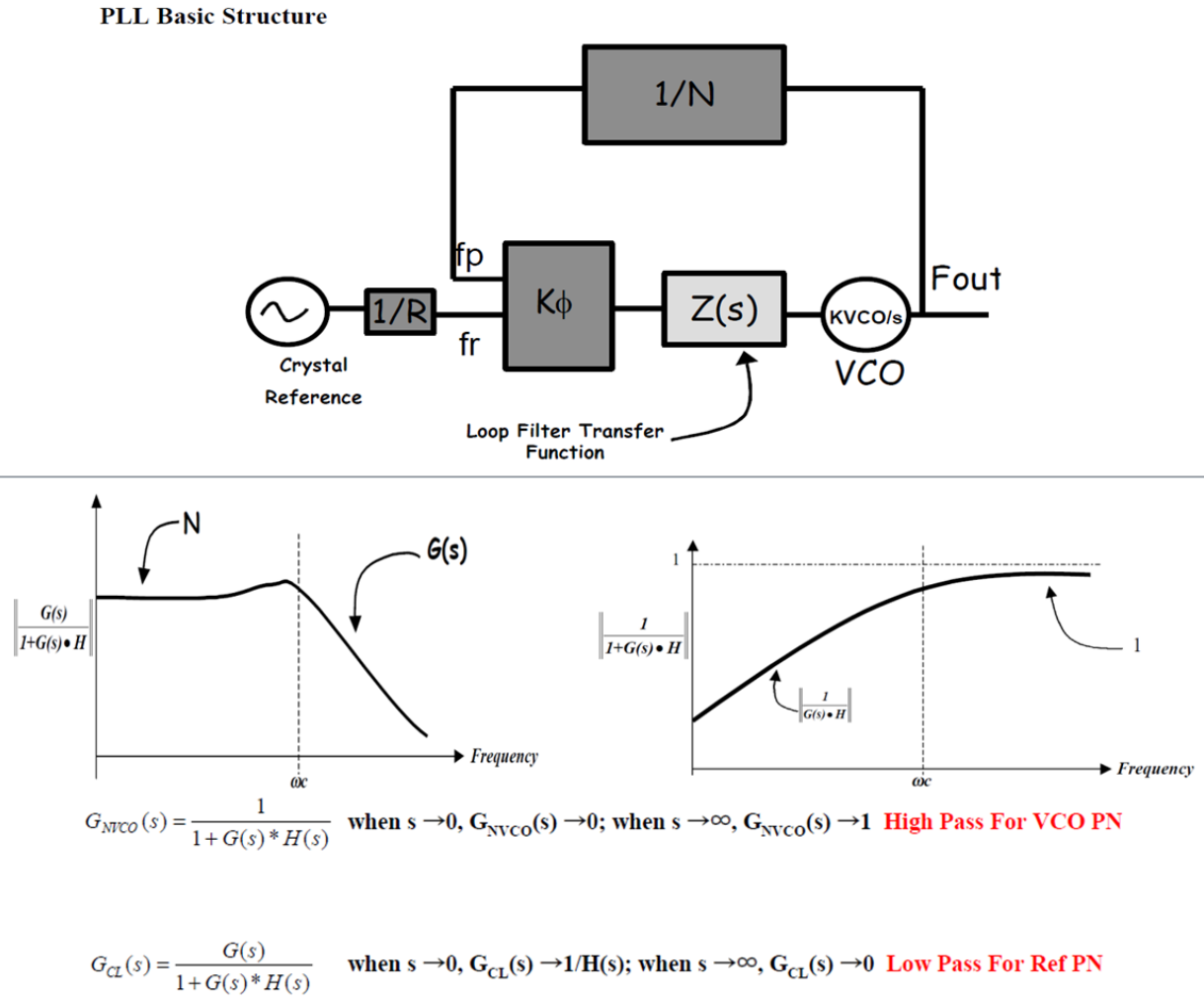


Figure 2. Typical Block Diagram of the PLL and the PLL Transfer Function

Figure 2 shows the typical block diagram of PLL, and the PLL noise transfer function. The ω denotes the PLL loop bandwidth. Based on the PLL transfer function, noise injected in the voltage-controlled oscillator (VCO) passes high-pass filtering at the PLL output, whereas noise injected in other parts passes low-pass filtering.

Based on the two types of PLL transfer functions, the PLL power-supply noise is divided into two related components: the VCO power supply noise and the non-VCO power-supply noise.

Power-supply noise is usually lower-frequency noise (< 1 MHz), so it is easily understood that non-VCO power-supply noise impacts the PLL phase noise because of the low-pass filter characteristics. On the other hand, VCO power-supply noise can be ignored because VCO power-supply noise has high-pass filter characteristics, and thus filters the low-frequency noise. Take extra care here because there is no absolute high-pass or low-pass filter; the VCO filter suppression depends on the PLL loop bandwidth setting. The PLL loop bandwidth controls the transition zone range. Therefore, if the loop bandwidth is

narrow (for example, 100 kHz), then the transition zone of the VCO transfer function is also very narrow, and there is almost no suppression for low-frequency power-supply noise. In such cases, the VCO power-supply low-frequency noise impacts on the PLL output directly. In a real application, always remember to choose a low-noise power supply for the non-VCO power design, but ignore the VCO power noise. This application report focuses on the analysis of VCO power supply noise impact on the PLL phase noise.

Based on the previous analysis, the following two methods improve the VCO power supply noise suppression:

- Increase the PLL loop bandwidth. The VCO noise transfer function is a high-pass type; therefore, when the loop bandwidth increases, the transition zone range increases as well, and low-frequency suppression is stronger. In that sense, the low-frequency noise of power supply must be well suppressed.
- Choose a good PSRR for the VCO power supply. Good VCO PSRR is also able to do a good job of suppressing the close-in phase noise.

3 Practical Measurement of Increasing the PLL Loop Bandwidth and Using a Better VCO Power Supply

In order to demonstrate the VCO power-supply noise impact on the PLL output phase noise, use a power supply with bad noise at 10 kHz offset, and assume a PSRR of 35 dB at 10 kHz. The following measurement shows the power noise effect at both a narrow and wide PLL loop bandwidth.

First, a narrow loop bandwidth measurement is performed. The internal PLL of the RF DAC multiplies the external reference clock (245.76 MHz) by 36 to 8847.36 MHz. The PLL loop bandwidth is set to 200 kHz and the phase noise of DAC can be observed when generating an output CW tone at 2605 MHz using the internal digital NCO, as shown in Figure 3.

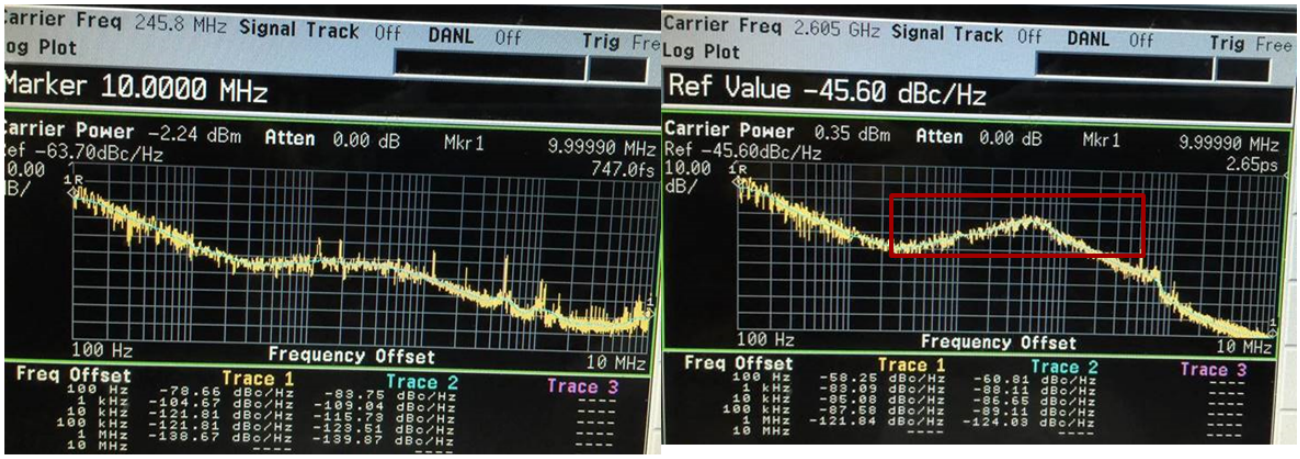


Figure 3. PLL Reference Clock Phase Noise (Left), and Abnormal DAC Output Phase Noise at 2605 MHz at 200-kHz PLL Loop Bandwidth (Right)

The phase noise plot on the left of Figure 3 shows the external reference clock 245.76 MHz. The plot on right side is the phase noise of CW tone at 2605 MHz. The DAC output CW-tone phase noise is used to represent the internal PLL/VCO performance. According to the basic theory of PLL, inside the PLL loop bandwidth, the PLL output phase noise is dominated by the reference input phase noise, and the in-band phase noise of PLL output is a scaled version of reference input by 20log(Fout / Fin). In this example, Fin is 245.76 MHz and Fout is 2605 MHz; therefore, the close-in (< 200-kHz offset) output phase noise is from the corresponding reference clock noise scaled up by 20.5 dB (20log(2605 / 245.76)). Table 1 shows that the phase noise from 10 kHz to 100 kHz deviates a lot from the expected number in theory, which is degraded compared to 20log(Fout / Fin) curve, and shows an obvious hump at around the 10-kHz offset (highlight in the red square).

Table 1. Comparison Between PLL Input and Output Phase Noise With Narrow Loop Bandwidth

Input Reference Clock		Output Clock		Delta Number
Offset	Phase Noise	Offset	Phase Noise	Pout-Pin
100 Hz	–78 dBc/Hz	100 Hz	–58 dBc/Hz	20 dB
1 kHz	–104 dBc/Hz	1 kHz	–83 dBc/Hz	21 dB
10 kHz	–121 dBc/Hz	10 kHz	–85 dBc/Hz	36 dB
100 kHz	–121 dBc/Hz	100 kHz	–87 dBc/Hz	34 dB

The close-in phase noise degradation at the DAC output degrades the in-band signal quality, and thus system transmit performance. By calculating integrated jitter from phase-noise measurement plot, the error vector magnitude (EVM) is degraded to ~6%, as shown in Figure 4, and does not meet the customer requirement of 3%.

100HZ	1KHZ	10KHZ	100KHZ	1MHZ	Jitter1	Jitter2	Jitter3	Jitter4	Jitter total	EVM
-58	-83	-85	-87	-121	-31.454163	-44.3434	-36.3434	-30.47	0.001883	6.14

Figure 4. Signal EVM With the Phase Noise From Table 1

The same measurement is repeated, increasing the PLL loop bandwidth from 200 kHz to 5 MHz, as shown in Figure 5. Now there is no obvious bump around the 10-kHz offset. Table 2 shows that the close in phase noise matches the 20log(Fout / Fin) curve very well.

Figure 5. PLL Reference Clock Phase Noise (Left), and Normal DAC Output Phase Noise at 2605 MHz at 5-MHz PLL Loop Bandwidth (Right)

Table 2. Comparison Between PLL Input and Output Phase Noise With Wide Loop Bandwidth

Input Reference Clock		Output Clock		Delta Number
Offset	Phase Noise	Offset	Phase Noise	Pout-Pin
100 Hz	–84 dBc/Hz	100 Hz	–61 dBc/Hz	23 dB
1 kHz	–108 dBc/Hz	1 kHz	–88 dBc/Hz	20 dB
10 kHz	–114 dBc/Hz	10 kHz	–95 dBc/Hz	19 dB
100 kHz	–123 dBc/Hz	100 kHz	–103 dBc/Hz	20 dB

The close-in phase noise degradation at the DAC output degrades the in-band signal quality. By calculating integrated jitter from phase noise measurement plot, the EVM is improved to ~3%, as shown in Figure 6, and meets the customer requirement of 3%.

100HZ	1KHZ	10KHZ	100KHZ	1MHZ	Jitter1	Jitter2	Jitter3	Jitter4	Jitter total	EVM
-61	-88	-95	-103	-115	-34.459218	-50.6778	-47.829	-46.20	0.000407	2.85

Figure 6. Signal EVM With the Phase Noise From Table 2.

Furthermore, by using a larger loop bandwidth, the DAC output signal adjacent channel power ratio (ACPR) is degraded. By changing from a 200k to a 5M loop bandwidth; the ACPR degrades from 71 dBc to 66 dBc, as shown in Figure 7. Therefore, in wireless communication products, a larger loop bandwidth cannot be used; usually, the ACPR must achieve 70 dBc.

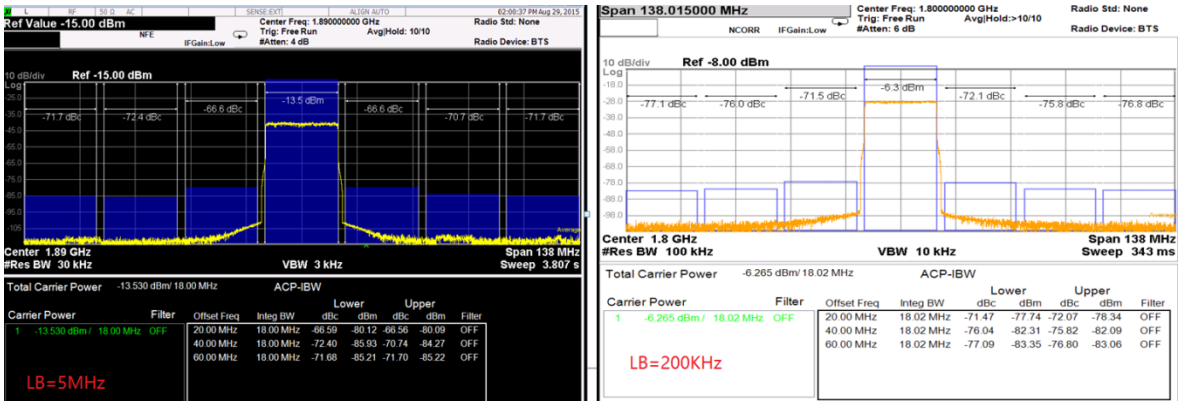


Figure 7. ACPR With 5-MHz PLL Loop Bandwidth (Left), and ACPR With 200-kHz PLL Loop Bandwidth (Right)

Practical measurement of using better power supply also had been done . Compared with PSRR of 35 dB at a 10-kHz power supply , a comparison measurement is done by using TI's TSP7A84 LDO that has a PSRR at 10-kHz offset of 57 dB, as shown in Figure 8 (right) . Now the DAC output phase noise at 10-kHz offset is significantly improved from –77 dBc to –94 dBc; a 17-dB improvement.

Figure 8. Phase Noise Improved by Using Good PSRR for the PLL VCO Power Supply

In order to get the good EVM and ACPR of an RF DAC output signal, choose a good performance LDO. In this case, TI's TPS7A84 allows the system to achieve EVM (1.35%) and ACPR (71 dBc) at 2.6-G RF DAC output.

4 Summary

The wireless system has a relatively tight requirement for TX ACPR performance, so good ACPR performance is achieved by using a narrow PLL loop bandwidth. In that sense, make sure to get good power-supply performance for the PLL. From the practical measurement conducted in this application report, the PLL VCO power supply must have a PSRR specified > 50-dB at 10 kHz, and power-supply noise must be < 10 µV. The guidance to design a power supply for an RF DAC using the 3-A TPS7A84 LDO provides overall greater system performance.

5 References

- Texas Instruments, *DAC38RFxx Dual- or Single-Channel, Single-Ended or Differential Output, 14-Bit, 9-GSPS, RF-Sampling DAC With JESD204B Interface and On-Chip PLL Data Sheet*
- Texas Instruments, *TPS7A84 High-Current (3 A), High-Accuracy (1%), Low-Noise (4.4 µVRMS), LDO Voltage Regulator Data Sheet*
- Dean Banerjee (2001). *PLL Performance, Simulation, and Design, Second Edition*

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