参考資料

Design Guide: TIDA-050063

高電圧ソリッドステート・リレー・アクティブ・プリチャージのリファレンス・デザイン

概要

このリファレンス・デザインでは、ハイブリッド電気自動車 (HEV) と電気自動車 (EV) 向けに大規模な DC リンク・コンデンサを事前充電する革新的な回路トポロジを紹介します。このリファレンス・デザインは、マイクロコントローラを必要とせず、5V 電源で動作できるシステムを採用しています。このリファレンス・デザインは、TPSI3052-Q1 を使用して、5kV$_{RMS}$ の強化絶縁定格を実現しています。TPSI3052-Q1 デバイスは、絶縁を実現すると同時に信号と電力を 2 次側に伝送するラミネート・トランスを内蔵しています。その結果、個別の絶縁型バイアス電源が不要になります。加えて、TPSI3052-Q1 デバイスは、回路監視用に高電圧 (HV) 側にある外部回路に電力を供給できます。このリファレンス・デザインは、最大 800V のシステムをサポートでき、最大 4A$_{AVG}$ の充電電流で最大 2mF の負荷容量を充電できます。

リソース

TIDA-050063	デザイン・フォルダ
TPSI3050-Q1、TPSI3052-Q1	プロダクト・フォルダ
TLV7011、UCC27517A-Q1	プロダクト・フォルダ

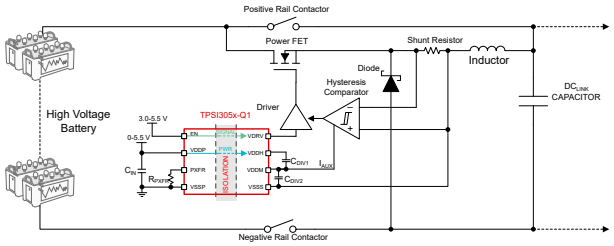
テキサス・インスツルメンツの TI E2E™ サポート・エキスパートにお問い合わせください

特長

- 5kV$_{RMS}$ に耐える強化絶縁
- 絶縁型バイアス電源を内蔵
- 800V のパワートレイン・アーキテクチャをサポート
- 4A$_{AVG}$、8A$_{PK-PK}$ の最大充電電流
- 2mF のコンデンサを 400ms で 800V まで充電可能

アプリケーション

- ソリッドステート・リレー (SSR)
- バッテリ管理システム
- オンボード・チャージャ
- ハイブリッド車、電気自動車、パワートレイン・システム



English Document: TIDUF21

1 System Description

This reference design introduces an active precharge circuit which is essentially a buck converter topology to achieve the precharge for high voltage (HV) DC link capacitors. This reference design will talk through the reasons for adopting an active precharge approach instead of a traditional resistive implementation. The operation of the reference circuit will be explained and analyzed in detail.

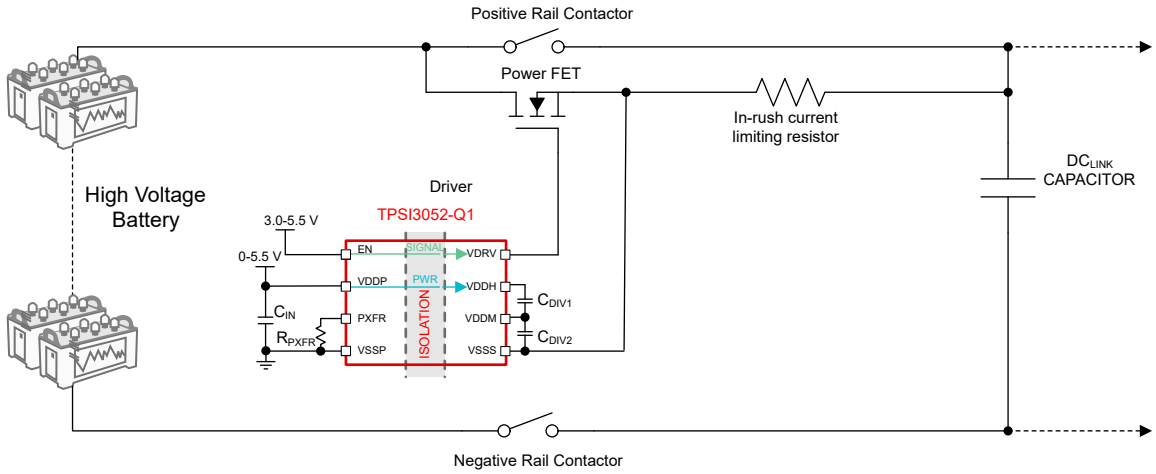


図 1-1. Resistor Precharge Design Using SSR

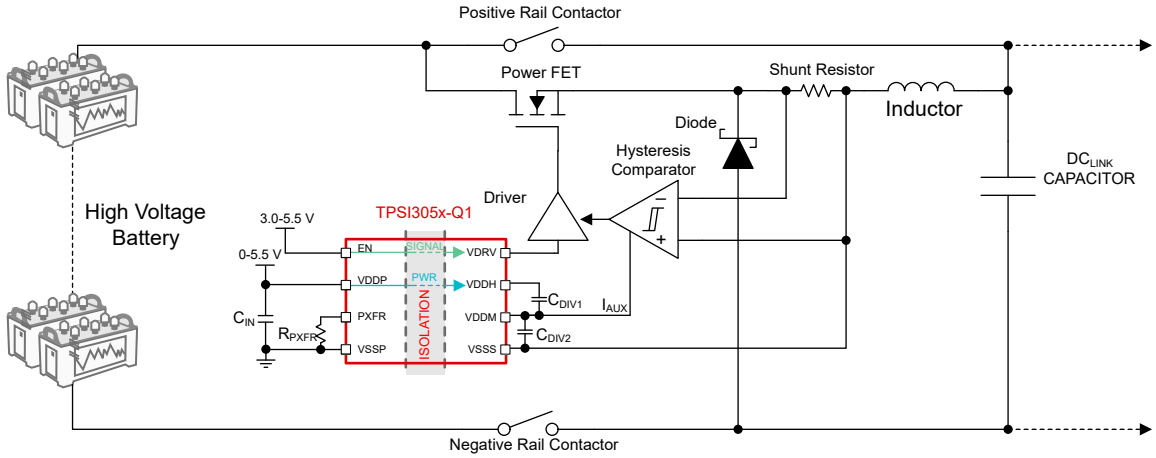


図 1-2. Active Precharge Design

The benefits of an active precharge solution can be seen from a power analysis perspective. Many existing high voltage batteries for HEV and EV market use a 400-V architecture with typical system's capacitance in the order of milli-Farads. The only value missing to complete the equation is the charging time for the capacitors. Usually these charging times allow for up to 400-ms delay approximately. The following calculations show the peak and average power across the resistor for the mentioned values.

$$R = \frac{charging\ time(s)}{5 \times C} = \frac{400\ ms}{5 \times 2\ mF} = 40\ \Omega \quad (1)$$

In equation (1) a factor of 5 time constants (5τ) is assumed for the charging time which provides that the voltage on the capacitor is 99% of the input voltage.

$$P_{PEAK} = \frac{V^2}{R} = \frac{(400\ V)^2}{40\ \Omega} = 4000\ W \quad (2)$$

$$P_{AVG} = \frac{Energy}{time\ (s)} = \frac{C \times V^2}{2 \times\ time} = \frac{\left(2\ mF\right)(400\ V)^2}{2(400\ ms)} = 400\ W \quad (3)$$

These calculations are taking the assumption that the system is a 400-V system. However, the HEV/EV industry has shown signs of planning to move to 800-V systems. This increase in voltage leads to lower currents, leading to lower DC conduction losses. By increasing the voltage, power can be supplied using less current. Less current allows to reduce the required size for the cables and required copper which effectively reduces the overall weight of the car and the cost for the system. Optimizing the weight allows to optimize the efficiency of the vehicle. In addition, 800-V systems allow for faster charging since the lower current reduces the overheating of the conductors and the battery. On the other hand, increasing the battery voltage to 800-V makes the DC link capacitor precharge more challenging. If the system needs to be precharged using the same charging time of 400-ms, the power requirements for the resistor can be described as resulting in four times higher power.

$$P_{PEAK} = \frac{V^2}{R} = \frac{(800\,V)^2}{40\,\Omega} = 16000\,W \tag{4}$$

$$P_{AVG} = \frac{Energy}{time\ (s)} = \frac{C \times V^2}{2 \times\ time} = \frac{\left(2\,mF\right)(400\,V)^2}{2(400\,ms)} = 1600\,W \tag{5}$$

Typical resistors that can meet these requirements are large, costly, heavy, and not as common or available as low-power resistors. In addition, using a resistor for the precharge is not very efficient and the increased power loss leads to more heat and increased temperature rise. The question that follows here, after describing the limitations for the resistor is simple. What other electrical component can be used to control current? Here is where the active precharge circuit topology comes as a buck converter topology configuration to precharge the DC link capacitor using an inductor to limit the current.

An inductor does not allow sudden current changes and stores the energy in the form of a magnetic field. An ideal inductor is essentially loss-less and the energy stored is not converter to heat. However, in reality, the quality factor of the inductor *Energy Stored / Energy Dissipated* can affect the efficiency of the system. Usually, the resistance of the inductor is very small and the power dissipated can be insignificant compared to a resistor precharge design.

2 System Overview

2.1 Block Diagram

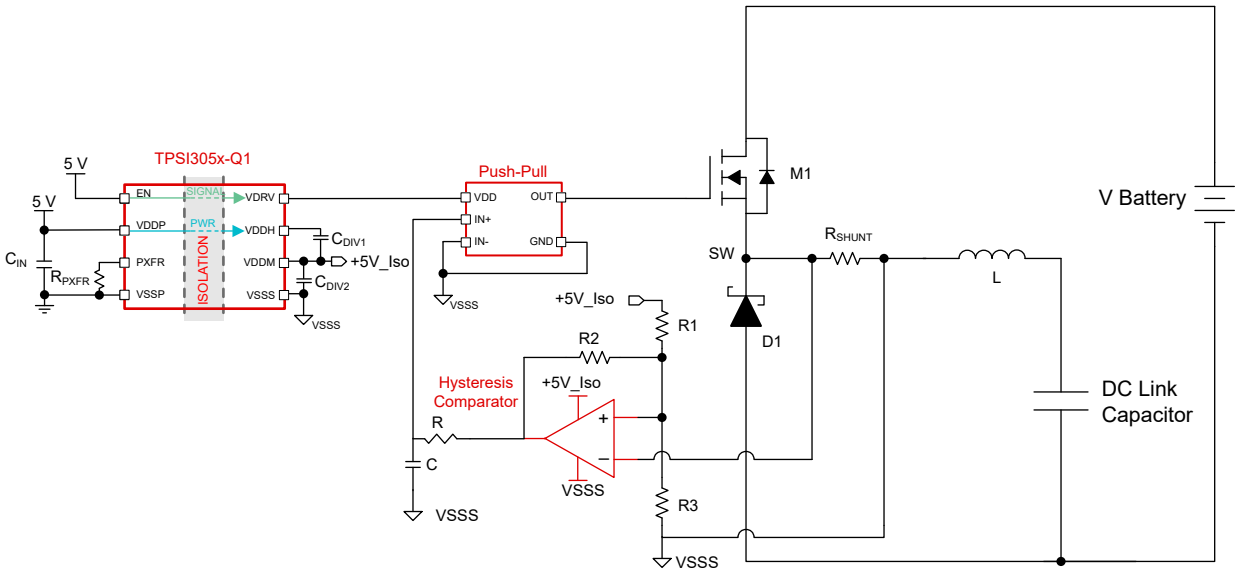


図 2-1. Block Diagram

2.2 Design Considerations

The active pre-charge topology takes advantage of the inductor electrical properties and charges the capacitor with an average current produced by connecting a disconnecting the inductor to the battery. The control circuitry that controls the FET ON/OFF cycle is described in detail below.

2.2.1 Description of Control Logic

For simplicity, EN and VDDP signals are both connected to the same supply and both are provided simultaneously. Before VDDP and EN signal are provided, M1 is opened and the inductor is disconnected from the system. When VDDP and EN are provided, TPSI3052-Q1 begins to transfer power to the secondary side and after VDDH is above its UVLO, then precharging begins. TLV7011 comparator and UCC27517A-Q1 driver are powered from the TPSI3052-Q1 device. The hysteresis comparator is explained in detail in the Comparator with Hysteresis Reference Design reference design. The comparator can be considered as a hysteresis comparator with VTH (high threshold) and VTL (low threshold). With the following conditions.

- V (R_{SHUNT}) = V_H → TLV7011 outputs 0 V → FET OFF

- V (R_{SHUNT}) = V_L → TLV7011 outputs 5 V → FET ON

The voltage across R_{SHUNT} can be determined as I×R. Essentially the current to the inductor is controlled by the voltage across R_{SHUNT}. The hysteresis comparator is described with the following equations. It is recommended to select R2 > 10 kΩ to minimize the current draw of the circuit.

$$\frac{R_2}{R_1} = \frac{V_L}{V_H - V_L} \tag{6}$$

$$\frac{R_3}{R_1} = \frac{V_L}{+5V\_Viso - V_H} \tag{7}$$

$$V_H = I_{PEAK} \times R_{SHUNT} \tag{8}$$

$$V_L = I_{MIN} \times R_{SHUNT} \tag{9}$$

V_L = falling hysteresis threshold which determines I_{MIN}

V_H = rising hysteresis threshold which determines I_{PEAK}

+5V_Iso = 5-V VDDM supply from TPSI3052-Q1 powering TLV7011

R_{SHUNT} = Shunt resistor for current sensing

TPSI3052-Q1 provides power to the control circuitry, but has limited power transfer capability. Aim to reduce the current draw from the control circuitry so that power can be allocated to the charging and discharging of the FET gate during switching at the desired switching frequency. Equations 6 and 7 show the relation between switching frequency, drive current, drive voltage, and total gate charge.

$$I_{DRIVER\_MAX} = Q_g \times F_{MAX} \tag{10}$$

$$P_{DRIVER\_MAX} = I_{DRIVER\_MAX} \times V_{DRIVER} \tag{11}$$

F_{MAX} = maximum switching frequency required for the active precharge

I_{DRIVER_MAX} = maximum driver current when the switching frequency is F_{MAX}

P_{DRIVER_MAX} = maximum power demand to achieve the expected F_{MAX}

2.2.2 Behavior Throughout Charge Cycle

Since no current is flowing through R_{SHUNT} initially, the circuit logic turns ON transistor M1. When transistor M1 is turned ON, the current through the inductor begins rise following constant rate of charge as shown in I of 図 2-2. Once the current in the inductor has increased such that the voltage across R_{SHUNT} generates a voltage V_H and the output of the comparator switches to 0-V. At this point transistor M1 is turned OFF. When this transistor is switched OFF, the current flow through the inductor tries to continue flowing in the same direction. The magnetic field of the inductor will force a negative voltage on the switch node (SW). Once the voltage has reached the forward voltage drop of the free-wheeling diode D1, this diode will turn ON creating a negative voltage across the inductor and the current through the inductor begins to decrease as shown in 図 2-2. When the current through the inductor creates a voltage across R_{SHUNT} equal to V_L, the output of the comparator will go high to 5-V. At this point transistor M1 is turned ON and the switching cycle repeats until the output voltage in the capacitor equals the input voltage. Once the output voltage equals the input voltage no current will flow in the inductor and the transistor M1 will remain on until the precharge circuit is turned off.

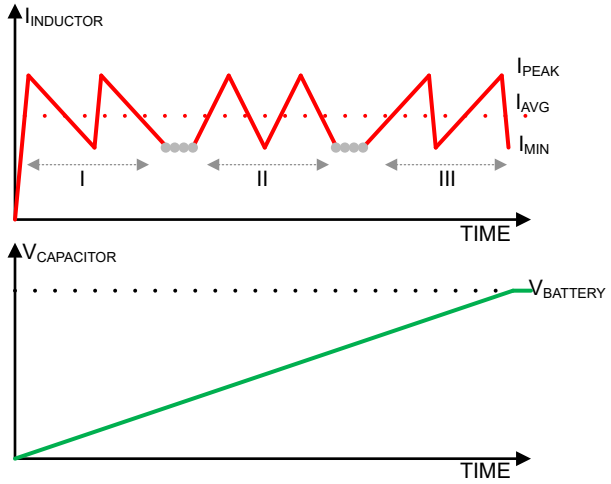


図 2-2. Charging Plot Behavior

The current through the inductor can be studied by separating it into three different sections I, II, and III. See 図 2-2. It is necessary to separate the current into these three sections and understand the dependencies because the behavior will directly affect the design requirements. Section I and III have the fastest slew rate. This fast slew rate is due to the high voltage across the inductor. Initially the capacitor does not have any charge and the voltage across the inductor when M1 is ON would be the battery voltage. Slew rate must be carefully taken into account when selecting the comparator and the push-pull driver. The propagation delay of these components will add up to the overall control loop delay.

The following equation describes the behavior for the slew rate. The fastest slew rate occurs at the beginning of the pre-charge cycle, where V is equal to the system voltage (for example, 800-V). Therefore only the inductance value can be manipulated to set the peak slew rate. The higher the inductance the lower the slew rate for the current through the inductor.

$$\frac{dI}{dt} = \frac{V}{L} \tag{12}$$

For example, if a 800-V system with a 560-uH inductor is designed to have a I_{PEAK} of 8-A, the di/dt is 1.429-A/us, and the loop propagation delay is 1-us. Then the effective I_{PEAK} will be 9.429-A instead of 8-A.

In addition to the slew rate, another important specification is the maximum required switching frequency. Since TPSI3052-Q1 has a limited power transfer, it is required and critical to ensure that TPSI3052-Q1 can achieve the expected switching frequency after providing power to the control loop devices. The following equation describes the relation between the maximum switching frequency seen during the precharge cycle and the design components. There are only two design parameters that can be set to ensure that the switching frequency remains low. Inductance and the current swing dI. At this point it is easy to see that the inductor is a critical components for this design. High inductance value with high current rating would the best options to limit the

switching frequency and the slew rate for the system. Once the maximum switching frequency seen during precharge for the design is calculated, use the TPSI3052-Q1 excel calculator to make sure the TPSI3052-Q1 can supply the necessary power at that switching frequency.

$$F_{MAX} = \frac{Vbatt/2}{2 \times L \times dI} \quad (13)$$

V_{batt} = battery voltage

L = inductance

dI = inductor peak-to-peak current

Now that all the equations and limitations have been studied and defined with equations, it can be easier to go through the design procedures for this reference design.

表 2-1. Design Requirements

Specifications	Max	Comments
Battery voltage	800-V	The case of 800-V system was used for this design procedure.
Total system capacitance	2-mF	This value represents the addition of all the capacitance on the HV DC-link bus.
Required charging time	400-ms	Duration of time the capacitor needs to charge from fully discharged, 0-V, up to the battery voltage level, 800-V. A short precharge time is preferred so that the vehicle starts quickly after power on.
Maximum Switching frequency	50-kHz	The switching frequency is limited by the maximum power transfer by the TPSI3052-Q1. Dependent on the total gate charge (Qg) of the FET, the inductance and the allowed ripple current.

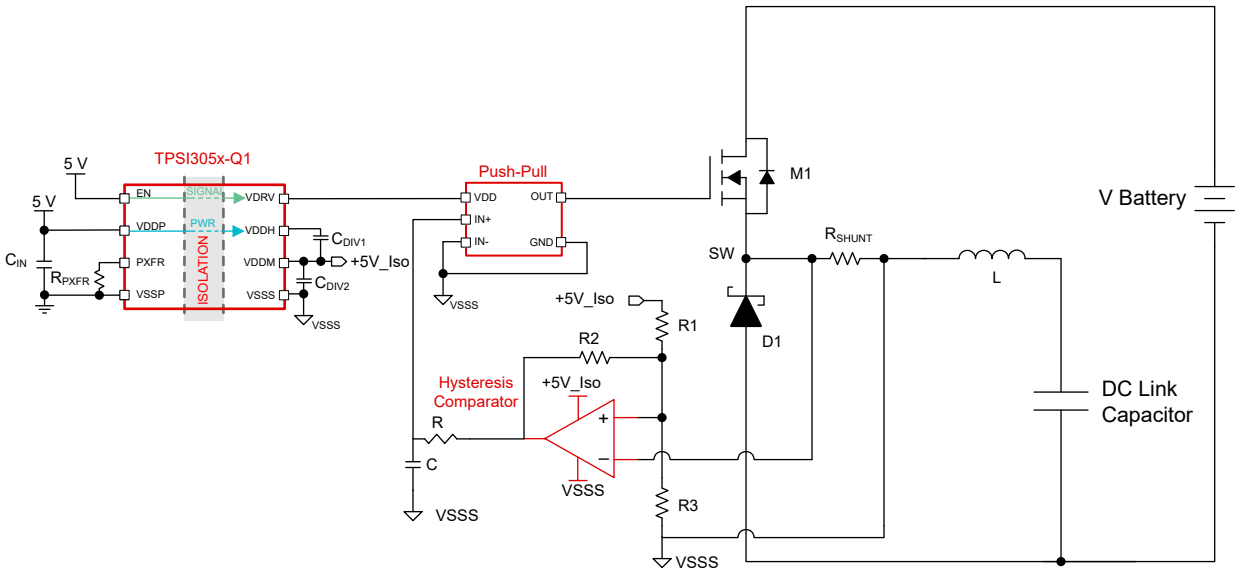


図 2-3. Block Diagram

The first value to calculate for the design is the required average current to precharge the capacitor within the required time.

$$I = C\frac{dV}{dt} = \frac{(2\,mF)(800V)}{(400\,ms)} = 4\,A \quad (14)$$

The average current is important for the charging time requirements, but even more important for this system is the peak-to-peak current (dI). Since the switching frequency must be limited, then dI must be large enough to maintain the switching frequency bounded. For this design the selected I_{PEAK} is 8-A and the I_{MIN} 0.5-A which results in a total dI of 7.5-A. In addition, the inductance value would be another critical parameter to help reduce the switching frequency. The inductor selected for this design has an inductance of 560-uH, a saturation current

rating of 8.6-A, a RMS current rating of 4.6-A, and a voltage rating of 1000-V. This inductor satisfy our voltage rating or 800-V, I_{PEAK} 0f 8-A, and I_{AVG} of 4-A. The following equations describe the expected maximum switching frequency for the system and the maximum slew rate.

$$F_{MAX} = \frac{Vbatt/2}{2 \times L \times dI} = \frac{400\,V}{2(560\,uH)(7.5\,A)} = 47\,kHz \quad (15)$$

$$\frac{dI}{dt} = \frac{V}{L} = \frac{800\,V}{560\,uH} = 1\,A/us \quad (16)$$

The previous equation describes the fastest current slope. This happens when the pre-charge has just started and the voltage on the capacitor is 0-V. This value is critical because if the control loop has a 1-us propagation delay, then the peak current can be 1-A higher than expected. Once I_{PEAK} and I_{MIN} are determined, then the thresholds for the comparator must be calculated and from there the resistors for the hysteresis. The following equations show how to calculate these values.

$$V_H = I_{PEAK} \times R_{SHUNT} = 8\,A \times 100\,m\Omega = 800\,mV \quad (17)$$

$$V_L = I_{MIN} \times R_{SHUNT} = 0.5\,A \times 100\,m\Omega = 50\,mV \quad (18)$$

$$\frac{R_2}{R_1} = \frac{V_L}{V_H - V_L} = \frac{50\,mV}{800\,mV - 50\,mV} \approx 0.06666 \quad (19)$$

$$\frac{R_3}{R_1} = \frac{V_L}{+5V\_Viso - V_H} = \frac{50\,mV}{5\,V - 800\,mV} \approx 0.0119 \quad (20)$$

If R_1 = 200 kΩ, then R_2 = 13.3 kΩ, and R_3 = 2.38 kΩ.

The final step to complete the design is selecting the FETs and free wheeling diode. For the FETs, it is recommended to select FETs with low gate charge (Q_g). Low Q_g will allow the TPSI3052-Q1 to achieve higher switching frequency. Visit the following excel calculator to assist calculating the max switching frequency depending on the total Q_g.

2.2.3 Additional Design Recommendations

- Comparator recommendations:
  - When selecting the comparator for the design, ensure that it has a low supply current. The calculator previously provided for the TPSI3052-Q1 will help make sure that the TPSI3052-Q1 can supply power for this comparator and achieve the expected switching frequency. Power the comparator from VDDM (+5V) rail to consume less power.
  - Do not load the output of the comparator and make sure to place an output resistance to limit the loading conditions. It is recommended to have a 200-Ω resistor between the comparator output and the FET driver input.
  - At the input of the comparator it is recommended to include a fast-recovery Scottky diode and resistor to clamp any negative transient voltages generated from the inductor that might damage the input of the comparator.
  - It is recommended to add a place holder for C8 to filter any high frequency noise that might falsely trigger the comparator
  - Select R8 to be greater than 10-kΩ to minimize power dissipation
- For the inductor it is recommended to use a shielded inductor to minimize the noise produce by switching the inductor. In addition, it is critical to mention that the inductor used for this reference design is not an automotive qualified inductor. This reference design serves as a prove of concept and not a complete solution. However, the inductor is rated for the voltages and currents needed for the reference design.
- It is recommended to add D1 for testing purposes as shown in Figure 2-4. When the inductor is disconnected from the battery and left floating with the capacitor, this can result in oscillations at the output of the circuit. This concern was discovered during simulations.
- R9, C7, and D3 may be used if creating a forced minimum OFF-time is desired. This will reduce the maximum switching frequency, however it may also lead to DCM operation, which may cause ringing of the switch node at various frequencies, potentially affecting EMI performance. Adding this minimum off time may allow to reduce the inductance value, but may required a faster control loop.

- It may be desired to block bidirectional current flow when precharge is disabled. The circuit shown can allow currents to flow back to the battery even when disabled due to the body diode of the FET. This current flow can be blocked by use of a standard precharge contactor in series with the MOSFET which also provides galvanic isolation. Alternatively, a FET can be placed in series with the switching FET between the R_{SHUNT} and the inductor such that the source of this blocking FET is tied to VSSS and the gate tied to the TPSI3052-Q1 VDDH power supply. This allows the FET to be enabled while TPSI3052-Q1 is providing secondary power and the body diode is oriented to block reverse currents when disabled.

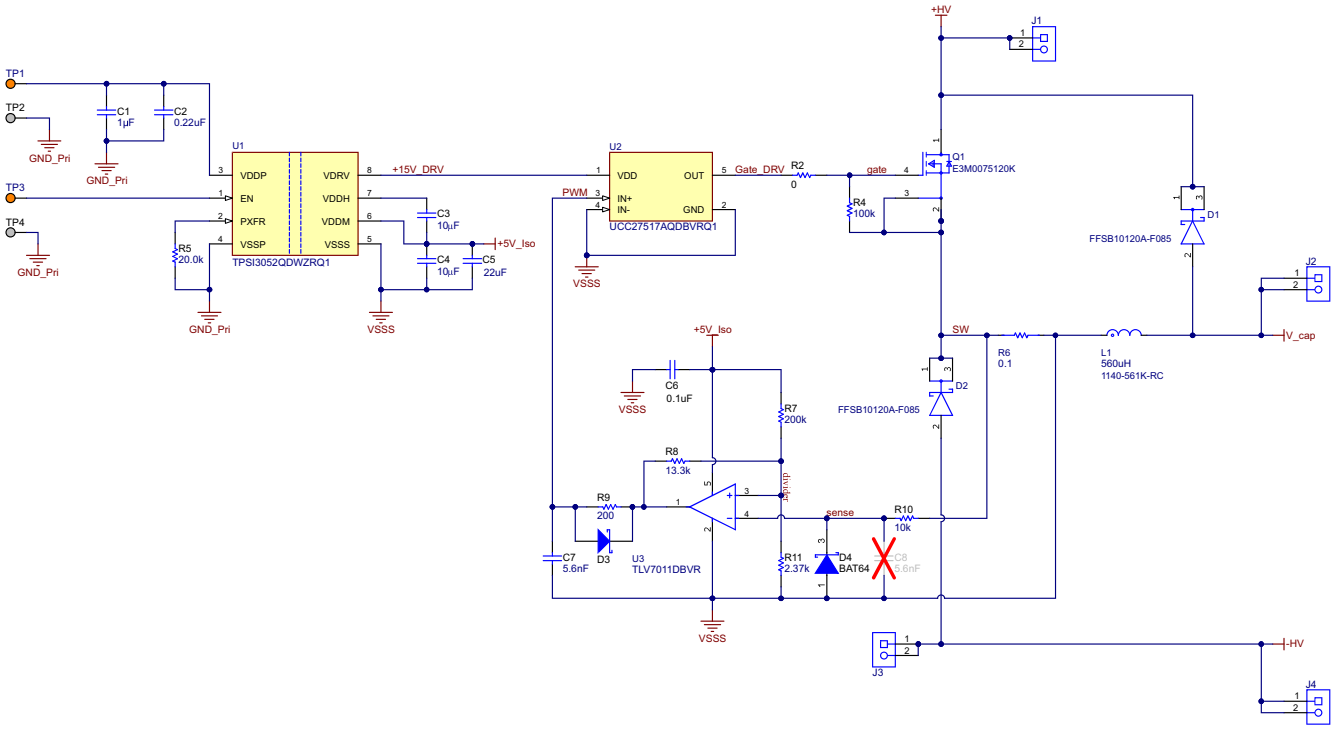


図 2-4. Reference Design Schematics

2.2.4 Simulation Results

The following section show simulation results to review the expected behavior before discussing the final measurement results. For the simulations a lower load capacitance value of 20-uF was selected in order to minimize run time. The following simulations show results with D2 and without D2 in Figure 2-5. This is a recommended diode to prevent the output from oscillating when the capacitor and inductor are left floating when precharge has been completed. Figure 2-7 shows the maximum switching frequency for the system. Figure 2-6 and Figure 2-8 show simulation with the transient clamping diode and without the transient clamping diode respectively.

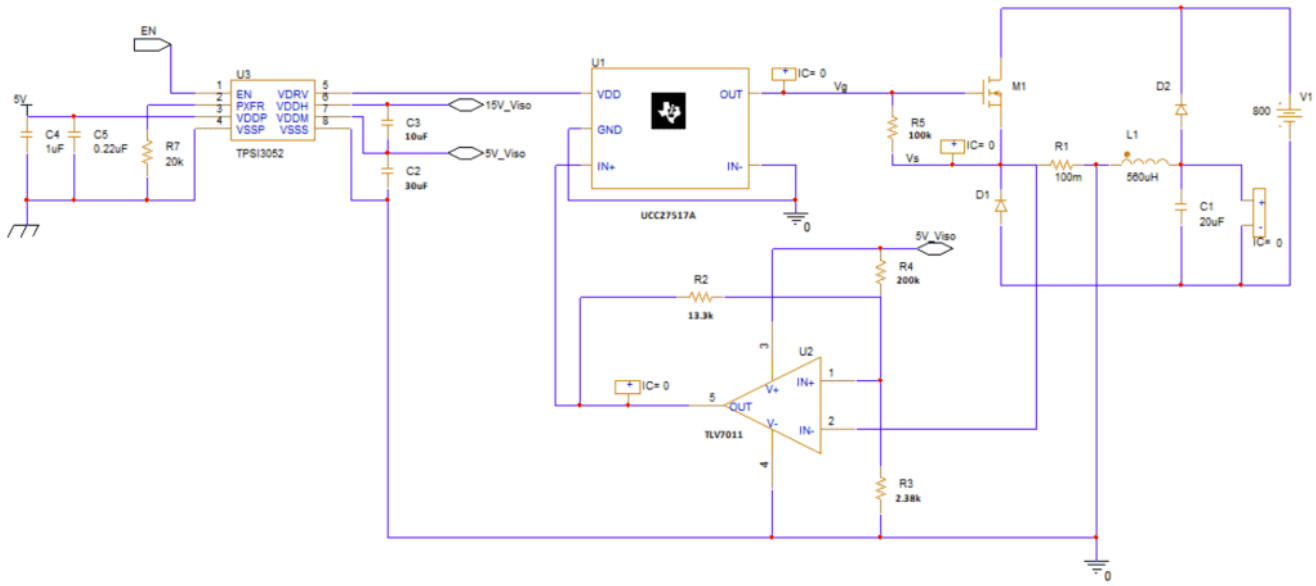


図 2-5. Simulation Circuit

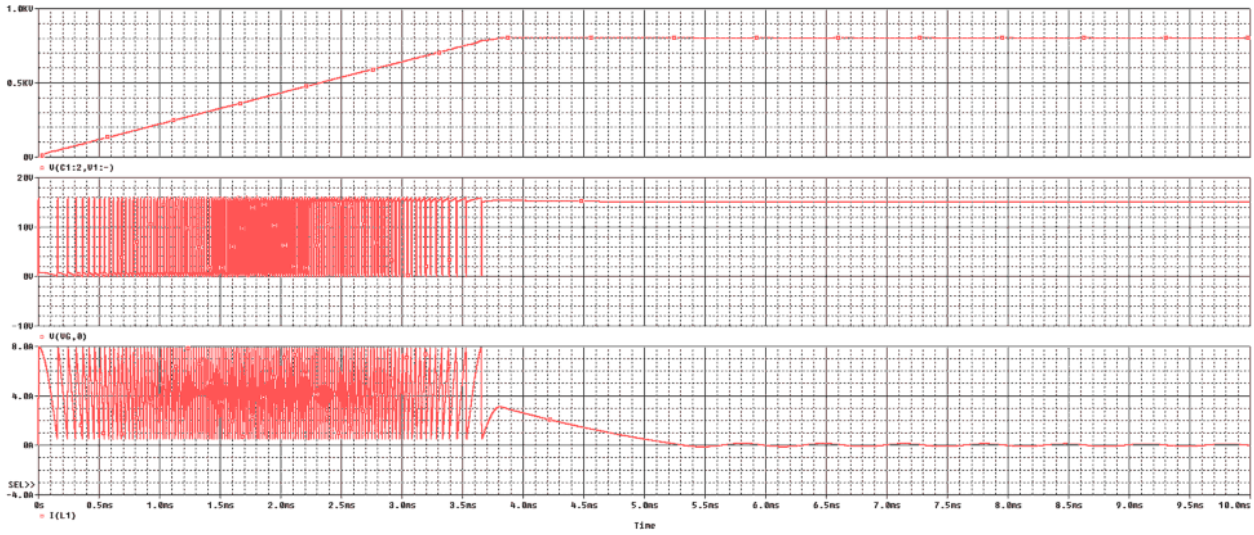


図 2-6. Simulation Waveform With D2

Evaluate	Measurement	Value
☑	1/ Period_XRange(V(VG,0),0.5m,0.75m)	24.73165k
☑	1/ Period_XRange(V(VG,0),1.5m,1.575m)	46.60980k
☑	1/ Period_XRange(V(VG,0),2.0m,2.25m)	47.60907k
☑	1/ Period_XRange(V(VG,0),3m,3.25m)	29.76220k

図 2-7. Simulation Measurements

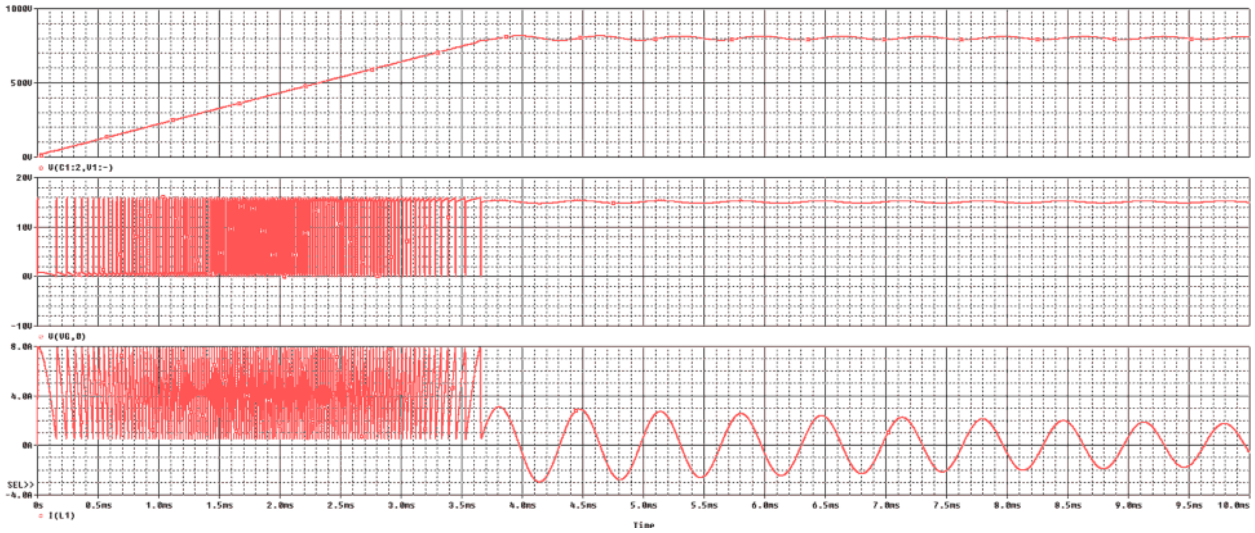


図 2-8. Simulation Waveform Without D2

2.3 Highlighted Products

2.3.1 TPSI3052-Q1

The TPSI3052-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated solid-state relay (SSR) replacement. With a nominal gate drive voltage of 15-V and 1.5/3.0-A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no discrete isolated bias power supply is required. Additionally, the TPSI3052-Q1 can optionally supply power to external supporting circuitry for various application needs. In three-wire mode, the primary supply of 3-V to 5.5-V is supplied externally, and the switch is controlled through a separate enable.

TPSI3052-Q1 features:

- Adjustable power transfer
- Integrated 15-V gate supply
- Up to 50-mW supply to power auxiliary circuitry (I_{AUX})
- UVLO to prevent switching when the supply voltage is too low

For the primary side, TPSI3052-Q1 is set to three-wire mode configuration to achieve the highest power transfer available. Using a 20-kΩ resistor with a 1 % tolerance in PXFR pin provides the highest power transfer available and supports up to 50-mW of I_{AUX}. It is recommended to add a 1-uF in parallel with a 0.1-uF ceramic capacitor with low ESR to VDDP.

For the secondary side, C_{DIV1} (C3) and C_{DIV2} (C4, C5) capacitors need to be properly selected to drive the back to back MOSFETs. If C_{DIV1} and C_{DIV2} are too small, then the voltage drop in VDDH will trigger an undervoltage lockout (UVLO) and disable the driver. The following two equations can be used for calculating the proper capacitance values.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V}, \quad n \geq 1.0 \tag{21}$$

$$C_{DIV2} = n \times C_{DIV1}, \quad n \geq 1.0 \tag{22}$$

- n is a real number greater than or equal to 1.0.
- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

The MOSFETs selected for this design each have a gate charge (Q_G) of 55-nC. Since the TPSI3052-Q1 needs to power other devices for the control logic. The, C_{DIV2} = 3 x C_{DIV1}, then C_{DIV1} is selected with capacitance of 10-uF to make sure that VDDH voltage drop is less than 1-V. Use this excel calculator to calculate for capacitors and power transfer selection.

2.3.2 TLV7011

The TLV7011 (single-channel) are micro-power comparators that feature low-voltage operation with rail-to-rail input capability. These comparators are available in an ultra-small, lead-less package measuring 0.8 mm × 0.8 mm and standard leaded packages, making them applicable for space-critical designs like smart phones and other portable or battery-powered applications.

The TLV701x offer an excellent speed-to-power combination with a propagation delay of 260-ns and a quiescent supply current of 5-µA. This combination of fast response time at micro-power enables power conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6-V to 6.5-V, these comparators are compatible with 3-V and 5-V systems. These comparators also feature no output phase inversion with over-driven inputs and internal hysteresis. These features make this family of comparators well designed for precision voltage monitoring in harsh, noisy environments where slow moving input signals must be converted into clean digital outputs. The TLV701x have push-pull output stages capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load.

2.3.3 UCC27517A-Q1

The UCC27517A-Q1 single-channel high-speed low-side gate-driver device effectively drives MOSFET and IGBT power switches. With a design that inherently minimizes shoot-through current, the UCC27517A-Q1 sources and sinks high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13-ns.

The UCC27517A-Q1 device handles –5 V at input.

The UCC27517A-Q1 provides 4-A source and 4-A sink (symmetrical drive) peak-drive current capability at VDD = 12-V.

The UCC27517A-Q1 operates over a wide VDD range of 4.5-V to 18-V and wide temperature range of –40°C to 140°C. Internal Undervoltage Lockout (UVLO) circuitry on VDD pin holds the output low outside VDD operating range. The ability to operate at low voltage levels such as below 5-V, along with best-in-class switching characteristics, is especially designed for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

For a functionality test of the reference design the user needs the following devices.

1. 5-V DC power source
2. Oscilloscope
3. 2 x Isolated probes
4. 2 x Current probes
5. High power, high voltage power supply. Capable of 800-V_{DC} and 15-A.
6. High voltage, high capacitance capacitor for output load.
7. Safety requirement for high voltage and high current tests such a high voltage enclosure and safety contingencies to discharge output capacitance.

3.2 Test Setup

To test the active pre-charge reference design, follow the next steps and recommendations.

1. Connect a single 5-V input supply to EN and +5V_Pri. This process provides a single trigger signal to power all the devices.
2. While the high-voltage supply is disconnected, power the TPSI3052-Q1 and check that all voltages are as expected.
3. Turn OFF 5-V supply, this supply will remain OFF until step 8.
4. Connect the output-load capacitance positive to J2 (V_Cap) and negative to J4 (-HV).
5. Connect input high-voltage supply to positive J1 (+HV) and negative to J3 (-HV).
6. Connect the isolated high voltage rated probes to J2-J4 to measure the output voltage and J1-J3 to measure the input voltage. Connect these probes as far as possible from the switching inductor to avoid any noise coupling.
7. Connect current probes to measure input current and output current.
8. Enable the high voltage power supply.
9. Provide the EN/+5V_Pri and observe the active precharge operation.
10. Turn OFF the 5-V supply connected to EN/+5V_Pri after precharge has been completed.
11. Safely discharge the output high voltage capacitors.
12. Disable high voltage power supply.

3.3 Test Results

The following PCB shows the area ocupied by the active precharge. In total the active precharge design occupies an area of (80 mm x 55 mm) and a heigth of 26 mm. The schematics shown below represent the tested design and the results are shown next.

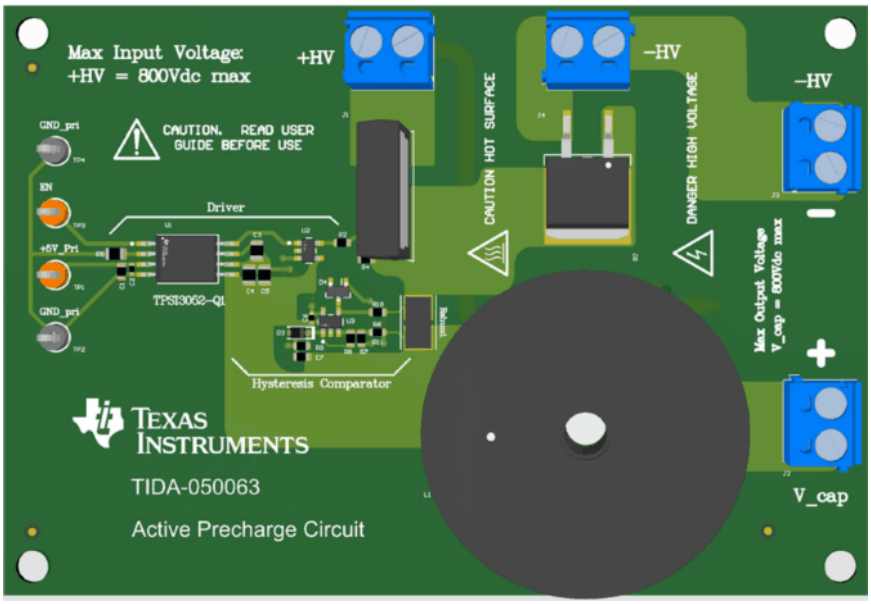


図 3-1. Circuit Board

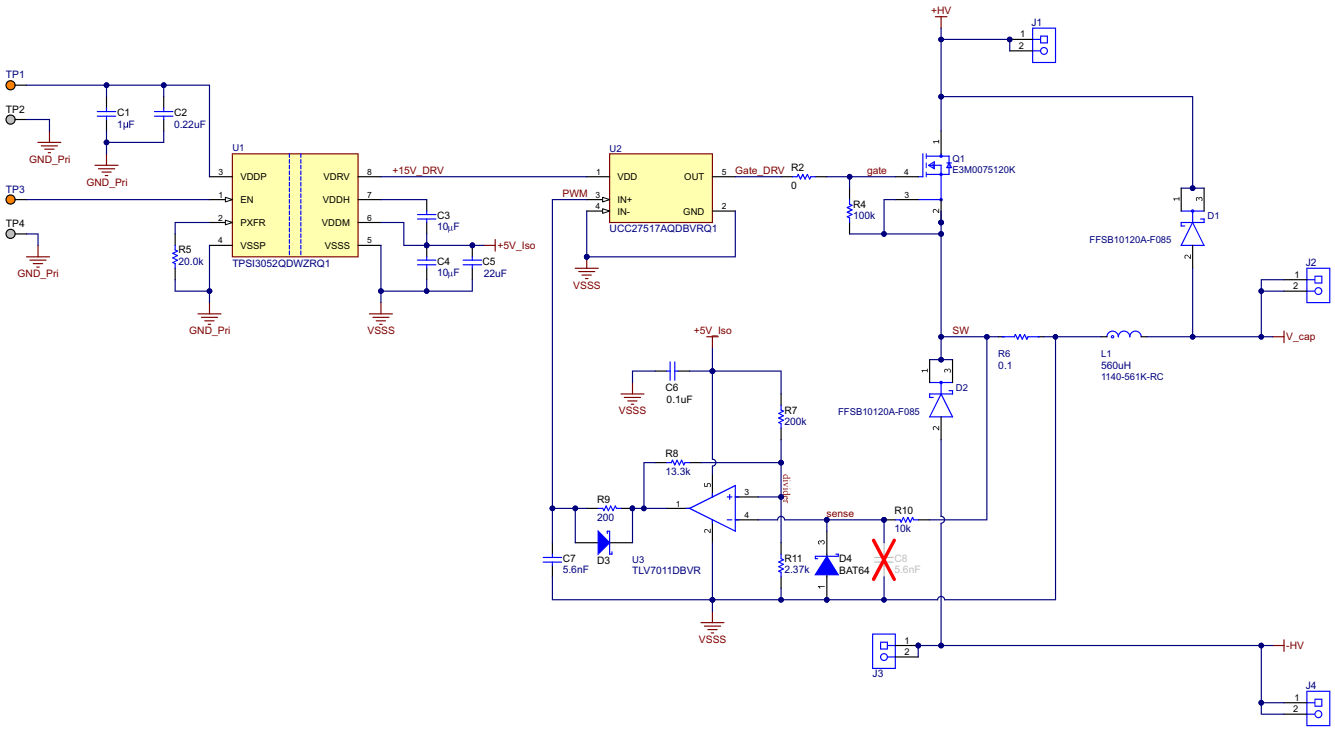


図 3-2. Schematics

The following scope capture shows the active precharge operating with a 400-V input and a 2-mF output capacitance. For this test E3M0075120K SiC MOSFETs were used which are rated for 1.2-kV. The large capacitance was precharged in 200-ms as expected.

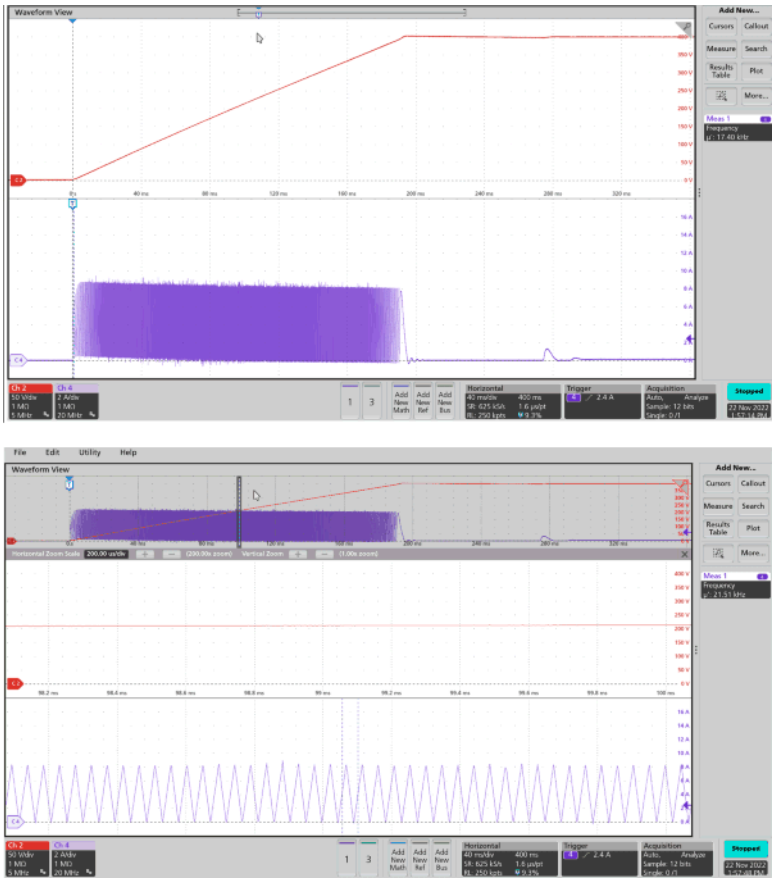


図 3-3. TPSI3052-Q1 at 400-V with E3M0075120K (MOSFET 1200 V/75 mOhm, SiC, E3M, TO-247-4)

The following scope capture shows the active precharge operating with a 800-V input and a 2-mF output capacitance. For this test E3M0075120K SiC MOSFETs were used which are rated for 1.2-kV. The large capacitance was precharged in 400-ms as expected.

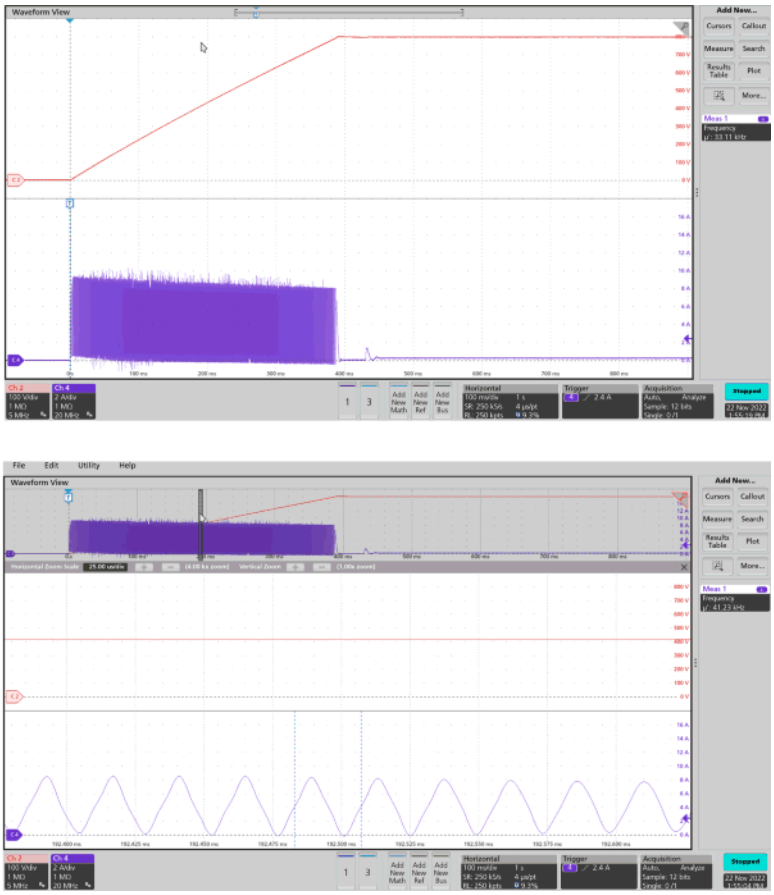


図 3-4. TPSI3052-Q1 at 800-V with E3M0075120K (MOSFET 1200 V/75mOhm, SiC, E3M, TO-247-4)

The following scope capture shows the active precharge operating with a 400-V input and a 2-mF output capacitance. For this test E3M0060065K SiC MOSFETs were used which are rated for 650-V. The large capacitance was precharged in 200-ms as expected.

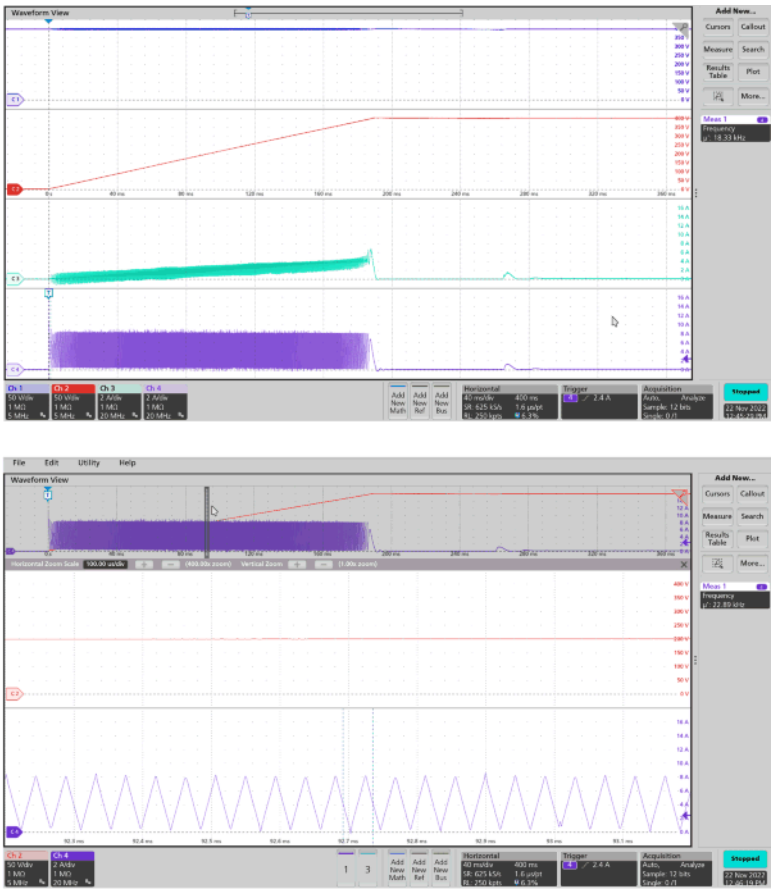


図 3-5. TPSI3052-Q1 at 400-V with E3M0060065K (MOSFET 650 V/60 mOhm, SiC, E3M, TO-247-4)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050063.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050063.

4.2 Documentation Support

1. Texas Instruments, TPSI3052-Q1 EVM Automotive Reinforced Isolated Switch Driver with Integrated 15-V Gate Supply EVM User's Guide user's guide.
2. Texas Instruments, TPSI3050-Q1 EVM Automotive Reinforced Isolated Switch Driver with Integrated 10-V Gate Supply EVM User's Guide user's guide.
3. Texas Instruments, Cascoding Two TPSI3050 Isolated Switch Drivers to Increase Gate Drive Voltage application note.

4.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

4.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

5 About the Authors

Hrag Kasparian joined Texas Instruments over 10 years ago. Hrag currently serves as a power applications engineer, designing custom DC-DC switch-mode power supplies. Previously, he worked on the development of battery packs, chargers, and electric vehicle (EV) battery management systems at a startup company in Silicon Valley. Hrag graduated from San Jose State University with a Bachelor of Science degree in Electrical Engineering.

Matthew Guibord is an Analog Field Applications Engineer for Texas Instruments supporting TI's electric vehicle product portfolio. Matthew also previously worked in TI's high-speed data converter team as a system engineer focused on aerospace and defense and test and measurement end equipments. Matthew joined TI in 2010 after receiving his Bachelor of Science in Computer Engineering from Michigan State University. Matthew completed his Master of Science in Electrical Engineering from the University of Texas at Dallas in 2017 with a focus on digital-signal processing.

Francisco Lauzurique is an Applications Engineer for Texas Instruments, where he is responsible for supporting solid -state relay devices. Francisco joined TI in 2020 after completing his Bachelor of Science in Electrical Engineering with a focus on Analog and Mixed Signals from Texas A&M University. He is currently working on obtaining his Master of Science in Electrical Engineering with a focus in Analog and Mixed Signals from Texas A&M University.

6 Revision History

Changes from Revision * (December 2022) to Revision A (January 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Updated *M2* to *M1* throughout document	5
• Updated di/dt from *1-A/us* to *1.429-A/us*	5

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265