参考資料

Design Guide: TIDA-050056

12Vin、3.3Vout、1A の高出力密度降圧コンバータのリファレンス・デザイン

概要

TIDA-050056 は、5V～17V の入力電圧を受け入れる降圧コンバータのリファレンス・デザインであり、設計スペースが非常に限られているアプリケーションを想定しています。TPS629210-Q1 降圧コンバータを採用したこのリファレンス・デザインは、入力電圧を 3.3V 出力に降圧し、高効率かつ低静止電流で最大 1A の負荷に電力供給できます。このデザインに使用されているインダクタは、DCR (直流抵抗) が約 138mΩ の 1.5µH インダクタです。すべての外部部品を含むソリューション全体のサイズは 20mm^2 です。このデザインは、業界最小の動作時静止電流 (I_Q) で高効率の DC/DC 変換と小型のソリューション・サイズを実現します。同じデザインを、TPS629210-Q1 とピン互換である TPS629210 デバイスにも適用できます。

Resources

TIDA-050056	Design Folder
TPS629210-Q1	Product Folder
TPS629210	Product Folder

Ask our TI E2E™ support experts

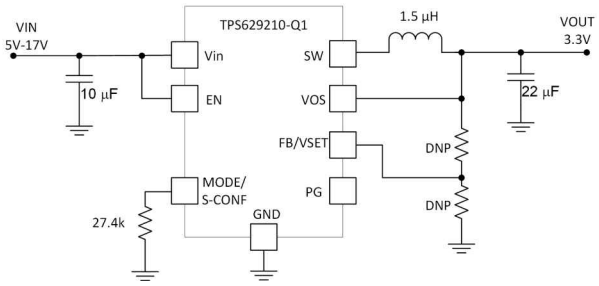
特長

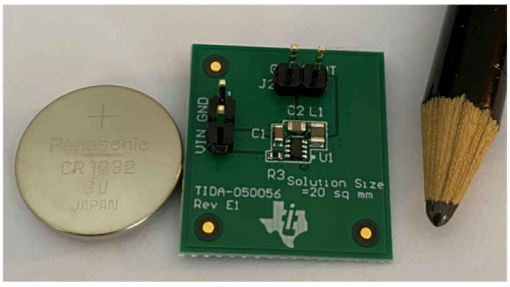
- 20mm^2 の小型トータル・ソリューション・サイズ
- 50mA/mm^2 の電力密度
- 5V～17V の入力電圧
- 最大 1A の連続出力電流
- 低 I_Q:4µA (標準値)
- 総合的なシステム電圧精度:-1.5% および +1.1% (-40℃～150℃の全温度範囲)
- 動作時接合部温度:-40℃～150℃
- 100% デューティ・サイクル・モードを備えた DCS-Control™ トポロジ

アプリケーション

- ADAS とインフォテインメント
- 電気通信および無線インフラ
- ファクトリ・オートメーション / 制御
- よりスマートな家電製品のエンジニアリング
- ビル・オートメーション
- グリッド・インフラ
- リテール・オートメーションおよびペイメント
- ワイヤレス・インフラ

Design Images





1 System Description

The TIDA-050056 is designed by using the TPS629210-Q1 high efficiency and low I_Q DC/DC Buck converter. The design is optimized for small total solution size, low BOM count, high efficiency, best thermal performance and lowest quiescent current possible. TPS629210-Q1 allows high switching frequency that enables small component selection without compromising on efficiency. The internal feedback (VSET) feature eliminates need of external feedback resistors. Small size and less pin count reduces external component counts. This design is ideal for applications where is limited space such as smart lock, wearable devices and so on. The efficiency and low I_Q are ideal for battery operating systems. The design allows to efficiently use the battery power and extend its life time.

表 1-1. Key System Specifications

Parameter	Min	Typ	Max	Unit
Input Voltage	5	12	17	V
Output Voltage	3.267	3.3	3.333	V
Output Current	0		1	A
Switching Frequency		2.5		MHz
Operating Quiescent Current		4		µA
Junction Temperature	-40		150	°C
Output Discharge		Enabled		

2 System Overview

2.1 Block Diagram

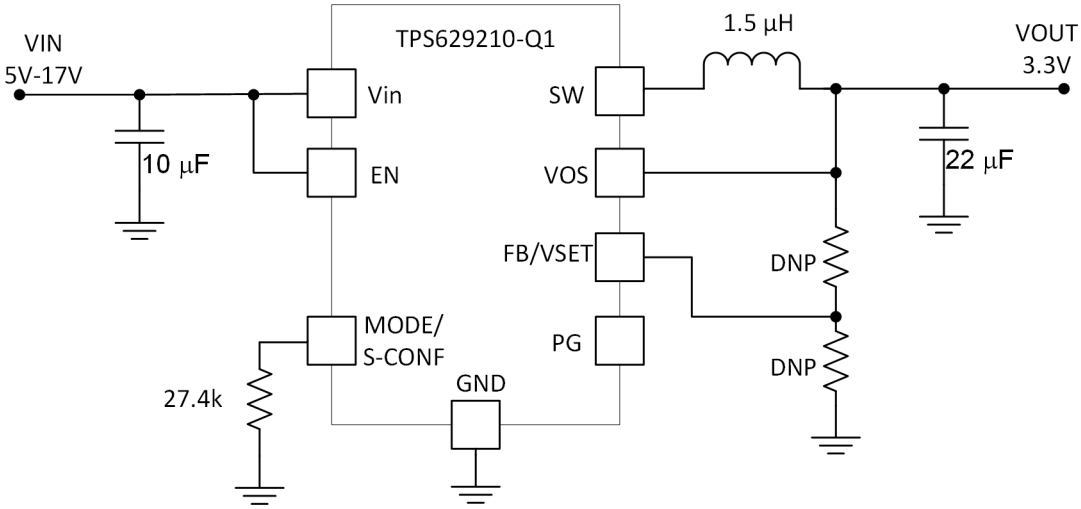


図 2-1. TIDA-050056 Block Diagram

2.2 Design Considerations

By connecting 27.4-kΩ resistor on MODE/S-CONF pin, the device is configured to:

- **VSET operation:** VOUT is sensed only through the VOS pin by an internal resistor divider. The target output voltage is programmed by an external resistor connected between the FB/VSET pin and GND. In this design, FB/VSET pin is floating and thus the VOUT is programmed to 3.3-V
- **2.5-MHz Switching Frequency with AEE (Automatic Efficiency Enhancement):** The MODE/S-CONF pin is configured to AEE mode which provides efficiency enhancement over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter. The efficiency decreases if VOUT decreases, VIN increases, or both. To keep the efficiency high over the entire duty cycle range (VOUT/VIN ratio), the switching frequency is adjusted while maintaining the ripple current. The AEE feature provides an efficiency enhancement for various duty cycle, especially for lower VOUT values where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycle of high VIN to low VOUT conversion, which limits the control range in other topology.
- **Power Save Mode Operation(Auto PFM/PWM):** The MODE/S-CONF pin is configured for power save mode(Auto PFM/PWM). The device operates in PWM mode as long as the output current is higher than half of the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half of the ripple current of the inductor. The power save mode is entered seamlessly when the load current decreases. This ensures a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous. In power save mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition in and out of power save mode is seamless in both directions.
- **Output Discharge Function Enabled:** The output discharge function is enabled to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0-V when the device is off. The output discharge feature is only active once TPS629210-Q1 have been enabled at least once since the supply voltage is applied.

2.3 Highlighted Features

The TPS629210-Q1 is a high efficiency, small and flexible synchronous step-down DC/DC converter that is easy to use. A selectable switching frequency of 2.5-MHz or 1.0-MHz allows the use of small inductors and provides fast transient response. The device supports high output voltage accuracy of -1.5% and +1.1% across temperature range (-40°C to 150°C) using VSET feature. The wide input voltage of 3-V to 17-V supports a variety of nominal inputs, like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

The TPS629210-Q1 provides a MODE/S-CONF input to set the internal/external feedback, switching frequency, output voltage discharge and auto PFM/PWM or forced PWM operation. To maintain high efficiency at light load, auto PFM/PWM should be selected. Additionally, to provide high efficiency at very small load, the device has a low typical quiescent current of 4-µA. If enabled AEE mode, the device provides automatic efficiency enhancement across VIN, VOUT and load current. The device is available in small 8-pin SOT583 package.

2.4 System Design Theory

The TPS629210-Q1 is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter. See the TPS629210-Q1 data sheet for more details.

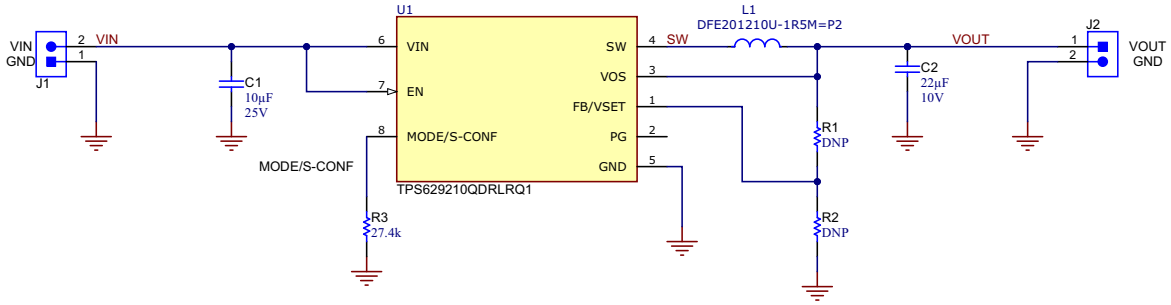


図 2-2. Buck Converter Circuit Design Using TPS629210-Q1

The TIDA-050056 is designed with a nominal 1.5-µH inductor to support 3.3-V output voltage. A shielded wire-wound inductor from Murata (DFE201210U-1R5=P2) is used in this design. It has 2.5-A saturation current and 138-mΩ maximum DCR. 1.5-µH inductance is ideal for size and ripple given the VOUT of this 3.3-V design. The larger values can be used to achieve a lower inductor ripple current but they can have a negative impact on efficiency and transient response. Small values that 1.5-µH will cause a larger inductor ripple current which causes a larger negative inductor current in forced PWM mode at low or no output current.

A small low equivalent series resistance(ESR) multilayer ceramic capacitor(MLCC) is recommended to obtain the best filtering. Fro this design, a 10-µF /25-V multilayer ceramic chip capacitor from Murata (GRM188R61E106MA73L) is used as an input capacitor. It is designed to withstand up to 25-V which is enough for input voltage range that we want to cover in this design.

For the output capacitor, the voltage rating is much smaller than the input, only 6-V to 10-V capacitor rating is needed. A 22-µF/10-V multilayer ceramic chip capacitor from Murata(GRM188R61A226ME15D) is chosen.

The MODE/S-CONF requires an E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200-ppm/°C. A small size 0402 package (CRCW040227K4FKED) from Vishay is used in this design.

3 Hardware Requirements, Test Setup, and Test Results

3.1 Hardware Requirements

For testing purposes, this reference design requires the following equipment:

- A power supply that is capable of supplying at least 1-A of current and up to 20-V.
- Current and voltage multimeters to measure the currents and voltages during the related tests.
- The TIDA-050056 board is a printed circuit board(PCB) with all the components in this design.
- Resistive load and electronic load that are capable at least 1-A.
- Thermal camera used to measure the thermal rise of the board during operation.
- Oscilloscope to capture voltage and current waveforms.

3.2 Test Setup

図 3-1 shows test setup for TIDA-050056.

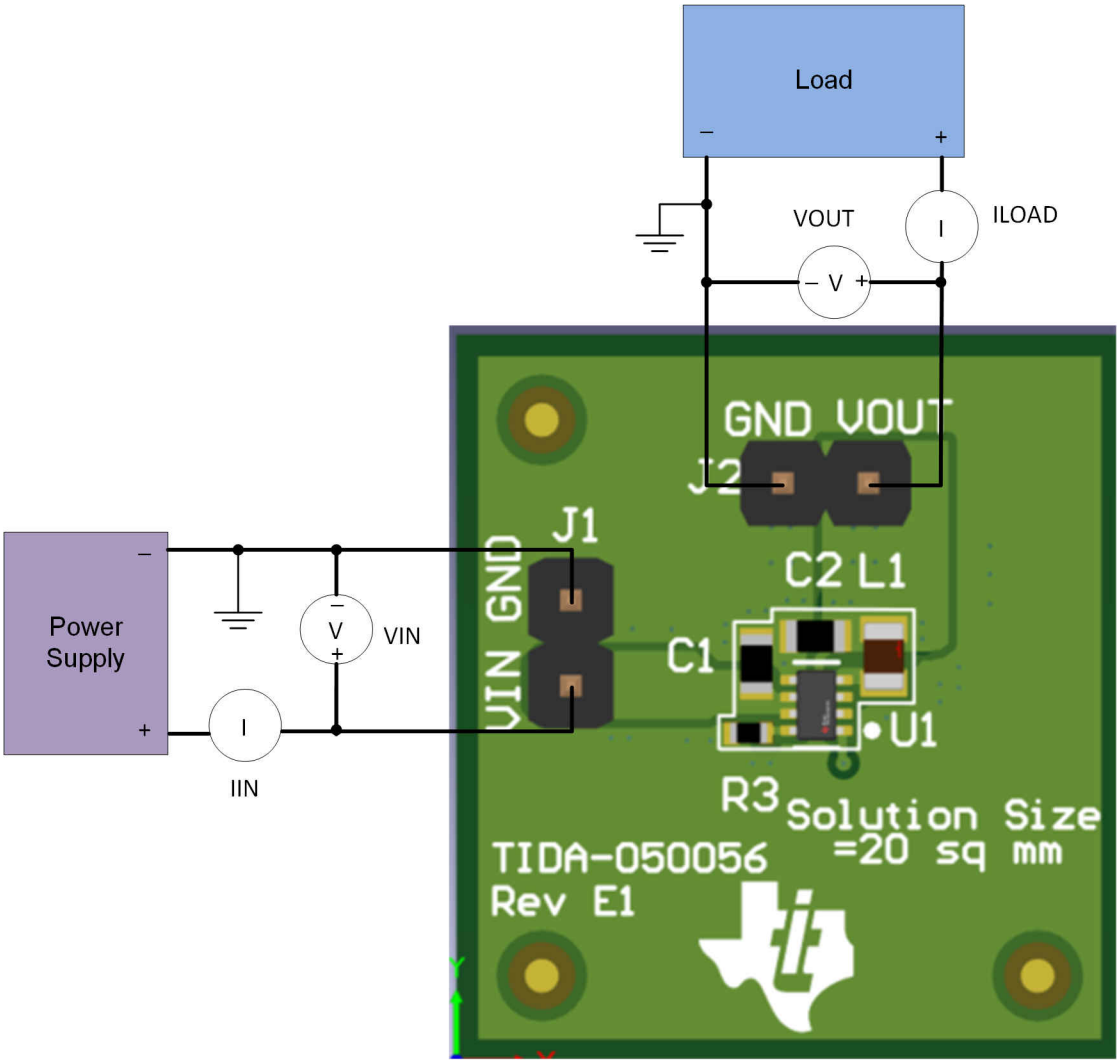


図 3-1. Test Setup

3.3 Test Results

This section provides the test results of TIDA-050056.

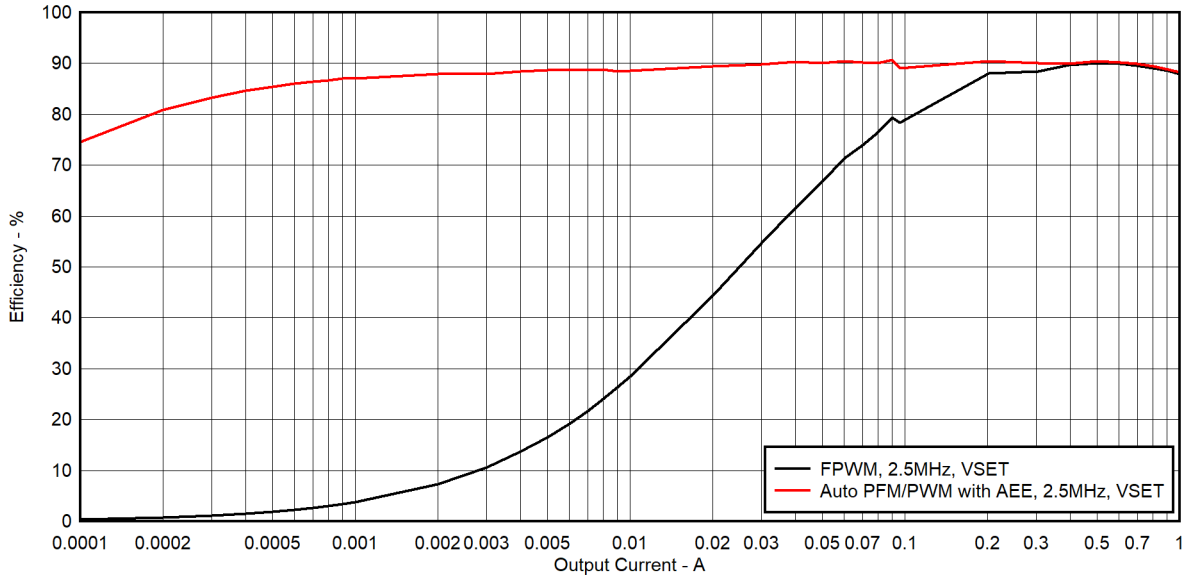


図 3-2. Efficiency V_{IN}=12-V, V_{OUT}=3.3-V, F_{SW}=2.5-MHz, VSET

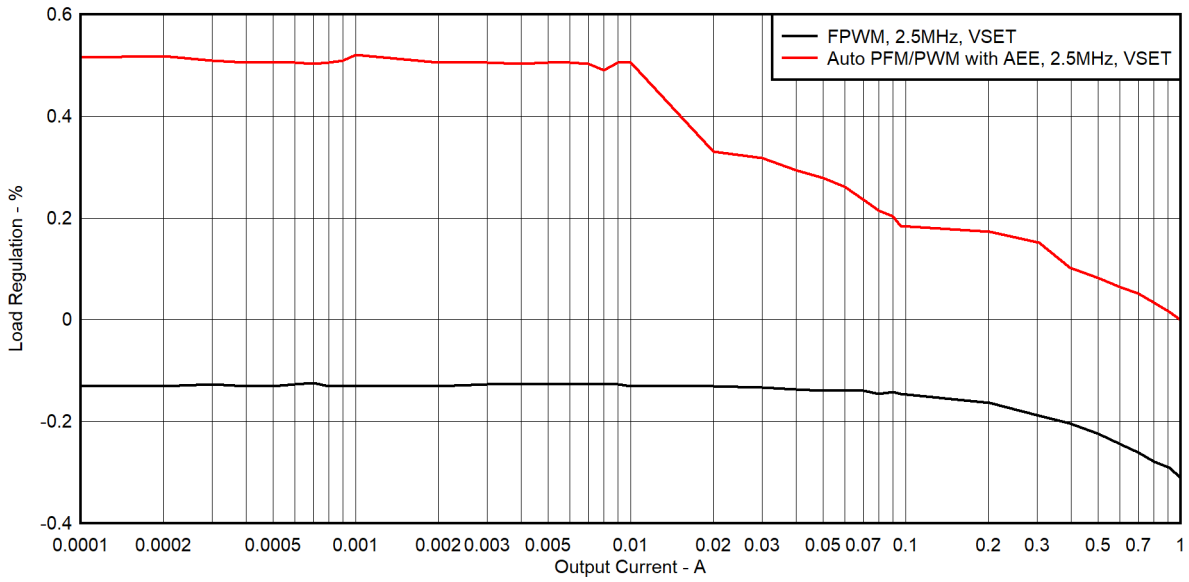


図 3-3. Load Regulation V_{IN}=12-V, V_{OUT}=3.3-V, F_{SW}=2.5-MHz, VSET

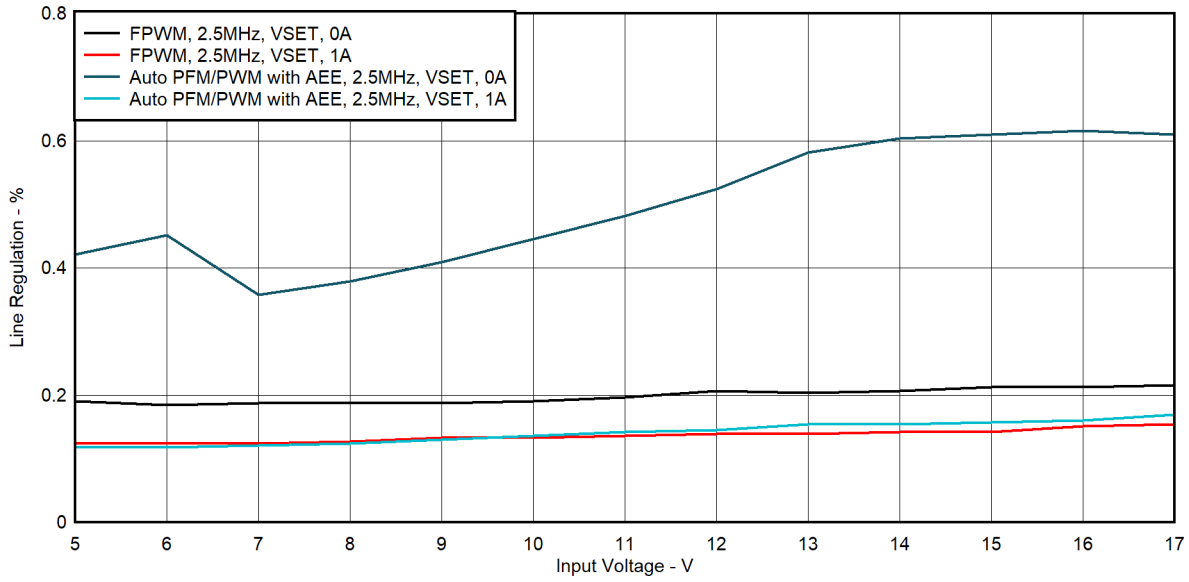


図 3-4. Line Regulation V_{IN}=5-V to 17-V, I_{OUT}=0-A and 1-A, F_{SW}=2.5-MHz, VSET

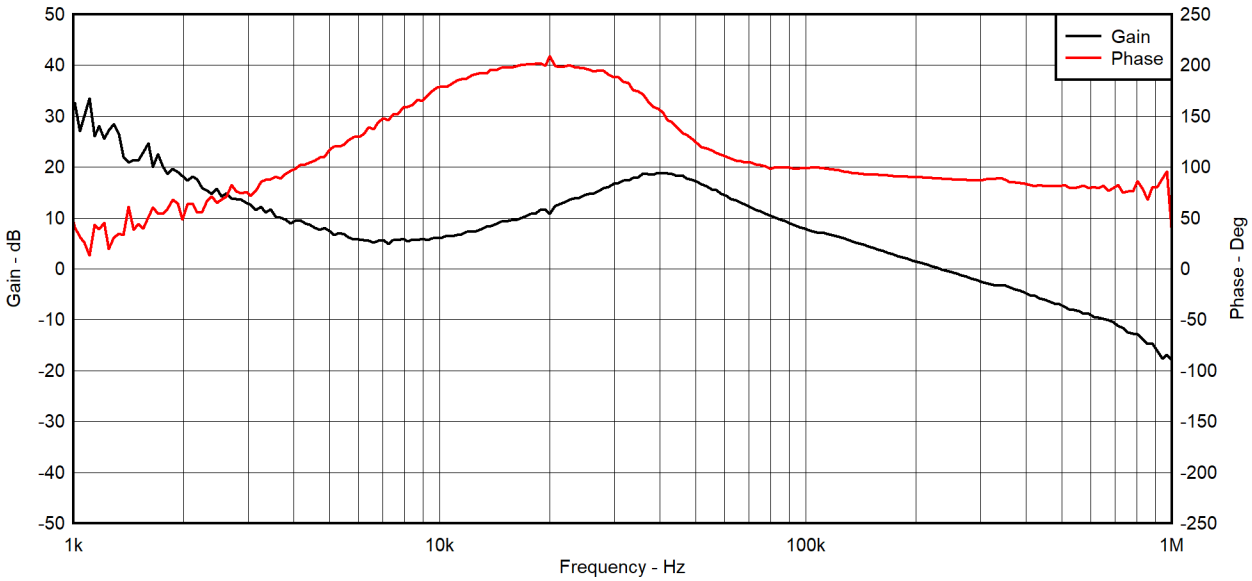


図 3-5. Loop Response Auto PFM/PWM with AEE, VSET, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

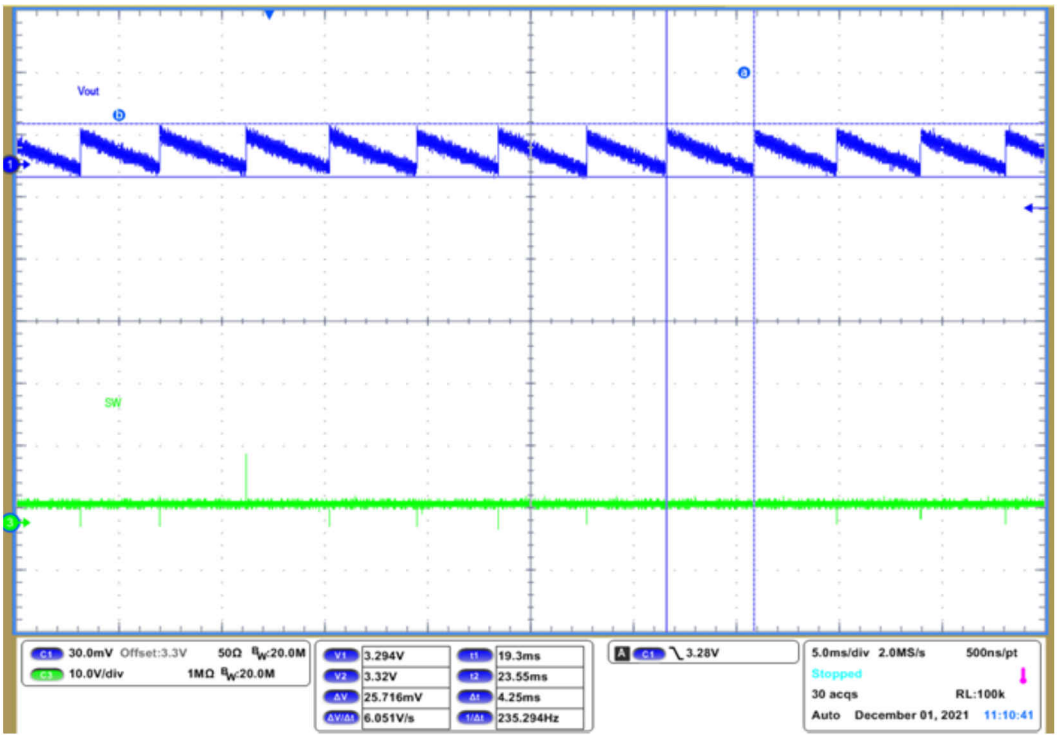


図 3-6. Output Voltage Ripple Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=0-A

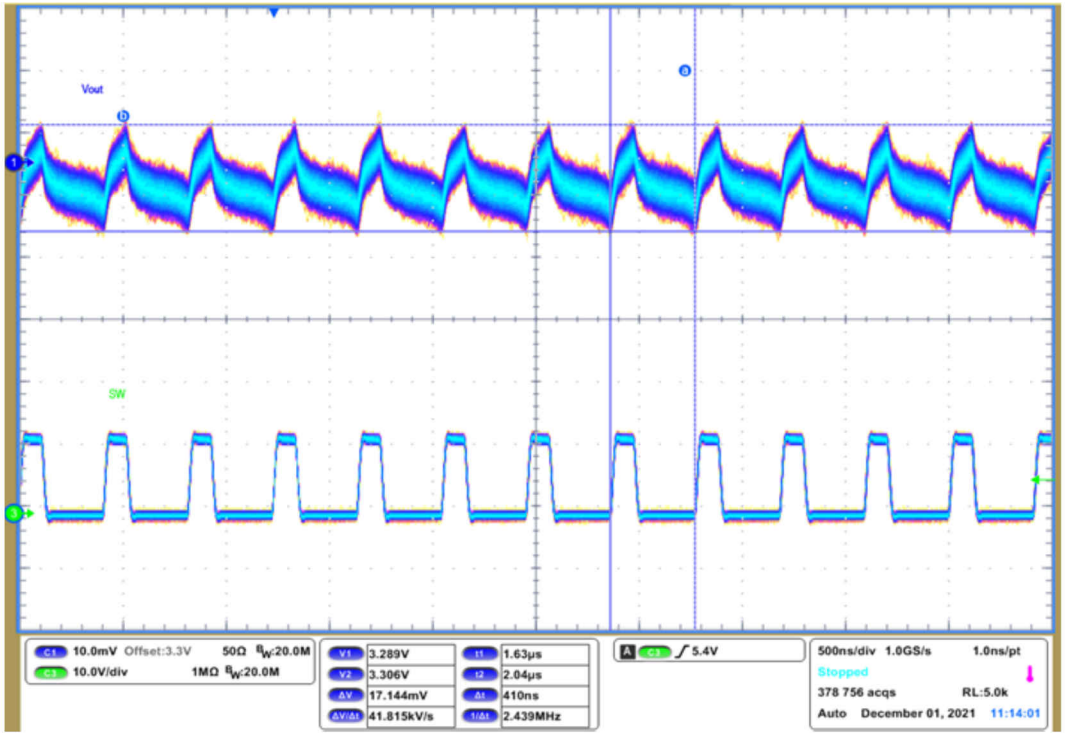


図 3-7. Output Voltage Ripple Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

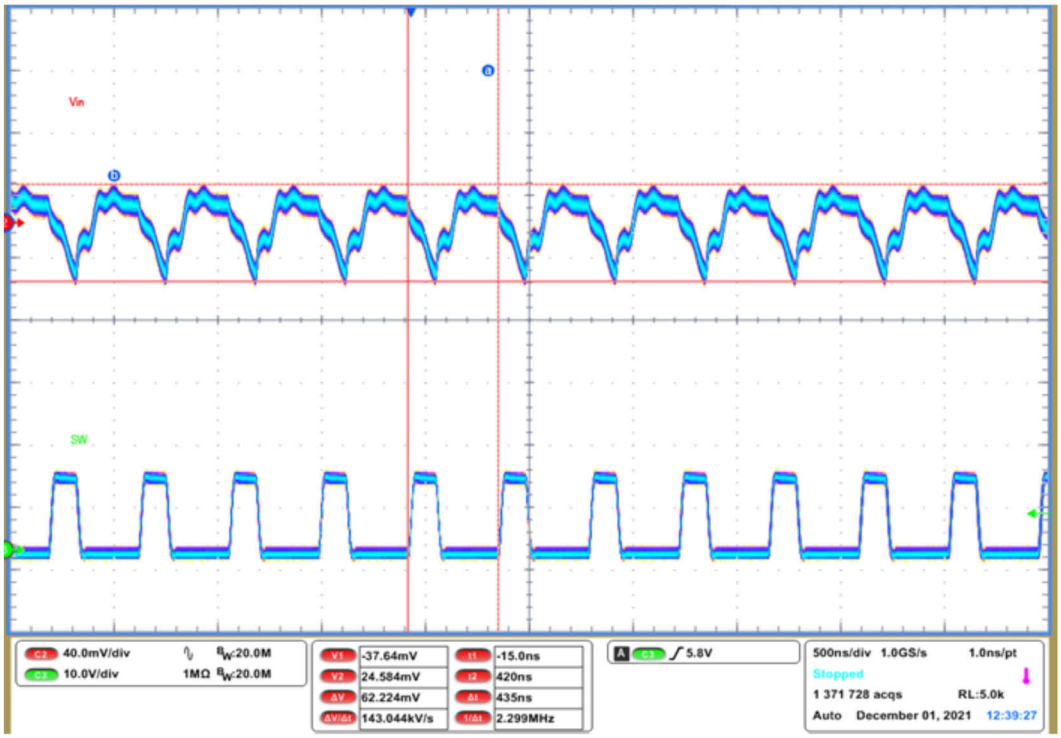


図 3-8. Input Voltage Ripple Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

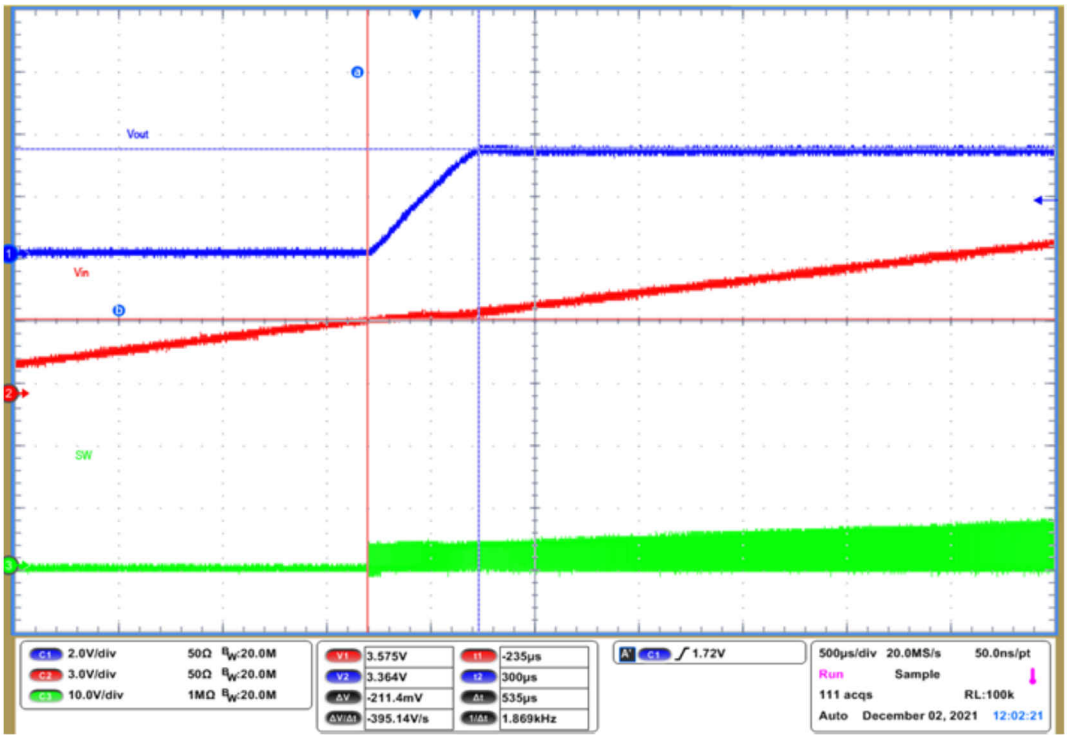


図 3-9. Start up Auto PFM/PWM with AEE, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

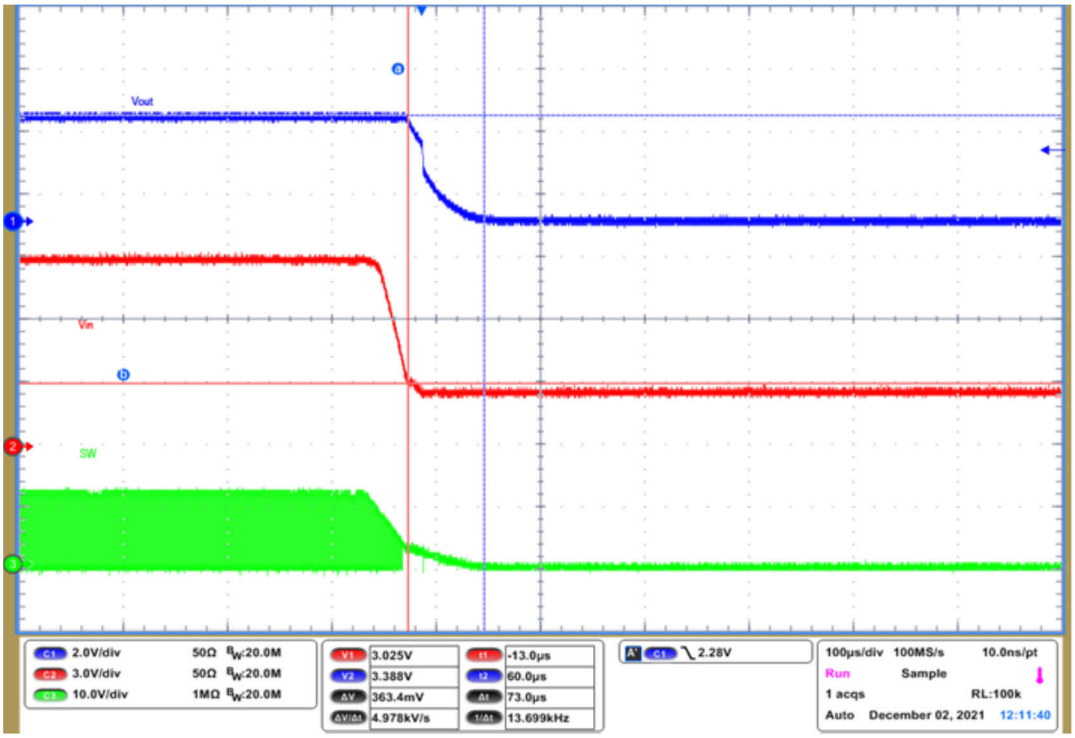


図 3-10. Shut down Auto PFM/PWM with AEE, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

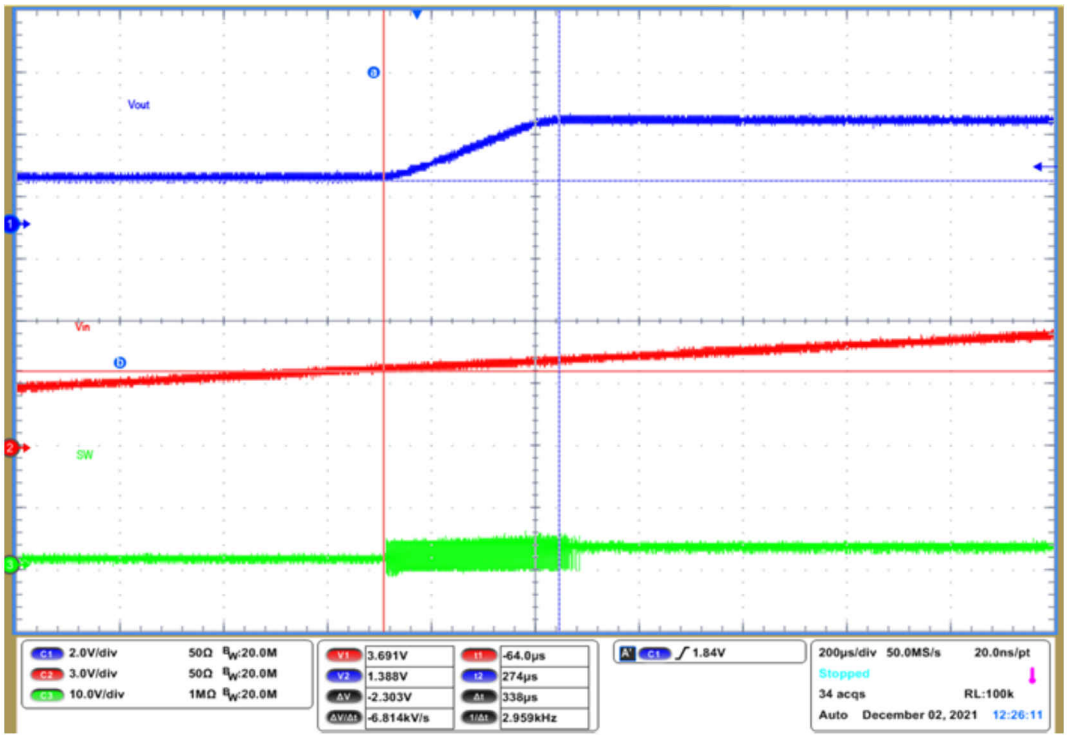


図 3-11. Pre-bias start up Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=0-A

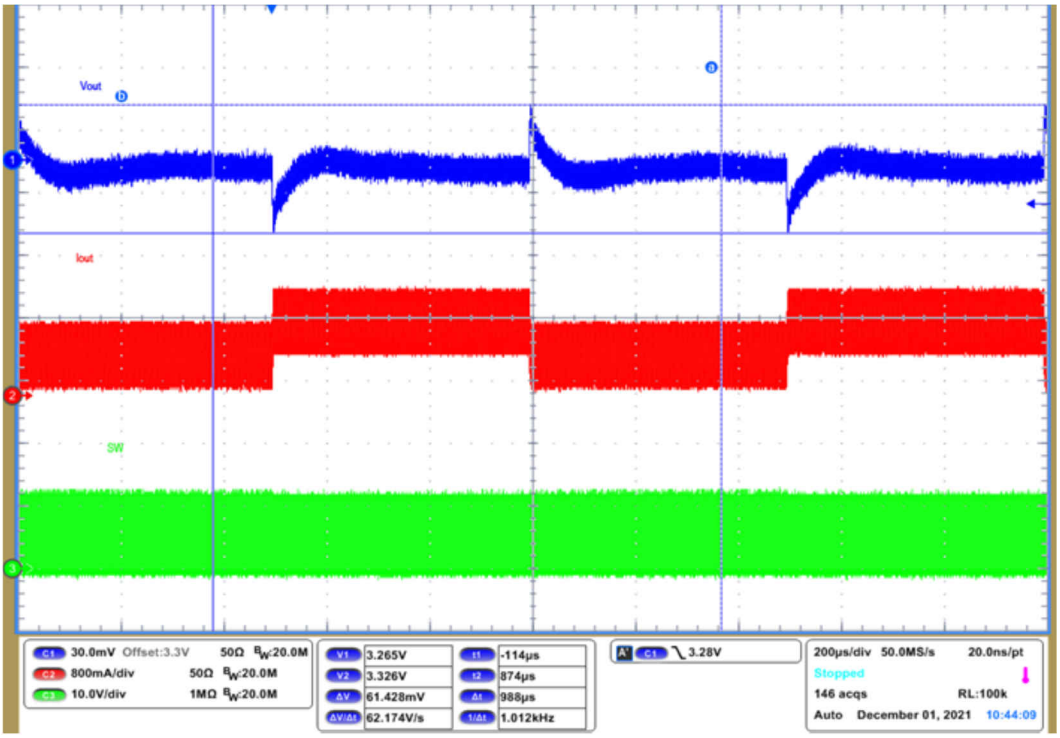


図 3-12. Load Transient Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=0.5-A to 1-A, Slew rate= 1-A/µs

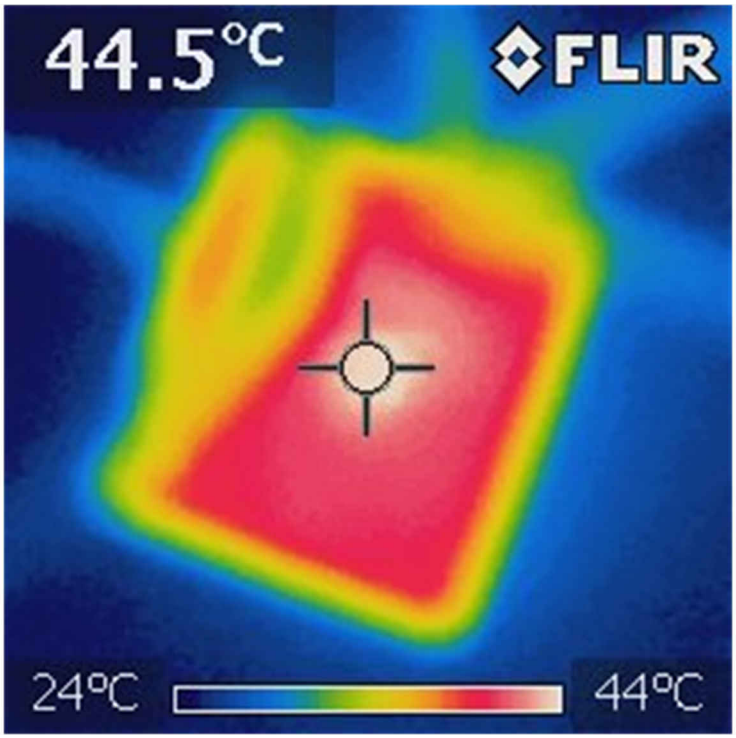


図 3-13. Thermal Image Auto PFM/PWM, V_{IN}=12-V, V_{OUT}=3.3-V, I_{OUT}=1-A

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050056.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050056.

4.1.3 PCB Layout Recommendations

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050056.

4.1.4 Altium Projects

To download the Altium Designer project files, see the design files at TIDA-050056.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-50056.

4.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050056.

4.2 Documentation Support

1. Texas Instruments, TPS629210-Q1 3-V to 17-V, 1-A Low I_Q Converter in a SOT583 Package data sheet.
2. Texas Instruments, TPS629210 3-V to 17-V1-A, Low I_Q Buck Converter in SOT583 Package data sheet.

4.3 サポート・リソース

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4.4 Trademarks

5 About the Author

Matthew Murdock is System Engineer at Texas Instruments for over a decade responsible for defining new products and technology platforms based on our marketing strategy and business opportunities.

Nancy Zhang is Application Engineer at Texas Instruments for over a decade responsible for Intel server platform, mid-voltage low current buck converter, and modules support.

Matthew Murdock and Nancy Zhang also provides application support and system design for customers to understand their overall product ecosystem and how best to use mid-voltage buck converters.

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