参考資料

デザイン・ガイド:TIDA-00731
IEC ESD、EFT、サージ RS-485 バス保護のデザイン・ガイド

概要

RS-485、RS-422、RS-232、CAN、Profibus などの産業用ネットワークは、最終アプリケーションでの過酷なシステム・レベルの過渡事象にも損傷しないで耐える必要があります。このような事象は、取り扱い時の静電放電、誘導性負荷の遮断、リレーの接点バウンス、落雷などが原因で発生することがあります。これらの要件を満たす設計を行うことは、適切なツールと、設計に必要な規格に関する知識なしでは困難です。

TIDA-00731 では、これらの破壊的な過渡事象に対して最も敏感な部品を保護する方法の実践的な例を紹介しています。このドキュメントでは TIA/EIA-485 規格、IEC 61000-4-x 過渡テスト規格、システムレベルの過渡保護の実装、全体回路設計およびレイアウトについて解説します。

リソース

TIDA-00731	デザイン・フォルダ
SN65HVD82	プロダクト・フォルダ
SN65HVD3082E	プロダクト・フォルダ

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特長

- 基板レベルの IEC ESD、EFT、サージの評価
- トランシーバのロジック I/O ピンを簡単に制御可能
- 複数 TVS ダイオード構造の PAD サイト評価
- パルス保護用直列抵抗パッド
- Bourns 製 TBU 高速保護部品の評価
- Bourns 製ラジアル・リード付きバリスタ保護の評価
- 半二重 RS-485 トランシーバ用の汎用評価基板

アプリケーション

- e メーター
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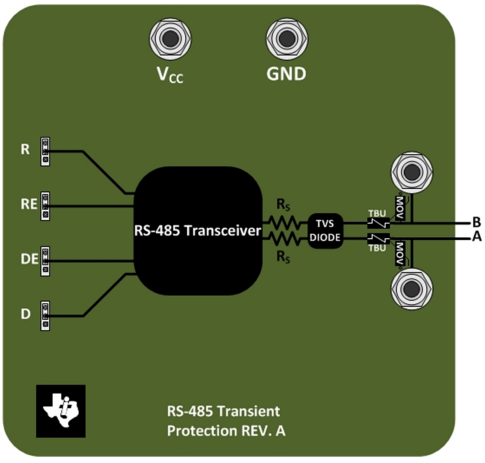
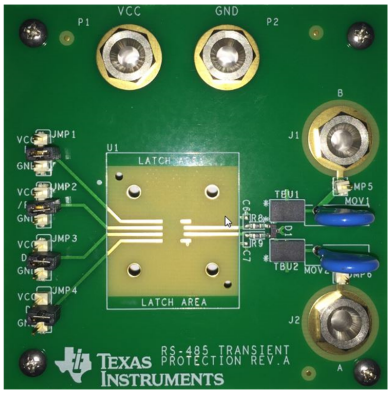




1 System Description

In this design, a TVS diode is implemented on each bus line along with series pulse proof resistors, metal oxide varistors (MOVs), and a transient blocking unit (TBU) protecting the RS-485 transceiver from lethal ESD, EFT (burst), and surge transients. The TVS diode acts as a clamping circuit redirecting the transient energy to ground while the pulse proof resistors act as a current limiter to protect the transceiver from dangerous overvoltage conditions. The MOV protects the Bourns TBU from exposure to excessive transient voltage, clamping or crowbarring the transient to a level less than the impulse. When the transient current exceeds the TBU trigger current limit, the sub-microsecond response of the TBU limits the current flow to the transceiver. The MOV reduces the transients to a few hundred volts of clamping voltage while the TBUs limit transient current to less than 1 mA. 図 1 shows the design with all of its components:

1.1 Key System Specifications

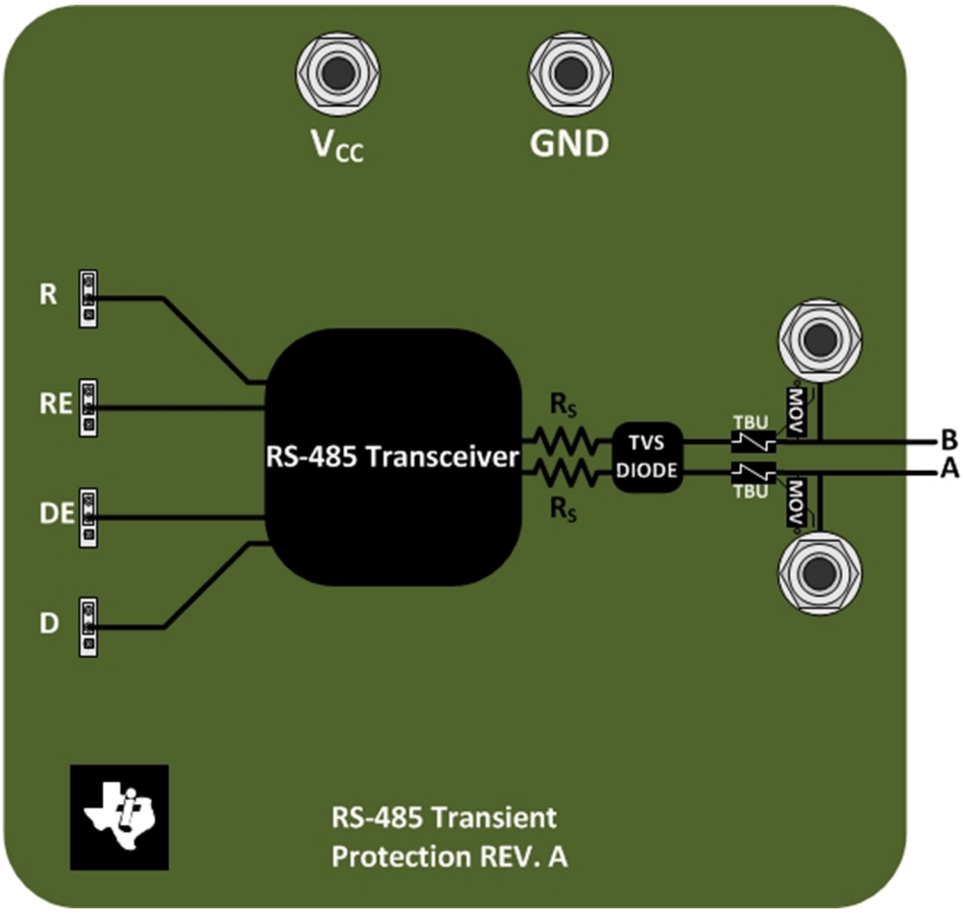
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Supply Voltage Range (SN65HVD82 and SN65HVD3082E)	4.5 V to 5.5 V
Supply Voltage Range (THVD1429)	3 V to 5.5 V
RS-485 Data Rates (SN65HVD82 and SN65HVD3082E)	Up to 250kbps
RS-485 Data Rates (THVD1429)	Up to 20Mbps
IEC ESD Protection Level (SN65HVD82)	±30 kV Contact and Air Discharge
IEC ESD Protection Level (SN65HVD3082E)	±30 kV Air Discharge, ±14 kV Contact Discharge
IEC EFT Protection Level (SN65HVD82 and SN65HVD3082E)	±4 kV
IEC Surge Protection Level (SN65HVD82)	±8 kV
IEC Surge Protection Level (SN65HVD3082E)	±6 kV

2 System Overview

2.1 Block Diagram

図 1. TIDA-00731 Block Diagram



2.2 Design Considerations

Device testing specifications have been defined to verify and validate system performance in an industrial environment. In this design guide, several standards were referenced to define the level of protection needed.

These standards are defined to ensure ESD robustness in their end design. Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) are the most common ESD standards in industry, as most vendors provide data on these parameters in the supporting documentation for a given device. These traditional ESD models do not take into account system-level ESD events and are solely meant as device level specs. These specifications ensure that the device can make it through the handling and assembly process without being damaged by ESD.

HBM, MM, and CDM are sufficient models for many applications, but some industrial applications are subjected too much greater stresses than the energy levels that these standards deliver. The next three sections will discuss the IEC 61000-4-2 Electrostatic Discharge Immunity Test, IEC 61000-4-4 Electrical Fast Transient/Burst Immunity Test, the IEC 61000-4-5 Surge Immunity Test standards and the expected levels of energy the industrial system can see.

2.2.1 IEC 61000-4-2 Electrostatic Discharge Immunity Test

The IEC 61000-4-2 ESD immunity test is a system-level ESD test that imitates a charged operator discharging onto an end system. The characteristics of the IEC ESD test differ from that of other ESD standards in rise times, the amount of energy delivered during the strike, and the number of strikes administered during the testing. There are two types of testing methods involved with the IEC ESD: contact discharge and air discharge. The contact ESD test discharges an ESD pulse from an IEC ESD gun directly onto the device under test (DUT). The air ESD discharge test involves moving the charged ESD gun towards the DUT until the air breaks down enough to allow conduction of the ESD strike between the ESD gun and the DUT. The IEC ESD testing is performed with both positive and negative polarities, and a passing score is not achieved unless both polarities at a single level are survived. 表 2 shows the IEC 61000-4-2 ESD test voltage levels and the peak current levels:

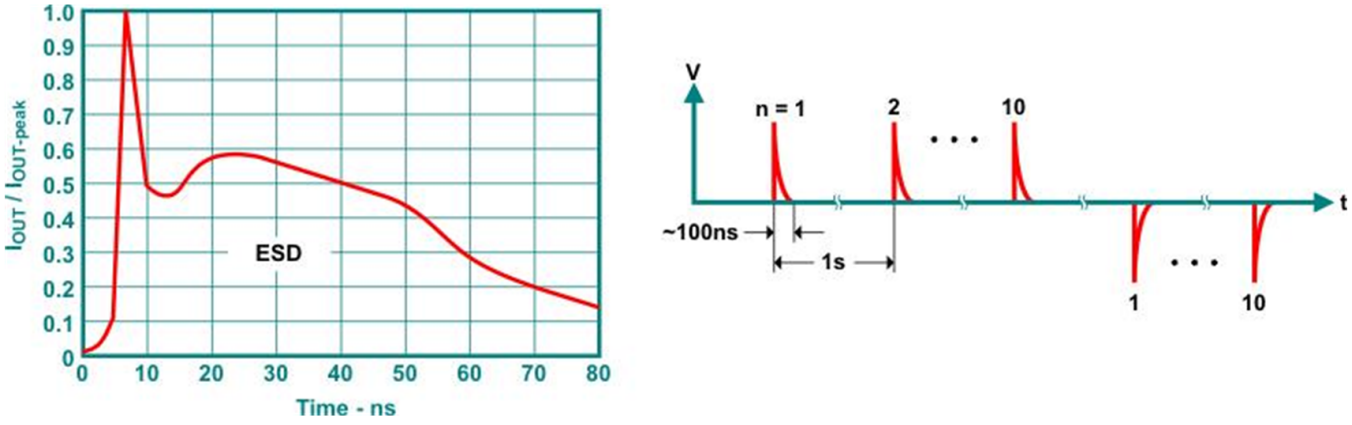
表 2. IEC 61000-4-2 ESD Test Voltage Levels

Contact Discharge			Air Discharge	
Level	Test Voltage (kV)	Peak Current (A)	Level	Test Voltage (kV)
1	2	7.5	1	2
2	4	15	2	4
3	6	22.5	3	8
4	8	30	4	15
*	Special	Special	*	Special

* is an open level. The level has to be specified in the dedicated equipment speciation. If higher voltages than those shown are specified, special test equipment may be needed.

図 2 depicts the basic shape of the IEC ESD pulse and shows the timing sequence of the test pulses.

図 2. Current Waveform of IEC ESD Pulse and Timing Sequence of Test



2.2.2 IEC 61000-4-4 Electrical Fast Transient/Burst Immunity Test

The IEC 61000-4-4 electrical fast transient (EFT) or burst immunity test is meant to simulate the switching transients caused by the interruption of inductive loads, relay contact bounce, and so on. The EFT test is performed on power lines, I/O data lines, I/O control lines and earth wires. The EFT test is a burst of pulses that have predetermined amplitude and limited duration. The typical duration of a burst is 15 ms at a repetition rate of 5 kHz, although 100 kHz repetition is a more realistic test. The burst period, which is

the time from the start of one burst to the start of the next burst, is 300 ms. The test requires the application of six burst frames of ten seconds duration with ten second pauses between frames. In a typical EFT test sequence 3 million pulses will be delivered to the DUT via a capacitive clamp which couples the energy into the system. 表 3 shows the IEC 61000-4-4 EFT test voltage levels and repetition rates:

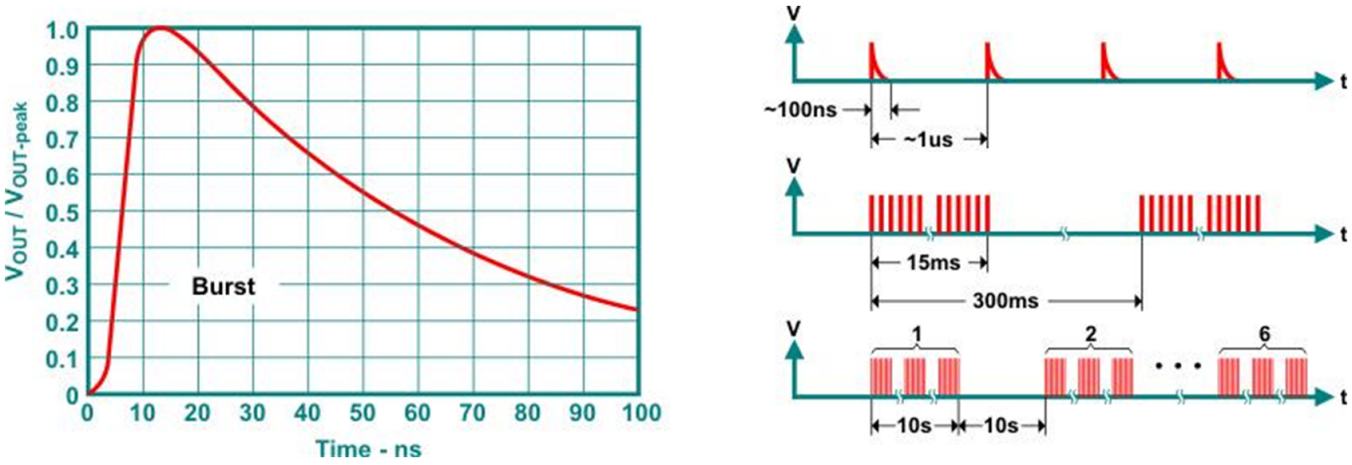
表 3. IEC 61000-4-2 ESD Test Voltage Levels

On Power Port, PE			On I/O, Data and Control Ports	
Level	Test Voltage (kV)	Repetition Rate (kHz)	Test Voltage (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
*	Special	Special	*	Special

* is an open level. The level has to be specified in the dedicated equipment specification.

図 3 depicts the basic shape of the IEC EFT pulse and shows the timing sequence of the test pulses.

図 3. Voltage Waveform of an EFT (Burst) Pulse and Timing Sequence of an Entire Test Cycle



2.2.3 IEC 61000-4-5 Surge Immunity Test

The IEC 61000-4-5 Surge immunity test is the most severe transient immunity test in terms of current and duration. This test is meant to simulate transients caused by direct or indirect lightning strikes as well as the switching of power systems including load changes and short circuits.

The surge generator's output waveforms are specified for open and short circuit conditions. Characteristics for this test are high current (due to low generator impedance) and long pulse duration. Pulse duration for the surge immunity test is approximately 1000 times longer than that of IEC ESD and IEC EFT, resulting in high-energy pulses.

This test requires five positive surge pulses and five negative surge pulses with a time interval between pulses of one minute. Typically though, this time interval is reduced to something shorter than one minute to help reduce overall test time.

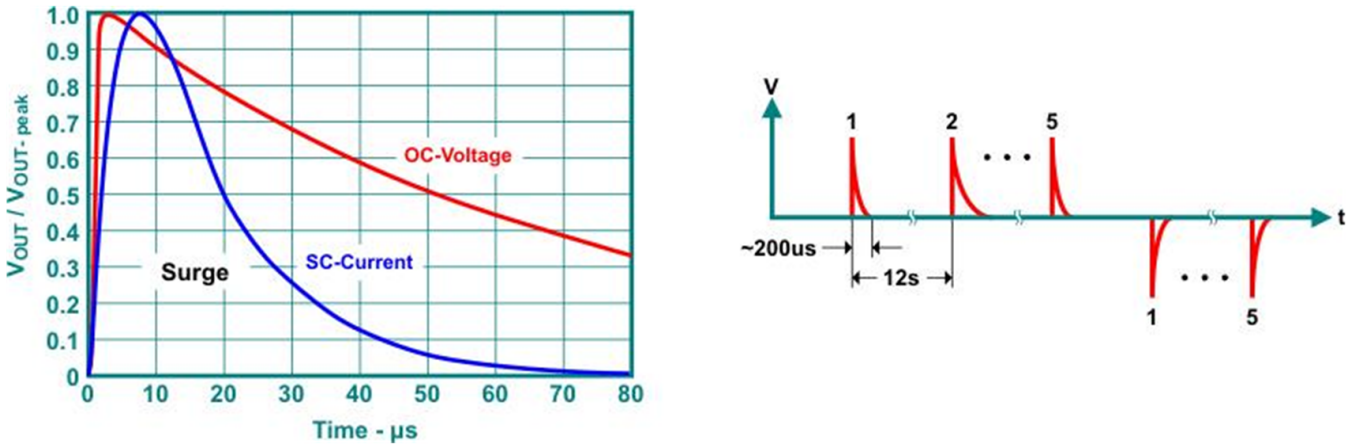
表 4. IEC Surge Open Circuit Voltage Test Levels

Level	Open-Circuit Voltage ±10% (kV)
1	0.5
2	1
3	2
4	4
*	Special

* can be any level above, below, or in between the other levels. This level can be specified in the product standard.

図 4 depicts the basic shape of the IEC surge pulse and shows the timing sequence of the test pulses.

図 4. Voltage and Current Waveform of a Surge Pulse and Timing Sequence of a Test Cycle



2.3 Highlighted Products

2.3.1 SN65HVD3082E

The SN65HVD308xE family of transceivers support half-duplex operation and are designed for RS-485 data bus networks. They are powered by a 5-V supply, support data rates up to 20 Mbps, and are fully compliant to the TIA/EIA-485 standard.

2.3.2 SN65HVD82

The SN65HVD82 transceiver supports half-duplex operation and is designed for RS-485 data bus networks in demanding industrial applications. The SN65HVD82 is powered by a 5-V supply, is optimized for data rates up to 250 kbps, and is fully compliant to the TIA/EIA-485 standard. The bus pins, A and B, have integrated ESD protection making them robust to ESD events with high levels of protection against HBM, Air-Gap Discharge, CDM, IEC 61000-4-2, and IEC 61000-4-4. The SN65HVD82 supports ±12 kV of IEC ESD protection, ±16 kV HBM protection, and ± 4kV IEC EFT protection on die.

2.4 System Design Theory

This design features a very robust three stage protection scheme that includes a TVS diode, a transient blocking unit (TBU), a metal oxide varistor (MOV), series pulse proof resistors, a pad site for an 8 pin SOIC RS-485 transceiver with the SN65HVD82 installed, and banana jacks for injecting the ESD, EFT, and surge test pulses. The concept behind the design is to protect the RS-485 transceiver from lethal transients caused by electrostatic discharge during handling, interruption of inductive loads, relay contact bounce, and/or lightning strikes. Without protection, if the energy that is delivered during one of these transient events is large enough in amplitude it can permanently damage the device.

The TVS is used to provide protection against voltage transients. It acts as a clamping circuit to redirect any high energy pulses to ground and away from the transceiver. The diode needs to be rated for the type of energy levels that are expected per the design. This design was done with the IEC 61000-4-2 standard in mind, and the CDSOT23-SM712 is rated for this application.

The TBU high speed protector is used to shield the TVS diode and the RS-485 driver from AC power cross events or large transients as well as overcurrent conditions. When the transient current exceeds the trigger current level on the TBU device, the TBU clamps or crowbars the current to a safe level by transitioning to a high impedance state.

The MOV protects the TBU device from high voltage surges caused by lightning strikes, power contact, and power induction. The MOV device has a fast turn on time and a high current handling capability to protect the TBU, TVS and RS-485 transceiver.

The series pulse-proof resistors on the A and B bus lines limit the residual clamping current the transceiver sees if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors are typically very low in value (~10-20Ω) and should be selected to accommodate the appropriate power levels.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

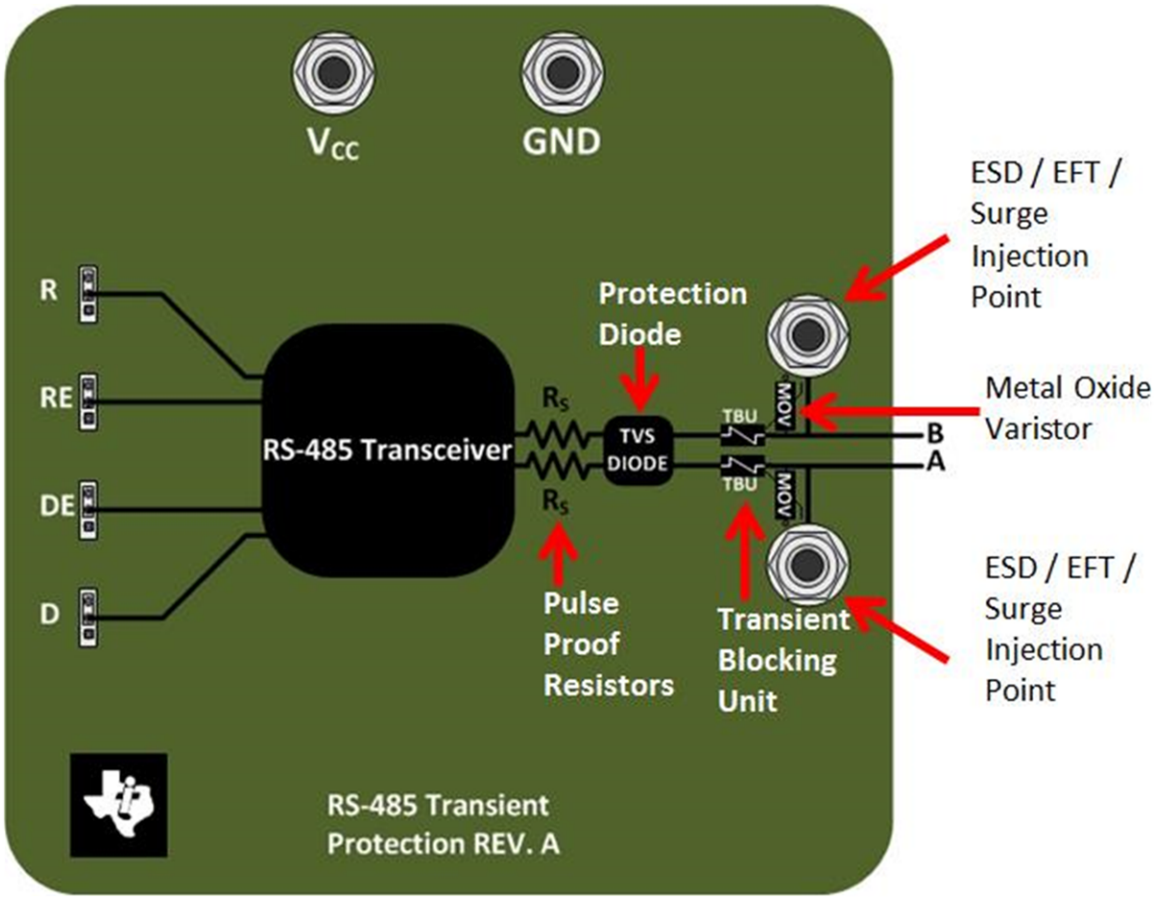
3.1.1 Hardware

The design includes a CDSOT23-SM712 TVS diode from Bourns, a TBU-CA0065-200-WH from Bourns, a MOV-14D561KTR from Bourns, pulse proof resistors, and a SN65HVD82 RS-485 transceiver from Texas Instruments. VCC and GND are connected to the reference design through the banana jacks that can be identified through the silkscreen on the board. The device can be placed into drive mode by pulling the driver enable (DE) pin high through the three pin berg header labeled DE. Pulling DE low disables the driver. The board can be placed into receive mode by pulling the receiver enable pin low (/RE) through the three pin berg header labeled /RE. Pulling /RE high disables the receiver. Once the proper mode is enabled, the device functionality can be checked via the three pin berg header labeled R which is the receiver pin, the three pin berg header labeled D which is the driver pin, and the bus pins via single terminal berg pins labeled A and B.

When device functionality is verified, the transient testing can be done via the two banana jacks connected to the bus pins. The IEC ESD contact test pulses can be injected onto the bus pins by directly touching the banana jacks and discharging the pulses. The IEC ESD air test pulses can be injected onto the bus pins by using either the banana jacks or the single pole berg headers by approaching the contact point slowly until the ESD gun discharges. Care should be taken to ensure that the appropriate bus pin is struck during the air testing as the ESD pulse can jump from pin to pin if the ESD gun is close to both the A and B pins. The EFT test can be performed by connecting the bus wire to the A and B pins and inserting it into the capacitive clamp defined by the IEC 61000-4-4 standard. The surge generator uses shrouded banana jacks to couple the energy onto the bus pins directly.

When performing these types of compliance tests, the test methods should be followed as they are laid out in the standards documentation. After each test level is completed the leakage current should be observed and verified with the leakage current prior to the test, as this can be an indication that something has been broken in the device. The device should be checked for general functionality in both the driver and receiver directions. 図 5 shows an overview of the board with descriptions of each point.

図 5. RS-485 Transient Board Overview



3.2 Testing and Results

3.2.1 Test Setup

Figures 6, 7, and 8 show the test setups used in the IEC immunity compliance testing for this RS-485 design. 図 6 shows the IEC ESD setup. The setup used for this testing is fully compliant to the IEC ESD specification. 図 7 shows the EFT and surge generator box. The EFT/surge generator box is made by EMC-Partner and is model number CDN-UTP. 図 8 shows the complete test setup with the capacitive clamp defined in the IEC 61000-4-4 standard as well as the protective cases used to encase the DUTS during testing. 図 9 shows a close up image of the capacitive clamp used to couple the EFT pulses onto the bus cable.

図 6. IEC ESD Compliant Setup

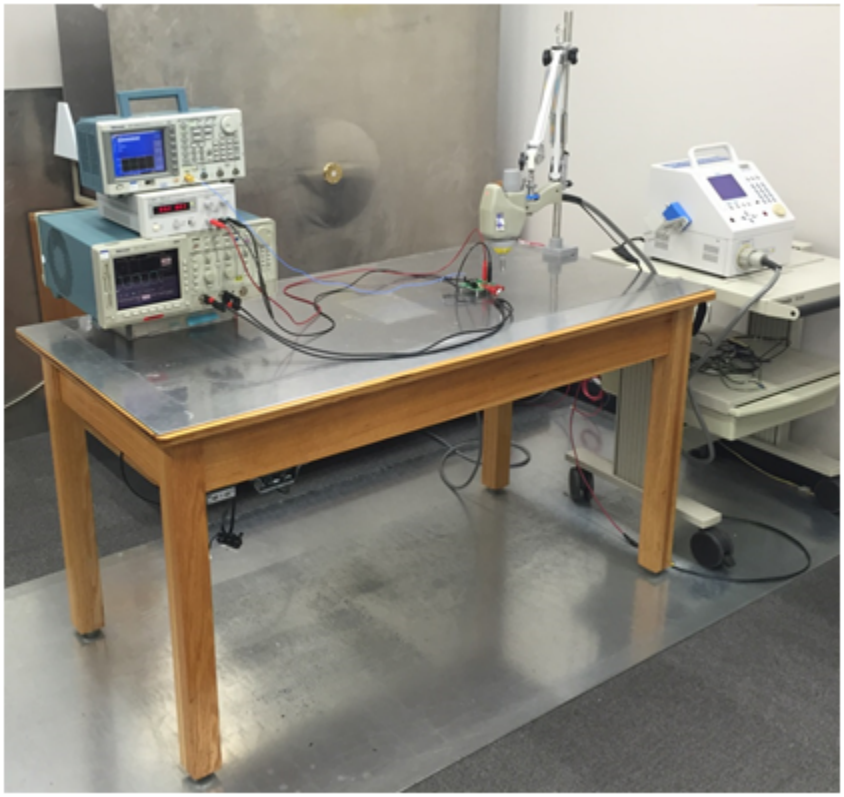


図 7. Electrical Fast Transient (EFT) and Surge Generator

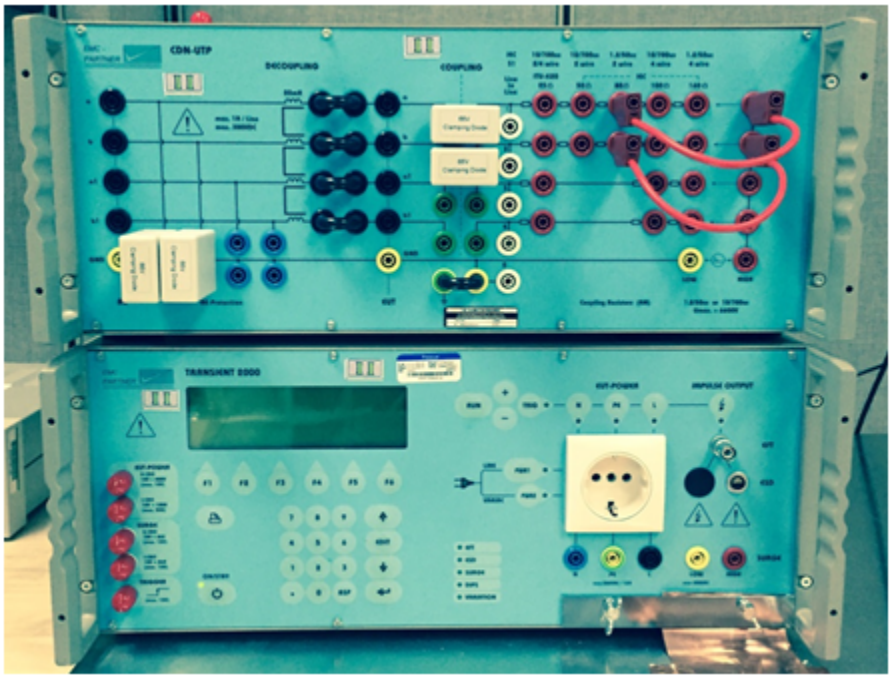


図 8. EFT and Surge Test Setup

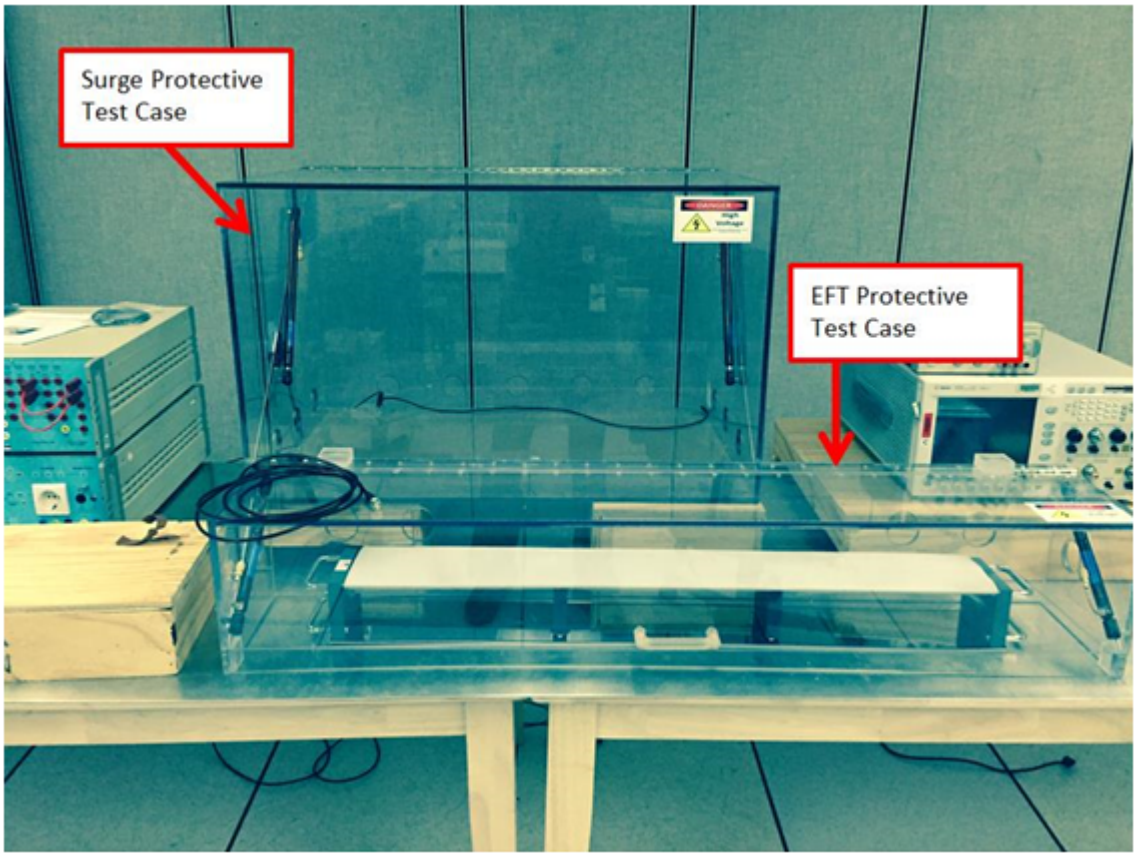
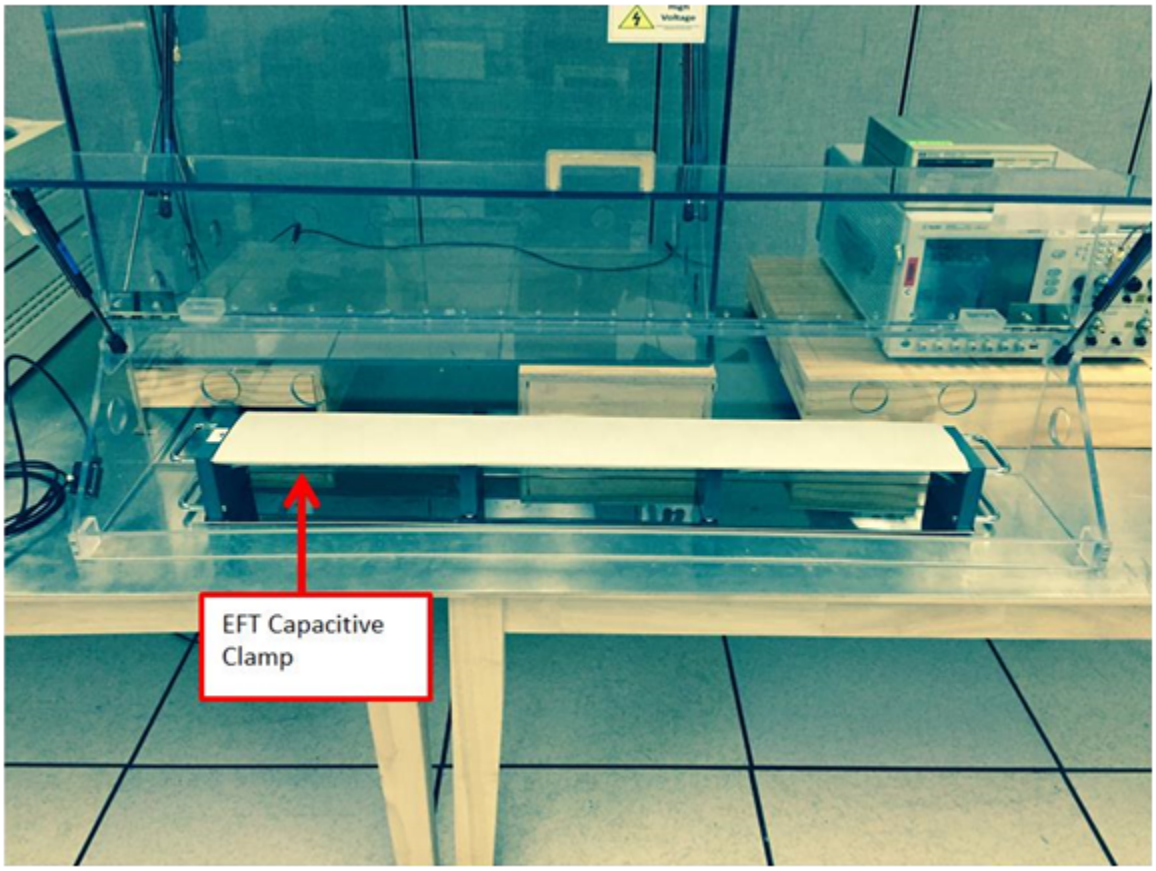


図 9. EFT Capacitive Clamp



3.2.2 Test Results

表 5 summarizes the test results for the SN65HVD3082E and the SN65HVD82 for the IEC 61000-4-2 ESD immunity test, the IEC 61000-4-4 EFT immunity test, and the IEC 61000-4-5 surge immunity test.

表 5. Summary of Test Results

Protection Scheme	IEC ESD (kV)	IEC EFT (kV)	IEC Surge (kV)
SN65HVD82			
MOV/TBU/TVS	±30 Contact	±4	±8
	±30 Air		
SN65HVD3082E			
MOV/TBU/TVS	±14 Contact	±4	±6
	±30 Air		

表 6. IEC Electrostatic Discharge (ESD) Contact Discharge Results

RS-485 IEC ESD Test Results						
IEC ESD Level	Positive Contact ESD Strikes					
	SN65HVD82			SN65HVD3082E		
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
+4kV	Pass	Pass	Pass	Pass	Pass	Pass
+5kV	Pass	Pass	Pass	Pass	Pass	Pass
+6kV	Pass	Pass	Pass	Pass	Pass	Pass

表 6. IEC Electrostatic Discharge (ESD) Contact Discharge Results (continued)

RS-485 IEC ESD Test Results						
+7kV	Pass	Pass	Pass	Pass	Pass	Pass
+8kV	Pass	Pass	Pass	Pass	Pass	Pass
+9kV	Pass	Pass	Pass	Pass	Pass	Pass
+10kV	Pass	Pass	Pass	Pass	Pass	Pass
+11kV	Pass	Pass	Pass	Pass	Pass	Pass
+12kV	Pass	Pass	Pass	Pass	Pass	Pass
+13kV	Pass	Pass	Pass	Pass	Pass	Pass
+14kV	Pass	Pass	Pass	Pass	Pass	Pass
+15kV	Pass	Pass	Pass	Failed	Failed	Failed
+16kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+17kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+18kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+19kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+20kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+21kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+22kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+23kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+24kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+25kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+26kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+27kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+28kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+29kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
+30kV	Pass	Pass	Pass	Not tested	Not tested	Not tested
IEC ESD Level	Negative Contact ESD Strikes					
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
-4kV	Pass	Pass	Pass	Pass	Pass	Pass
-5kV	Pass	Pass	Pass	Pass	Pass	Pass
-6kV	Pass	Pass	Pass	Pass	Pass	Pass
-7kV	Pass	Pass	Pass	Pass	Pass	Pass
-8kV	Pass	Pass	Pass	Pass	Pass	Pass
-9kV	Pass	Pass	Pass	Pass	Pass	Pass
-10kV	Pass	Pass	Pass	Pass	Pass	Pass
-11kV	Pass	Pass	Pass	Pass	Pass	Pass
-12kV	Pass	Pass	Pass	Pass	Pass	Pass
-13kV	Pass	Pass	Pass	Pass	Pass	Pass
-14kV	Pass	Pass	Pass	Pass	Pass	Pass
-15kV	Pass	Pass	Pass	Pass	Pass	Pass
-16kV	Pass	Pass	Pass	Pass	Pass	Pass
-17kV	Pass	Pass	Pass	Pass	Pass	Pass
-18kV	Pass	Pass	Pass	Pass	Pass	Pass
-19kV	Pass	Pass	Pass	Pass	Pass	Pass
-20kV	Pass	Pass	Pass	Pass	Pass	Pass
-21kV	Pass	Pass	Pass	Pass	Pass	Pass
-22kV	Pass	Pass	Pass	Pass	Pass	Pass
-23kV	Pass	Pass	Pass	Pass	Pass	Pass
-24kV	Pass	Pass	Pass	Pass	Pass	Pass

表 6. IEC Electrostatic Discharge (ESD) Contact Discharge Results (continued)

RS-485 IEC ESD Test Results						
-25kV	Pass	Pass	Pass	Pass	Pass	Pass
-26kV	Pass	Pass	Pass	Pass	Pass	Pass
-27kV	Pass	Pass	Pass	Pass	Pass	Pass
-28kV	Pass	Pass	Pass	Pass	Pass	Pass
-29kV	Pass	Pass	Pass	Pass	Pass	Pass
-30kV	Pass	Pass	Pass	Pass	Pass	Pass

表 7. IEC Electrostatic Discharge (ESD) Air Discharge Results

RS-485 IEC ESD Test Results						
IEC ESD Level	Positive Air ESD Strikes					
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
+4kV	Pass	Pass	Pass	Pass	Pass	Pass
+5kV	Pass	Pass	Pass	Pass	Pass	Pass
+6kV	Pass	Pass	Pass	Pass	Pass	Pass
+7kV	Pass	Pass	Pass	Pass	Pass	Pass
+8kV	Pass	Pass	Pass	Pass	Pass	Pass
+9kV	Pass	Pass	Pass	Pass	Pass	Pass
+10kV	Pass	Pass	Pass	Pass	Pass	Pass
+11kV	Pass	Pass	Pass	Pass	Pass	Pass
+12kV	Pass	Pass	Pass	Pass	Pass	Pass
+13kV	Pass	Pass	Pass	Pass	Pass	Pass
+14kV	Pass	Pass	Pass	Pass	Pass	Pass
+15kV	Pass	Pass	Pass	Pass	Pass	Pass
+16kV	Pass	Pass	Pass	Pass	Pass	Pass
+17kV	Pass	Pass	Pass	Pass	Pass	Pass
+18kV	Pass	Pass	Pass	Pass	Pass	Pass
+19kV	Pass	Pass	Pass	Pass	Pass	Pass
+20kV	Pass	Pass	Pass	Pass	Pass	Pass
+21kV	Pass	Pass	Pass	Pass	Pass	Pass
+22kV	Pass	Pass	Pass	Pass	Pass	Pass
+23kV	Pass	Pass	Pass	Pass	Pass	Pass
+24kV	Pass	Pass	Pass	Pass	Pass	Pass
+25kV	Pass	Pass	Pass	Pass	Pass	Pass
+26kV	Pass	Pass	Pass	Pass	Pass	Pass
+27kV	Pass	Pass	Pass	Pass	Pass	Pass
+28kV	Pass	Pass	Pass	Pass	Pass	Pass
+29kV	Pass	Pass	Pass	Pass	Pass	Pass
+30kV	Pass	Pass	Pass	Pass	Pass	Pass
IEC ESD Level	Negative Air ESD Strikes					
	Board 1	Board 2	Board 3	Board 1	Board 2	Board 3
-4kV	Pass	Pass	Pass	Pass	Pass	Pass
-5kV	Pass	Pass	Pass	Pass	Pass	Pass
-6kV	Pass	Pass	Pass	Pass	Pass	Pass
-7kV	Pass	Pass	Pass	Pass	Pass	Pass
-8kV	Pass	Pass	Pass	Pass	Pass	Pass
-9kV	Pass	Pass	Pass	Pass	Pass	Pass

表 7. IEC Electrostatic Discharge (ESD) Air Discharge Results (continued)

RS-485 IEC ESD Test Results						
-10kV	Pass	Pass	Pass	Pass	Pass	Pass
-11kV	Pass	Pass	Pass	Pass	Pass	Pass
-12kV	Pass	Pass	Pass	Pass	Pass	Pass
-13kV	Pass	Pass	Pass	Pass	Pass	Pass
-14kV	Pass	Pass	Pass	Pass	Pass	Pass
-15kV	Pass	Pass	Pass	Pass	Pass	Pass
-16kV	Pass	Pass	Pass	Pass	Pass	Pass
-17kV	Pass	Pass	Pass	Pass	Pass	Pass
-18kV	Pass	Pass	Pass	Pass	Pass	Pass
-19kV	Pass	Pass	Pass	Pass	Pass	Pass
-20kV	Pass	Pass	Pass	Pass	Pass	Pass
-21kV	Pass	Pass	Pass	Pass	Pass	Pass
-22kV	Pass	Pass	Pass	Pass	Pass	Pass
-23kV	Pass	Pass	Pass	Pass	Pass	Pass
-24kV	Pass	Pass	Pass	Pass	Pass	Pass
-25kV	Pass	Pass	Pass	Pass	Pass	Pass
-26kV	Pass	Pass	Pass	Pass	Pass	Pass
-27kV	Pass	Pass	Pass	Pass	Pass	Pass
-28kV	Pass	Pass	Pass	Pass	Pass	Pass
-29kV	Pass	Pass	Pass	Pass	Pass	Pass
-30kV	Pass	Pass	Pass	Pass	Pass	Pass

表 8. IEC Electrical Fast Transient (EFT) Results

RS-485 IEC EFT Test Results			
Positive EFT Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
+0.5kV	Pass	Pass	Pass
+1kV	Pass	Pass	Pass
+2kV	Pass	Pass	Pass
+4kV	Pass	Pass	Pass
Negative EFT Strikes			
IEC EFT Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
-0.5kV	Pass	Pass	Pass
-1kV	Pass	Pass	Pass
-2kV	Pass	Pass	Pass
-4kV	Pass	Pass	Pass
Positive EFT Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
+0.5kV	Pass	Pass	Pass
+1kV	Pass	Pass	Pass
+2kV	Pass	Pass	Pass
+4kV	Pass	Pass	Pass
Negative EFT Strikes			
IEC EFT Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3

表 8. IEC Electrical Fast Transient (EFT) Results (continued)

RS-485 IEC EFT Test Results			
-0.5kV	Pass	Pass	Pass
-1kV	Pass	Pass	Pass
-2kV	Pass	Pass	Pass
-4kV	Pass	Pass	Pass

表 9. IEC Surge Results

RS-485 IEC Surge Test Results			
Positive Surge Strikes			
IEC Surge Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
+0.5kV	Pass	Pass	Pass
+1kV	Pass	Pass	Pass
+2kV	Pass	Pass	Pass
+4kV	Pass	Pass	Pass
+6kV	Pass	Pass	Pass
Negative Surge Strikes			
IEC Surge Level	SN65HVD82 Board 1	SN65HVD82 Board 2	SN65HVD82 Board 3
-0.5kV	Pass	Pass	Pass
-1kV	Pass	Pass	Pass
-2kV	Pass	Pass	Pass
-4kV	Pass	Pass	Pass
-6kV	Pass	Pass	Pass
Positive Surge Strikes			
IEC Surge Level	SN65HV3082E Board 1	SN65HV3082E Board 2	SN65HV3082E Board 3
+0.5kV	Pass	Pass	Pass
+1kV	Pass	Pass	Pass
+2kV	Pass	Pass	Pass
+4kV	Pass	Pass	Pass
+6kV	Pass	Pass	Pass
Negative Surge Strikes			
IEC Surge Level	SN65HVD3082E Board 1	SN65HVD3082E Board 2	SN65HVD3082E Board 3
-0.5kV	Pass	Pass	Pass
-1kV	Pass	Pass	Pass
-2kV	Pass	Pass	Pass
-4kV	Pass	Pass	Pass
-6kV	Pass	Pass	Pass

3.2.3 Conclusion of Test Results

The test results show that by adding the TVS diode, the transient blocking unit, the metal oxide varistor, and the pulse proof resistors to the A and B bus lines of both the SN65HVD3082E and SN65HVD82 transceivers, the transient immunity increases significantly. The designs pass IEC ESD level 4 criteria, IEC EFT level 4 criteria, and IEC surge level 4 criteria. Both designs also fall into the “special” characteristic per the IEC ESD standard as the SN65HVD3082E passes IEC ESD up to ±14 kV while the SN65HVD82 passes up to ±30 kV IEC ESD, surpassing the level 4 ESD voltage.

Not every design or application will require ±30 kV of ESD protection, but for those applications that do, the SN65HVD82 coupled with the CDSOT23-SM712 TVS diode, the TBU-CA0065-200-WH, and the MOV-14D561KTR from Bourns will provide this as well as level 4 IEC ESD and surge protection.

For designs that do not require this level of protection but need to be rated up to level 4 IEC ESD (±8 kV), coupling the SN65HVD3082E with the same CDSOT23-SM712 TVS diode, TBU-CA0065-200-WH, and MOV-14D561KTR from Bourns takes a standard RS-485 transceiver with no integrated IEC ESD protection to ±14 kV IEC ESD protection and level 4 IEC EFT/surge.

Certain specialized transceivers are available that can provide some level of IEC 61000-4-5 surge immunity without the need for any external protection components. For example, the THVD1429 device is designed to withstand 1.2/50-µs surges up to 2.5 kV. This device would be suitable for applications requiring up to Level 3 protection.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00731.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00731.

4.3 PCB Layout Recommendations

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance.
3. NOTE: High-frequency currents follow the path of least inductance and not the path of least impedance.
4. Design the protection components into the direction of the signal path. Do not force the transient's currents to divert from the signal path to reach the protection device.
5. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of transceiver, UART, and controller ICs on the board.
6. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
7. Use 1-kΩ to 10-kΩ pull up or pull-down resistors for enable lines to limit noise currents in these lines during transient events.
8. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00731.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-00731.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00731.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00731.

5 Related Documentation

Texas Instruments, *Protecting RS-485 Interfaces Against Lethal Electrical Transients*

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6 About the Author

Michael Peffers is an applications engineer at Texas Instruments supporting the RS-485, LVDS, PECL, CAN, LIN, IO-Link, and Profibus interface products. Michael is responsible for developing reference design solutions for the industrial segment and direct customer support including onsite support as well as onsite training. Michael is also responsible for producing technical content such as application notes, datasheets, white papers, and is the author of a recurring blog on the Texas Instruments E2E forum called Analog Wire: Get Connected. Michael brings to this role his experience in high-speed SERDES applications as well as experience in the optical transceiver space. Michael earned his Bachelors of Science in Electrical Engineering (BSEE) from the University of Central Florida (UCF).

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2015) から **Revision B** に変更	**Page**
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