参考資料

デザイン・ガイド：TIDA-020003
MIPI CSI-2、PMIC、FPD-Link III、POC を搭載した、車載用 2MP カメラ・モジュールのリファレンス・デザイン

概要

このカメラ・モジュールのリファレンス・デザインは、2 メガピクセルの撮像素子と 4Gbps のシリアライザを組み合わせることで、車載システム用小型カメラの要求に対応しています。また、電源管理集積回路 (PMIC) により、超小型のフォームファクタで 2 つのデバイスに電力を供給できます。このデザインには、リモート車載用カメラ・モジュールをディスプレイやマシン・ビジョン処理システムに同軸ケーブルで接続し、データと電力の両方を伝送する、高速シリアル・インターフェイスが含まれています。このリファレンス・デザインで使用している 4Gbps FPD-Link III SerDes テクノロジを使うと、非圧縮の 2MP ビデオ・データ、双方向制御信号、POC (Power Over Coax) を 1 本のケーブルで伝送できます。

リソース

TIDA-020003	デザイン・フォルダ
TPS650330-Q1	プロダクト・フォルダ
DS90UB953-Q1	プロダクト・フォルダ

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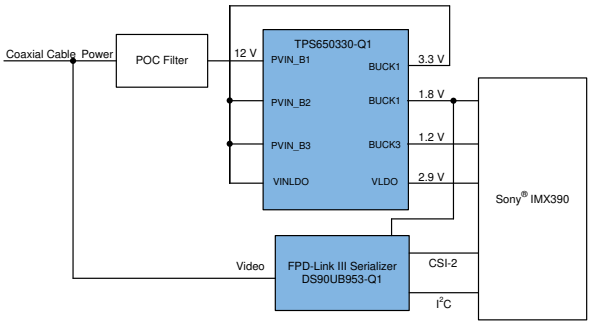
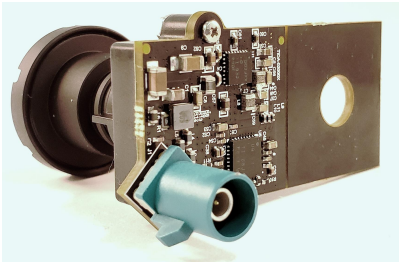
特長

- 1 枚の 21mm × 21mm の PCB に統合型電源を搭載した省スペース設計
- 統合型電源に 3 つの降圧コンバータと LDO を内蔵し、高効率と低ノイズの電源生成を実現
- 4Gbps の DS90UB953 を使用して高分解能のカメラ・アプリケーションに対応
- Sony®の 2.1MP IMX390 イメージ・センサにより、フル HD、AD 10 ビット、MIPI 4 レーン、RAW24、RAW20、RAW12 を実現
- デジタル・ビデオ、電力供給、制御、診断用に Rosenberger 製 FAKRA 同軸コネクタを 1 個実装
- 追加診断機能により ASIL アプリケーションに対応
- 設計上の考慮事項と特性テスト・データが付属

アプリケーション

- 処理なしのカメラ・モジュール
- フロント・カメラ
- ミラー代替/CMS
- サラウンド・ビュー・システムの ECU





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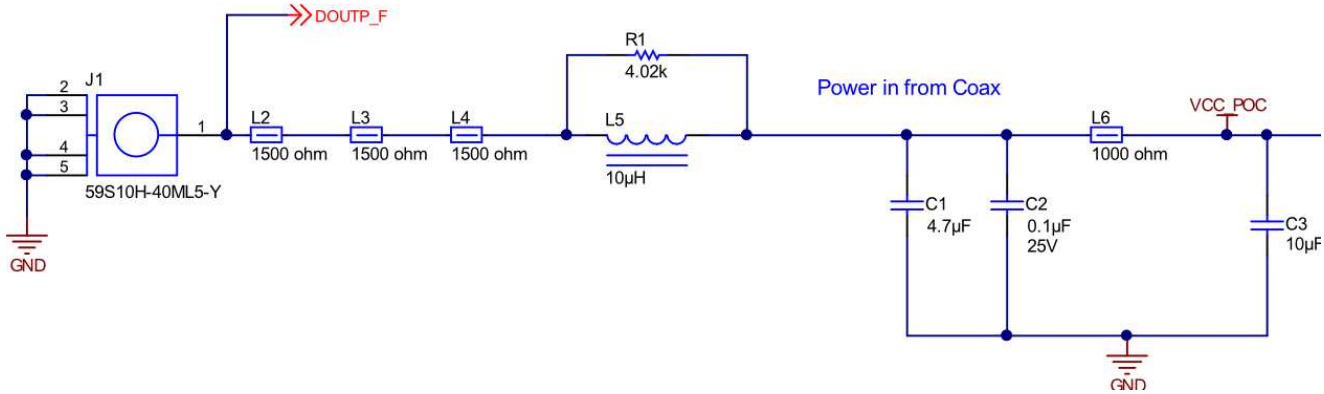
1 System Description

Many automotive applications require small form factors with reduced circuit area that enable compact and modular systems. As a result, most cameras along with electronic components must meet this minimal area constraint when designing ADAS camera applications. This reference design addresses these needs by including a 2-megapixel imager, 4 Gbps serializer, and a single Power Management IC, and all components contained within an area of 21-mm × 21-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power, the FPD-Link front and backchannels enter the board through the FAKRA coax connector. The filter in 図 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

図 1. FPD-Link III Signal Path



The DC portion is connected to the Buck 1 input of the TPS650330 Power Management IC. This voltage powers Buck 2 and Buck 3 of the device, which are responsible for creating the supply rails to the imager and serializer. The LDO input pin is supplied 3.3 V, which is responsible for providing a low-noise, 2.9-V analog supply to the imager. Buck 3 outputs the imager-dedicated 1.2 V and Buck 2 generates a universal 1.8-V digital supply that is shared by both the imager and serializer. The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel takes between the serializer and deserializer.

The output of the imager is connected through a four-lane MIPI CSI-2 interface to the serializer. The serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

Additionally, on the same coax cable, there is a separate low-latency, bidirectional control channel that provides the additional function of transmitting control information from an I^2C port. This control channel is independent of the video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (PoC)	4	12	18.3	V
P_{TOTAL}	Total power consumption	V_{PoC} = 12 V	—	0.6	1	W

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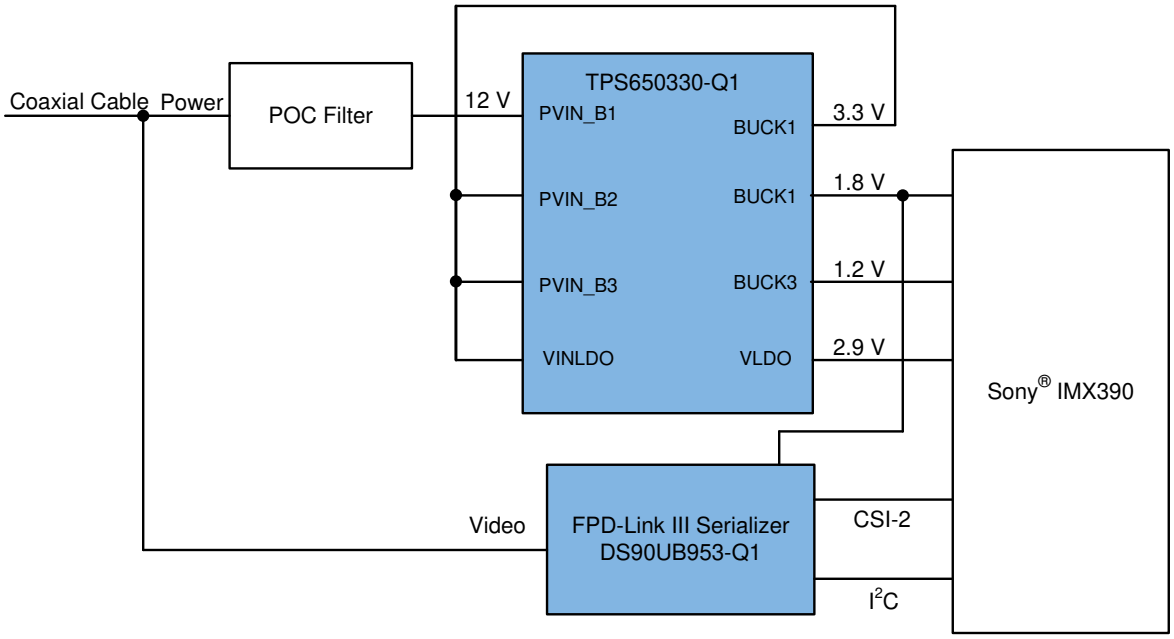
2 System Overview

2.1 Block Diagram

図 2. Camera Block Diagram



2.2 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS650330-Q1: an automotive qualified, four-channel PMIC optimized for camera applications. The device integrates three buck converters and one LDO, along with overvoltage and undervoltage supervisors for each voltage rail. A high, fixed PWM 2.2-MHz switching frequency enables the use of small inductors with a fast transient response. The low-noise, high-PSRR LDO provides an output voltage option for sensitive analog circuits. The output voltage and sequencing settings, along with other operational settings are programmable via I^2C for compatibility with a variety of imagers without the need for any additional components.

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2.2.1 IMX390 Imager

The Sony® IMX390 is a diagonal 6.67-mm (Type 1/2.7) CMOS active pixel type solid-state image sensor with a square pixel array and 2.12 effective pixels. The sensor supports Full-HD, AD 12-bit, MIPI 4-lane, RAW24, RAW20, RAW12 output. Other included features follow:

- Supports image sizes: (2.07MB pixels) 1920 × 1080 Full-HD, (2.30M pixels) 1920 × 1200 WUXGA
- Requires three voltage rails (2.9 V, 1.8 V, and 1.2 V)
- Can be configured using an I^2C-compatible two-wire serial interface

2.2.2 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 mates well with the MIPI CSI-2 video output of the IMX390 imager. Once combined with the filters for the PoC, video, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the *Cable requirements for the DS90UB913A and DS90UB914A application report*.

2.2.3 TPS650330-Q1

The TPS650330-Q1 device is a highly-integrated power management IC for automotive camera modules. This device combines three step down converters and one low-dropout (LDO) regulator. The BUCK1 stepdown converter has an input voltage range up to 18.3 V for connections to Power over Coax (PoC). All converters operate in a forced fixed-frequency PWM mode. The LDO can supply 300 mA and operate with an input voltage range from 3.0 V to 5.5 V. The step-down converters and the LDO have separate voltage inputs that enable maximum design and sequencing flexibility. Additionally, an integrated Spread-Spectrum Clock (SSC) enables robust EMI performance. A small form-factor, added rail supervision features, and programmability make this device a very attractive candidate for designs that need to be expedited or scaled for future applications.

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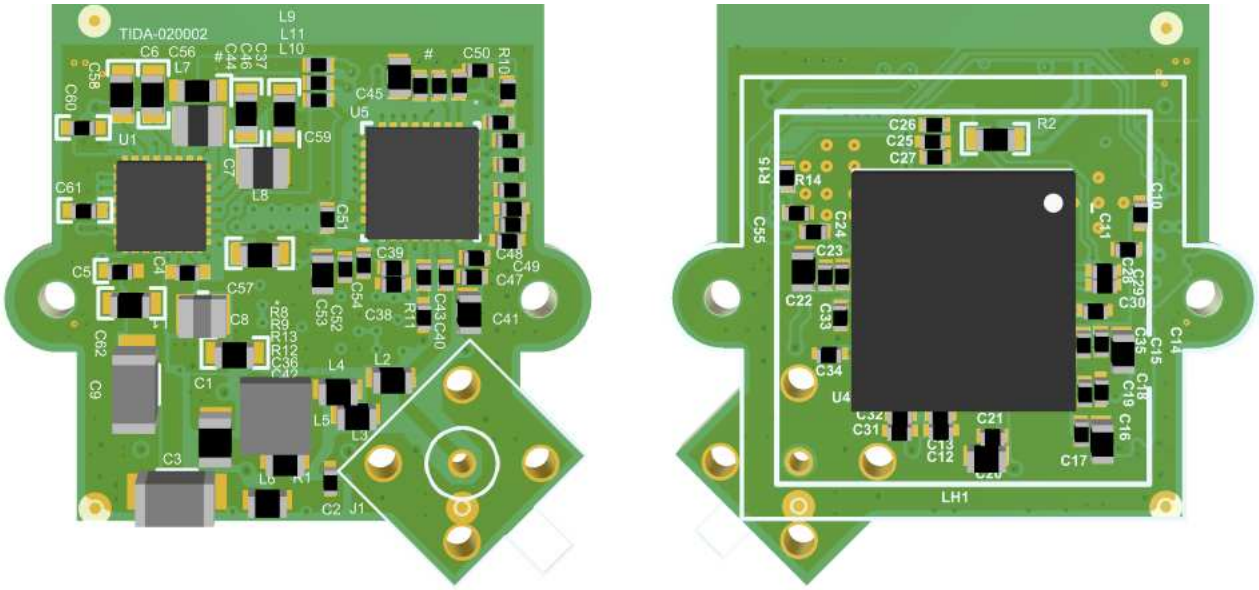
2.3 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.3.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor; however, the goal of the design is to showcase a solution with minimal PCB area and compact design. The area of the board roughly equates to a dimension of 21 mm × 21 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

図 3. PCB Top and Bottom Views



2.3.2 Power Supply Design

2.3.2.1 PoC Filter

One of the most critical portions of a design that uses PoC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise-coupled backwards from the rest of the system.

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC.

For the PoC design, to enable the forward channel and backchannel to pass uninterrupted over the coax, an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 10-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2.2-GHz frequency band. This complete filter is shown by L2 in 図 4. L1 would be the same but its PoC filter for the deserializer side of the FPD-Link III transmission.

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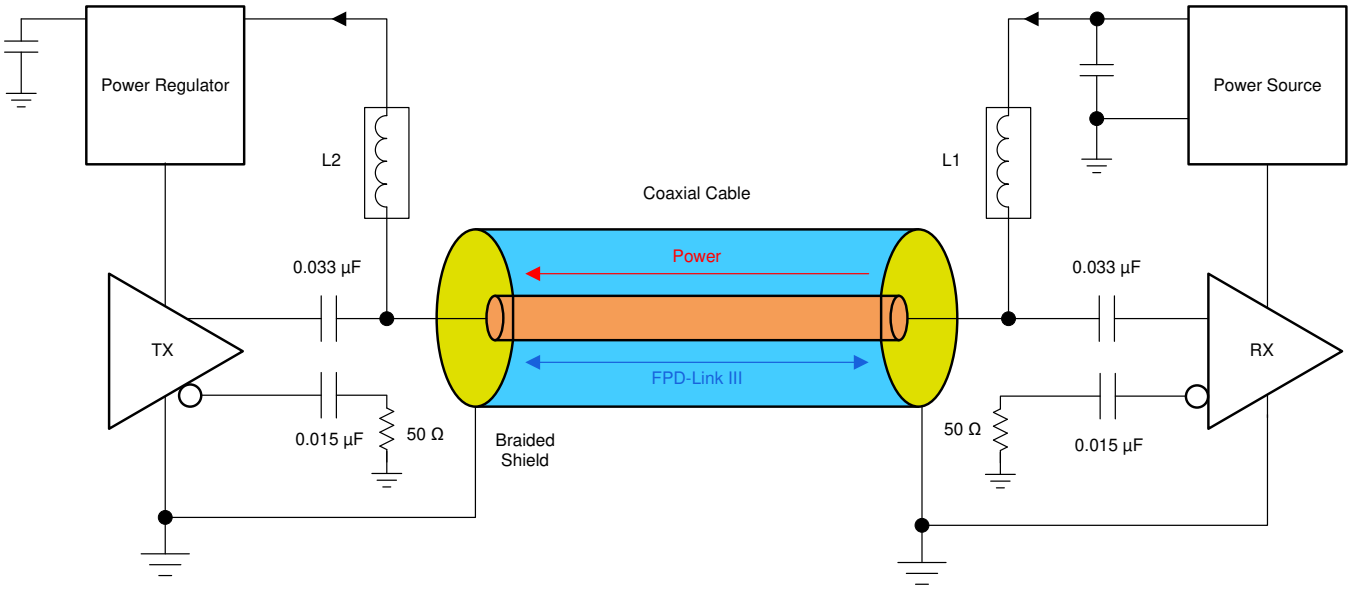
In this camera design, it is imperative that this filter has the smallest footprint allowable. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward-channel filtering, inductors usually are not sufficient to filter above 1 GHz. This reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized onboard for the PoC inductor filtering. For more details, see the *Sending power over coax in DS90UB913A designs application report*.

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors shown by the 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through but that the DC is blocked from getting on the data lines. A smaller capacitance is required for the DS90UB953-Q1 and DS90UB954-Q1 devices than previous generations, because they need to pass 4 Gbps of data while the previous generation only needed to pass the 2 Gbps of data seen on 1-MP cameras.

図 4. Power Over Coax



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2.3.2.2 Power Supply Considerations

As this reference design is targeted at automotive applications, there are several considerations that limit design choices. Additionally, the following list of system-level specifications helped shape the final overall design:

- The total solution size needs to be minimized to meet the size requirement of this design, which is equivalent to 21 mm × 21 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate the need for external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design looks at higher frequency switchers.
- All devices need to be AEC Q100-Q1 rated.

Before parts can be chosen, the input voltage range, required voltage rails, and required current per rail must be known. In this case, the input voltage is a pre-regulated 12-V supply coming in over the coaxial cable. This system has only two main devices, the imager and serializer, which are responsible for power consumption during operation. 表 2 shows the requirements of the supplies:

表 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (MAX) (A)	POWER (MAX) (W)
DS90UB953			
VDD-1.8	1.8	0.225	0.405
IMX390			
VDD-1.2	1.2	0.388	0.4656
VDD-1.8	1.8	negligible	0
VDD-2.9	2.9	0.063	0.1827
Supply Rails Total Current Requirement and Maximum Power			
1.2-V rail	1.2	0.388	0.4656
1.8-V rail	1.8	0.225	0.405
2.9-V rail	2.9	0.063	0.1827
3.3-V rail	3.3	0.327	1.0785

The 12-V supply over the coaxial cable is first stepped down to 3.3 V, which then supplies the rest of the system on the camera module. In this design, the 1.8-V rail supplies both the DS90UB953 supply, and the interface supply of the IMX390 imager. Since the current consumed by the DS90UB953 serializer is predominantly greater than the IMX390 interface supply, the 1.8-V current provided to the IMX390 imager can be considered as negligible. The IMX390 2.9-V analog rail requires 63 mA, the DS90UB953 serializer 1.8-V rail requires 225 mA, and the IMX390 digital 1.2-V rail requires 388 mA. Assuming 100% efficiency to simplify calculations with the previous values, it is calculated that the 3.3-V supply will require 327 mA to successfully power the 1.2-V, 1.8-V, and 2.9-V rails. Because the input and output voltages, output current requirements, and total wattage consumption are known, the input current can be calculated with 式 1:

$$P = V \times I = 12V \times I_{IN} = 1.0785\ W$$
$$\therefore I_{IN} = (1.0785\ W \times 12V) = 89.9\ mA \quad (1)$$

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This information provides a strong foundation in the selection of power topologies and inductive passives that will be explained in later sections. This approximation does ease calculations with the assumption of 100% efficiency; however, for more understanding of true efficiency values reference the device data sheets.

Due to the requirement of Q100, it is mandatory that the switching frequency is rated outside of the AM band and must satisfy the voltage and current requirements derived previously. As the input voltage is a regulated voltage that will always be greater than any of the power rails produced, it is easily understood that the power topologies selected should either be step-down converters (bucks) or LDOs. Bucks are generally included in supplies where switching noise is not a significant concern, and power savings is the largest care about. On the other hand, LDOs can be incorporated in establishing low-noise analog supplies that reduce inherent noise and are more robust against EMI interactions; however, this is at the expense of larger current consumption.

In this design, a single Power Management IC is responsible for powering the supply rails. This device, the TPS650330-Q1, was chosen as it incorporates three step-down converters (BUCKS) and an LDO in a single 4.0-mm x 4.0-mm VQFN package. The current requirements of the design also played an important role in the selection of the device, as the BUCKS are capable of providing more than 1 A, while the LDO is capable of supplying a maximum current output of 300 mA. Buck 1 steps down the 12-V PoC input to 3.3 V. The 3.3-V rail then supplies power to BUCK2, BUCK3, and the LDO input. BUCK 2 provides the interface and digital supply for both the IMX390 imager and DS90UB953 serializer, while the LDO output creates a clean, low-noise supply for the 2.9-V analog supply for the IMX390.

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2.3.2.2.1 Choosing the TPS650330-Q1 BUCK1 Output Inductor and Capacitor

The high, fixed PWM 2.3-MHz switching frequency enables the use of small inductors with a fast transient response. A value of 1.5 µH is typically recommended for the BUCK1 channel output; however, in an effort to further reduce inductor ripple current, a value of 2.2 µH was chosen.

With the inductance value chosen, the design now needs an inductor with a proper saturation current. This is the combination of the steady-state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate inductor ripple with 式 2:

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L(min) \times f_{SW}} \right)$$

where:

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- $L_{(min)}$ is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency (2)

The parameters for this reference design using the TPS650330-Q1 are:

- V_{OUT} = 3.3 V
- $V_{IN(max)}$ = 18.3 V
- $L_{(min)}$ = 2.2 µH
- f_{SW} = 2.3 MHz

These parameters yield an inductor current of ΔI_L = 535 mA. The maximum current draw of the system through this regulator is 327 mA. The minimum saturation current is calculated as:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 327\ mA + \frac{535\ mA}{2} = 594\ mA \quad (3)$$

The TPS650330-Q1 device on this design uses a Murata® LQM2MPN2R2NG0, which has a rated current of 1.2 A and a DC resistance maximum of 138 mΩ. Additionally, this device has an operating temperature of –55°C to 125°C and comes in a very small 2-mm × 1.6-mm package.

2.3.2.2.2 Choosing TPS650330-Q1 BUCK2 and BUCK3 Output Inductor and Capacitor

BUCK2 and BUCK3 have a recommended output inductor value of 1.0 µH. When selecting a component, it is important to verify the DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly -- lower DC resistance is directly proportional to efficiency.

The saturation requirement of the inductor is determined by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current using:

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$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- f = Switching frequency (2.3-MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current (4)

The parameters for this design using the BUCK2 1.8-V output rail are:

- V_{OUT} = 1.8 V
- V_{IN} = 3.3 V
- L = 1 µH
- f_{SW} = 2.3 MHz

These parameters yield an inductor current of ΔI_L = 356 mA. The maximum current draw through this regulator is 255 mA, which results in the following minimum saturation current calculation:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 225\ mA + \frac{356\ mA}{2} = 403\ mA \quad (5)$$

While the parameters for the BUCK3 1.2-V rail are:

- V_{OUT} = 1.2 V
- V_{IN} = 3.3 V
- L = 1 µH
- f_{SW} = 2.3 MHz

These parameters yield an inductor current of ΔI_L = 332 mA. The maximum current draw through this regulator is 388 mA, resulting in the following minimum saturation current calculation:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 388\ mA + \frac{332\ mA}{2} = 554\ mA \quad (6)$$

BUCK 2 and BUCK 3 outputs of this design use a TDK Corporation® TFM201610ALMA1R0MTAA, which has a rated current of 3.1 A, DC resistance of 60 mΩ, and includes an operating temperature range of –55°C–150C. This part comes in a very small 1.6-mm × 2.0-mm package.

2.3.2.2.3 TPS650330-Q1 LDO

Design considerations for the LDO are more relaxed than the previous buck converters as they do not require an output inductor. The only considerations for this LDO are sizing the input and output capacitance. For the input capacitance, a capacitor is not required for stability but for improved transient response performance, a 0.1-µF effective capacitance is recommended. The output capacitor requires a minimum effective capacitance of 0.1 µF for stability. In both cases, the input and output capacitor can benefit from using a 1-µF X7R capacitor so that when experiencing derating, they will be above 0.1 µF.

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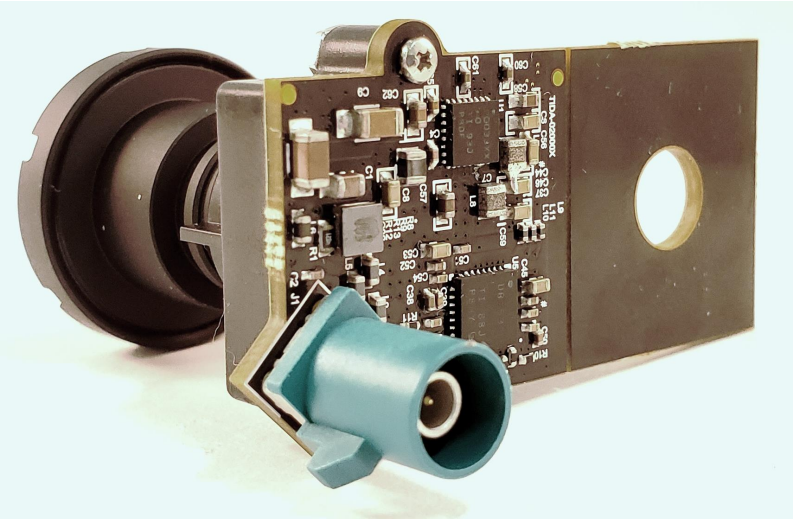
3 Hardware, Testing Requirements, Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in 図 5.

図 5. Getting Started With Board



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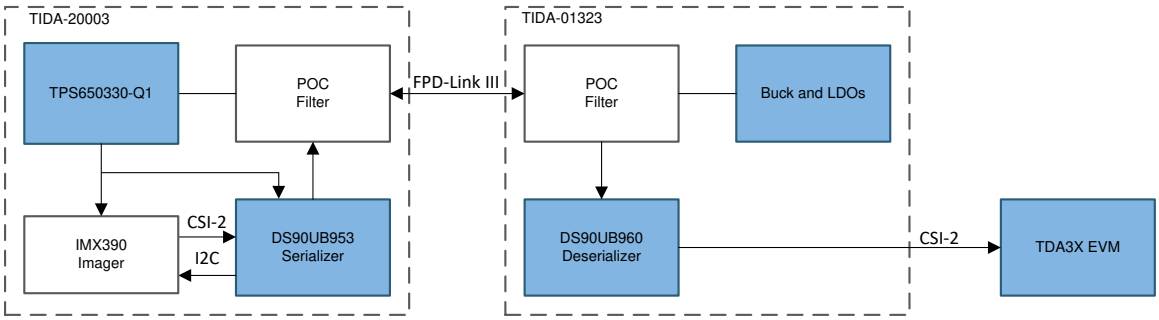
3.1.1 Video Output Hardware Setup

図 6 shows the setup to test the video output of the camera module on this reference design. This reference design includes an IMX390 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I^2C interfaces. The DS90UB953-Q1 serializer then connects through PoC to a DS90UB960-Q1 quad deserializer. Note that for test setup, only one channel is used from the DS90UB960-Q1 device.

To enable video output from the DS90UB960-Q1 device, the EVM is connected to the CSI-2 Samtec connector on the TDA3x EVM. The TDA3x EVM enables video output by writing all the backchannel I^2C setting configurations for the IMX390, DS90UB953-Q1, and DS90UB960-Q1 devices. When these writes are completed, Vision SDK software enables video output to an HDMI-connected monitor.

図 6. Block Diagram of Video Output Setup



3.1.2 FPD-Link III I^2C Initialization

With the setup in 図 6 connected, the TIDA-01323 design is supplied 12-V input power, which is delivered through PoC to power the TIDA-020003 camera module. It is additionally used to step down to 1.8 V and 1.1 V for the DS90UB960-Q1 supplies. Once all rails are established, all devices (MX390, DS90UB953-Q1, and DS90UB960-Q1) receive power. Lastly, by connecting the TDA3x EVM to the TIDA-01323 design, the I^2C writes for initialization can begin. Note that the following writes are only showing one channel camera and may not be the mode wanted for specific multi-camera mode. For example, each camera requires its own port initialization using address 0x3A for that specific port. The writes to initialize the DS90UB960-Q1 deserializer and DS90UB953-Q1 serializer are as follows:

- Deserializer slave I^2C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x5D: I^2C passthrough enabled and backchannel frequency select
  - Register 0x5C with 0x30: Sets serializer alias to 0x30 (8-bit) or 0x18 (7-bit)
  - Register 0x5D with 0x34: Sets slave ID for imager to 0x34 (8-bit) or 0x1A (7-bit)
  - Register 0x65 with 0x34: Sets slave alias for imager to 0x34 (8-bit) or 0x1A (7-bit)
  - Register 0x6D with 0x7C: Configures port to coaxial mode and FPD III to CSI mode
  - Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
  - Register 0x33 with 0x03: Enables DS90UB960-Q1 CSI output and sets to 2 lane mode
  - Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
  - Register 0x20 with 0x00: Forwarding enabled for all ports and ports forwarded to CSI-2 Port 0
- Serializer slave I^2C address 0x30 (8-bit) or 0x18 (7-bit):
  - Register 0x06 with 0x21: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from DS90UB953-Q1 to

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IMX390

- Register 0x07 with 0x28: Sets DIV_N_VAL for CLKOUT from DS90UB953-Q1 to IMX390
- Register 0x0E with 0xF0: Sets GPIO0 and GPIO1 as outputs, and GPIO2 and GPIO3 as outputs on DS90UB953-Q1
- Register 0x0D with 0x01: Pulls RESET pin on IMX390 high to bring imager out of reset

3.1.3 IMX390 Initialization

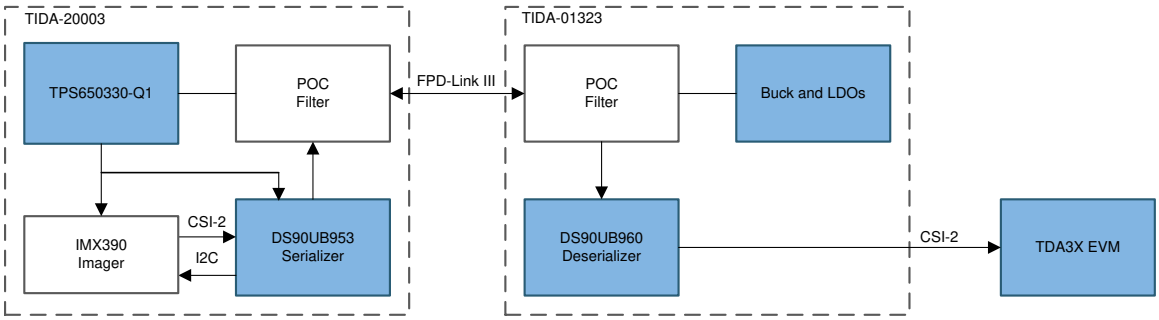
Once the FPD-Link III setup is done for the DS90UB953-Q1 and DS90UB960-Q1 devices, the I^2C initialization can now be done on the IMX390. For these writes, see the IMX390 data sheet for register settings. There are many register settings listed, but as long as the DS90UB953-Q1 and DS90UB960-Q1 FPD-Link III parts are configured, the I^2C backchannel allows for the IMX390 to be accessed at address 0x34 in 8-bit addressing or 0x1A in 7-bit addressing.

3.2 Testing and Results

3.2.1 Characterization Test Setup

For the following tests to verify power supply and I^2C communication, the camera is connected to TIDA-01323, a quad 2MP FPD-Link III hub which utilizes the DS90UB960-Q1 deserializer. The TIDA-01323 then connects to the TDA3XEVM.

図 7. Block Diagram of Characterization Test Setup



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3.2.1.1 Power Supplies Start Up

図 8 shows the probe setup to measure the power sequence turnon for the system power, measuring 12-V input from PoC and the 3.3-V supply to the system.

図 8. Measuring System Power Supply

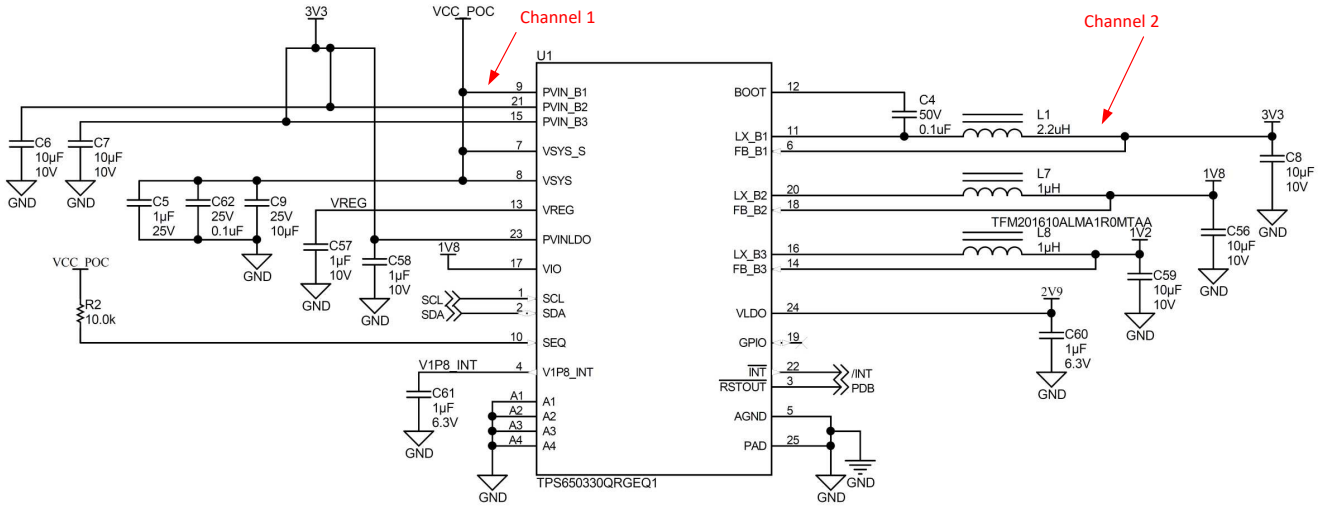
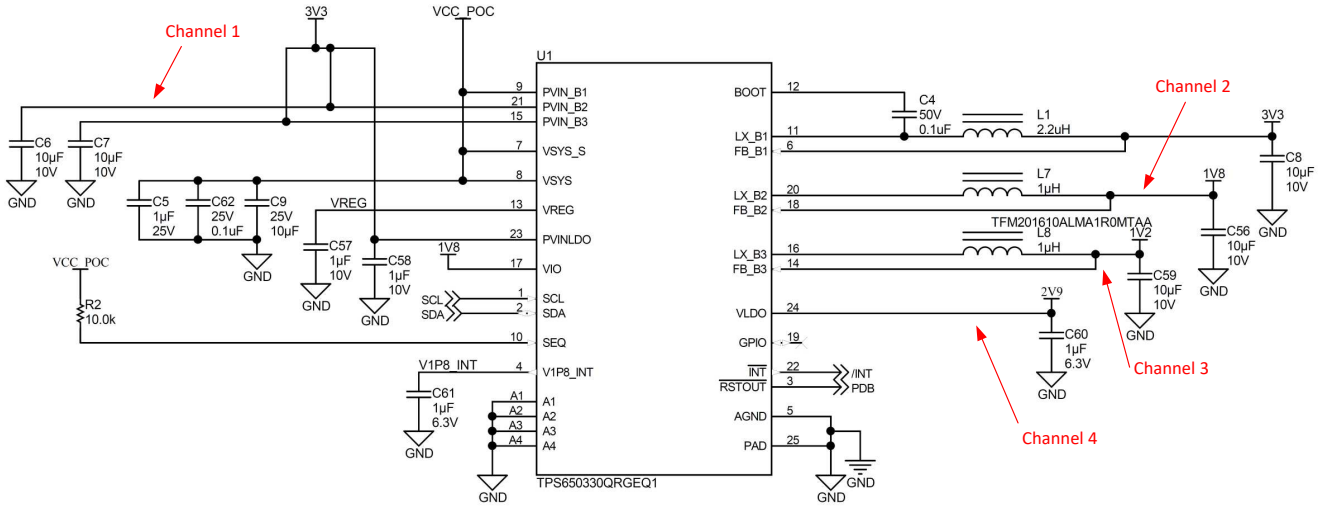


図 9 shows the probe setup to measure the power sequence turnon for the point-of-load power, measuring the 3.3-V system supply, 2.9-V supply to imager, 1.8 V to the imager and serializer, and 1.2 V to the imager.

図 9. Measuring Point-of-Load Power Supplies



3.2.1.2 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

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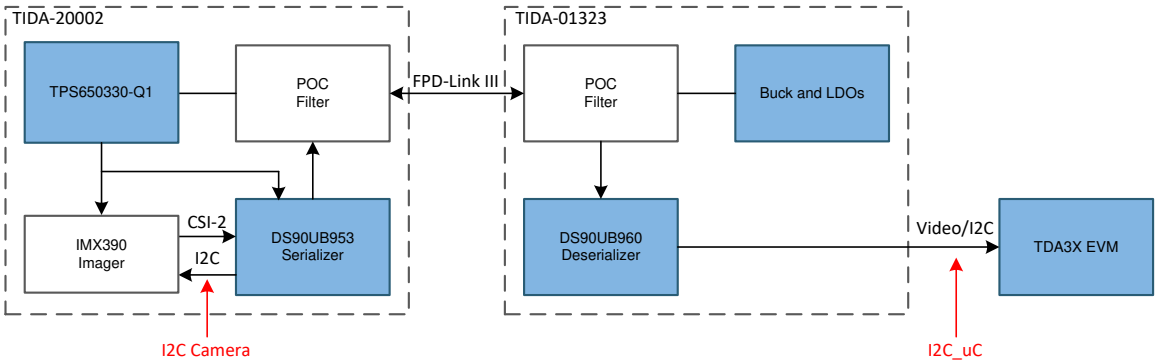
Connections are made to both the clock and data lines of each bus as 図 10 shows.

図 10. Setup for Monitoring I²C Transactions



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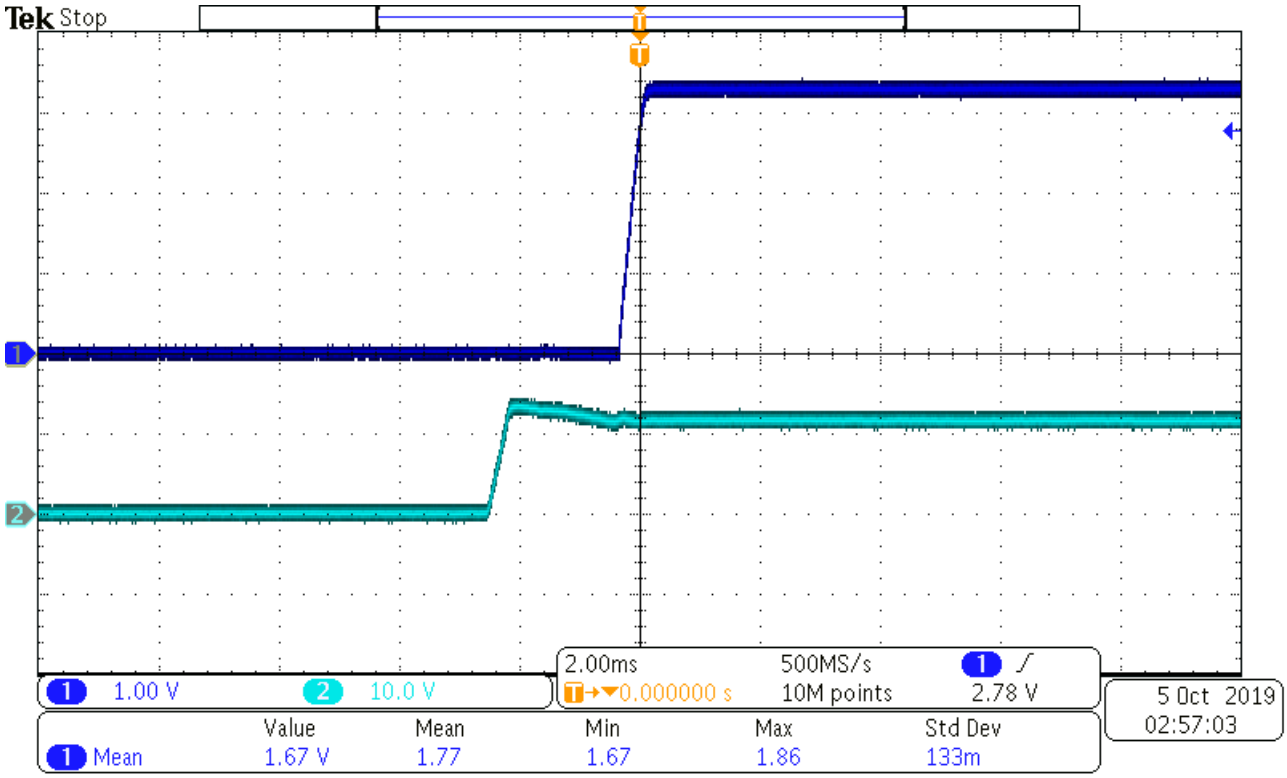
3.2.2 Characterization Test Data

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Start Up

図 11 shows power start-up behavior for the input power supply, and a 3.3-V system supply. The start-up sequence displays the ramping of 3.3 V after the 12-V rail is established.

図 11. System Power Supply Start Up



The same behavior is exhibited for the 2.9-, 1.8-, and 1.2-V supplies, which ramp in sequence after the 3.3-V rail is established on the TPS650330-Q1 device. 図 12 displays the POL supply sequence.

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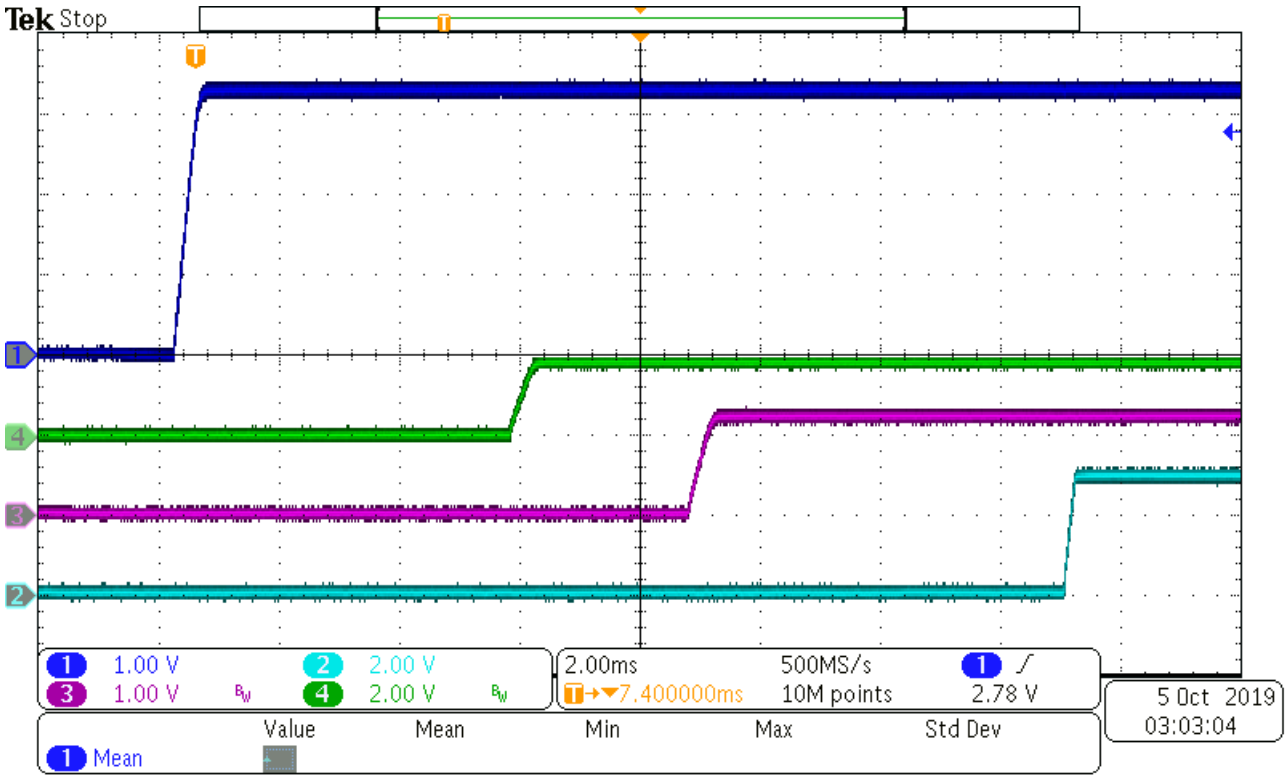
図 12. Point-of-Load Power Supply Start Up



注: (Channel 1): 3.3-V supply; (Channel 2): 2.9-V supply; (Channel 3): 1.2-V supply; (Channel 4): 1.8-V supply

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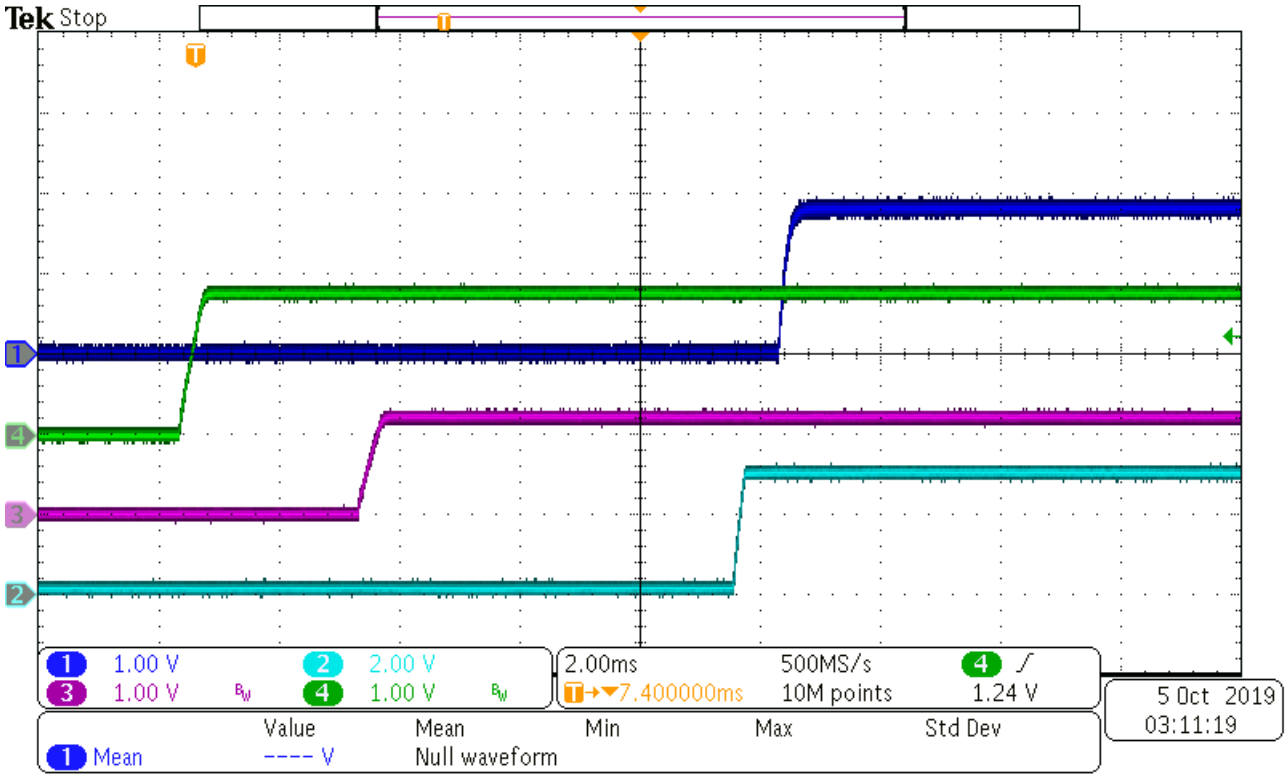
3.2.2.2 Power Supply Start Up—1.8-V Rail and PDB

To properly initialize the PDB pin of the serializer remains low until all power supplies stabilize to their final voltages. 図 13 shows the power supply start up. Note that the PDB pin is directly connected to $\overline{\text{RSTOUT}}$ the of TPS650330-Q1 device and allows proper PDB synchronization after all rails are established.

図 13. Serializer Power-Up Sequence



注: (Channel 1): PDB; (Channel 2): 2.9-V supply; (Channel 3): 1.2-V supply; (Channel 4): 1.8-V supply

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3.2.2.3 Power Supply Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the IMX390 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. Measurements for 3.3-V, 2.9-V, 1.8-V, and 1.2-V rails are shown in 図 14, 図 15, and 図 16, respectively. The rails that impact imager performance are the 2.9-V and 1.2-V rails as they are responsible for providing a clean analog rail and digital supply. The 3.3-V rail powers the entire system and also has excellent ripple performance of 0.3%. As measured, the 2.9-V and 1.2-V rails have a ripple performance of 0.5% and 0.6%, respectively. The 1.8-V rail is significant to the serializer, as it supplies the VDD and VDD_PLL rails. The 1.8-V rail has great voltage ripple performance at 0.8%. The voltage ripple on all rails is low enough for video output to be successfully transmitted.

図 14. Output Voltage Ripple - 3.3 V

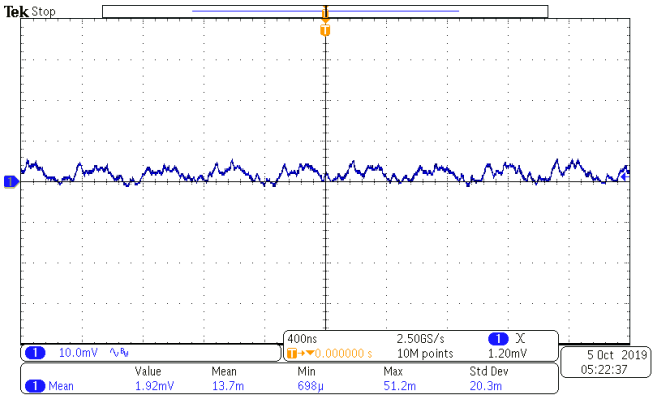


図 15. Output Voltage Ripple - 2.9 V

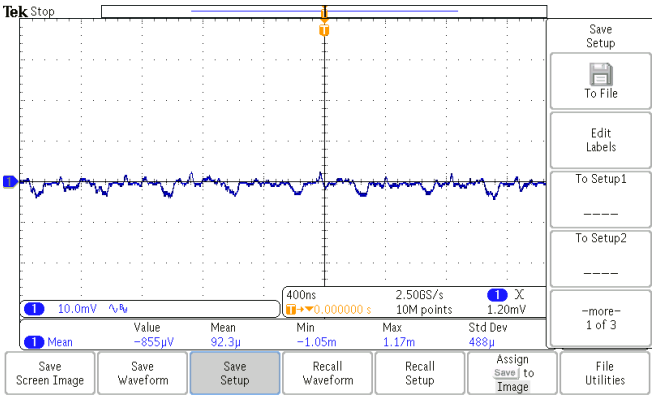


図 16. Output Voltage Ripple - 1.8 V

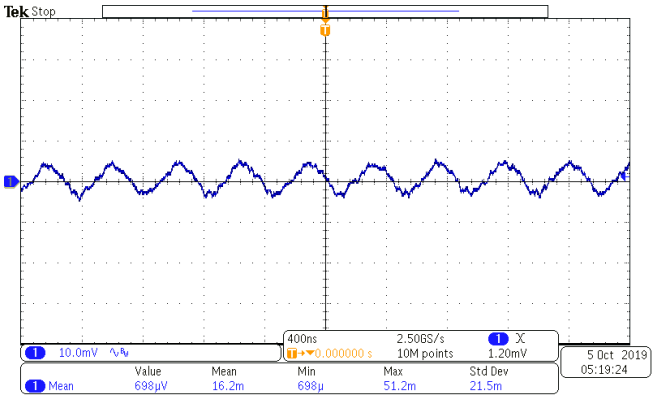
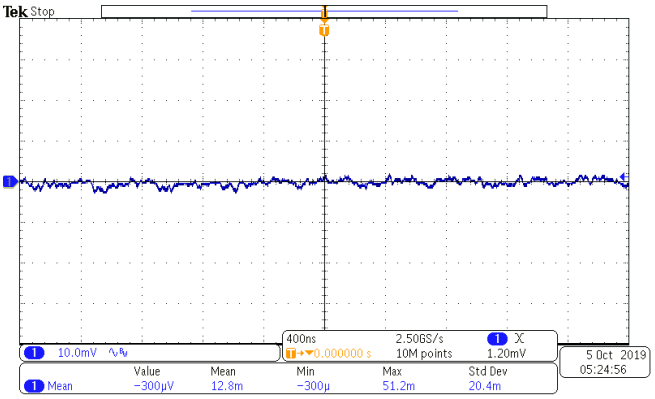


図 17. Output Voltage Ripple - 1.2 V



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3.2.2.4 Power Supply Load Currents

The last measurements to take in regard to the power supplies on the camera module are the load currents for the system supply, and the load currents on the IMX390 imager. These measurements verify total power consumption of the camera module as well as the load current for each individual rail on the IMX390 imager. For the following test data, each rail is drawing the specific load current outlined for the serializer and imager. All load current measurements are taken while a video output stream is present.

表 3 displays the currents measured through each supply voltage in this reference design. The 12-V load current is the total input load for the camera module and measures at 79 mA. With this amount of current, the total input power consumption of the camera module is 948 mW. The 3.3-V system voltage from BUCK1 is measured to be drawing 254 mA.

表 3. Measured Supply Currents

VOLTAGE RAIL	MEASURED CURRENT
3.3 V	254 mA
1.2 V	241 mA
1.8 V	129 mA
2.9 V	57 mA
12 V	79mA

These values give both the input and output currents and voltages for the TPS650330-Q1 device, providing an estimate of the efficiency for this switching supply. The input power already mentioned is 948 mW from the 12-V power over coax. For the output power, using measured voltages of 3.29 V on the board and 254 mA, the total output power is calculated as 836 mW. To calculate system efficiency, the output power is divided by the input power to get 88%. With the larger step-down from 12 V to 3.3 V and a fairly low load current, 88% efficiency is reasonable.

As mentioned previously, BUCK2 and BUCK3 provide the design with the 1.8-V and 1.2-V supplies, and these rails source 129 mA and 241 mA, respectively. Using the previously-specified principal, the combined efficiency for BUCK2 and BUCK3 is 80%. The low-noise LDO sinks an additional 57 mA from the 3.3-V supply to provide a 2.9-V (VDDH) supply to the IMX390.

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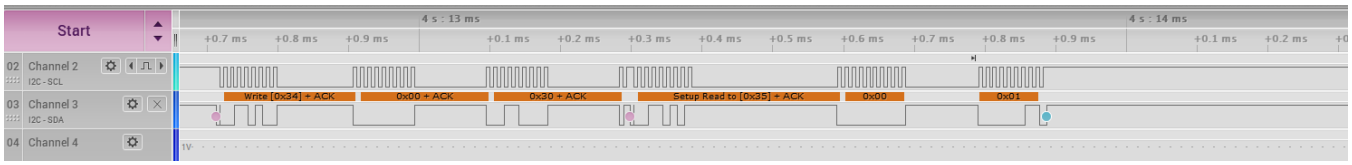
3.2.2.5 I²C Communications

Now that the power supplies are up and running, the I²C communication between the processor and the IMX390 imager over the FPD-Link III backchannel can be confirmed. 図 18 shows a read I²C communication from the TDA3x EVM to the IMX390 imager on this reference design.

図 18. I²C Transactions



The I²C transactions are measured at the deserializer side between the host microprocessor and the DS90UB960-Q1 device. The read is to the imager, which is at slave alias address 0x1A (7-bit) or 0x34 (8-bit). The read to the imager is for its register 0x0030 with data 0x0100, which is a default value for the imagers *White Balance Gain Register*.

The image illustrates successful communication over the FPD-Link III backchannel as the imager is able to relay register contents to the deserializer. By acknowledging the I²C read, the imager has confirmed that it is present and at the correct slave address.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020002.

4.2 Bill of Materials

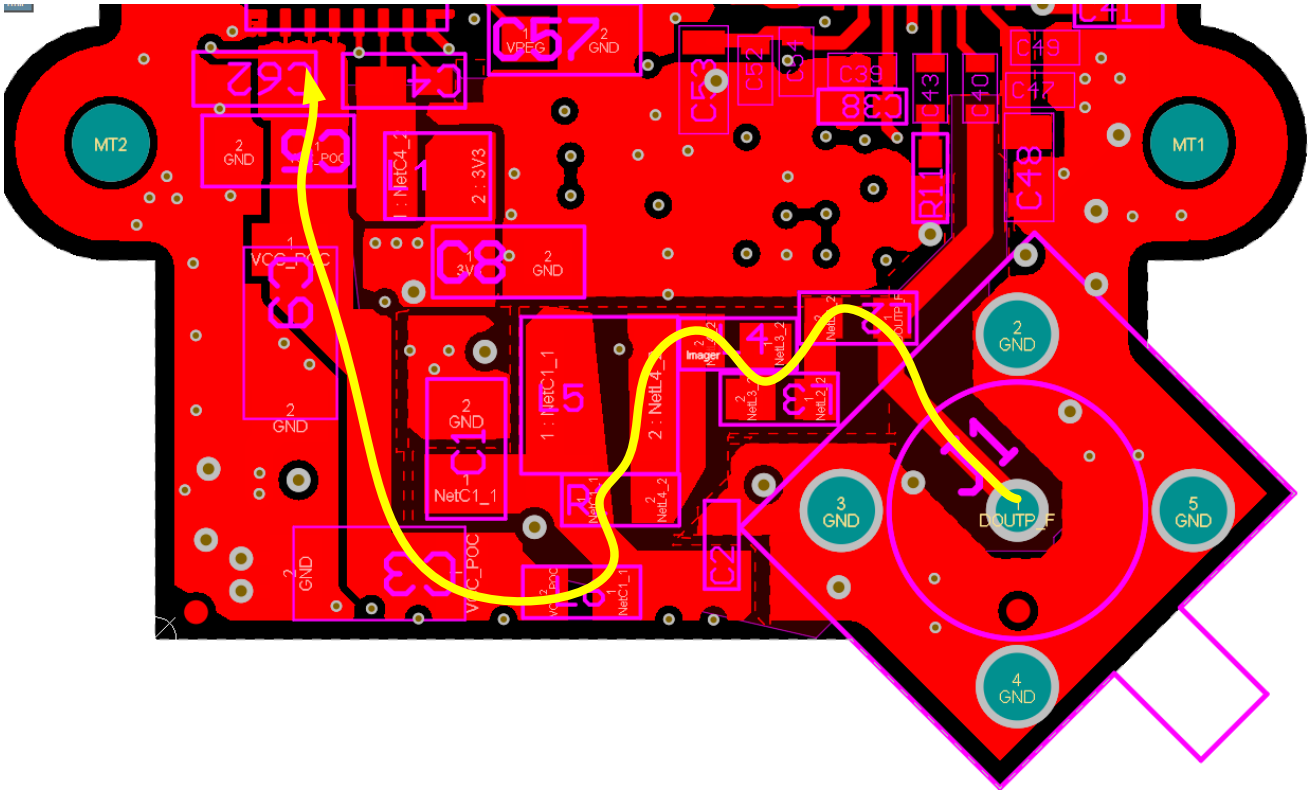
To download the bill of materials (BOM), see the design files at TIDA-020002.

4.3 PCB Layout Recommendations

4.3.1 Switching DC/DC Converters

During part placement and routing, it is helpful to always consider the path the current will be taking through the circuit. The yellow line in 図 19 shows the current path from the coax in through the PoC filter -- L2, L3, L4, L5, R1, C1, C2 -- and then out to the ferrite bead, L6, input capacitor bank of C3,C9,C5,C62 to U1, or the TPS650330-Q1. The path then continues to the 3.3-V output of the switcher to the output inductor L1 and output capacitor C8. Any return currents from the input capacitor bank or the output capacitor C8 are joined together at the adjacent ground plane. It is important to minimize the distance of this connection to reduce the amount of return currents, which would then reduce the voltage gradients that may develop from the resistance of the path. Additionally, a shorter ground connection path will help reduce the chance of coupled noise from the net.

図 19. Routing FB Traces Around SW Nodes



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4.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs:

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers are used in this board to simplify BGA fan out and routing. 図 20 shows the stackup used in this board:

図 20. Layer Stackup

	Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
	Top Overlay	Overlay				
	Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
1	Layer 1 - Top Layer	Signal	Copper	1.4		
	Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
2	Layer 2 - GND	Signal	Copper	1.4		
	Dielectric 2	Dielectric	Core	8	370HR	4.2
3	Layer 3 - PWR	Signal	Copper	1.4		
	Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
4	Layer 4 - Signal	Signal	Copper	1.4		
	Dielectric 4	Dielectric	Core	8	370HR	4.2
5	Layer 5 - Signal/...	Signal	Copper	1.4		
	Dielectric 3	Dielectric	Prepreg	12.6	370HR	4.2
6	Layer 6 - Bottom...	Signal	Copper	1.4		
	Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
	Bottom Overlay	Overlay				

4.3.3 Serializer Layout Recommendations

High-speed CSI-2 routing is an important design aspect for the DS90UB953 on this reference design. Layout considerations for trace impedance and length matching must be a high priority for good signal quality of the high-speed video data. For location of the CSI-2 traces, crosstalk can easily happen with high-speed signals, so it is important on this camera module design that the traces are away from the FPD-Link III RX traces to reduce coupling.

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Trace impedance is one critical aspect to the CSI-2 lane routing. Route the differential pairs for CLK and DATA with a controlled 100-Ω differential impedance (±20%). For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specs, length specifications also need to be strict within the positive-to-negative differential pair length and pair-to-pair length. If the length is not matched, at these high data switching speeds, the data can arrive at the 953 at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. The vias must ideally be two or fewer to minimize stubs that cause reflections. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees. When these layout considerations are followed, the video data integrity can be maintained. If for any reason there are high-speed concerns on the CSI-2 lane design, debug tools are available to run video data over the 1, 2, or 4 lanes. The imager must be set to output over the specified number of data lanes, and the DS90UB953 can then be set to correct number of lanes in register 0x02.

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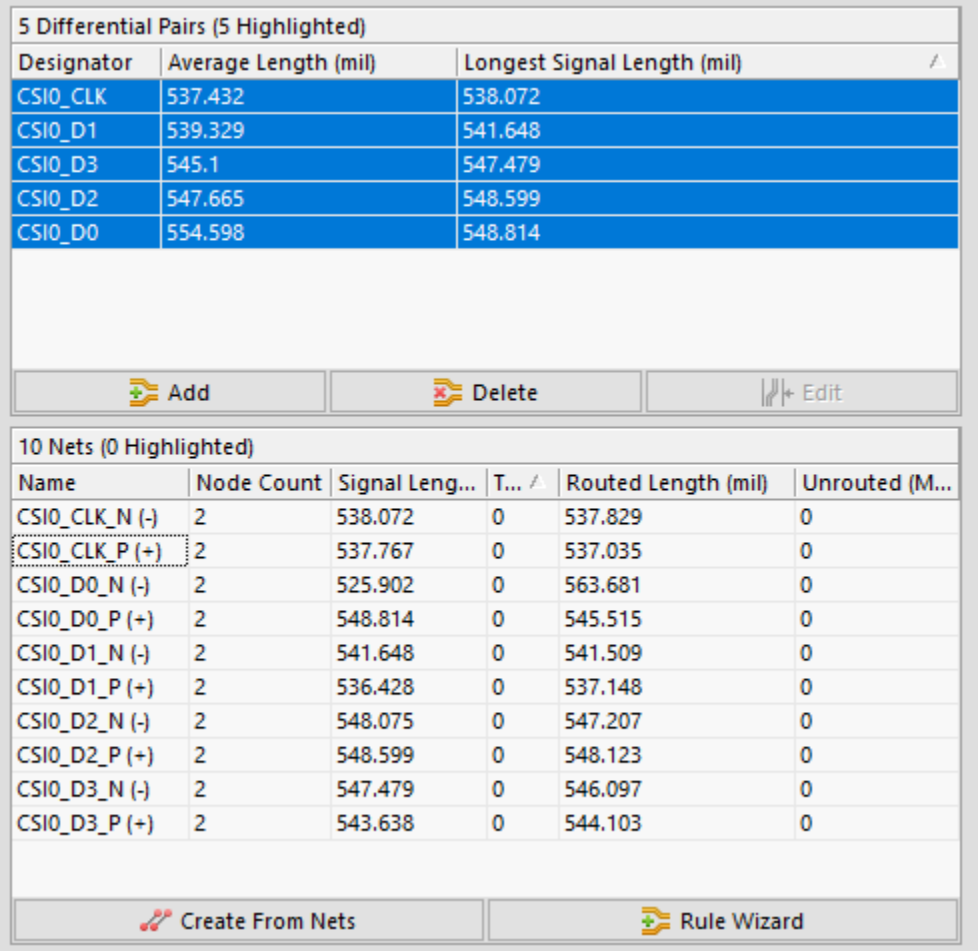
図 21. CSI-2 Differential Trace Routing



Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

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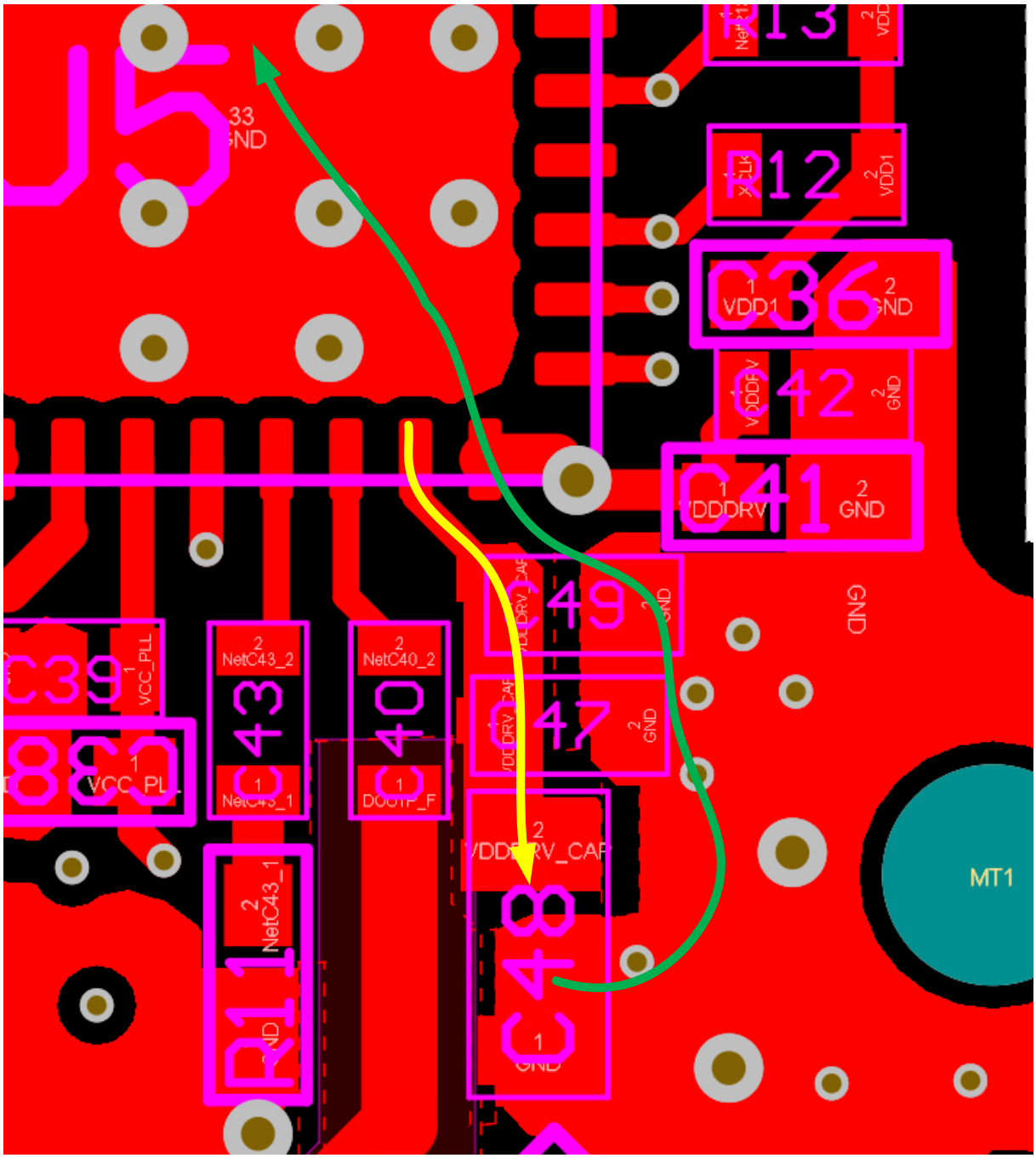
図 22 shows the supply current from C48 in yellow. The green line is the return path. The cross sectional area of this loop is very small.

図 22. Decoupling Current Loop



For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. 図 23 shows the routing of the high-speed serial line, highlighted by the yellow line. The total length of the yellow line is about ½ inch.

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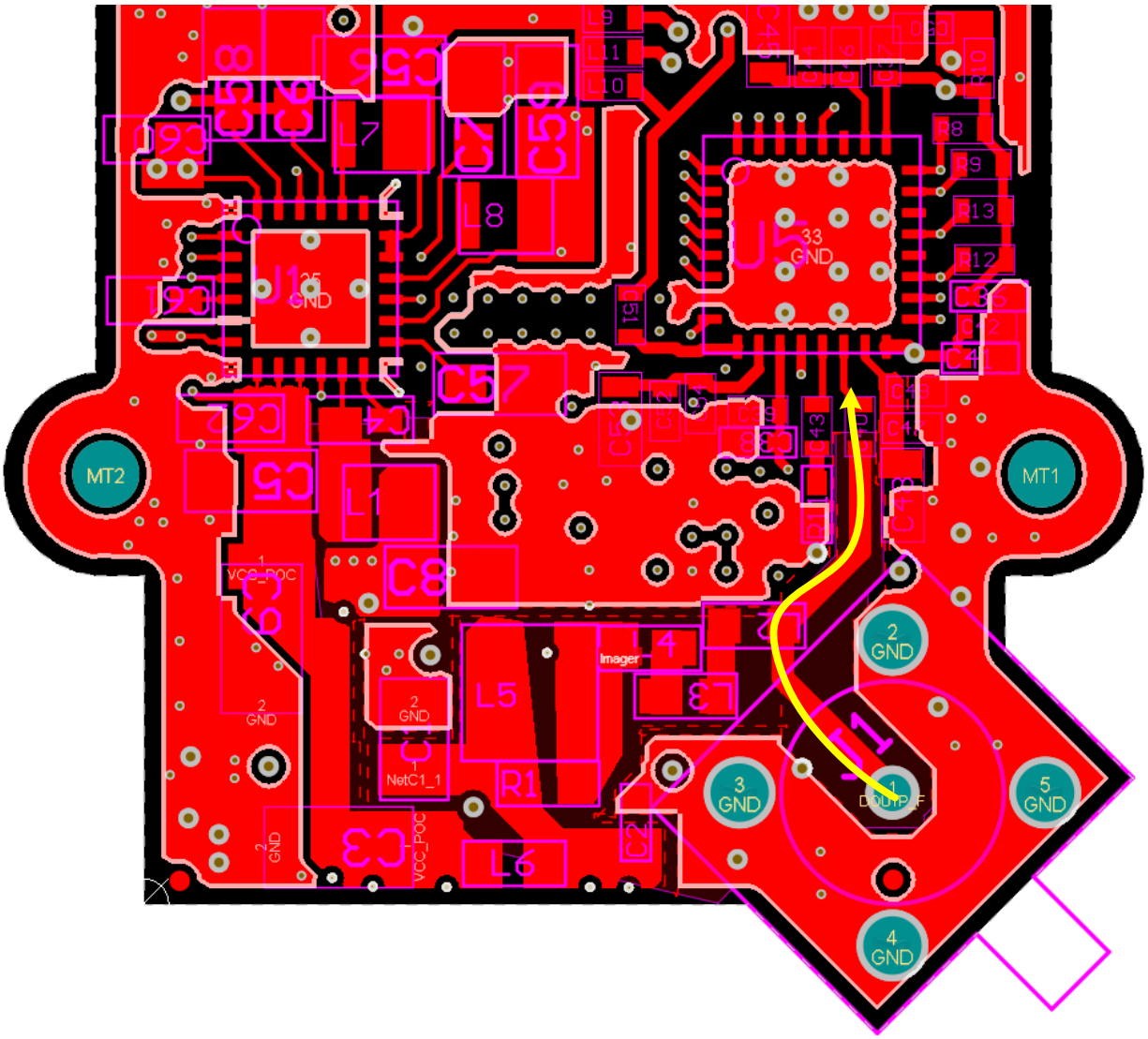
図 23. High-Speed Serial Trace



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4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-020003.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-020003.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020003.

5 Related Documentation

1. Texas Instruments, *DS90UB953-Q1 MIPI CSI-2 FPD-Link III serializer for 2-MP/60-fps cameras and RADAR data sheet*
2. Texas Instruments, *Sending power over coax in DS90UB913A designs application report*
3. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 output filter application report*

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