参考資料

デザイン・ガイド：TIDA-050036
DMS や他のカメラ・モジュール向け車載 2MP カメラ・モジュールのリファレンス・デザイン

概要

このリファレンス・デザインは、自動車ドライバー監視システム (DMS) などのビジョン・アプリケーションに適した、小型で拡張性の高いカメラ・モジュールを提供します。1 個の 2 メガピクセル (2MP) のイメージャに、1 個の 4Gbps シリアライザと 1 個の 4 チャネル・パワー・マネージメント IC (PMIC) を組み合わせています。このカメラ・モジュールは、2 枚の基板を使用する設計で、アプリケーションに応じてさまざまなイメージ・センサで電源とシリアライザの各コンポーネントのフレキシビリティとスケーラビリティを実現する方法を示します。4Gbps シリアライザは、FPD-Link III SerDes テクノロジーを採用しており、非圧縮ビデオ・データをリモートのディスプレイまたはマシン・ビジョン処理システムに送信できます。1 本のケーブルを使用して、双方向の制御信号と POC (power-over-coaxial、同軸ケーブル経由の電力伝送) をカメラ・モジュールに伝送することも可能です。カメラ PMIC は、3 個の降圧コンバータと、プログラマブル出力電圧やシーケンシングに対応した 1 個の LDO レギュレータを統合しており、フレキシビリティと放熱性能を重視して最適化された小型設計を実現できます。スーパーバイザを各レールに搭載しているので、部品点数を削減し、フォーム・ファクタ全体を小型化できます。

リソース

TIDA-050036	デザイン・フォルダ
DS90UB953-Q1	プロダクト・フォルダ
TPS650330-Q1	プロダクト・フォルダ

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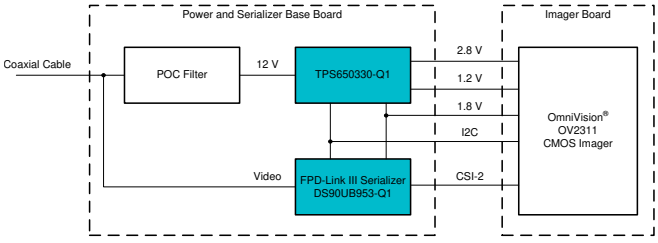
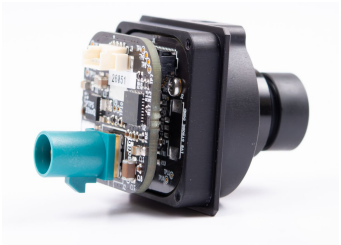
特長

- 電源とシリアライザの PCB (プリント基板) は、各種イメージ・センサとの互換性を確保できる 20mm × 20mm のサイズ
- 高効率で低ノイズの電源
- 4Gbps の DS90UB953 を採用した高解像度のカメラ・アプリケーション
- OmniVision™の 2.1MP OV02311 イメージャによりフル HD、AD 10 ビット、MIPI 2 レーン、RAW10 を実現
- デジタル・ビデオ、電力供給、制御、診断向けに Rosenberger 製 FAKRA 同軸コネクタを 1 個実装
- 追加診断機能により ASIL に対応

アプリケーション

- 処理なしのカメラ・モジュール
- ドライバー監視



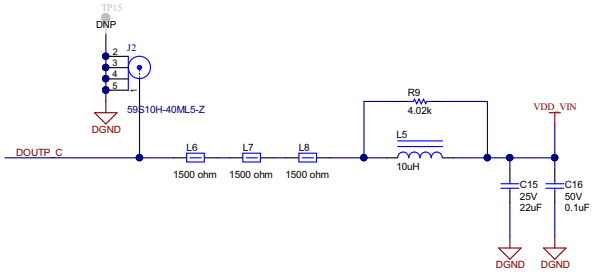


1 System Description

Many automotive applications require small form factors that enable compact, modular, and remote systems. The growing demand for automotive vision systems also requires the flexibility of system components to meet the requirements of various image sensors to reduce the camera module design cycle and time-to-market. This reference design address both these needs by including a 2-megapixel imager, 4-Gbps serializer, and four-channel PMIC within two 20-mm x 20-mm circuit boards. The only connection required by the system is a single 50-Ω coaxial (coax) cable.

A combined signal with DC power, the FPD-Link front and backchannels enter the board through the FAKRA coax connector. The POC filter in 図 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

図 1. POC Filter Schematic



The DC portion is connected to the input of the TPS650330-Q1 PMIC. A dedicated mid-voltage buck regulator converts this to an intermediate 3.5 V. The two low-voltage buck regulators provide a dedicated 1.2 V for the imager and a dedicated 1.8 V shared by both the imager and serializer. An integrated high-PSRR, low-noise LDO provides a clean 2.8 V analog supply for the imager. The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and control backchannel take between the serializer and deserializer.

The output of the imager is connected through a two-lane MIPI CSI-2 interface to the serializer. The serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

Additionally, on the same coax cable, there is a separate low-latency, bidirectional control channel that provides the additional function of transmitting control information from an I2C port. This control channel is independent of the video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

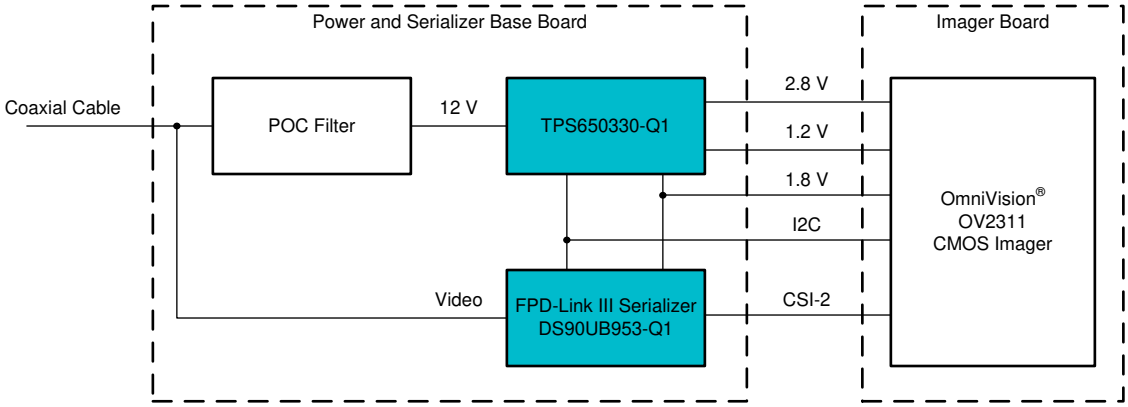
表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	4	12	18.3	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V	-	0.6	1	W

2 System Overview

2.1 Block Diagram

図 2. TIDA-050036 Block Diagram



2.2 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.2.1 PCB and Form Factor

The goal of this design is to combine the flexibility of a two-board solution within a compact area of 20 mm x 20 mm. The lens mounting on the imager board and FAKRA connector on the power and serializer board all fit within this area. 図 3 and 図 4 show the base board 3-D PCB views and 図 5 and 図 6 show the imager board 3-D PCB views.

図 3. 3-D PCB Base Board (Top)

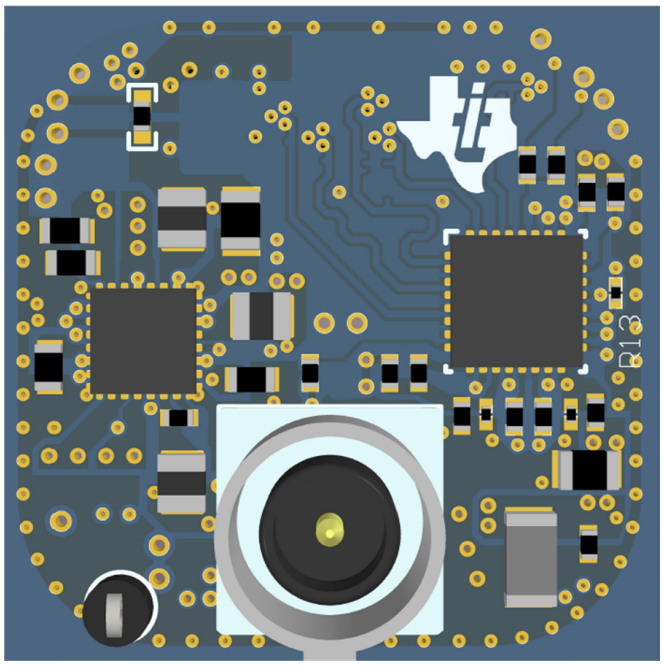


図 4. 3-D PCB Base Board (Bottom)

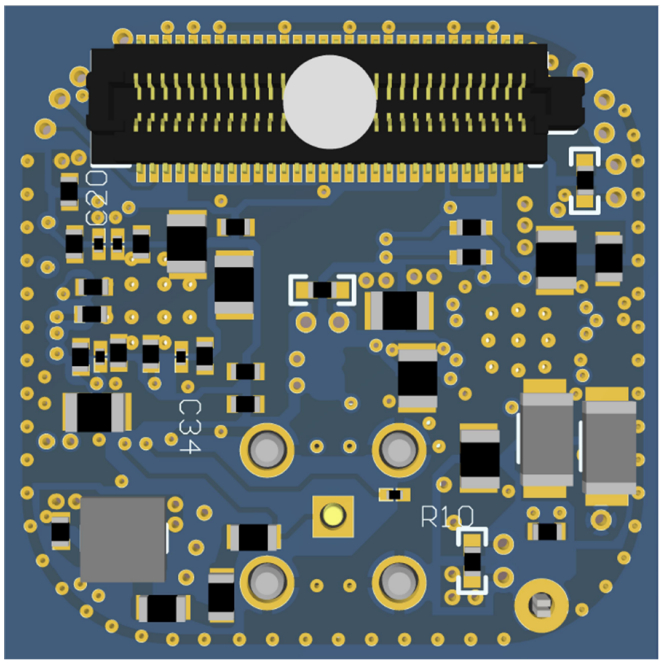


図 5. 3-D PCB Imager Board (Top)

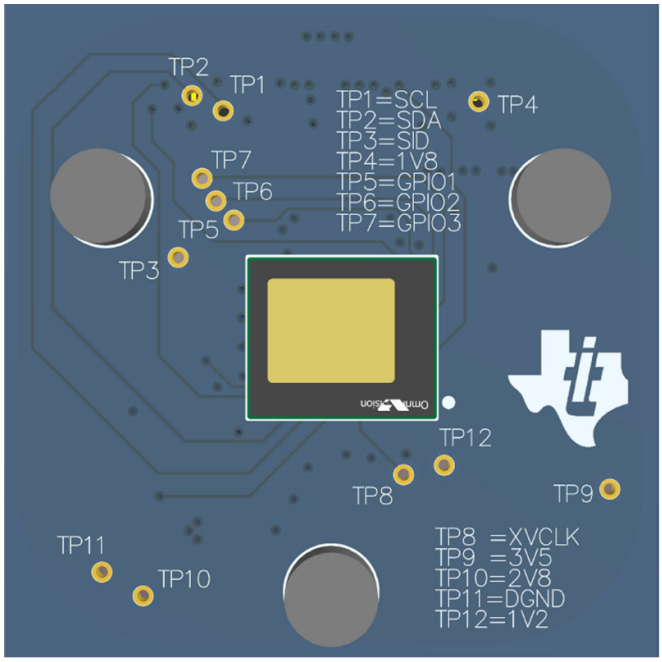


図 6. 3-D PCB Imager Board (Bottom)

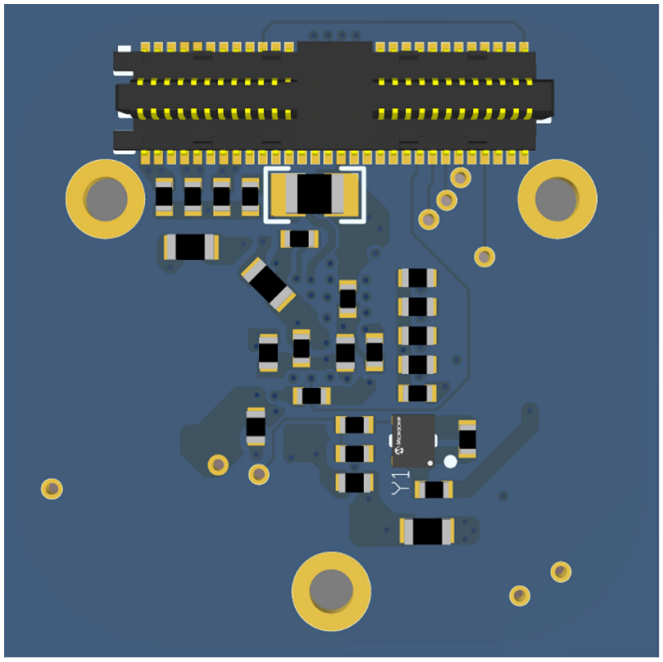


図 7 and 図 8 show 3-D PCB views of the assembled boards.

図 7. 3-D PCB Assembled Boards (Side View)

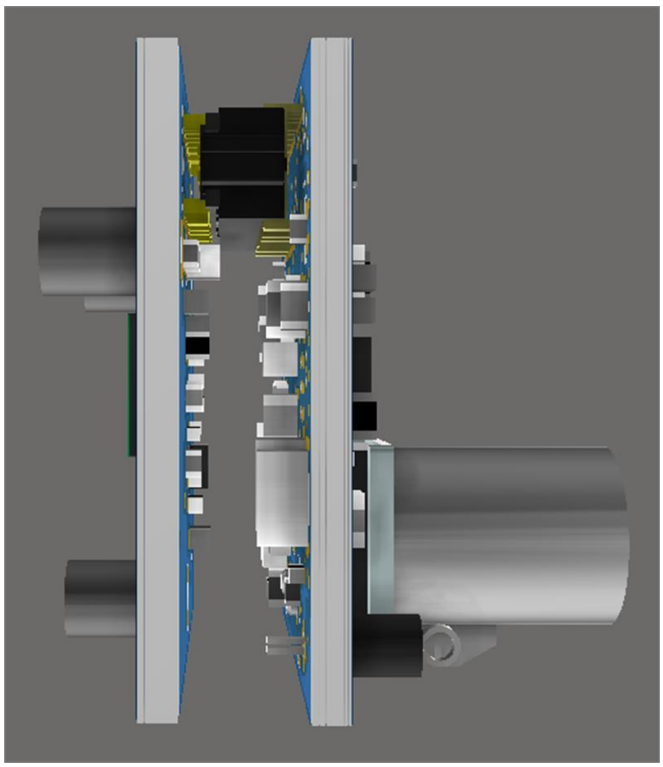
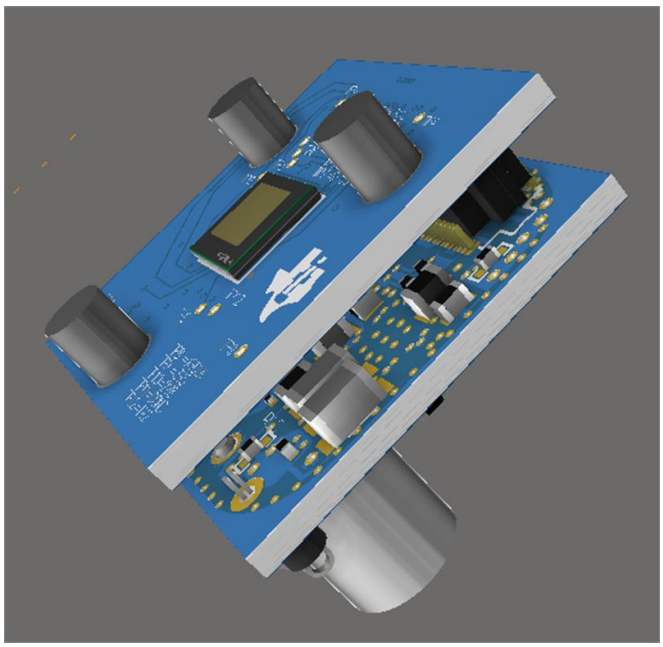


図 8. 3-D PCB Assembled Boards (Angled View)



2.2.2 Power Supply Design

2.2.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

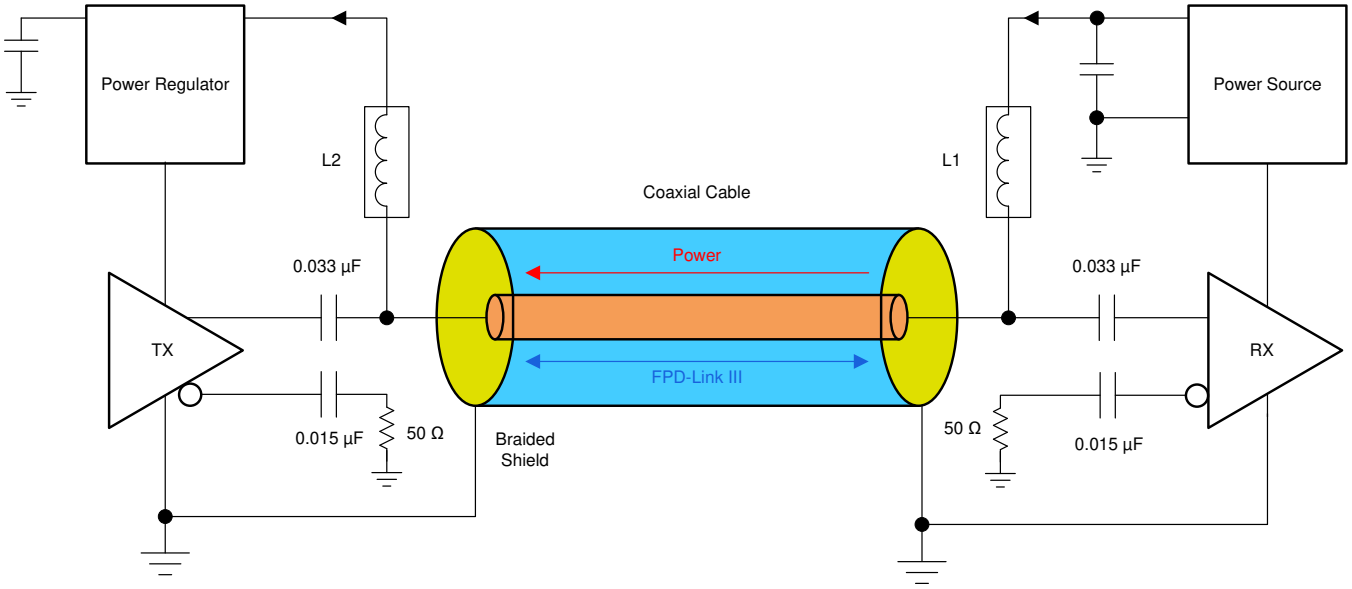
1. Deliver a clean DC supply to the input of the switching regulators
2. Protect the FPD-Link communication channels from noise-coupled backwards from the rest of the system

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. For the POC design, to enable the forward channel and backchannel to pass uninterrupted over the coax, an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 10-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2.2-GHz frequency band. This complete filter is shown by L2 in 図 9. L1 is the same inductor for the POC filter on the deserializer side. In this camera design, it is imperative that this filter has the smallest footprint allowable. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward-channel filtering, inductors usually are not sufficient to filter above 1 GHz. This reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore, three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized onboard for the POC inductor filtering. For more details, see the *Sending Power Over Coax in DS90UB913A Designs* application report.

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors of 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through, but the DC is blocked from getting on the data lines.

図 9. Power Over Coax



2.2.2.2 Power Supply Considerations

This reference design targets automotive applications, so there are several requirements that shape the design choices:

- The board area needs to be minimized to 20 mm × 20 mm. A fully-integrated PMIC power solution minimizes the external component count, making this requirement easier to achieve.
- Switching frequencies must be lower than 540 kHz or higher than 1700 kHz to avoid interfering with the AM radio band. Choosing a higher switching frequency prevents harmonics encroaching in the AM band, and allows for smaller external components to aid the board area requirements.
- All devices must be AEC Q100-Q1 rated.

The system input voltage is a pre-regulated 12-V supply over coax. As the PMIC integrates supervisors and monitoring, the only system components requiring power are the imager, serializer, and oscillator. 表 2 shows the typical power consumption of these devices:

表 2. System Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (mA)	POWER (mW)
Imager			
	2.8	32	90
	1.8	1	2
	1.2	80	96
Serializer			
	1.8	160	290
Oscillator			
	1.8	3	7
Total			
	2.8	32	90
	1.8	164	299
	1.2	80	96

2.2.2.2.1 Choosing External Components

For simplicity, the efficiency of the buck regulators is assumed to be 80% for the operating conditions listed in 表 2, while the efficiency of the LDO is given by 式 1:

$$\eta_{LDO} = \frac{V_{OUT}}{V_{IN}} = \frac{2.8}{3.5} = 0.8 \quad (1)$$

式 2, which calculates the input power of a converter as a function of the output power and efficiency, is used to calculate the system and Buck 1 output currents.

$$P_{IN} = V_{IN} \times I_{IN} = \frac{P_{OUT}}{\eta} \quad (2)$$

$$I_{OUT,\ Buck1} = \frac{\frac{P_{OUT,\ Buck2}}{\eta_{Buck2}} + \frac{P_{OUT,\ Buck3}}{\eta_{Buck3}} + \frac{P_{OUT,\ LDO}}{\eta_{LDO}}}{V_{OUT,\ Buck1}} = 140 \ \ mA \quad (3)$$

表 3 shows the load capability of each regulator compared to the requirements of the camera module. The TPS650330-Q1 device is capable of supplying the system power with plenty of margin to account for variations between typical and maximum current variation.

表 3. TPS650330-Q1 Capabilities vs. System Requirements

REGULATOR	OUTPUT VOLTAGE (V)	MAXIMUM CURRENT (mA)	REQUIRED CURRENT (mA)
Buck 1	3.5	1500	140
Buck 2	1.8	1200	164
Buck 3	1.2	1200	80
LDO	2.8	300	32

After determining that the TPS650330-Q1 device is suitable based on the power requirements, the external components can be chosen quickly based on the data sheet recommendations, simplifying the design process. These recommendations are shown in 図 10 and 表 4.

図 10. Typical Application

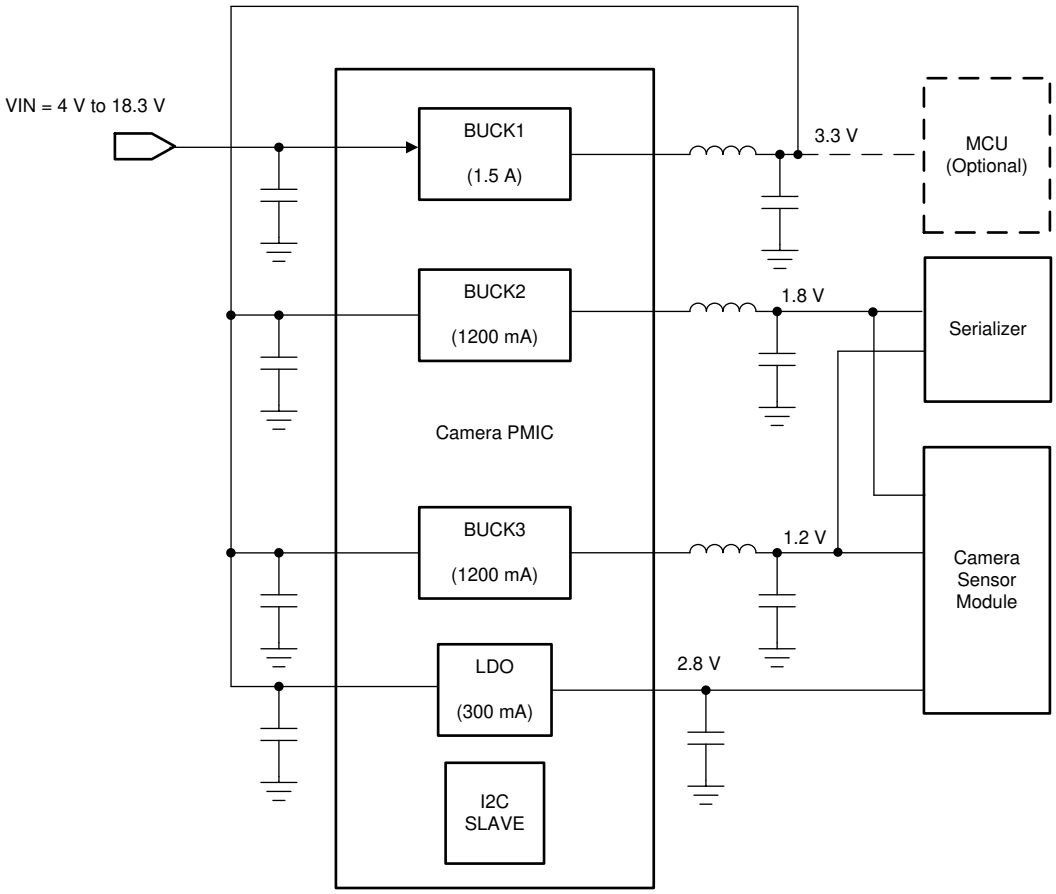


表 4. TPS650330-Q1 Recommended Components

COMPONENT	DESCRIPTION	VALUE	UNIT
$C_{VSYS,VSYS\_S}$	VSYS and VSYS_S decoupling	10	µF
C_{PVIN_B1}	Buck 1 input capacitor	10	µF
L_{SW_B1}	Buck 1 inductor	1.5	µH
C_{OUT_B1}	Buck 1 output capacitor	10	µF
C_{PVIN_B2}	Buck 2 input capacitor	10	µF
L_{SW_B2}	Buck 2 inductor	1.0	µH
C_{OUT_B2}	Buck 2 output capacitor	10	µF
C_{PVIN_B3}	Buck 3 input capacitor	10	µF
L_{SW_B3}	Buck 3 inductor	1.0	µH
C_{OUT_B3}	Buck 3 output capacitor	10	µF
C_{PVIN_LDO}	LDO input capacitor	1.0	µF
C_{OUT_LDO}	LDO output capacitor	2.2	µF

2.2.2.2.2 Choosing the Buck 1 Inductor

Although 1.5 µH was chosen for this design to balance size and performance, a 2.2-µH inductor can also be used to reduce the inductor current ripple. With an inductance value chosen, the minimum inductor saturation current must be derived to choose an appropriate inductor for the design. This is the combination of the steady-state supply current as well as the inductor ripple current. To ensure flexibility of the power and serializer base board to higher power image sensors, the inductor is chosen based on each maximum rated output current of the regulator . 式 4 calculates inductor ripple current:

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{sw}} \right)$$

where

- $\Delta I_{L(max)}$ is the maximum peak-to-peak inductor ripple current
- $L_{(min)}$ is the minimum effective inductor value
- f_{sw} is the actual PWM switching frequency

(4)

The parameters for Buck 1 of this reference design are:

- V_{OUT} = 3.5 V
- $V_{IN(max)}$ = 18.3 V
- $L_{(min)}$ = 1.5 uH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 820 mA. Assuming a maximum load current of 1.5 A, 式 5 can be used to calculate a minimum saturation current of 1.9 A.

$$L_{SAT} \geq I_{OUT,(MAX)} + \frac{\Delta I_{L(MAX)}}{2}$$

(5)

The TPS650330-Q1 device on this design uses a TDK Corporation® TFM201610ALMA1R5MTAA, which has a rated current of 2.3 A and a DC resistance maximum of 110 mΩ. The large current rating ensures compatibility of the power and serialier base board with higher power imager boards. Additionally, this inductor has an operating temperature of -55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.2.3 Choosing the Buck 2 and Buck 3 Inductors

Buck 2 and Buck 3 have a recommended inductor value of 1.0 µH. When selecting a component, it is important to verify the DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly -- lower DC resistance is directly proportional to efficiency. The saturation requirement of the inductor is determined by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current using 式 4.

The parameters for the Buck 2 1.8-V rail include:

- V_{OUT} = 1.8 V
- $V_{IN(max)}$ = 3.5 V
- $L_{(min)}$ = 1.0 uH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 380 mA. Assuming a maximum load current of 1.2 A, 式 5 can be used to calculate a minimum saturation current of 1.4 A.

The parameters for the Buck 3 1.2-V rail include:

- V_{OUT} = 1.2 V
- $V_{IN(max)}$ = 3.5 V
- $L_{(min)}$ = 1.0 uH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 343 mA. Assuming a maximum load current of 1.2 A, 式 5 can be used to calculate a minimum saturation current of 1.4 A.

Buck 2 and Buck 3 of this design use the TDK Corporation® TFM201610ALMA1R0MTAA, which has a current rating of 3.1 A and a DC resistance of 60 mΩ. The large current rating ensures compatibility of the power and serializer base board with higher power imager boards. Additionally, this inductor has an operating temperature of –55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.2.4 Functional Safety

The TPS650330-Q1 device has integrated supervisors in addition to temperature and current monitoring, allowing utilization in applications requiring functional safety. The interrupt pin or status bit of this PMIC can be used to detect when a fault condition has occurred, at which point a local or remote MCU or processor can query the fault mechanism via I2C, and take the appropriate action. The TPS650330-Q1 is also pin-compatible with the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1. Each of these devices provides additional safety features, allowing the scalability of this design to camera applications with more stringent safety requirements.

2.3 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coax cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS650330-Q1: an automotive qualified, four channel PMIC optimized for camera applications. The device integrates three buck converters and one LDO, along with overvoltage and undervoltage supervisors for each voltage rail. A high, fixed PWM 2.3-MHz switching frequency enables the use of small inductors with a fast transient response. The low-noise, high-PSRR LDO provides an output voltage option for sensitive analog circuits. The output voltage and sequencing settings, along with other operational settings are programmable via I2C for compatibility with a variety of imagers without the need for any additional components.

2.3.1 DS90UB953-Q1

Using a serializer to combine 10-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 device mates well with the MIPI CSI-2 video output of the OV2311 imager. Once combined with the filters for the POC, video, I2C control, diagnostics, and power can all be transmitted on a single inexpensive coax cable. For more information on the cable itself, see the *Cable Requirements for the DS90UB913A and DS90UB914A* application report.

2.3.2 TPS650330-Q1

To minimize form factor, a PMIC is selected to provide the power, supervision, and sequencing requirements for the system. A power topology consisting of three buck regulators and one LDO provides a balance between power efficiency and noise performance. A 2.2-MHz operating frequency is beneficial for two reasons: it avoids the especially sensitive frequencies of image sensor circuits (typically 1 MHz or less) and it avoids interfering in the AM radio band for automotive applications. The low noise, and high PSRR LDO of the PMIC can provide up to 300 mA of current with a tight output voltage tolerance (±1%) appropriate for the analog voltage rail requirements in ADAS camera applications. The PMIC offers programmable output voltages and sequencing, allowing the same power and serializer design to be reused with a variety of imagers depending on the vision application.

2.4 System Design Theory

The main design challenges to consider for automotive cameras are size, ease of use, and thermal efficiency. Automotive cameras are often placed in remote regions of the vehicle where area is limited, requiring an overall compact solution. Because of this, the system is designed around having the lowest number of components with a fully-integrated PMIC power solution. As ADAS applications continue to grow in capability and complexity, the increase in demand for automotive cameras requires that ease of use, or flexibility, becomes another critical factor to reduce system design cycle and time-to-market. The choice of the DS90UB953-Q1 and TPS650330-Q1 devices are important here as they are compatible with a wide range of imagers. The choice of a two-board solution highlights this flexibility, as the power and serializer base board can be re-used with different imager boards depending on the ADAS application. Lastly, the small size and remote placement of these cameras increases their susceptibility to heat. A power efficient system is crucial to preserve the image quality in these conditions. The TPS650330-Q1 device is optimized for efficiency with a three buck and one LDO regulator topology, enabling the support of medium and high quality imagers without sacrificing thermal performance. Due to the impact of thermals on the system performance, it is important to calculate total system efficiency as part of the design process. From the Buck 1 output power in 表 3 and assuming an efficiency of 70%, 式 2 calculates a system input power of about 700 mW. 式 6 can then be used with the output power of Buck 2, Buck 3, and the LDO to calculate the overall system efficiency.

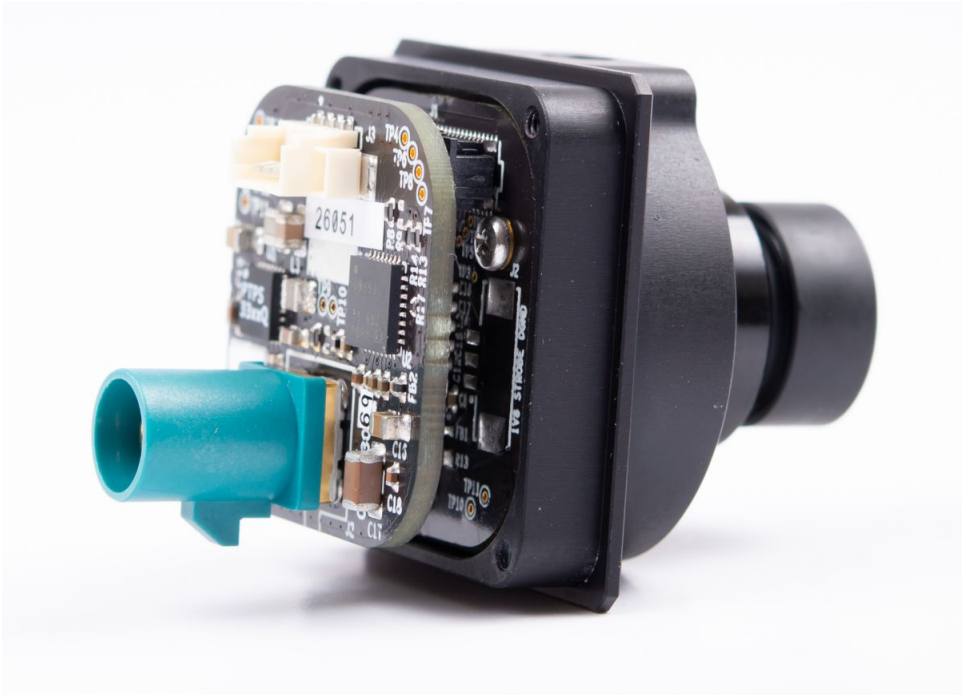
$$\eta_{SYSTEM} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT,\ Buck\ 2} + P_{OUT,\ Buck\ 3} + P_{OUT,\ LDO}}{P_{IN,\ Buck\ 1}} = 69\% \quad (6)$$

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as 図 11 shows. This camera module is compatible with both the Rugged Vision Platform (RVP) and automotive starter kit from D3 Engineering™.

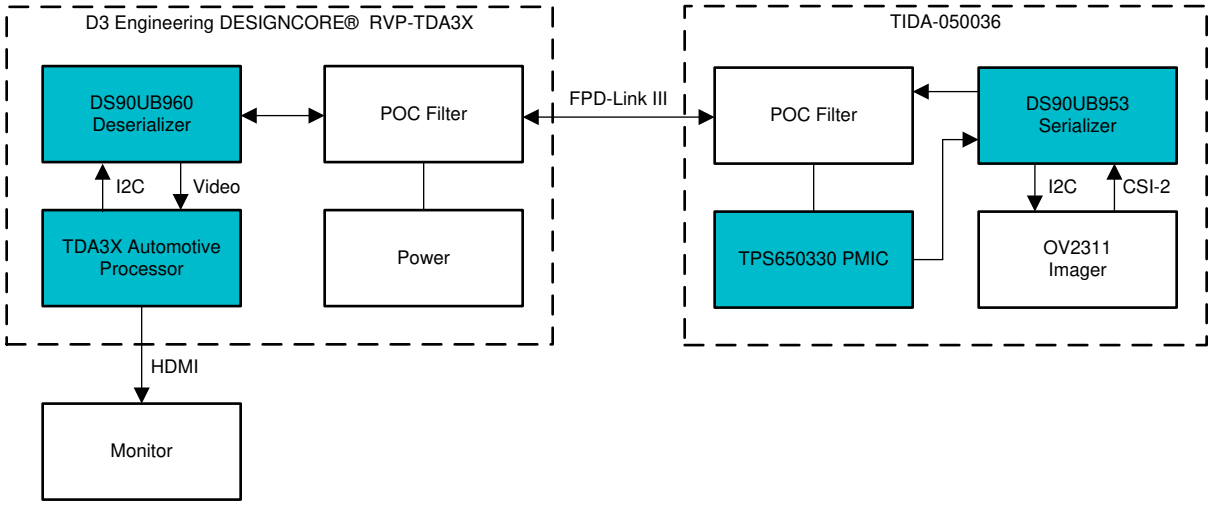
図 11. Board Image



3.1.1 Video Output Hardware Setup

図 12 shows the test setup to stream video output with this reference design. This reference design includes an OV02311 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I2C interfaces. The DS90UB953-Q1 serializer then connects through POC to a DS90UB960-Q1 quad deserializer. Note that for test setup, only one channel is used from the DS90UB960-Q1 device. To enable video output from the DS90UB960-Q1 device, the RVP or starter kit writes all the backchannel I2C setting configurations for the OV2311, DS90UB953-Q1, and DS90UB960-Q1 devices. When these writes are completed, Vision SDK software enables video output to an HDMI-connected monitor.

図 12. Test Setup



3.2 Testing and Results

3.2.1 Test Setup

The setup used to verify power supply functionality is the same as that used to verify video output shown in 図 12.

3.2.1.1 Power Supplies Startup

To verify the power supply sequencing and startup behavior, each voltage rail output from the TPS650330-Q1 device was measured after applying power over coax to the system.

3.2.1.2 Power Supply Startup - 1.8 V Rail and Serializer PDB Setup

The PDB reset signal of the DS90UB953-Q1 device is connected directly to the nRSTOUT pin of the TPS650330-Q1 device . With the integrated sequencing capabilities of the PMIC, this ensures that the PDB reset line goes high after the 1.8-V supply is stable, eliminating the need for an external RC network.

3.2.2 Test Results

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Start Up

図 13 shows the start-up behavior for the 3.5-V, 1.8-V, 1.2-V (DVDD), and 2.8-V (AVDD) rails.

図 13. Point-of-Load Power Supply Start Up

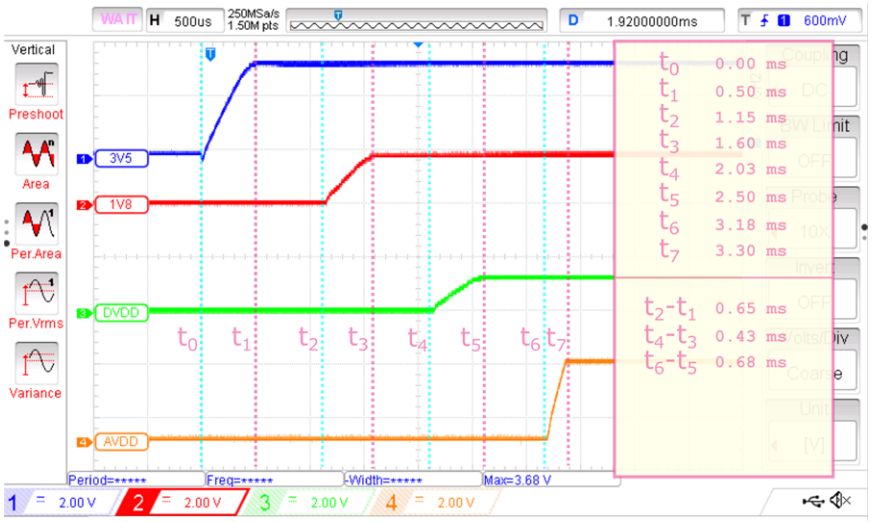
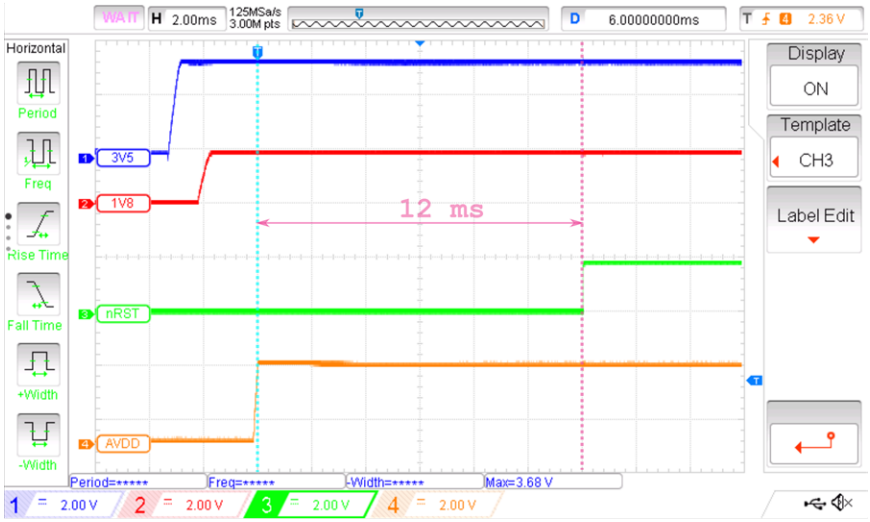


図 14 shows the delay requirement between the 1.8-V rail and PDB reset line (nRST) is met.

図 14. Serializer Power-Up Sequence



3.2.2.2 *Power Supply Output Voltage Ripple*

To achieve a quality output video stream, the output voltage ripple on the OV2311 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. 図 15 to 図 18 show the measurements for 3.5-V, 1.8-V, 1.2-V, and 2.8-V rails while the camera is streaming video. The measured peak-to-peak ripple voltages are 0.3%, 0.4%, 1.0%, and 0.3% respectively. The ±2% voltage accuracy, even with load transients introduced by the operation of the imager and serializer, allow for the video output to be successfully transmitted.

図 15. Output Voltage Ripple: 3.5 V

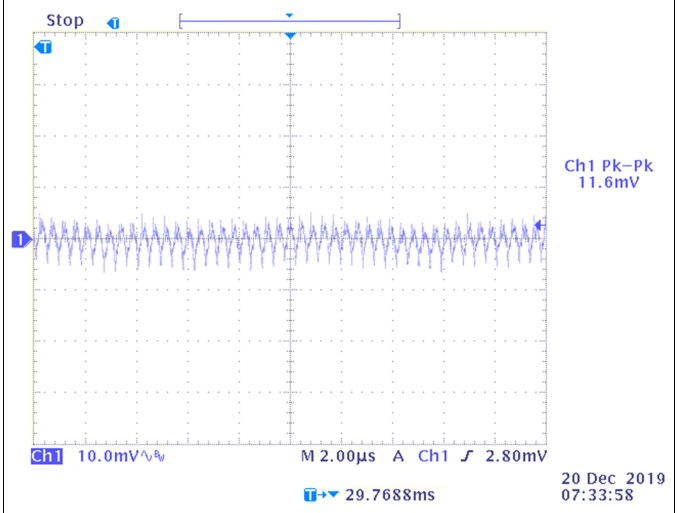


図 16. Output Voltage Ripple: 1.8 V

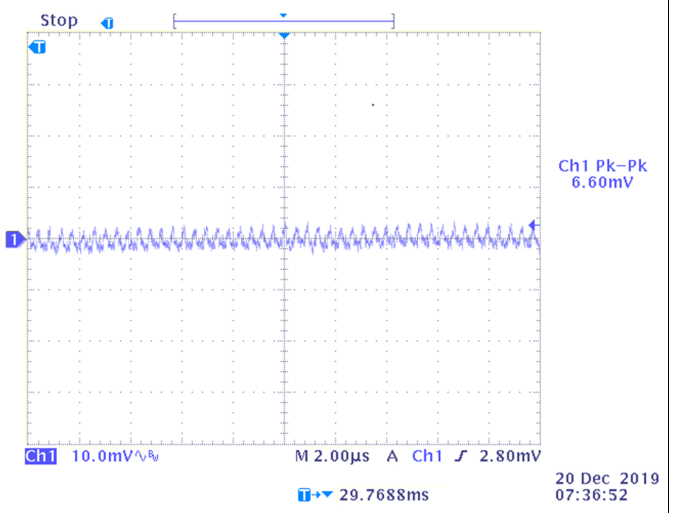


図 17. Output Voltage Ripple: 1.2 V

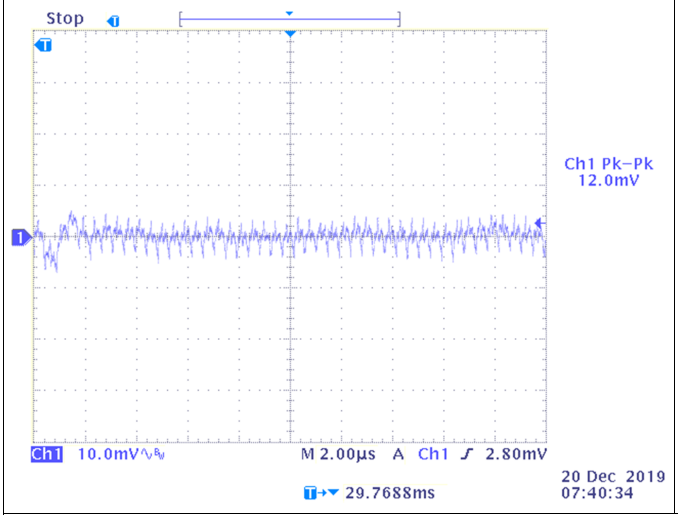
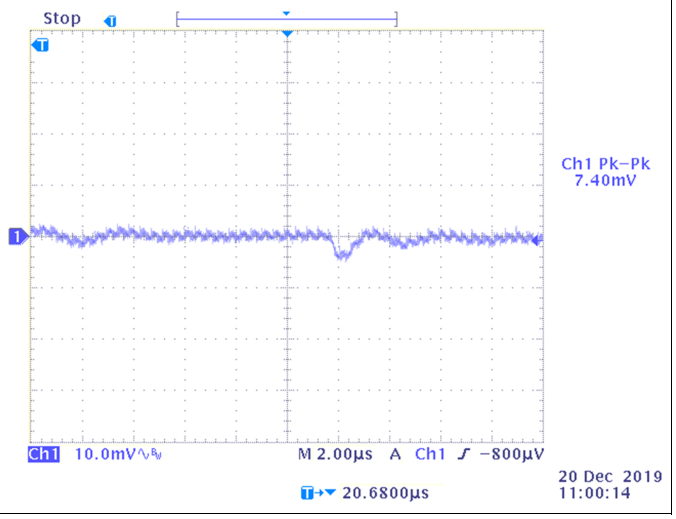


図 18. Output Voltage Ripple: 2.8 V



3.2.2.3 Power Supply Load Currents

表 5 shows the currents measured for each supply voltage in this reference design. The measurements correspond to an overall system efficiency of 67%, close to the 69% derived in 2.4.

表 5. Measured Supply Currents

VOLTAGE RAIL (V)	MEASURED CURRENT (mA)
12	48
3.5	131
2.8	26
1.8	141
1.2	54

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050036.

4.2 Bill of Materials

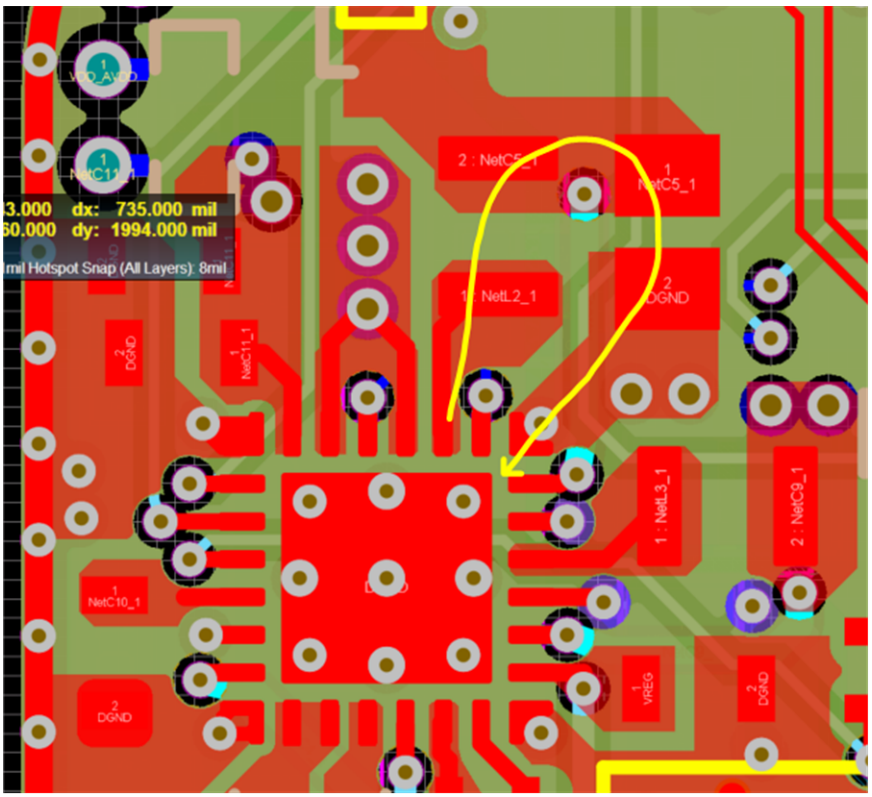
To download the bill of materials (BOM), see the design files at TIDA-050036.

4.3 PCB Layout Recommendations

4.3.1 PMIC Layout Recommendations

The PMIC portion of the layout requires careful consideration to minimize both PCB area and noise. As EMI is a critical concern in automotive systems, the TPS650330-Q1 device includes a spread spectrum feature to reduce conducted and radiated emissions, allowing more flexibility with placement and layout for space-constrained applications. However, it is still recommended to follow as many best practices as possible. This includes minimizing the area traveled by switching currents between buck regulator input capacitor, inductor, and output capacitor with tight component placement and minimal return path to the PMIC thermal pad. 図 19 shows an example of this for Buck 2.

図 19. Buck 2 Layout Considerations



For the LDO, separation of input and output capacitor ground planes will reduce noise coupling from the 3.5-V switching rail to the sensitive 2.8-V analog rail. To further reduce noise coupling, the dedicated AGND pin of the PMIC is connected to the ground plane on an internal layer with a via, rather than directly to the noisier thermal pad on the top layer.

4.3.2 PCB Layer Stackup

図 20 shows the 8-layer stackup used for the PMIC and serializer board. Two signal layers are required due to the complex routing requirements introduced by I2C, GPIO, clock, and control signals between the PMIC, serializer, and header, which provide an interface with the imager. The separation between planes carrying high-speed CSI data lines should be selected to ensure a characteristic differential impedance of 100 Ω ±10%.

図 21 shows the 6-layer stackup for the imager board. This has similarly been designed around the target differential impedance of the CSI-2 traces.

図 20. Eight-Layer Stackup PMIC and Serializer Board

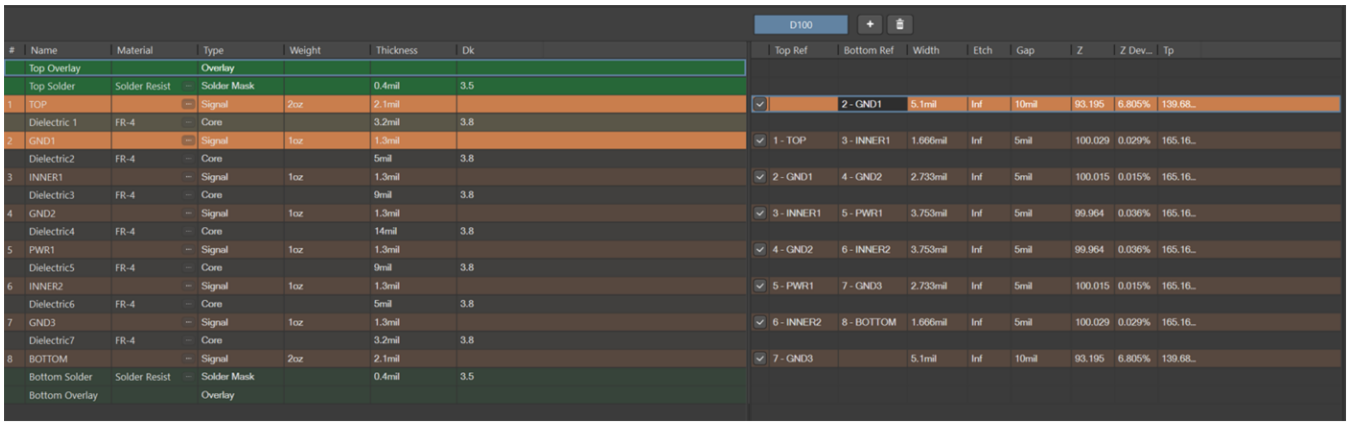
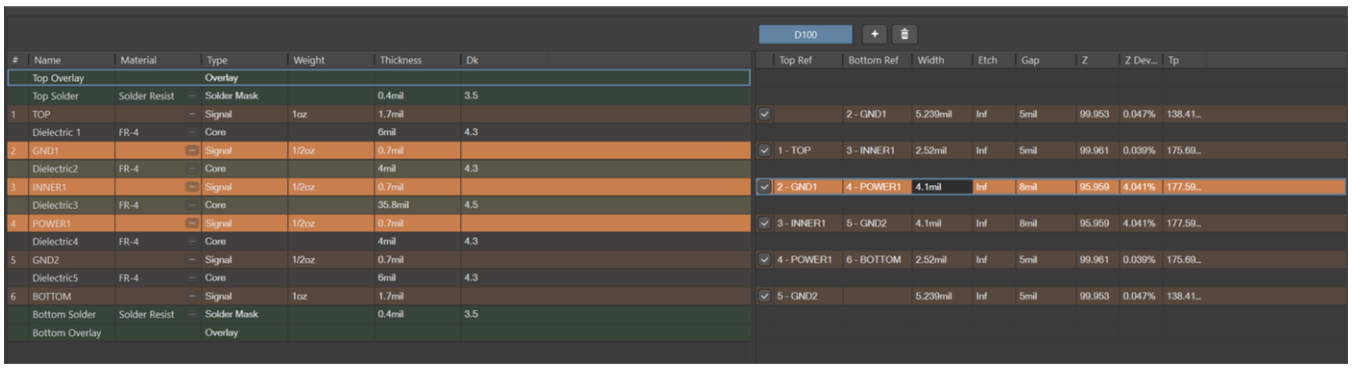


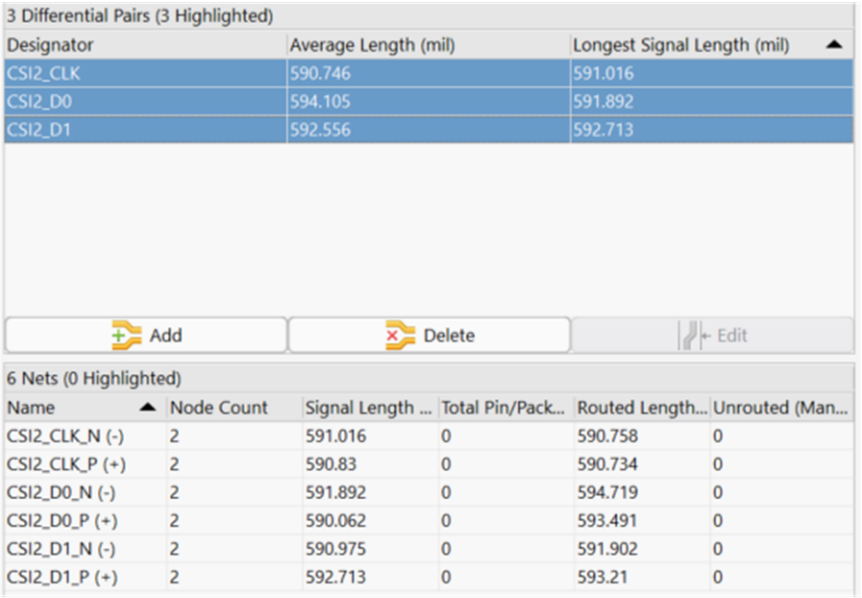
図 21. Six-Layer Stackup Imager Board



4.3.3 Serializer Layout Recommendations

Trace impedance is one critical aspect to the CSI-2 lane routing. For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specs, length specifications also need to be strict within the positive-to-negative differential pair length and pair-to-pair length. If the length is not matched, at these high-data switching speeds, the data can arrive at the 953 at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

図 22. CSI Routing Matching

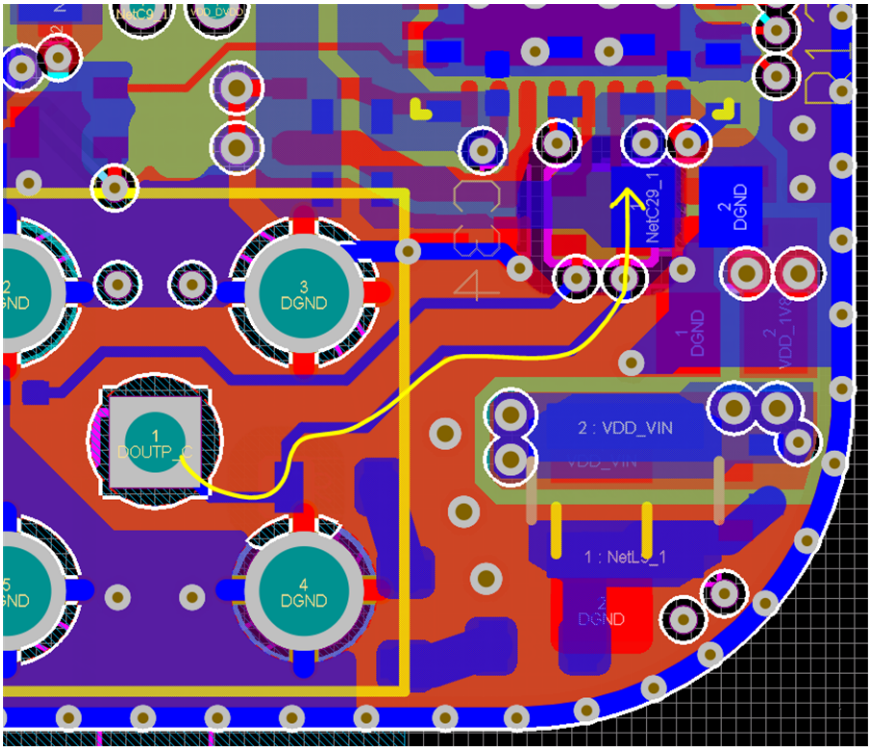


The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees.

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. For decoupling capacitors placed on the opposite layer of the serializer, the return path to the serializer thermal pad should be minimized. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. 図 23 shows the routing of the high-speed serial line, highlighted by the yellow line. The total length of the yellow line is about ½ inch.

図 23. DOUT Path on Base Board



4.3.4 Imager Layout Recommendations

CSI-2 lane routing must follow the same guidelines previously outlined for the imager layout. Similarly, decoupling capacitors should be placed as close as possible to the supply pins, with smaller capacitors taking priority in terms of distance to the pin. Minimize the parasitic resistance and inductance to the ground plane with vias and wide traces.

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-050036.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050036.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050036.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050036.

5 Related Documentation

1. Texas Instruments, *DS90UB953-Q1 FPD-Link III 4.16-Gbps Serializer With CSI-2 Interface for 2.3MP/60fps Cameras, RADAR, and Other Sensors Data Sheet*
2. Texas Instruments, *TPS650330-Q1 Automotive Camera PMIC Data Sheet*
3. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*

4. Texas Instruments, *Cable Requirements for the DS90UB913A & DS90UB914A Application Report*

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2019年12月発行のものから更新 **Page**

- minimum and maximum supply voltage in 表 1. 変更 2
- Buck 2 and Buck 3 from 1000 to 1200. 変更 7
- *Choosing the Buck 1 Inductor* section. 追加 9
- *Choosing the Buck 2 and Buck 3 Inductors* section. 追加 9
- "The TPS650330-Q1 is also pin-compatible with the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1. Each of these devices provides additional safety features, allowing the scalability of this design to camera applications with more stringent safety requirements." to the *Functional Safety* section. 追加 10
- DS90UB950-Q1 to DS90UB953-Q1 in the *Highlighted Products* section. 変更 10
- the PWM switching frequency to 2.3 MHz in the TPS650330-Q1 synopsys in the *Highlighted Products* section. 変更 ... 10
- peak-to-peak ripple voltages from 0.7%, 0.3%, 0.8%, and 1.9% to 0.3%, 0.4%, 1.0%, and 0.3%. 変更 15

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