参考資料

デザイン・ガイド：TIDA-050034
NXP iMX 7D プロセッサ向け統合型電源のリファレンス・デザイン

概要

TIDA-050034 は TI PMIC、TPS6521815、NXP™ i.MX 7Dual アプリケーション・プロセッサを内蔵するフル機能の開発ボードです。このハードウェア・デザインは、DDR3L SDRAM (2x512MB)、64MB シリアル NOR フラッシュ、8GB eMMC 5.0 iNAND、SD カード・インターフェイス v3.0、外部 TFT ディスプレイ・インターフェイス用 50 ピン LCD コネクタ、1000Base-T イーサネット、USB2.0 Type A および micro-AB、外部カメラ・インターフェイス用 MIPI CSI、mini-PCIe インターフェイスで構成されます。このデザインは、i.MX 7Solo または i.MX 7Dual プロセッサを使用し、代替電源ソリューションの評価を必要とするプロジェクトに適しています。

リソース

TIDA-050034	デザイン・フォルダ
TPS6521815	プロダクト・フォルダ
TPS51200	プロダクト・フォルダ
TPS62067	プロダクト・フォルダ
TPS3808	プロダクト・フォルダ
INA3221	プロダクト・フォルダ
TLV755P	プロダクト・フォルダ
WL1831MOD	プロダクト・フォルダ
DP83867CR	プロダクト・フォルダ
OPT3001	プロダクト・フォルダ

Search Our E2E™ support forums

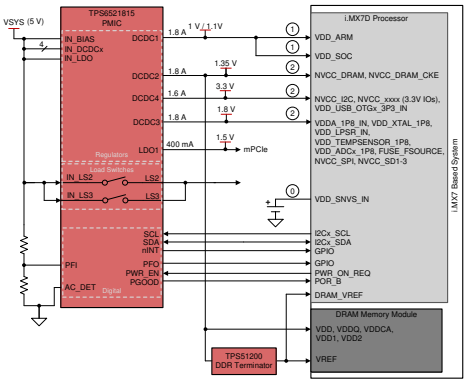
特長

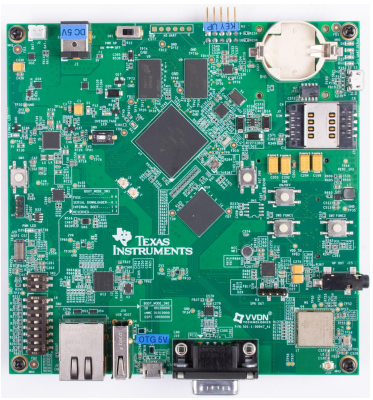
- NXP i.MX 7D および i.MX 7S システムを短期間で開発できるフル・システム・オン・ボード
- 低消費電力モードと DVFS をサポート
- Wi-Fi®+ Bluetooth®ワイヤレス・コネクティビティ
- イーサネット、CAN、USB 有線接続機能
- LCD、HDMI®、MIPI DSI ディスプレイ・オプション
- 選択可能な昇圧オプション (SD、eMMC、QSPI)

アプリケーション

- データ・コンセントレータ
- 電気メーター
- HVAC ゲートウェイ
- サーモスタット
- 侵入管理パネル
- ビルのセキュリティ・ゲートウェイ
- ARM ベースの SoM/CoM
- パネル PLC (HMI)
- バーコード・スキャナ
- ポータブル POS

RadiumBoards でご注文いただけます。





1 System Description

TIDA-050034 is first-and-foremost a reference design for powering the NXP i.MX 7Dual processor from the TPS6521815 PMIC. To show that the PMIC can power the processor, it made the most sense to build a full evaluation kit (EVK) board with a variety of peripheral devices to assist with development of various end equipments. As a result, there are a variety of wired and wireless connections available, as well as multiple BOOT options. The end result of adding all the peripherals is that some external DC-DCs and LDO regulators have been added to provide more voltage rails and current delivery as needed. Finally, to ensure the entire board is operational, we developed and tested software using the open-source embedded Linux Yocto SDK to get started testing this design.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Processor	i.MX 7Dual, Dual-Core Applications Processor, MCIMX7D7DVM10SC	2.2.1
PMIC	TPS6521815 user-programmable PMIC with automatic sequencing and DVFS	2.3.1
Auxiliary power	TPS51200 DDR terminator, TPS62067 2-A buck, TLV755P LDOs	2.3.7
Memory	2x4Gb DDR3L (1GB total), 512Mb QSPI NOR-Flash (64MB), 8GB eMMC 5.0, SD v3.0 interface	2.2.2
Audio CODEC	SAI (Serial Audo Interface) to support the WM8960CGEFL/V-ND CODEC from Cirrus Logic for microphone, speaker, and headphones.	2.2.3
Ethernet	Gigabit ethernet interface - TI DP83867CS PHY and J1011F21PNL RJ45 jack from Pulse Electronics	2.3.3
Wi-Fi + Bluetooth	Support Wi-Fi + Bluetooth with TI WL1831MOD device	2.3.2
Debug method (USB-to-UART)	FTDI FT2232D is required to implement USB to serial UART conversion	2.2.4
USB ports	USB Type-A (TE 1-1734775-1) and micro-AB interface (Hirose ZX62D-AB- 5P8)	2.2.5
LCD display	RGB TFT 50-pin connector for LCD support (Hirose FH40-50S-0.5SV)	2.2.6
MIPI CSI	2-lane MIPI CSI through 30-pin connector (Panasonic AXT530124)	2.2.7
mini-PCIe	TE AXT530124 30-pin connector, Diodes PI6C557-03LE PCIe clock generator, Molex 78723-1001 micro-SIM card socket	2.2.8
JTAG header	JTAG connection to i.MX 7D processor with 50-mil pitch, 10-pin header	2.2.10
USB2ANY header	Debug method for PMIC separate from processor I^2C bus. Provided by USB2ANY (standard 100-mil pitch, 10-pin header)	2.2.11
CAN interface	Microchip MCP2562-E/MF CAN Transceiver, TE 5747840-4 DB9 Male connector	2.2.9
Ambient Light Sensor	TI OPT3001DNPR device with I2C communication	2.3.4
Current monitoring	2x TI INA3221 devices are used to monitor current through 6 rails in the system	2.3.5
Operation with Coin Cell	Coin cell directly attaches to i.MX 7D SNVS input. Using TI TPS3808G25 supervisor, system prevents turn on until coin cell battery is inserted.	2.3.6

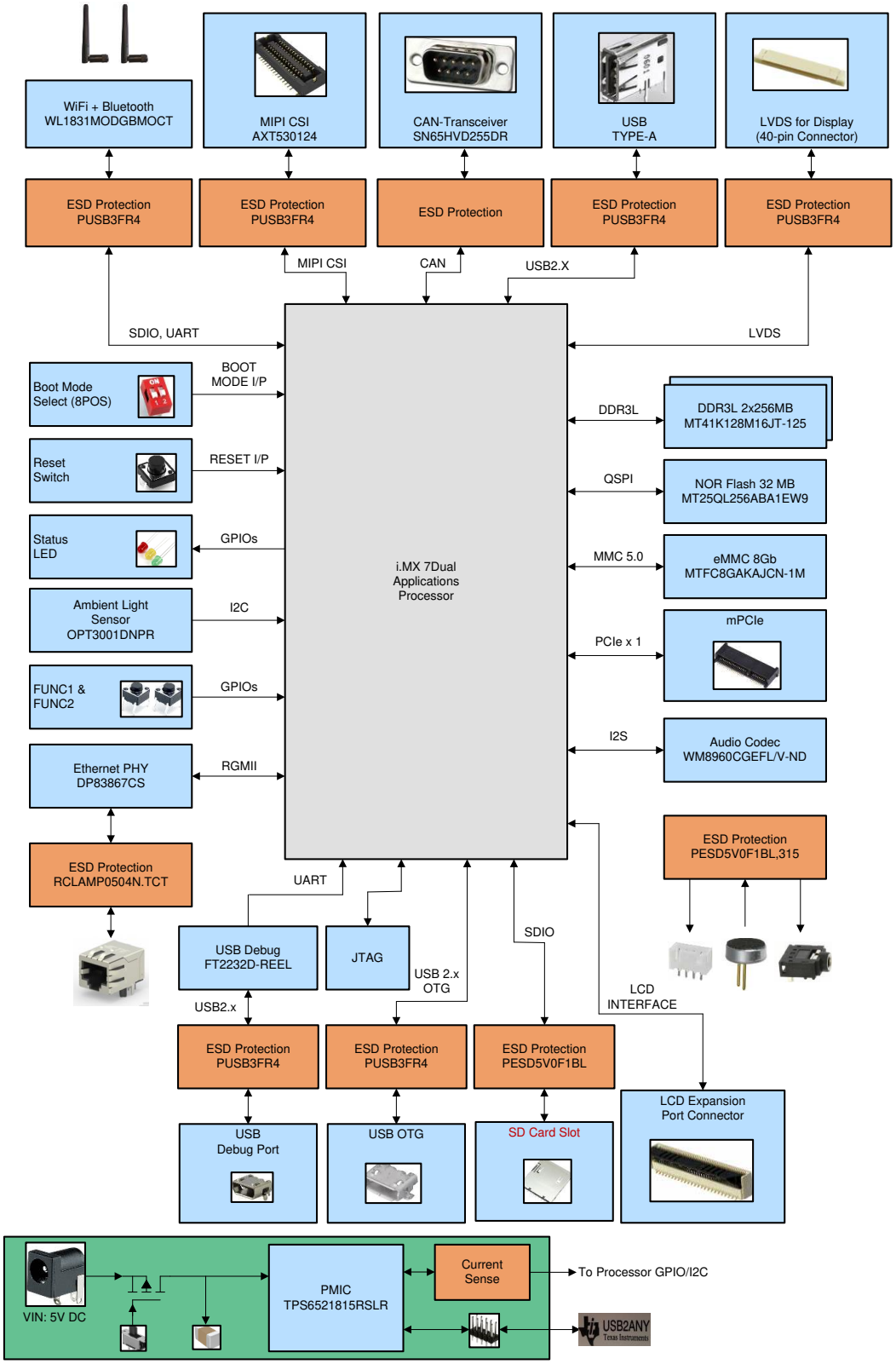
表 **1. Key System Specifications (continued)**

PARAMETER	SPECIFICATIONS	DETAILS
Tactile inputs, visual feedback	Push-buttons and status LEDs connected to GPIOs of the processor to assist with debugging software	2.2.12

2 System Overview

2.1 Block Diagram

図 1. TIDA-050034 Block Diagram



2.2 Design Considerations

This design is intended to show the ability of the TI power devices to provide power to the i.MX 7Dual processor and all of the peripheral ICs in a variety of designs. To verify this, we had to populate all of these other ICs on the design, starting with the processor. All other devices necessary to build an operational evaluation kit are included in this section. The power devices and other TI devices used in this design are described in 2.3.

2.2.1 Processor – i.MX 7Dual Applications Processor

The i.MX 7Dual family of processors are used for high-performance processing with low-power requirements also incorporating high degree of functional integration. These processors are targeted towards the growing market of connected and portable devices. i.MX 7Dual processor consists of three cores (2 × Arm® Cortex®-A7 core operating at 800MHz to 1.2GHz, depending on the part number and one Cortex®-M4 core operating at 200MHz). It provides a 32-bit DDR3 - 1066 memory interface and also supports DDR3L, LPDDR2 and LPDDR3 interface (DDR3L which is used in this design). This processor has number of other interfaces like Ethernet, EPD Controller, MIPI CSI, DSI and LCD interface, WLAN, Bluetooth, GPS, display, camera sensors along with improved security and tamper protection. A detailed table listing the mapping for each pin on the iMX7D processor can be found in Appendix A.

DESCRIPTION	MFG.	PART NUMBER
i.MX 7 series 32-bit MPU, Dual ARM	NXP	MCIMX7D7DVM10SC

2.2.2 i.MX 7Dual Memory Interfaces

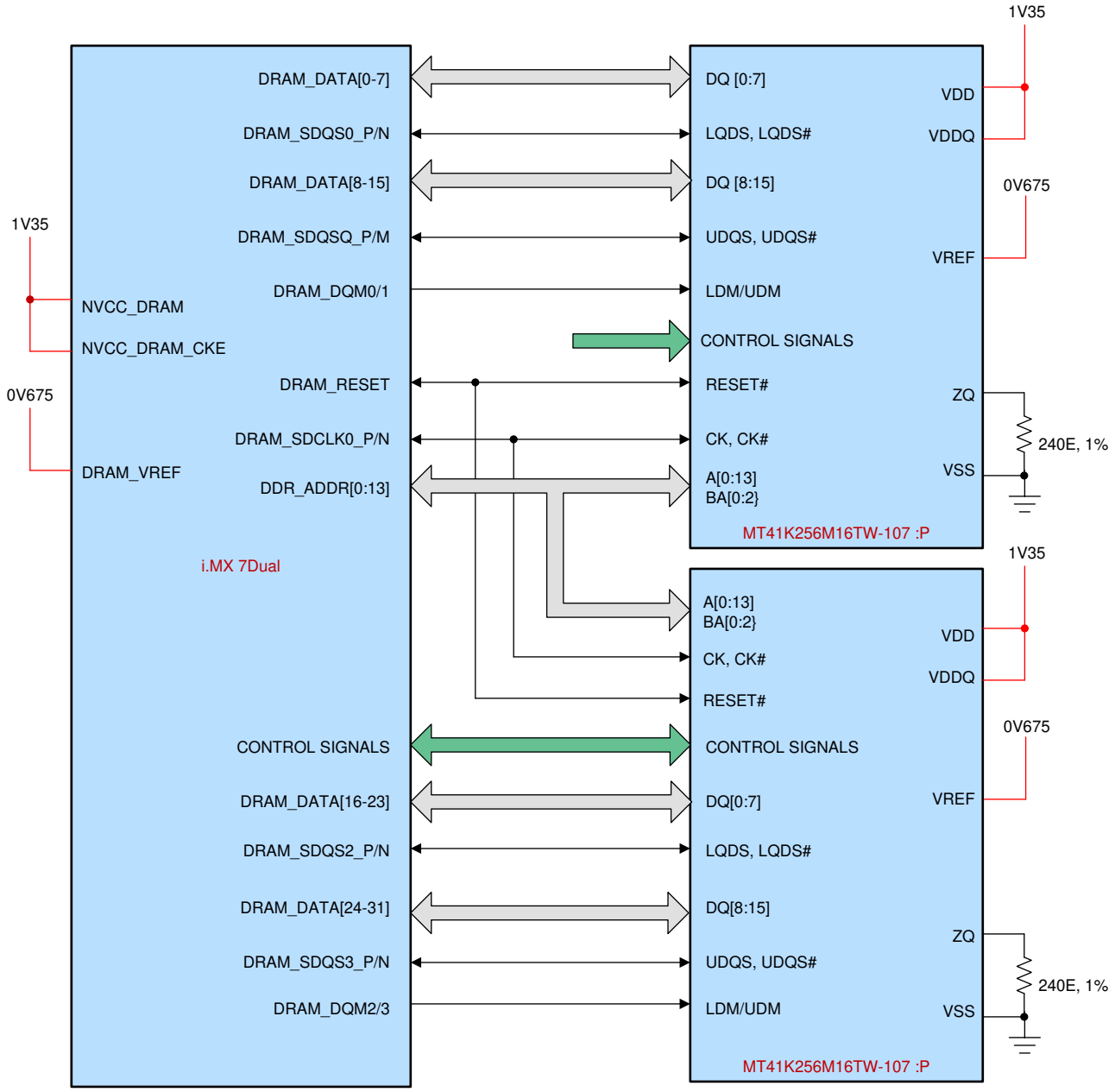
This project makes use of i.MX 7D processor's four different external memory interfaces using 2x4Gb DDR3L (1GB), 512Mb QSPI NOR-Flash (64MB), 8GB eMMC 5.0, and SD v3.0.

2.2.2.1 DDR3L

i.MX 7Dual has dedicated DDR memory controller which support LP-DDR2, DDR3, DDR3L and LPDDR3 all of which supports only 1066 MT/s data rate. This design is provided with two 4Gb x16 (1GB) DDR3L memory. Micron's, MT41K256M16TW-107:P is a 4Gb DDR3L SDRAM, currently used in this design. This design uses two DDR3L memory, together providing 1GB memory required for this design. The memory interface comprises of two channel of 16-bit data signals, along with shared command and address signals. The DDR interface is shown in 図 2.

DESCRIPTION	MFG.	PART NUMBER
IC, DDR3L, 4Gb, x16bit, 1866MHz, FBGA-96	Micron	MT41K256M16TW-107 :P

図 2. DDR3L Interface



2.2.2.2 *Quad SPI NOR Flash*

The i.MX 7Dual processor supports both Parallel NOR Flash interface as well as Quad SPI NOR Flash interface. This project will support only one Serial NOR Flash. Micron's, MT25QL256ABA1EW9- 0SIT TR is a Serial NOR Flash Memory with a density of 512Mb (64MB) at clock frequency 133MHz and data through-put up to 90MB/s.

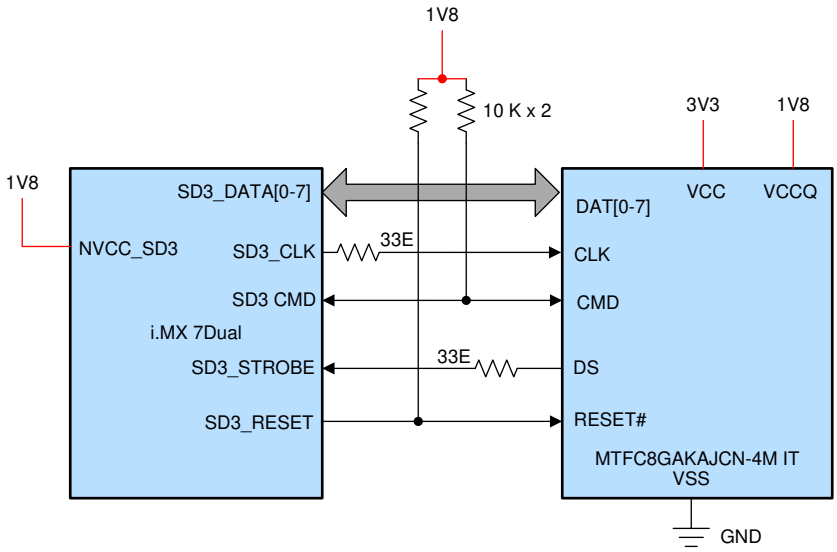
DESCRIPTION	MFG.	PART NUMBER
IC, NOR Flash, 64MB, SPI, 133MHz, 2.7- 3.6V, W-PDFN-8	Micron	MT25QL512ABB1EW9-0SIT

2.2.2.3 eMMC iNAND

For this design an 8GB eMMC 5.0 compliant Memory is included. The interface diagram of eMMC with processor is shown in 図 3. The part used here is an IC from Micron, the MTFC8GAKAJCN- 4M IT. It supports HS400 which is High Speed Mode supporting 400MBps at 200MHz dual data-rate bus.

DESCRIPTION	MFG.	PART NUMBER
IC, eMMC, 8GB, VFBGA-153	Micron	MTFC8GAKAJCN-4M IT

図 3. eMMC Interface

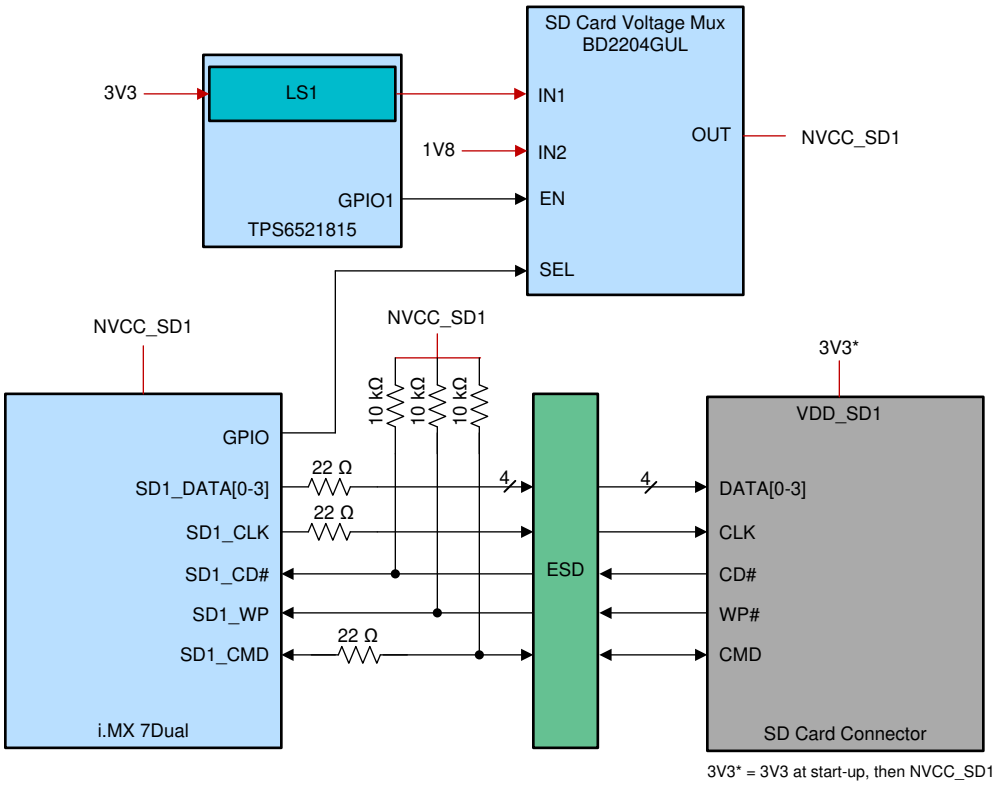


2.2.2.4 SD Card Connector

In this design, there is an SD card connector and interface provided. The power supply to the SD card is selectable between 1.8 V and 3.3 V using a power multiplexer, and both input voltages to the multiplexer are provided by the TPS6521815 PMIC. The initial voltage applied to the VDD pin of the SD card connector must always be 3.3 V, which is achieved with additional circuitry. The power and wiring for the SD Card connector are shown in 図 4

DESCRIPTION	MFG.	PART NUMBER
Connector, SD card, Push-Pull	Amphenol ICC	10067847-001RLF
Diode, ESD-Bidir, 5.5V, SOD-882D	NXP	PESD5V0F1BL
IC, Power Switch N-Channel 2:1, 50VCSP	ROHM	BD2204GUL-E2

図 4. SD Card Power and Connector



2.2.3 Audio CODEC

To include an audio CODEC to this design, an IC from Cirrus Logic, the WM8960CGEFL/V-ND, is used to provide connectivity to a microphone, speaker and a headphone. The digital interface to processor is through SAI (Serial Audio Interface). For this project, there is an additional onboard microphone from PUI Inc, the TOM-1545P-R.

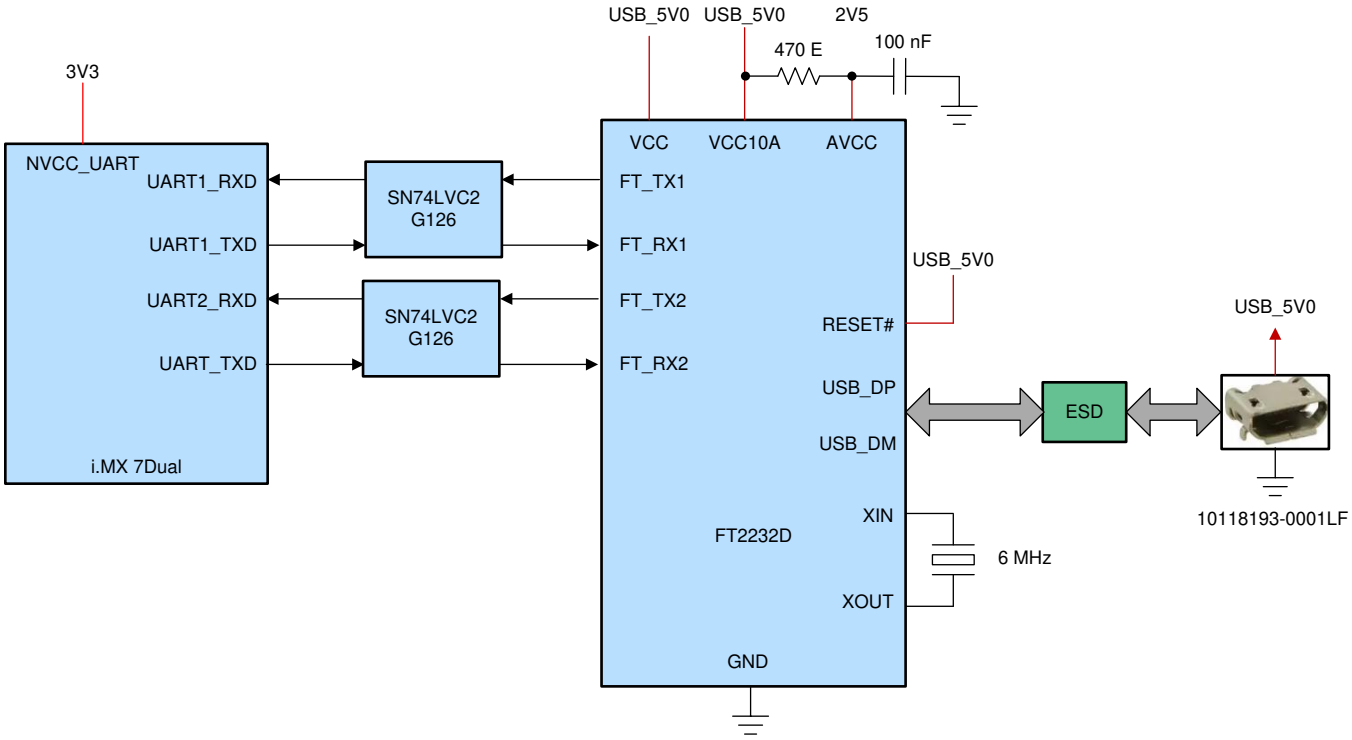
DESCRIPTION	MFG.	PART NUMBER
1C, Audio codec, Stereo, Class D,QFN-32	CIRRUS LOGIC	WM8960CGEFL/V-ND
MIC, Analog Electret Condenser 2V - 10V, -45dB	PUI Audio, Inc.	TOM-1545P-R

2.2.4 USB to UART Converter

There is a USB to Serial (UART) interface in the design. To implement this feature, the FT2232D chip from FTDI is used which is a USB to dual port RS232 converter. The detailed diagram of interconnection is in 図 5.

DESCRIPTION	MFG.	PART NUMBER
IC, FT2232D, USB to UART Converter, Dual UART, LQFP-48	FTDI Chip	FT2232D-REEL

図 5. USB to Serial UART Interface With FT2232

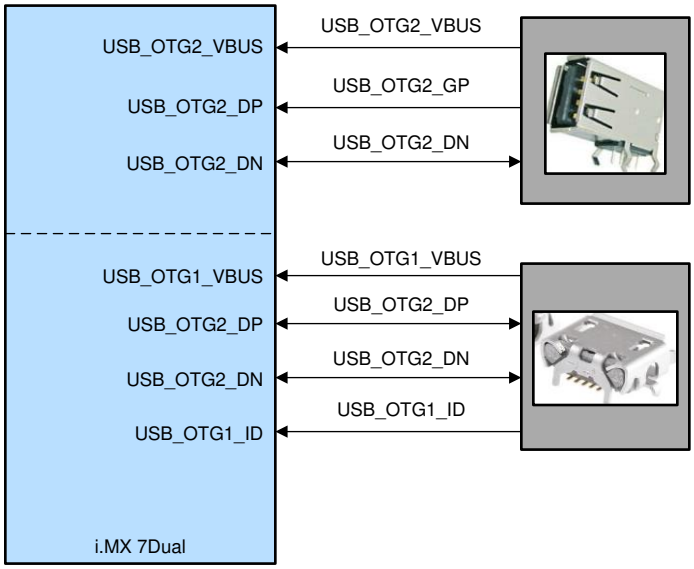


2.2.5 USB Ports

This design incorporates two USB interfaces, one Type A interface and the other a micro-AB interface. Both of the processor's dedicated USB interfaces OTG and connect directly to the receptacle, as shown in 図 6.

DESCRIPTION	MFG.	PART NUMBER
Conn, USB2.0 Type A, RA, TH	TE	1-1734775-1
Conn, USB2.0 microAB, RA, SMD	Hirose	ZX62D-AB- 5P8(30)

図 6. USB Interface

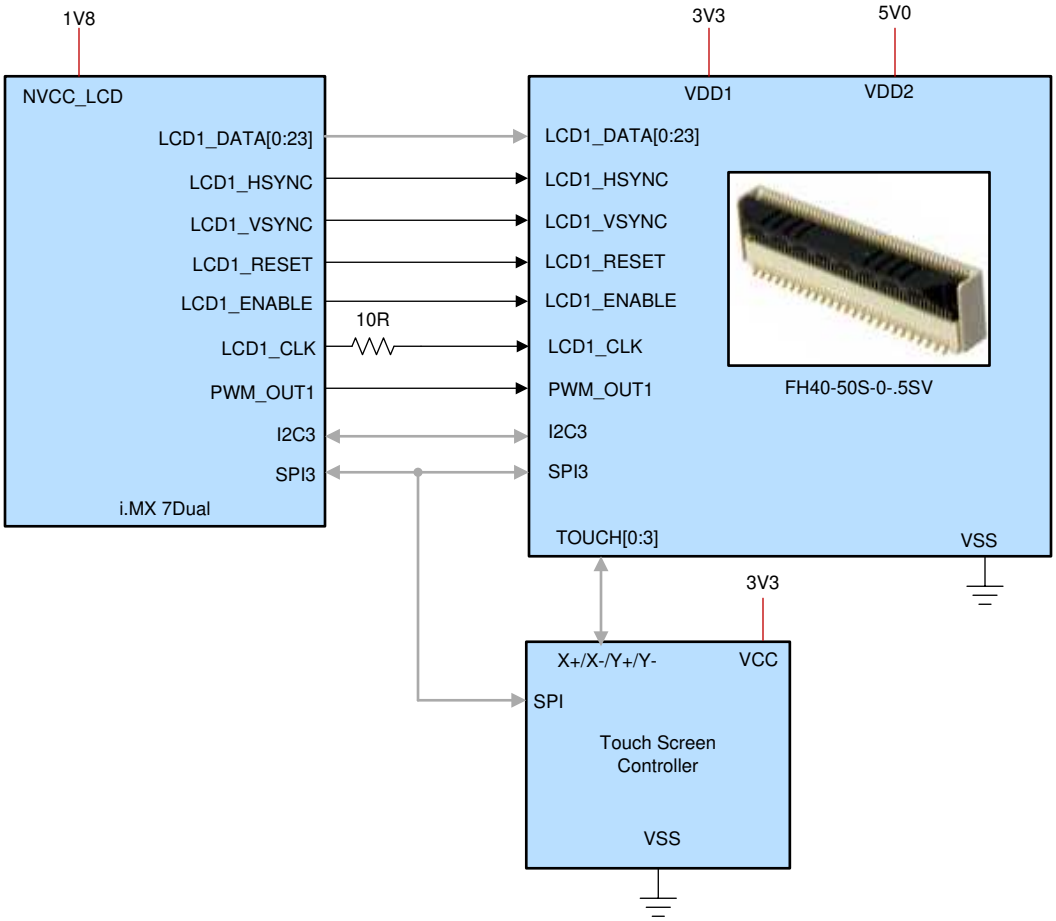


2.2.6 LCD Screen Connector

The LCD interface is a RGB TFT interface with 24 signals connected through a 50-pin connector. The connection diagram is shown in 図 7.

DESCRIPTION	MFG.	PART NUMBER
Conn, FPC, Vertical, 50 Position	Hirose Electric Co Ltd	FH40-50S-0.5SV

図 7. LCD Interface From i.MX 7D Processor to Connector

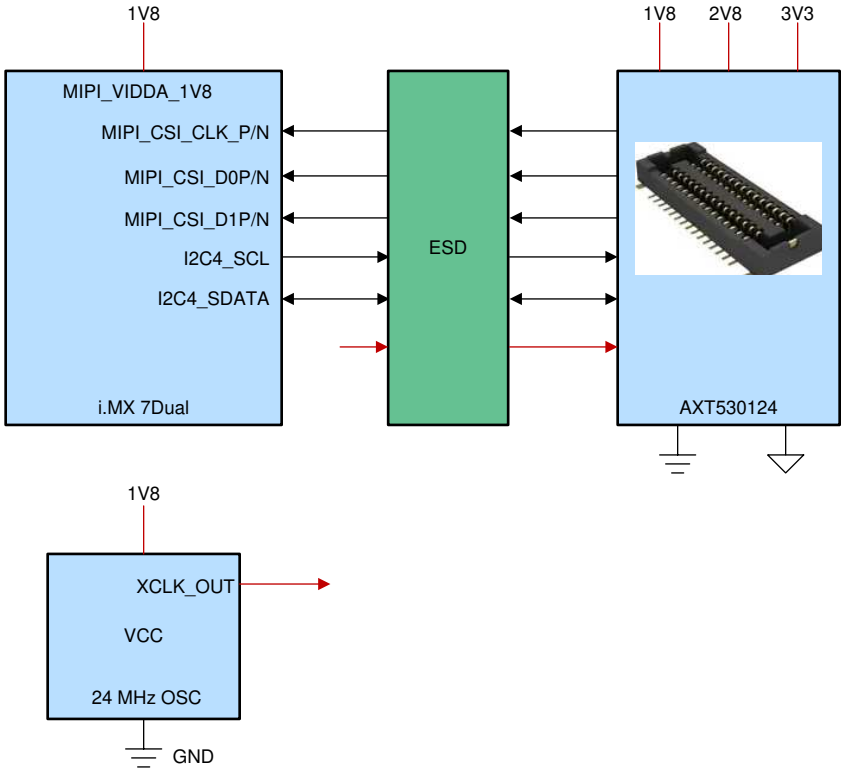


2.2.7 MIPI CSI Connector

MIPI CSI for camera is provided with this design. The i.MX 7D processor supports 2 lane MIPI interface, which is connector to a 30-pin connector from Panasonic as shown in 図 8.

DESCRIPTION	MFG.	PART NUMBER
Connector, Socket, 0.4mm, 30 Position	Panasonic Electric Works	AXT530124

図 8. MIPI CSI Connector

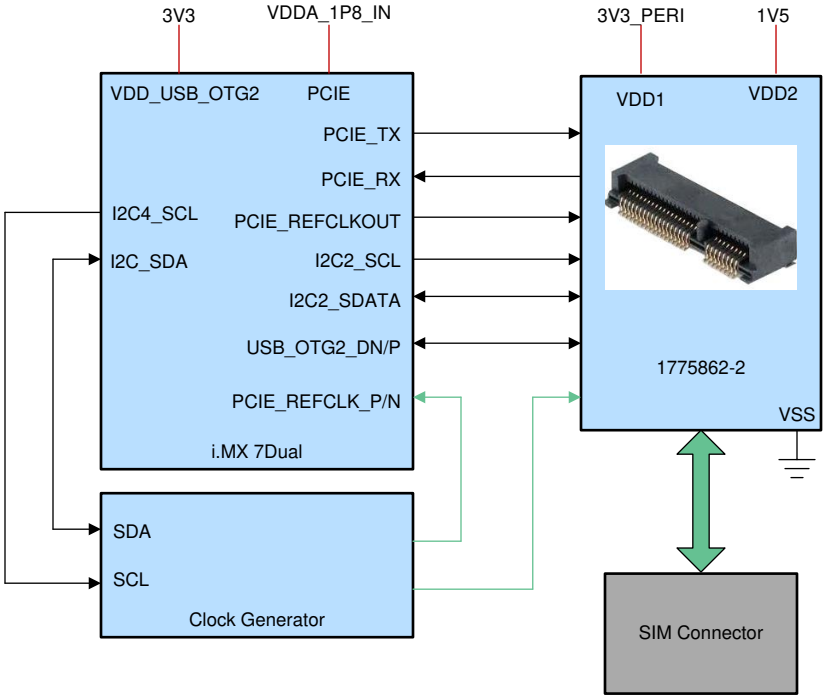


2.2.8 Mini PCI Express® Connector

The signals for mini-PCI Express, or mPCIe, are terminated to a connector in this design as shown in 図 9. An onboard reference clock generator is used.

DESCRIPTION	MFG.	PART NUMBER
Conn, Socket, mPCIe, 52 Position	TE	1775862-2
IC, PI6C557, PCIe Clock Generator, 200MHz, TSSOP-16	Diodes	PI6C557-03LE
Conn, Micro SIM Card Socket, 1X1, Shielded, RA	Molex	78723-1001

図 9. mPCIe Interface

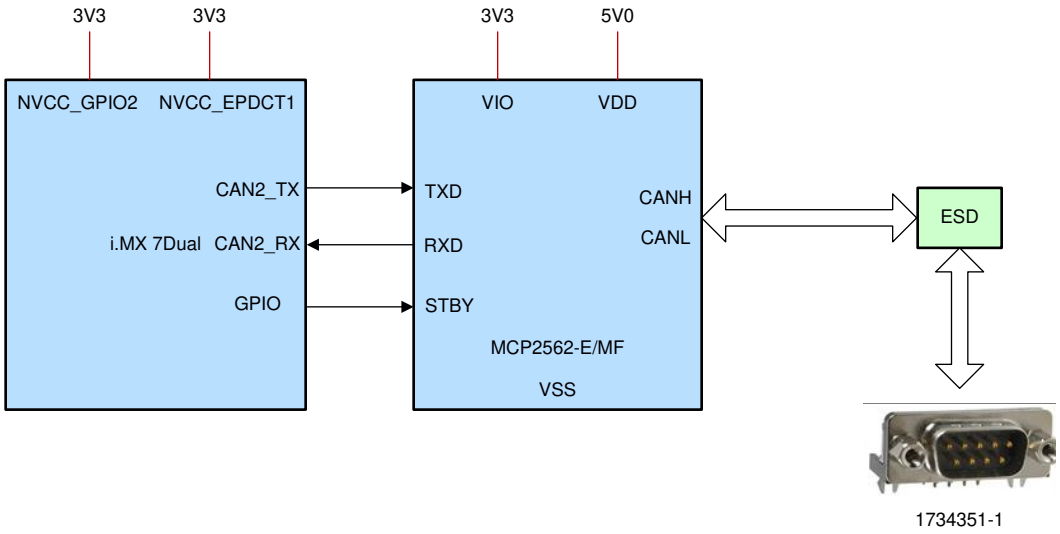


2.2.9 CAN Transceiver and Standard Connector

This design includes a CAN interface. The transceiver is a MCP2562 from Microchip, which is wired to a standard 9-pin D-Sub connector, as shown in 図 10.

DESCRIPTION	MFG.	PART NUMBER
IC, CAN Transceiver, SOIC-8	Microchip	MCP2562-E/MF
Conn, DE-9, Male, 1x1, 6A, Board Lock, RA, TH	TE	5747840-4

図 10. CAN Interface



2.2.10 JTAG Header

The JTAG connections match the requirements of the i.MX 7Dual for direct access to the processor for programming and debugging.

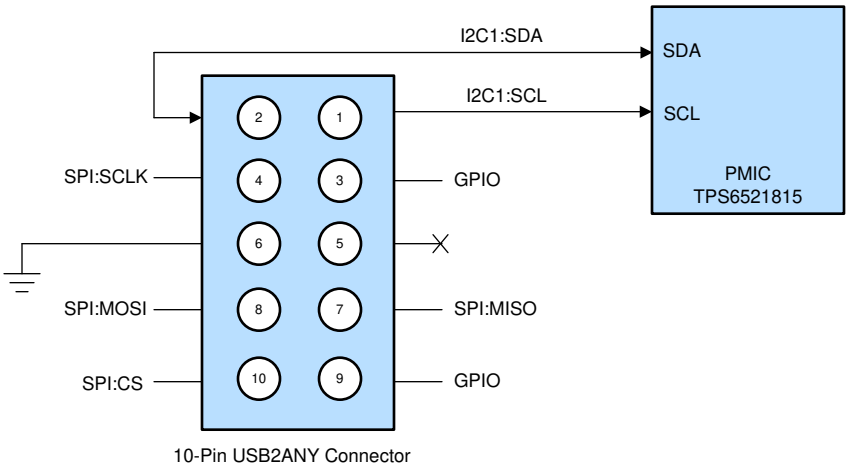
DESCRIPTION	MFG.	PART NUMBER
Connector, Berg strip, 2x5, 1.27mm, 1A, ST, SMD	FCI	20021121-00010*4LF

2.2.11 USB2ANY Header

USB2ANY is TI MCU-based adapter intended to allow a computer to control an electronic evaluation module (EVM) via a USB connection. In this design, the I^2C interface of USB2ANY is used to externally monitor, control, and or re-program the internal registers of PMIC. The wiring of the USB2ANY header is shown in 図 11.

DESCRIPTION	MFG.	PART NUMBER
Connector, Berg strip, 2x5, 2.54mm, 3A, RA, TH	FCI	68021-210HLF

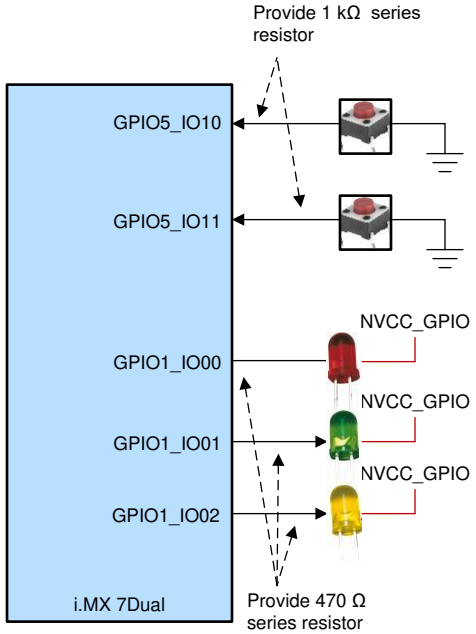
図 11. USB2ANY Header Connections to PMIC I^2C Pins



2.2.12 Functional Switches and Status LEDs

There are two functional multi-purpose push buttons connected to GPIOs configured as inputs on the processor that can be used for software developers to test applications developed using this board. Three LED are connected to three GPIOs of the processor to indicate the status of processes that are running, completed, or may have failed. Both the push-buttons and status LEDs can be used for debugging or to provide tactile inputs and visual feedback to the user. These connections are shown in 図 12.

図 12. GPIO Connections to Push-buttons and LEDs



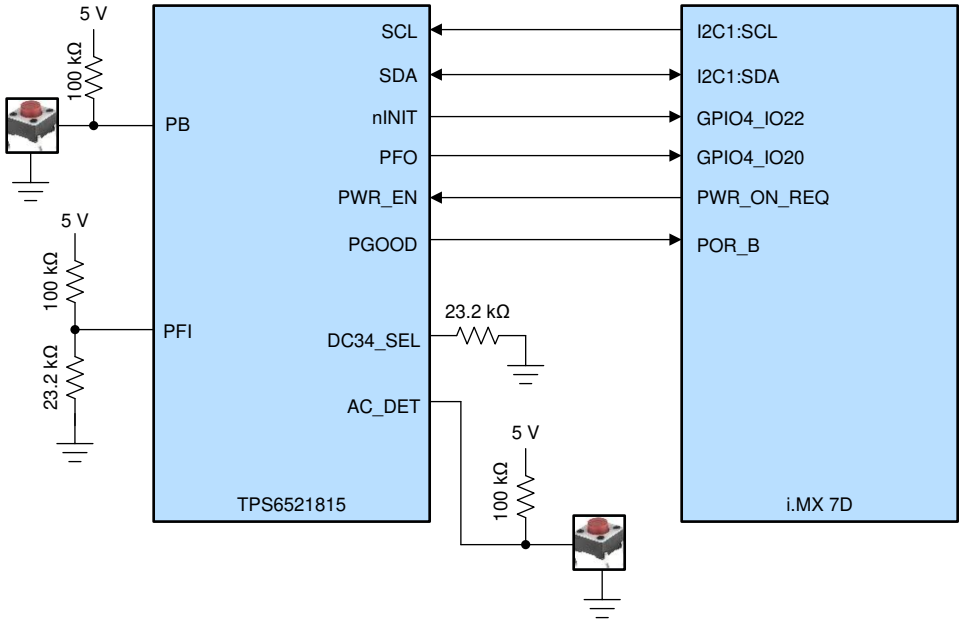
2.3 Highlighted Products

2.3.1 TPS6521815 - Power Management IC

The TPS6521815 device is a Power Management IC (PMIC) specifically designed to support Arm Cortex processors like the i.MX 7Dual from NXP. The PMIC is a good fit for applications powered from a 5-V supply or a Li-Ion battery. The IC consists of three adjustable step-down (buck) converters, one buck-boost converter, one adjustable LDO regulator and three load switches with two selectable current limit. The PMIC supports undervoltage lockout (UVLO), over-temperature warning and shutdown, separate power-good output for all regulators, programmable power sequencing for all regulators, and an I^2C interface for register reading and writing to the device. The full power architecture of this design is shown in 図 17.

The I/O connections between the processor and the TPS6521815 PMIC are shown in 図 13, as well as analog and digital input pins on the PMIC.

図 13. TPS6521815 PMIC I/O Wiring to i.MX 7D Processor



2.3.2 WL1831MOD - Wi-Fi® + Bluetooth® Module

This design makes use of TI's Wi-Fi + Bluetooth module, the WL1831MODGBMOCT device. The interface with the processor is through UART for Bluetooth and SDIO for WLAN (Wi-Fi). The design provides two coaxial connections for monopole antenna connection.

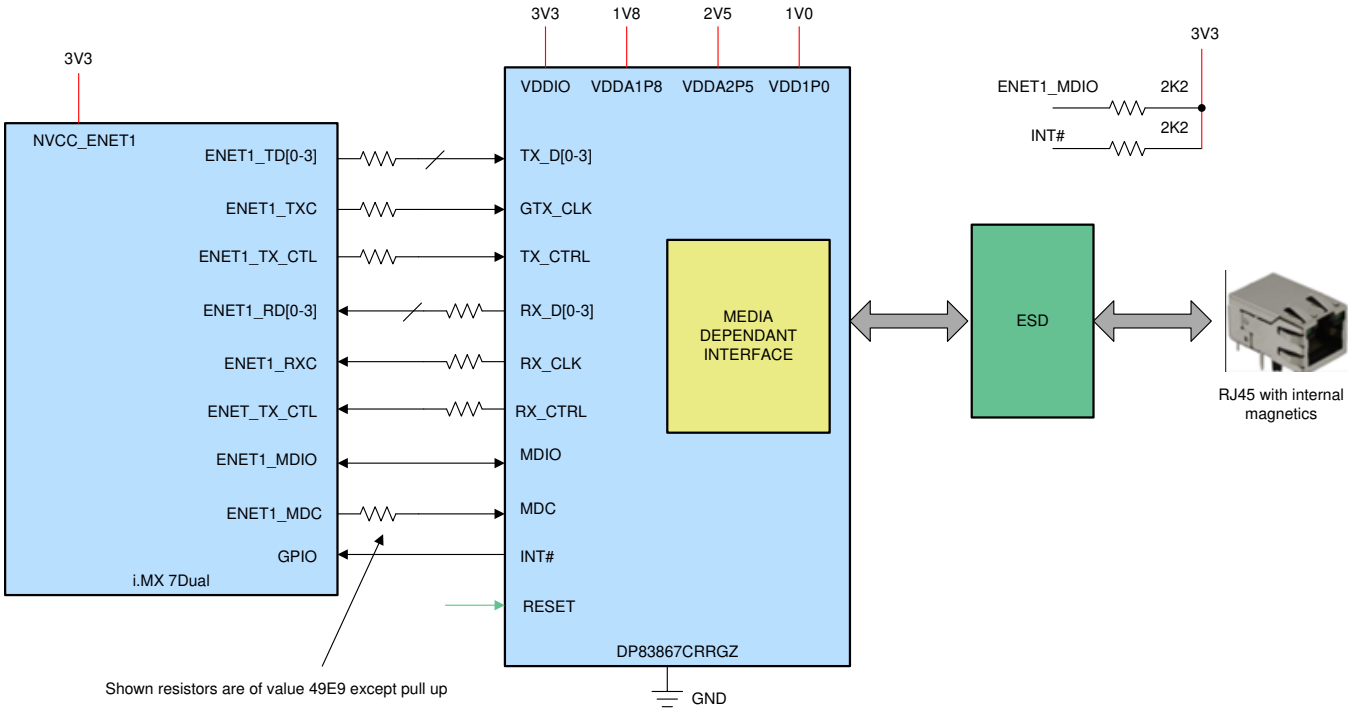
Description	Mfg.	Part Number
Module, Wi-Fi-Bluetooth,IEEE 802.11b, 802.11g, 802.11n, QFM-100	TI	WL1831MODGBMOCT

2.3.3 DP83867CR - Ethernet PHY

The i.MX 7Dual processor supports dual Ethernet PHY interfaces, but for this design we are using only one gigabit Ethernet. The 1000Base-T PHY used in this design is the DP83867CR device. The interface to the processor is through RGMII, also connecting MDC/MDIO for management of the PHY. To connect MDI to the Cat5e cable, we used an RJ45 with internal magnetics from Pulse Electronics. The Ethernet interface connections are shown in 図 14.

Description	Mfg.	Part Number
IC, Gigabit Ethernet PHY	TI	DP83867CRRGZ
Conn, RJ45 Jack with integrated magnetics, 1x1, shielded, LED(G,Y) RA, TH	PULSE ELECTRONICS	J1011F21PNL

図 14. Ethernet Interface With DP83867CR PHY



2.3.4 OPT3001 - Ambient Light Sensor

The ambient light sensor (ALS) provided in this design uses TI's IC. The interface to the processor is through shared I^2C lines. The address (ADDR) pin of the sensor IC needs to be pulled up or down with a resistor to determine the address setting according to 表 2.

Description	Mfg.	Part Number
IC, Ambient Light Sensor, I2C, USON-6	TI	OPT3001DNPR

表 2. OPT3001 I^2C Slave Address Options

7-bit Binary Address	7-bit Hex Address	ADDR Pin Termination
1000100b	0x44	GND
1000101b	0x45	VDD
1000110b	0x46	SDA
1000111b	0x47	SCL

2.3.5 INA3221 - Current Monitor

To measure the live current information, a current sense circuit is integrated to the Power section of this design. The current sensing is done with the INA3221 device. There are two devices used to monitor all the TPS6521815 PMIC power rails. The wiring is shown in 図 15. The address pin A0 of the INA3221 device needs to be terminated according to 表 3.

図 15. INA3221 Current Sensor Wiring From PMIC to Processor

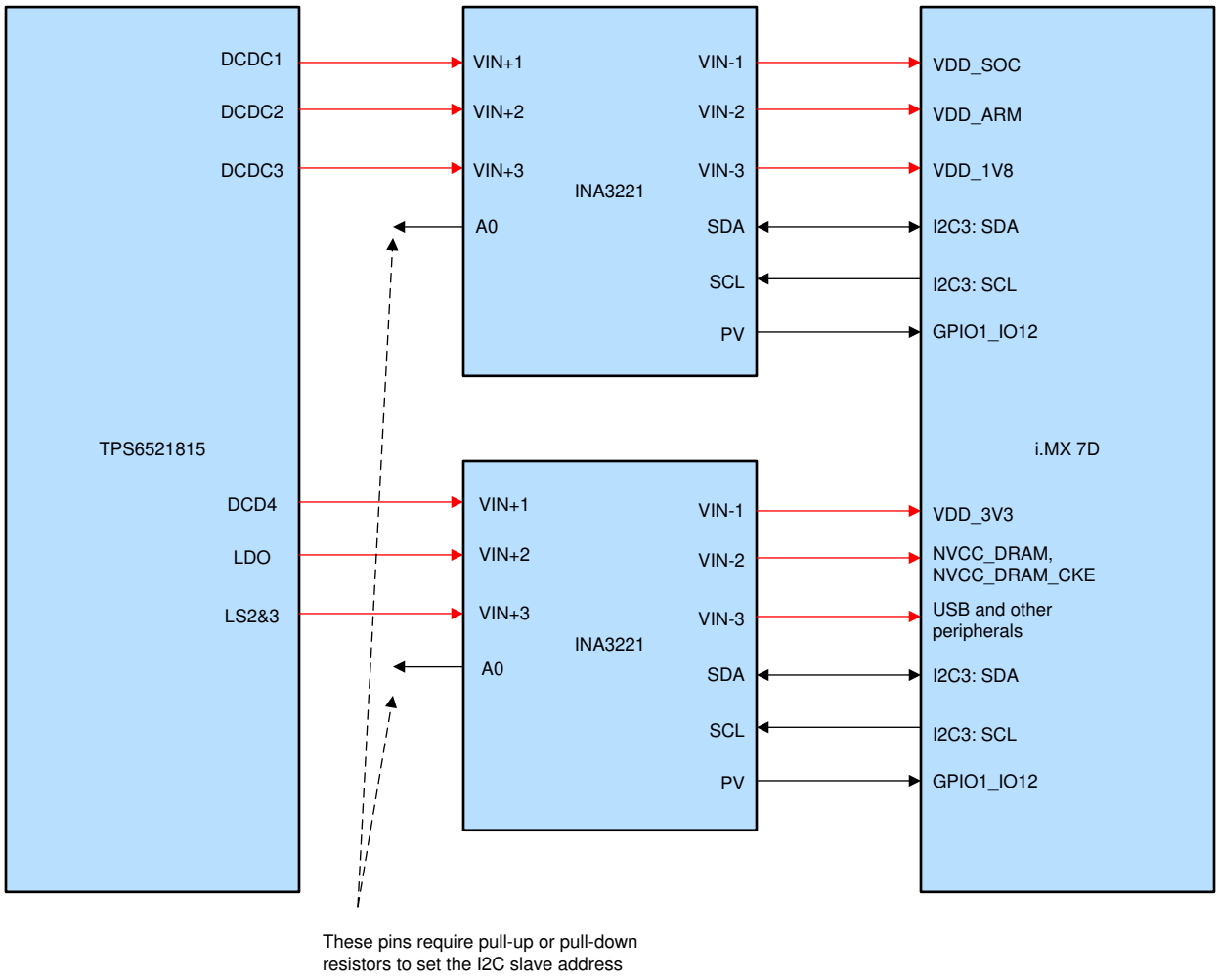


表 3. INA3221 I²C Slave Address Options

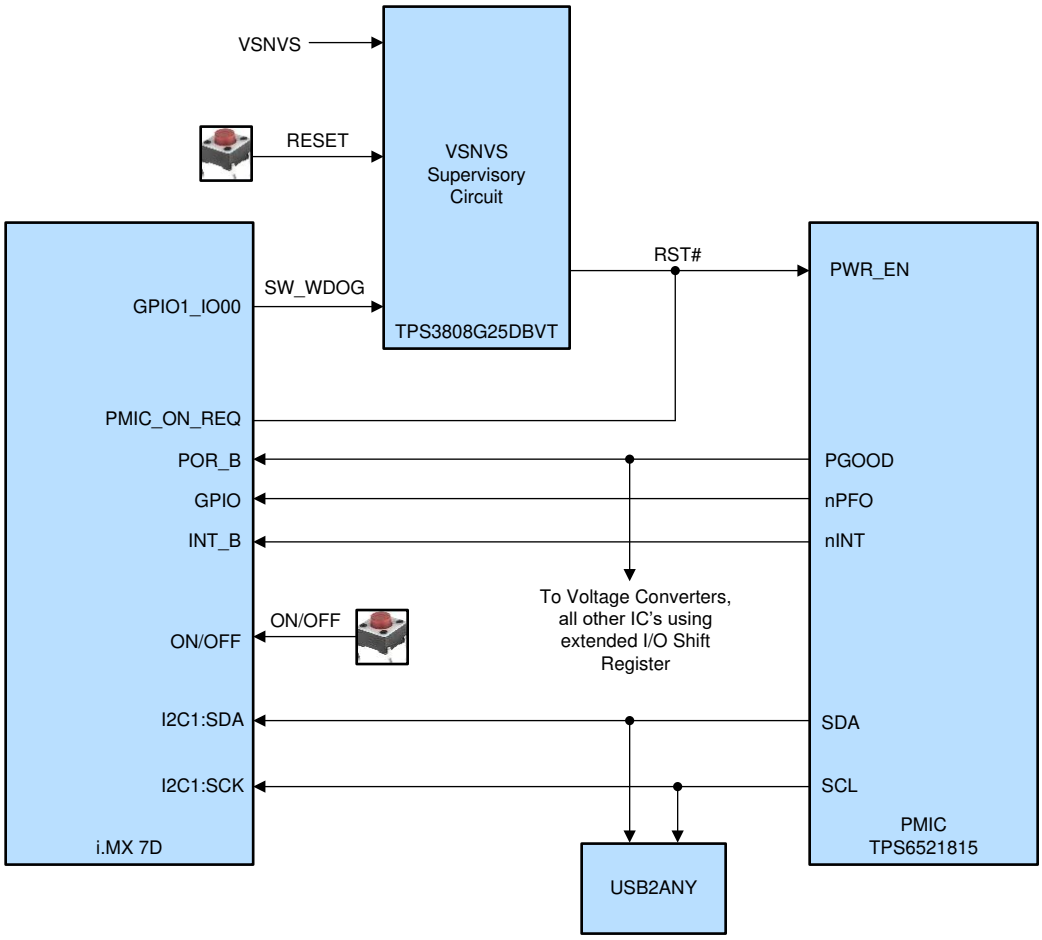
7-BIT BINARY ADDRESS	7-BIT HEX ADDRESS	ADDR PIN TERMINATION
1000000b	0x40	GND
1000001b	0x41	V_S
1000010b	0x42	SDA
1000011b	0x43	SCL

2.3.6 TPS3808 - Voltage Supervisor for Reset Scheme

The reset scheme for this project is shown in 図 16. The TPS3808 voltage supervisor senses the VSNS voltage from the coin-cell. Unless the coin-cell is inserted, the TPS3808 supervisor will prevent the PMIC from turning on. This is critical to ensure the power-up sequence is correct.

The TPS3808 device has its input MR# connected to RESET Switch and watch dog from processor. If any of the inputs de-asserts (logic low), then this will disable the PMIC. Once the reset and VSNVS is stable along with all the power outputs, the PGOOD pin will de-assert the Power-ON Reset (POR_B).

図 16. Reset Scheme With TPS3808 Supervisor



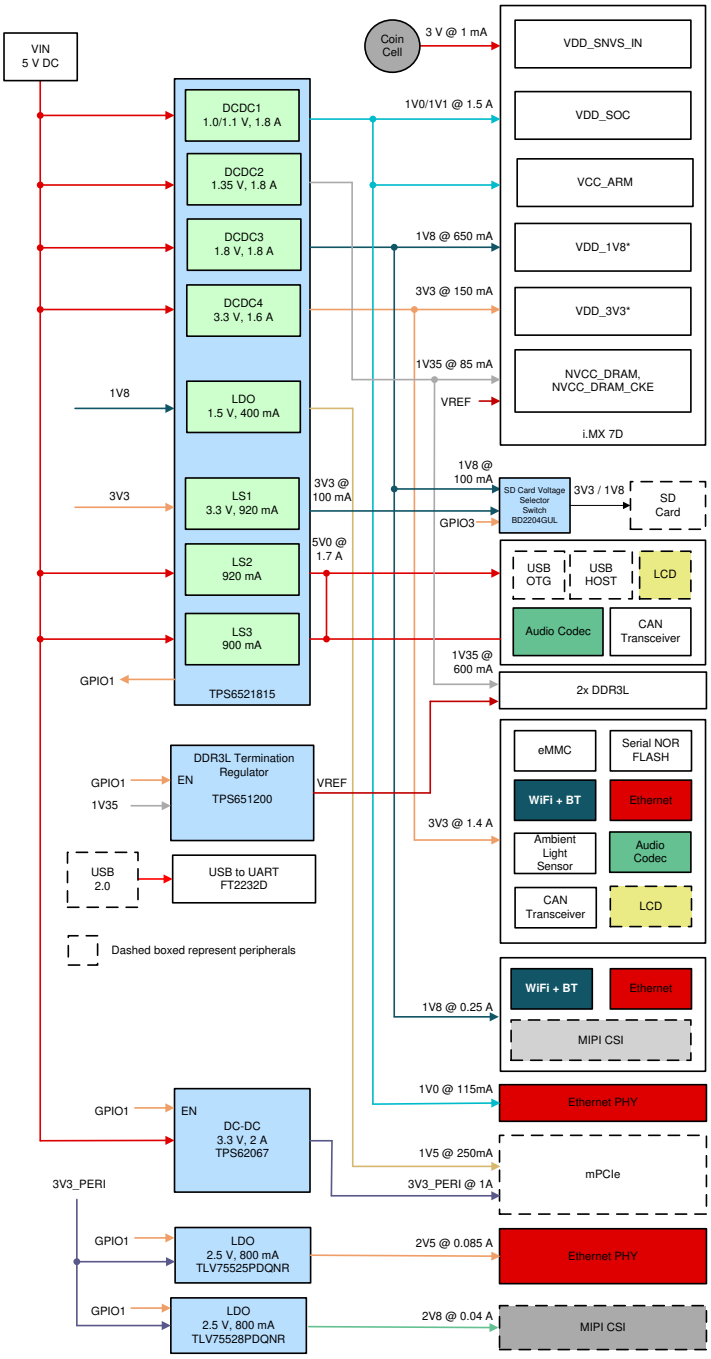
2.3.7 TLV755P, TPS62067, TPS51200 - Auxiliary Power

図 17 shows the full power architecture. Each peripheral device added to a design may require additional voltage levels not required by the processor. For this design, we had to add 2.5 V for the Ethernet PHY and 2.8 V for the MIPI CSI. Both of these power rails are generated by a TLV722P fixed-voltage LDO.

Some designs will also require additional current to power a second rail at the same voltage as a processor supply. In this case, the mPCIe interface could require up to 1 A of current in addition to the 1.4 A allotted for the NVCC_3V3 supply to the processor and other peripherals (Wi-Fi + Bluetooth, Ethernet, Audio CODEC, LCD, ALS, eMMC, and NOR Flash). For this reason, the TPS62067 was added to supply the 3V3_PERI rail for mPCIe. The TPS62067 can also be wired in parallel to the main NVCC_3V3 rail if needed.

Finally, it is sometimes necessary to terminate DDR memory. DDR termination provides a supply (0.675 V) that is half the voltage of the main supply (1.35 V) with the ability to sink or source current. If only one channel of DDR is used, the current consumption is low, or the routing is point-to-point, then tapping off the center of an evenly matched voltage divider may be sufficient. In other cases, a DDR terminator is needed. For this design, we used the TPS51200 device to terminate the two DDR3L ICs in the system.

図 17. TIDA-050034 Full Power Architecture



2.4 System Design Theory

The full power architecture is the result of carefully estimating the power consumed by ICs on the board and peripherals that can be connected to the board. The ideal power sequencing of the i.MX 7D processor must be known to ensure the power sequencing of the TPS6521815 is correct. The I^2C chain must be drawn in its entirety to ensure there are no I^2C address conflicts. The BOOT Mode settings must be mapped to boot the processor using the intended memory storage IC. And finally, PCB floor planning must be completed to make sure the layout of the board is reasonable. All of this system design theory is taken into consideration in this section.

2.4.1 Power Estimation

This design is powered from a 5-V adapter. This 5 V is the main power supply to the TPS6521815 device. The PMIC will generate 5 different voltages: 1.0 V/1.1 V with dynamic voltage scaling (DVS), 1.8 V, 3.3 V, 1.35 V, and 1.5 V. The load switches LS2 and LS3 are used to power ICs and USBs with 5.0 V. The estimated current consumption for each rail is listed in 表 4.

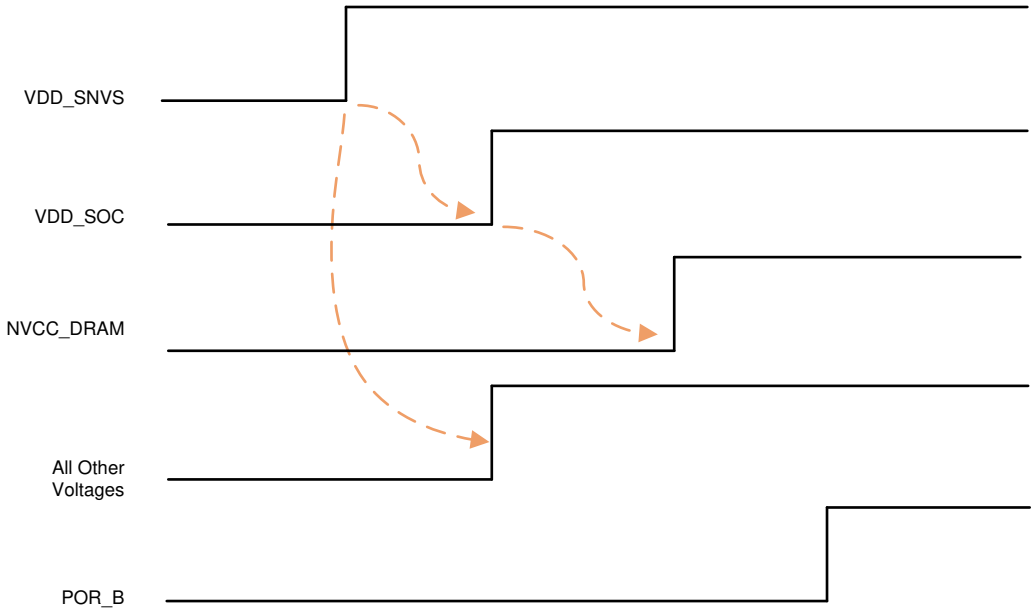
表 4. System Power Estimation

VOLTAGE (V)	SUPPLY IC, RAIL NAME	SUPPLY CURRENT (mA)	LOAD IC, RAIL NAME	CURRENT (mA)	POWER (mW)
1/1.1	TPS6521815, DCDC1	1800	iMX7 VDD_ARM	500	550
			iMX7 VDD_SOC	1000	1100
			DP83867 VDD1P1	115	127
1.35	TPS6521815, DCDC2	1800	iMX7 NVCC_DRAM	85	115
			DDR3L VDD/VDDQ	295	400
0.675	TPS51200	3000	iMX7 VREF	1	0.675
			DDR3L VREF/VTT	295 (max)	200
1.8	TPS6521815, DCDC3	1800	iMX7 NVCC_1P8	625	1125
			WL1831MOD Vxx	200	360
			DP83867 VDDA1P8	50	90
			MIPI CSI	350	630
1.5	TPS6521815, LDO1	400	mPCIe	250	375
3.3	TPS6521815, DCDC4	1600	i.MX7 NVCC_3V3	148	489
			MTFC8GAKAJCN-1M WT	150	495
			MT25QL256	35	116
			WL1831MOD	1105	3647
			DP83867 VDDIO	50	165
			OPT3001 VDD	0.0037	0.0122
			MCP2562	0.5	1.65
			WM8960CGEFL	16	53
			LCD	15	50
3.3 (Auxiliary)	TPS62067	2000	mPCIe	1000	3300
5	TPS6521815, LS2/3	1820	FTD2232D	31	155
			2x USB2 Ports	1000	5000
			MCP2562	70	350
			WM8960CGEFL	511	2555
			LCD	Not Tested	-
2.5	TLV75525P	500	DP83867 VDDA2P5	86	215
2.8	TLV75528PP	500	MIPI CSI	350	980
				Total Estimated Power	**23 W**

2.4.2 Power Sequencing

The processor power sequencing is shown in 図 18. First the VDD_SNVS needs to turn on up before any other power. For our design, VDD_SNVS is powered through a coin cell connected directly to the processor input. Once SNVS voltage is stabilized all other power except NVCC_DRAM and NVCC_DRAM_CKE can be turned on. NVCC_DRAM and NVCC_CKE can only power up after VDD_SOC. Once all these voltages stabilize, should lead to power on reset (POR_B).

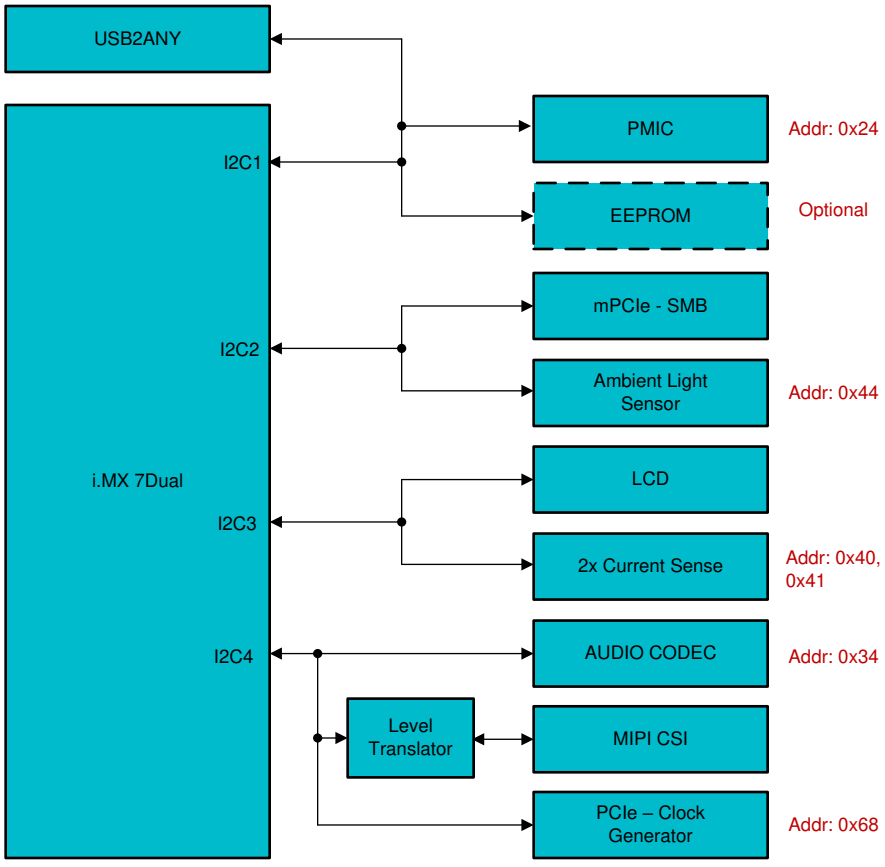
図 18. Required Power Sequence for i.MX 7D Processor



2.4.3 I²C Device Chain

図 19 shows the I²C channel mapping from the processor to each slave device.

図 19. I²C Device Chain



2.4.4 Clock Scheme

Below is a list matching the required clock frequency to each IC that needs clocking.

- i.MX 7Dual – 24MHz and 32.768KHz
- PI6CFGL201BZDIEX (Clock Generator) – 25MHz
- WL1831 (Wi-Fi/BT) – 32.768KHz
- FT2232 (USB to UART) – 6MHz
- WM8960CGEFL/V-ND (Audio Codec) – 24MHz
- DP83867CRRGZ (Ethernet PHY) – 25MHz
- MIPI CSI – 24MHz

2.4.5 BOOT Configuration

This design uses two BOOT configuration. BOOT Mode pins controlled by SW3 DIP switches are connected to dedicated BOOT_MODE0 and BOOT_MODE1 input pins of i.MX 7D Processor. Along with these, there are 20 different pins for setting Booting configuration which shares pins with LCD Data. These 20 pins are controlled by the 8 DIP Switches of SW2. All of the possible BOOT options are given in 表 5 (SW3) and 表 6 (SW2).

表 5. SW3 BOOT Mode Settings

BOOT_MODE[1..0]	BIT 1	BIT 0
Fuses	0	0
Serial Download	0	1
Internal BOOT	1	0
Test Mode	1	1

表 6. SW2 BOOT Mode Settings

SW2, pin 1	SW2, pin 2	SW2, pin 3	SW2, pin 4	SW2, pin 5	SW2, pin 6	SW2, pin 7	SW2, pin 8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001b = SD/eSD Boot			Port Select: 00b=eSDHC1, 01b=eSDHC2, 10b=eSDHC3		0b	0b	Bus Width: 0b=1-bit, 1b=4-bit
010b = MMC/eMMC Boot					Bus Width: 000b=1-bit, 001b=4-bit, 010b=8-bit, 101b=4-bit DDR (MMC4.4), 110b=8-bit DDR (MMC4.4)		
011b = NAND Boot			Pages In Block: 00b=128, 01b=64, 10b=32, 11b=256		BOOT_SEARCH_COUNT: 00b=2, 01b=2, 10b=4, 11b=8		0b
100b = QSPI Boot			0b	0b	0b	0b	0b

2.4.6 PCB Floor Planning

図 20 shows the floor planning for the top side of the PCB and 図 21 shows the floor planning for the bottom side of the PCB.

図 20. PCB Floor Planning (top)

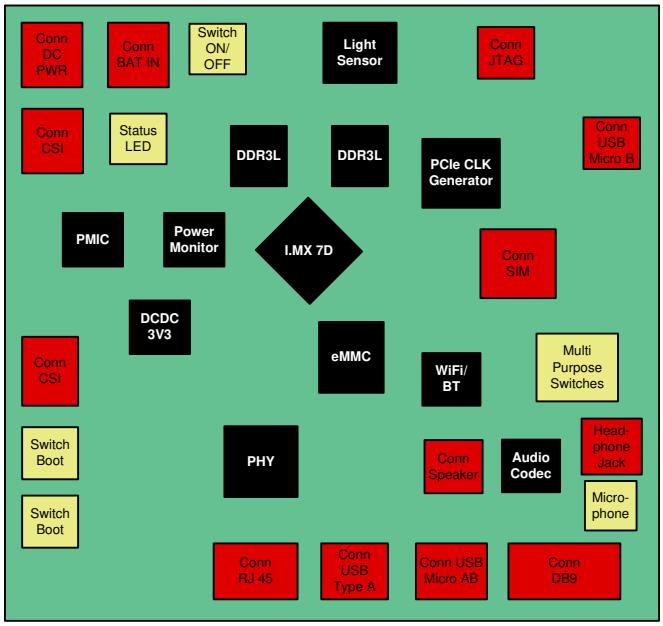
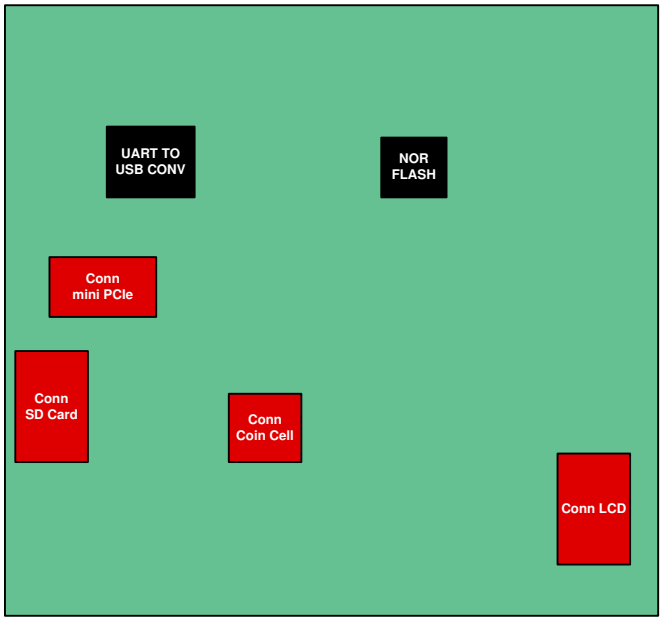


図 21. PCB Floor Planning (bottom)



3 Getting Started, Testing Setup, and Test Results

3.1 Getting Started with Hardware and Software

3.1.1 Hardware

This section contains information about the initial set-up of the TIDA-050034 board, power-up options and user interfaces. 図 22 shows the top side of the fully assembled PCB with labels to help locate connectors or switches on the boards.

図 22. Top of TIDA-050034 PCB With Labels

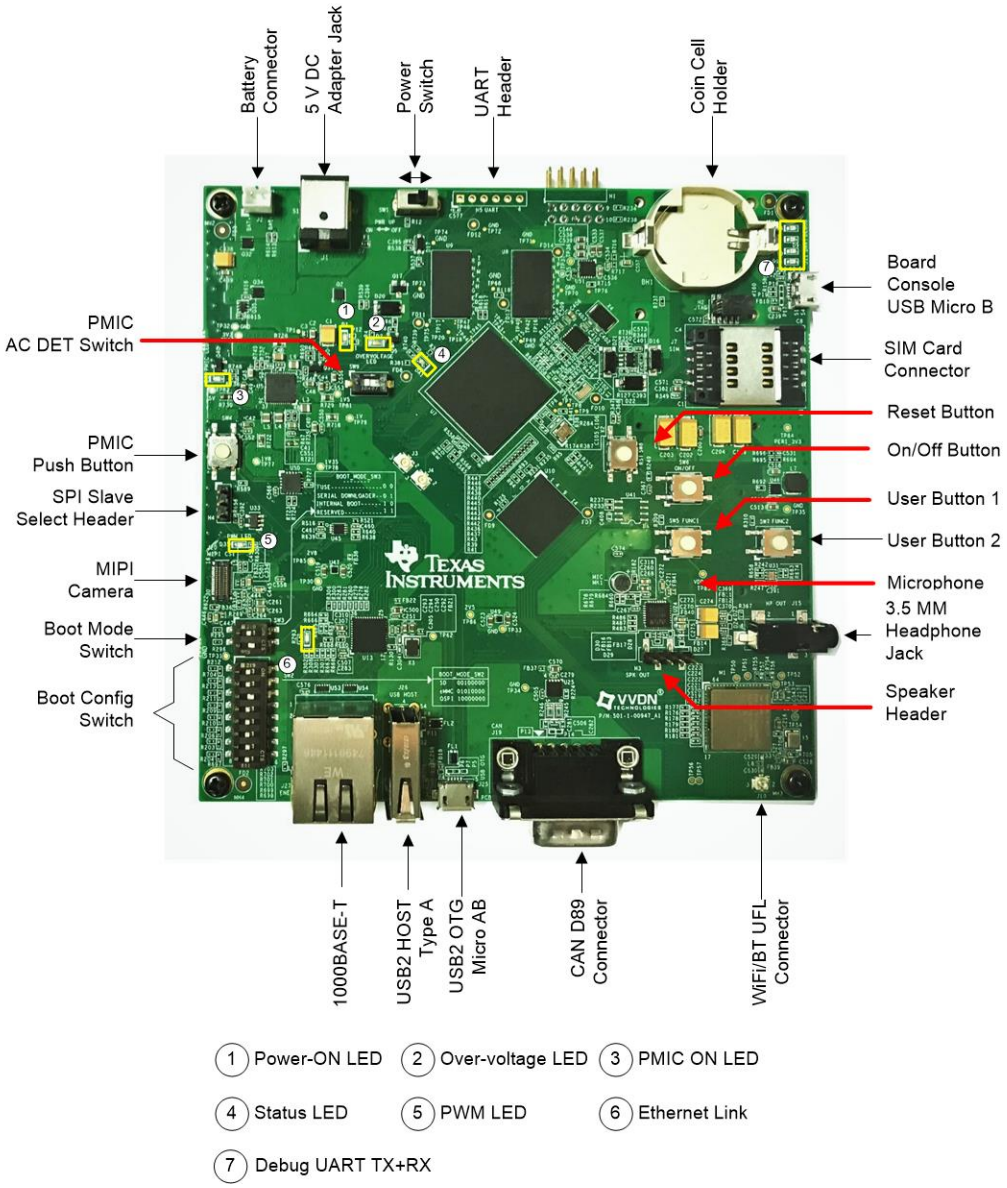
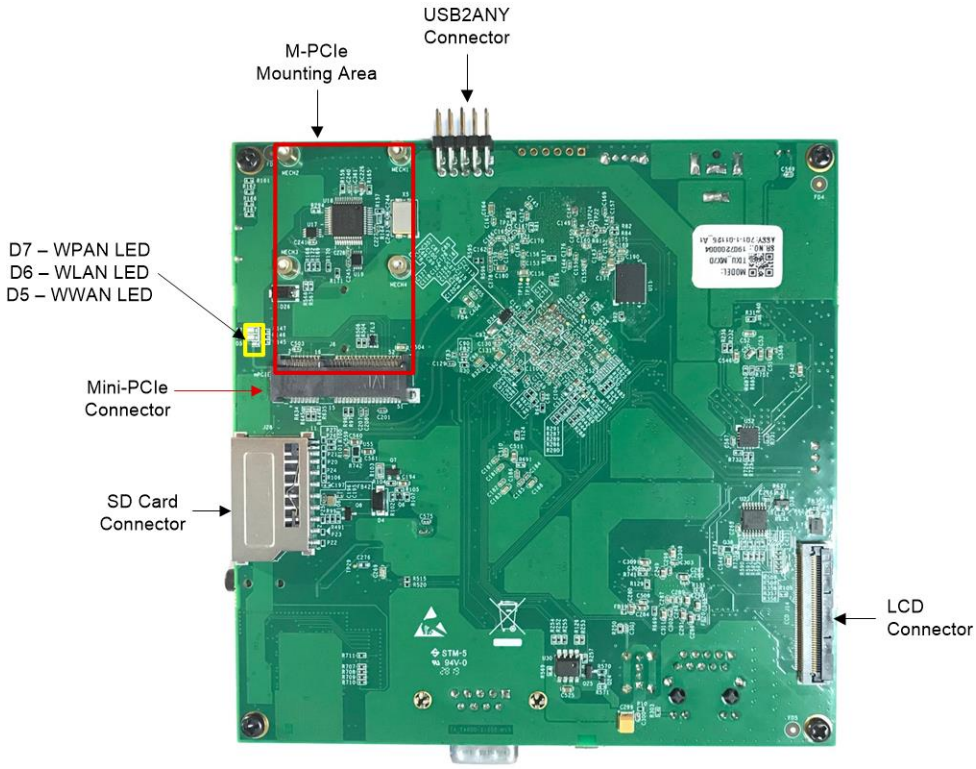


図 23 shows the bottom side of the fully assembled PCB with labels.

図 23. Bottom of TIDA-050034 PCB With Labels



Below is a list of steps that must be followed to set up the hardware of the system.

1. Attach stand-offs to the board with screws inserted in the four holes at the edge of the PCB.
2. Set the BOOT option using SW2/SW3 DIP switches (図 24).
3. Insert CR2032 coin-cell battery in the holder BH1 (図 25).
4. Insert the SD card in J28 connector, if SD Card is used for BOOT (図 26).
5. Insert the USB micro-B cable into J11 connector for UART debug in Terminal window (図 27). Type-A plug connects to computer USB port
6. Insert the 5-V DC adapter barrel jack into J1 connector to supply power (図 28). SMI24-5-V-P6 from CUI Inc is the recommended power supply.
7. Set SW1 to the *ON* position.
8. After BOOT is complete, connect the desired peripherals. For example: RJ-45 Ethernet (J27), mni-PCIe (J8), 3.5-mm headphone jack (J15), MIPI camera (J20), LCD screen (J14), USB device (J26).

図 24. Setting DIP Switches (SW2, SW3) for BOOT From SD Card

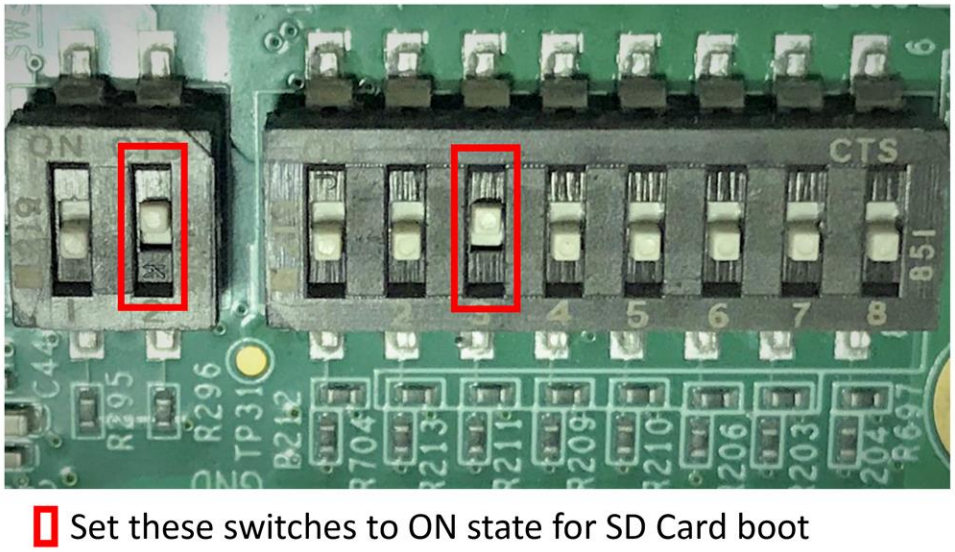
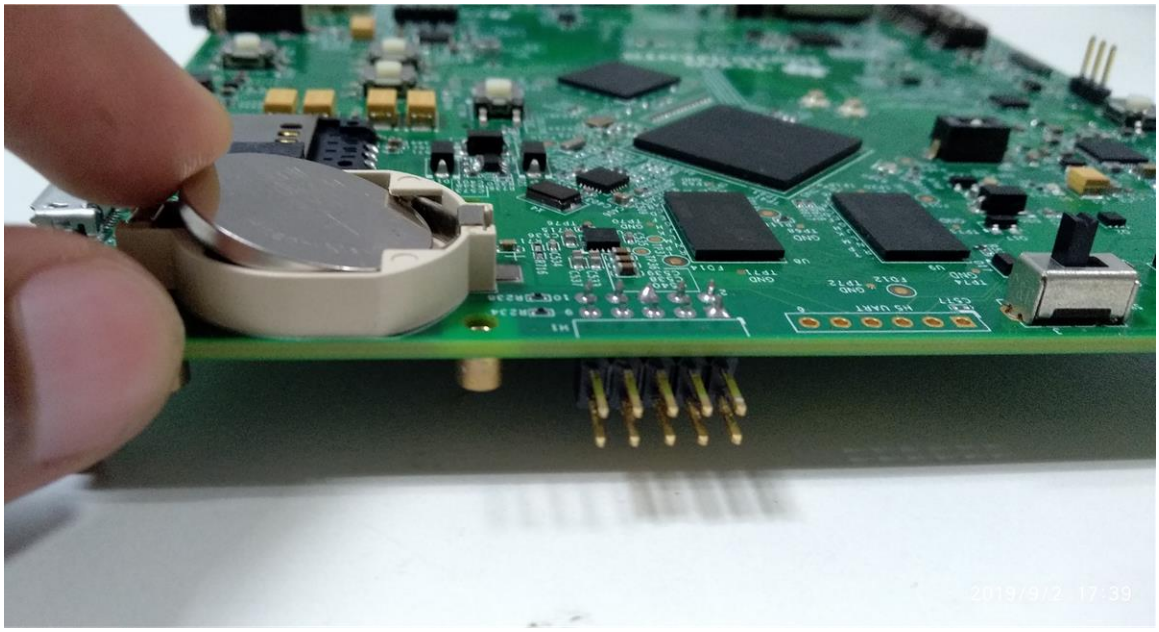


図 25. Inserting Coin Cell Battery Into BH1



注: The voltage of the coin-cell battery (3.0 V nominal) must be above 2.4 V for the supervisor to allow system power-on. If the coin-cell battery voltage is too low, it must be replaced with a fresh battery to continue testing.

図 26. Inserting SD Card Into J28

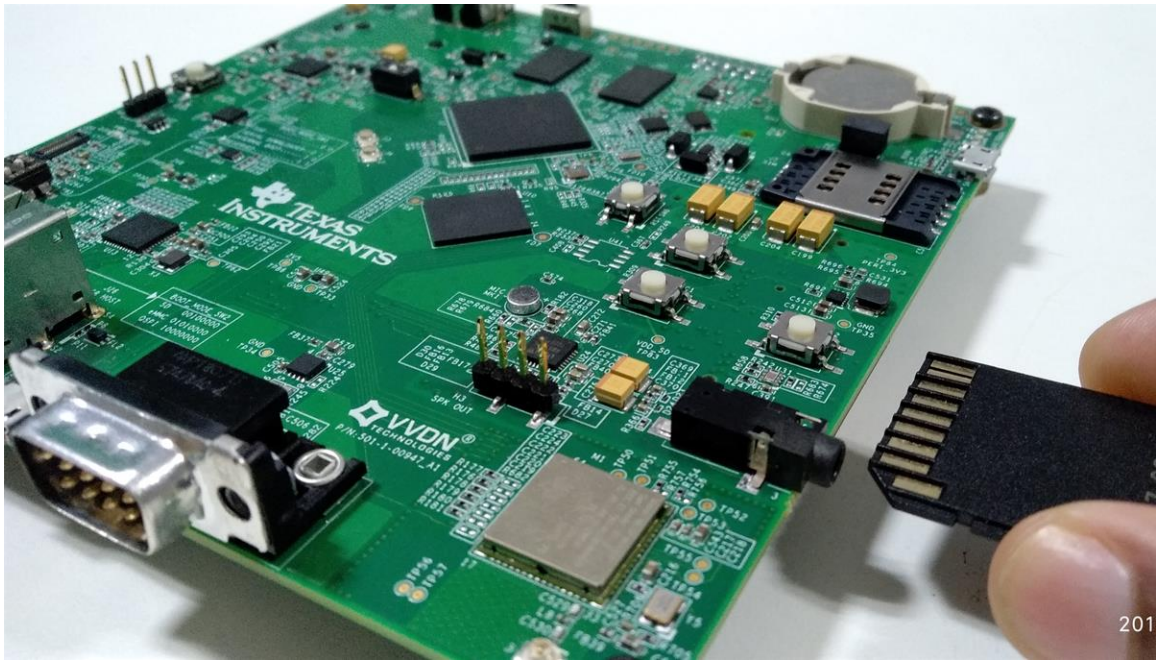
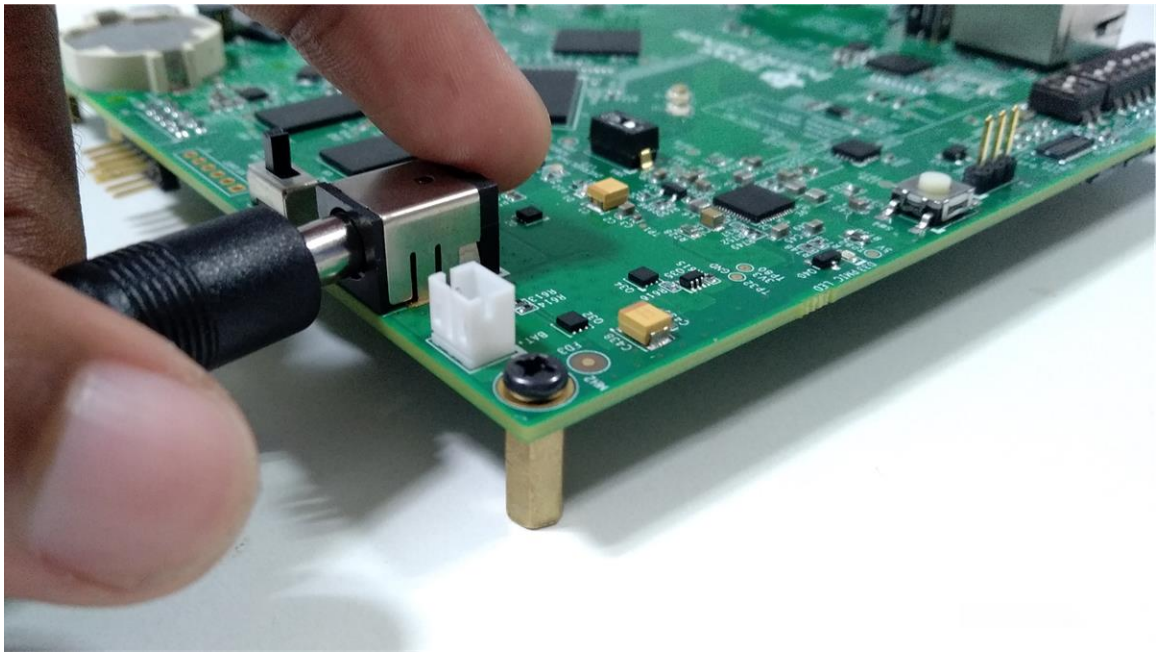


図 27. Inserting micro-B Cable Into J11

注: Refer to 3.1.2 for the procedure to debug TIDA-050034 through Terminal window

図 28. Inserting 5-V DC Adapter Into J1



注: Power supplies other than the SMI24-5-V-P6 may be substituted if the DC output voltage, current rating, polarity, and barrel jack size (inside diameter and outside diameter) are equivalent. Power supplies with DC voltage greater than 5.25V are not acceptable because of the over voltage protection circuit on the board which is intended to prevent damage to the ICs.

注: It is always recommended to power-down the system by switching SW1 to the *OFF* position before unplugging the DC adapter power supply.

3.1.1.1 Onboard LED Information

表 7 lists the indicator LEDs installed on the PCB and provides a short description of their meaning to improve the user experience getting started with the TIDA-050034 reference design.

表 7. Indicator LEDs

NUMBER (IN 図 22)	DESIGNATOR	DESCRIPTION	MEANING
1	D1	Power-On LED	ON: Power-On
			OFF: Power-Off
2	D2	Over-voltage LED	ON: Input over-voltage (>5.25 V)
			OFF: Input voltage within recommended range
3	D33	PMIC-On LED	ON: PGOOD is high (PMIC Active)
			OFF: PGOOD is low (PMIC not in Active state)
4	DA1	Processor Status LED	RED ON: U-boot running
			LED OFF: U-boot to Kernel transition
			RED Blinking: Kernel running
			GREEN ON: File system running
5	D35	PWM LED	DIM: ambient light intensity is low
			BRIGHT: ambient light intensity is high

表 7. Indicator LEDs (continued)

NUMBER (IN 図 22)	DESIGNATOR	DESCRIPTION	MEANING
6	D14	Ethernet Link LED	ON: Ethernet link established
			OFF: Ethernet link down
7	D9, D8 (COMx); D10,D11 (COMy)	Debug UART TX/RX	D9 and D10 blinking: Transmitting data
			D8 and D10 blinking: Receiving data
N/A (bottom)	D5, D6, D7	mini-PCIe LEDs	WWAN
			WLAN
			WPAN

3.1.2 Software

The primary boot source used for testing TIDA-050034 was the SD card. The primary method for testing was using a pre-built binary image to prepare SD card. The purpose of this section is getting started using the software and assumes the software used is already written onto an SD Card that is inserted into the correct slot on the PCB and the BOOT switches are set properly.

The software used for testing is an embedded Linux Yocto build with drivers written for all of the TI ICs and patches to modify the original SDK written for the NXP i.MX 7D processor. Building and installing the image requires a laptop running Ubuntu 16.04 (or later), 120 GB HDD, a fully-assembled TIDA-050034 board, micro-SD card, micro-SD to SD Card adaptor, a micro-USB cable, and a 5-V DC power supply. The procedure for building and installing the software image is outside the scope of this document.

3.1.2.1 Booting of TIDA-050034

Insert the SD card into the SD card slot provided in the board and set the boot switches to boot from SD card. If executables are not found in the configured boot source, then the software is automatically fetched from the SD card.

Connect micro-B side of a USB cable to debug port of the board and Type-A side to a host PC. The connections on the board at this step will look like 図 29.

図 29. Board Connections for BOOT From SD Card With Debug Over USB

Use TeraTerm or Putty to open a Terminal and get the debug log from the device node if the host PC is running Windows. Change port number according to the COMxx port found in Device Manager for the FTDI chip. Note that two (2) COMxx ports will be available even though only one USB cable is connected between the PC and the TIDA-050034 board.

For example, when I am testing this board I can select either **COM7** or **COM8** port with a baud rate of **115200** and leave the other **Putty** settings as the default option.

If the debug prints are coming when the board is powered on, then that interface is working. When prompted to logon, enter *'root'* and press the **Enter** key.

```
timx7d login: root
root@timx7d:~#
```

At the time of writing, the latest software/firmware version for TIDA-050034 is 1.1.0_1, which can be verified using a simple Linux command.

```
root@timx7d:~# fw-version
firmware version : 1.1.0_1
```

There are many other Linux functions and commands that are useful for testing the power supplies and consumption of TIDA-050034, and the next section provides some examples.

3.1.2.2 Example Linux Commands for Testing TIDA-050034

To figure out which I²C devices are on the bus, where "0" means I am looking for I²C devices on channel 0 (because the TPS6521815 should be here at 0x24):

```
root@timx7d:~# i2cdetect -y -r 0
     0   1   2  3   4   5   6   7   8   9   a   b   c   d  e   f
00:             --  --  --  --  --  --  --  --  --  --  --  --  --
10: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
20: --  --  --  --  UU  --  --  --  --  --  --  --  --  --  --  --
30: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
40: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
50: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
60: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
70: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

To test the reading of the ambient light sensor, where I read once with the lights on in the room and then read again with the lights turned off:

```
root@timx7d:~# test_als
lux value : 384.000000
root@timx7d:~# test_als
lux value : 16.020000
```

To verify dynamic voltage scaling is working for the PMIC with respect to the CPU frequency of the processor, where 792 MHz corresponds to DCDC1 = 1.0 V while 996 MHz corresponds to DCDC1 = 1.1 V:

```
root@timx7d:~# echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
root@timx7d:~# echo 996000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
root@timx7d:~# echo 792000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

To run a current sensor application and measure the current on any rail coming out of the TPS6521815 PMIC, where "1" in the first prompt is current sensor IC #1, "1" in the second prompt is channel 1, and "*curr1_input*" returns a value of 248 mA that is being used by the VDD_ARM and VDD_SOC rails:

```
root@timx7d:~# test_currentsensor
Enter current sensor no[1-2]: 1
Enter voltage Level[1-3]: 1
/*****************************************************************************/
/*                              CURRENT SENSOR2                              */
/*            Location of node:/sys/bus/i2c/devices/2-0040/hwmon/h1mon1/     */
/*****************************************************************************/
/* ========================================================================= */
/*                             VDD_SOC_ARM                                   */
/* ========================================================================= */
      curr1_crit :  16380 mA
curr1_crit_alarm :  0
     curr1_input :  248 mA
       curr1_max :  16380 mA
 curr1_max_alarm :  0
       in1_input :  1104 mV
/*****************************************************************************/
```

There are many other useful functions that are written specifically for testing TIDA-050034 in addition to the thousands of pre-defined Linux commands that can be included as part of the Yocto build for iMX. The most useful one for stress testing the processor and increase load current to test the PMIC is "stress-ng." More information on Linux commands can be found in the Ubuntu manual.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050034.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050034.

4.3 CAD Files

To download the CAD files, see the design files at TIDA-050034.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-050034.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050034.

5 Software Files

To download the software files, see the design files at TIDA-050034.

6 Related Documentation

1. Texas Instruments, *TPS6521815 User-Programmable Power Management IC (PMIC) With 6 DC/DC Converters, 1 LDO, and 3 Load Switches Data Sheet*
2. Texas Instruments, *Powering the NXP i.MX 7 processor with the TPS6521815 PMIC Tech Note*
3. *MCIMX7SABRE: SABRE Board for Smart Devices Based on the i.MX 7Dual Applications Processors*
4. *Ubuntu Manpage Repository*
5. *Yocto Project* home page

6.1 商標

6.2 Third-Party Products Disclaimer

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年12月発行のものから更新	**Page**
• link to download software files 追加	33

Appendix A Processor Pin Mapping

A.1 i.MX 7Dual Pin Mapping

The following table is a detailed list of the mapping for each pin on the i.MX 7Dual processor.

表 8. i.MX 7D Pin Mapping

PIN	PERIPHERAL	SIGNAL	ROUTE TO	POWER GROUP	DIRECTION
AD14	MMDC	dram_data, 13	DRAM_DATA13	NVCC_DRAM (0V)	Output
AC14	MMDC	dram_cas_b	DRAM_CAS_B	NVCC_DRAM (0V)	Output
AB14	MMDC	dram_sdwe_b	DRAM_SDWE_B	NVCC_DRAM (0V)	Output
AA14	MMDC	dram_odt, 1	DRAM_ODT1	NVCC_DRAM (0V)	Output
AE14	MMDC	dram_data, 08	DRAM_DATA08	NVCC_DRAM (0V)	Output
AB15	MMDC	dram_ras_b	DRAM_RAS_B	NVCC_DRAM (0V)	Output
AD15	MMDC	dram_sdqs1_p	DRAM_SDQS1_P	NVCC_DRAM (0V)	Input/Output
AE15	MMDC	dram_sdqs1_n	DRAM_SDQS1_N	NVCC_DRAM (0V)	Input/Output
AB16	MMDC	dram_addr, 01	DRAM_ADDR01	NVCC_DRAM (0V)	Output
AC16	MMDC	dram_odt, 0	DRAM_ODT0	NVCC_DRAM (0V)	Output
AD16	MMDC	dram_data, 11	DRAM_DATA11	NVCC_DRAM (0V)	Output
AE16	MMDC	dram_data, 12	DRAM_DATA12	NVCC_DRAM (0V)	Output
AB17	MMDC	dram_sdcke, 0	DRAM_SDCKE0	NVCC_DRAM_CKE (0V)	Output
AD17	MMDC	dram_dqm, 1	DRAM_DQM1	NVCC_DRAM (0V)	Output
AE17	MMDC	dram_data, 10	DRAM_DATA10	NVCC_DRAM (0V)	Output
AB18	MMDC	dram_addr, 14	DRAM_ADDR14	NVCC_DRAM (0V)	Output
AC18	MMDC	dram_addr, 02	DRAM_ADDR02	NVCC_DRAM (0V)	Output
AD18	MMDC	dram_data, 06	DRAM_DATA06	NVCC_DRAM (0V)	Output
AE18	MMDC	dram_data, 09	DRAM_DATA09	NVCC_DRAM (0V)	Output
AB19	MMDC	dram_addr, 00	DRAM_ADDR00	NVCC_DRAM (0V)	Output
AD19	MMDC	dram_data, 05	DRAM_DATA05	NVCC_DRAM (0V)	Output
AE19	MMDC	dram_data, 07	DRAM_DATA07	NVCC_DRAM (0V)	Output
AB20	MMDC	dram_addr, 15	DRAM_ADDR15	NVCC_DRAM (0V)	Output
AC20	MMDC	dram_addr, 03	DRAM_ADDR03	NVCC_DRAM (0V)	Output
AD20	MMDC	dram_dqm, 0	DRAM_DQM0	NVCC_DRAM (0V)	Output
AE20	MMDC	dram_data, 02	DRAM_DATA02	NVCC_DRAM (0V)	Output
AB21	MMDC	dram_addr, 04	DRAM_ADDR04	NVCC_DRAM (0V)	Output
AD21	MMDC	dram_sdqs0_n	DRAM_SDQS0_N	NVCC_DRAM (0V)	Input/Output
AE21	MMDC	dram_sdqs0_p	DRAM_SDQS0_P	NVCC_DRAM (0V)	Input/Output
P22	MMDC	dram_sdba, 1	DRAM_SDBA1	NVCC_DRAM (0V)	Output
R22	MMDC	dram_sdba, 0	DRAM_SDBA0	NVCC_DRAM (0V)	Output
T22	MMDC	dram_addr, 12	DRAM_ADDR12	NVCC_DRAM (0V)	Output
U22	MMDC	dram_addr, 11	DRAM_ADDR11	NVCC_DRAM (0V)	Output
V22	MMDC	dram_addr, 06	DRAM_ADDR06	NVCC_DRAM (0V)	Output
W22	MMDC	dram_addr, 08	DRAM_ADDR08	NVCC_DRAM (0V)	Output
Y22	MMDC	dram_addr, 07	DRAM_ADDR07	NVCC_DRAM (0V)	Output
AA22	MMDC	dram_cs1_b	DRAM_CS1_B	NVCC_DRAM (0V)	Output
AB22	MMDC	dram_sdcke, 1	DRAM_SDCKE1	NVCC_DRAM_CKE (0V)	Output
AC22	MMDC	dram_reset	DRAM_RESET	NVCC_DRAM_CKE (0V)	Output
AD22	MMDC	dram_data, 00	DRAM_DATA00	NVCC_DRAM (0V)	Output
AE22	MMDC	dram_data, 04	DRAM_DATA04	NVCC_DRAM (0V)	Output

表 8. i.MX 7D Pin Mapping (continued)

PIN	PERIPHERAL	SIGNAL	ROUTE TO	POWER GROUP	DIRECTION
N23	MMDC	dram_sdba, 2	DRAM_SDBA2	NVCC_DRAM (0V)	Output
P23	MMDC	dram_addr, 13	DRAM_ADDR13	NVCC_DRAM (0V)	Output
T23	MMDC	dram_addr, 10	DRAM_ADDR10	NVCC_DRAM (0V)	Output
V23	MMDC	dram_addr, 09	DRAM_ADDR09	NVCC_DRAM (0V)	Output
Y23	MMDC	dram_addr, 05	DRAM_ADDR05	NVCC_DRAM (0V)	Output
AB23	MMDC	dram_cs0_b	DRAM_CS0_B	NVCC_DRAM (0V)	Output
AD23	MMDC	dram_data, 01	DRAM_DATA01	NVCC_DRAM (0V)	Output
AE23	MMDC	dram_data, 03	DRAM_DATA03	NVCC_DRAM (0V)	Output
N24	MMDC	dram_data, 25	DRAM_DATA25	NVCC_DRAM (0V)	Output
P24	MMDC	dram_dqm, 3	DRAM_DQM3	NVCC_DRAM (0V)	Output
R24	MMDC	dram_data, 29	DRAM_DATA29	NVCC_DRAM (0V)	Output
T24	MMDC	dram_sdqs3_p	DRAM_SDQS3_P	NVCC_DRAM (0V)	Input/Output
U24	MMDC	dram_data, 30	DRAM_DATA30	NVCC_DRAM (0V)	Output
V24	MMDC	dram_data, 31	DRAM_DATA31	NVCC_DRAM (0V)	Output
W24	MMDC	dram_data, 17	DRAM_DATA17	NVCC_DRAM (0V)	Output
Y24	MMDC	dram_sdqs2_p	DRAM_SDQS2_P	NVCC_DRAM (0V)	Input/Output
AA24	MMDC	dram_dqm, 2	DRAM_DQM2	NVCC_DRAM (0V)	Output
AB24	MMDC	dram_data, 22	DRAM_DATA22	NVCC_DRAM (0V)	Output
AC24	MMDC	dram_data, 23	DRAM_DATA23	NVCC_DRAM (0V)	Output
AD24	MMDC	dram_sdclk0_p	DRAM_SDCLK0_P	NVCC_DRAM (0V)	Output
N25	MMDC	dram_data, 27	DRAM_DATA27	NVCC_DRAM (0V)	Output
P25	MMDC	dram_data, 26	DRAM_DATA26	NVCC_DRAM (0V)	Output
R25	MMDC	dram_data, 24	DRAM_DATA24	NVCC_DRAM (0V)	Output
T25	MMDC	dram_sdqs3_n	DRAM_SDQS3_N	NVCC_DRAM (0V)	Input/Output
U25	MMDC	dram_data, 28	DRAM_DATA28	NVCC_DRAM (0V)	Output
V25	MMDC	dram_data, 18	DRAM_DATA18	NVCC_DRAM (0V)	Output
W25	MMDC	dram_data, 19	DRAM_DATA19	NVCC_DRAM (0V)	Output
Y25	MMDC	dram_sdqs2_n	DRAM_SDQS2_N	NVCC_DRAM (0V)	Input/Output
AA25	MMDC	dram_data, 16	DRAM_DATA16	NVCC_DRAM (0V)	Output
AB25	MMDC	dram_data, 21	DRAM_DATA21	NVCC_DRAM (0V)	Output
AC25	MMDC	dram_data, 20	DRAM_DATA20	NVCC_DRAM (0V)	Output
AD25	MMDC	dram_sdclk0_n	DRAM_SDCLK0_N	NVCC_DRAM (0V)	Output
AB13	MMDC	dram_zqpad	DRAM_ZQPAD	NVCC_DRAM (0V)	Input
AC13	MMDC	dram_vref	DRAM_VREF	DRAM_VREF (0V)	Input
AD13	MMDC	dram_data, 14	DRAM_DATA14	NVCC_DRAM (0V)	Output
AE13	MMDC	dram_data, 15	DRAM_DATA15	NVCC_DRAM (0V)	Output
T1	ENET1	enet_mdc	GPIO1_IO11	NVCC_GPIO2 (0V)	Output
R5	ENET1	enet_mdio	GPIO1_IO10	NVCC_GPIO2 (0V)	Input/Output
F14	ENET1	rgmii_rd, 1	ENET1_RDATA1	NVCC_ENET1 (0V)	Input
E14	ENET1	rgmii_rd, 0	ENET1_RDATA0	NVCC_ENET1 (0V)	Input
D13	ENET1	rgmii_rd, 2	ENET1_RDATA2	NVCC_ENET1 (0V)	Input
E13	ENET1	rgmii_rd, 3	ENET1_RDATA3	NVCC_ENET1 (0V)	Input
F16	ENET1	rgmii_txc	ENET1_TXC	NVCC_ENET1 (0V)	Output
E16	ENET1	rgmii_tx_ctl	ENET1_TX_CTL	NVCC_ENET1 (0V)	Output
F15	ENET1	rgmii_rxc	ENET1_RXC	NVCC_ENET1 (0V)	Input
E15	ENET1	rgmii_rx_ctl	ENET1_RX_CTL	NVCC_ENET1 (0V)	Input
F17	ENET1	rgmii_td, 0	ENET1_TDATA0	NVCC_ENET1 (0V)	Output

表 8. i.MX 7D Pin Mapping (continued)

PIN	PERIPHERAL	SIGNAL	ROUTE TO	POWER GROUP	DIRECTION
E17	ENET1	rgmii_td, 1	ENET1_TDATA1	NVCC_ENET1 (0V)	Output
E18	ENET1	rgmii_td, 2	ENET1_TDATA2	NVCC_ENET1 (0V)	Output
D18	ENET1	rgmii_td, 3	ENET1_TDATA3	NVCC_ENET1 (0V)	Output
P21	QSPI	qspi_a_data, 1	EPDC1_DATA01	NVCC_EPDC1 (0V)	Input/Output
N20	QSPI	qspi_a_data, 2	EPDC1_DATA02	NVCC_EPDC1 (0V)	Input/Output
N21	QSPI	qspi_a_data, 3	EPDC1_DATA03	NVCC_EPDC1 (0V)	Input/Output
M20	QSPI	qspi_a_sclk	EPDC1_DATA05	NVCC_EPDC1 (0V)	Output
M21	QSPI	qspi_a_ss0_b	EPDC1_DATA06	NVCC_EPDC1 (0V)	Output
M23	QSPI	qspi_b_data, 0	EPDC1_DATA08	NVCC_EPDC1 (0V)	Input/Output
L25	QSPI	qspi_b_data, 1	EPDC1_DATA09	NVCC_EPDC1 (0V)	Input/Output
A5	uSDHC1	sd_data, 0	SD1_DATA0	NVCC_SD1 (0V)	Input/Output
D6	uSDHC1	sd_data, 1	SD1_DATA1	NVCC_SD1 (0V)	Input/Output
A4	uSDHC1	sd_data, 2	SD1_DATA2	NVCC_SD1 (0V)	Input/Output
D5	uSDHC1	sd_data, 3	SD1_DATA3	NVCC_SD1 (0V)	Input/Output
C5	uSDHC1	sd_cmd	SD1_CMD	NVCC_SD1 (0V)	Input/Output
B5	uSDHC1	sd_clk	SD1_CLK	NVCC_SD1 (0V)	Output
C6	uSDHC1	sd_cd_b	SD1_CD_B	NVCC_SD1 (0V)	Input
B4	uSDHC1	sd_reset_b	SD1_RESET_B	NVCC_SD1 (0V)	Output
C4	uSDHC1	sd_wp	SD1_WP	NVCC_SD1 (0V)	Input
L3	UART1	uart_rx_data	UART1_RXD	NVCC_UART (0V)	Input
L4	UART1	uart_tx_data	UART1_TXD	NVCC_UART (0V)	Output
L5	UART2	uart_rx_data	UART2_RXD	NVCC_UART (0V)	Input
L6	UART2	uart_tx_data	UART2_TXD	NVCC_UART (0V)	Output
H3	UART6	uart_rx_data	ECSPI1_SCLK	NVCC_SPI (0V)	Input
H4	UART6	uart_rts_b	ECSPI1_MISO	NVCC_SPI (0V)	Input
G5	UART6	uart_tx_data	ECSPI1_MOSI	NVCC_SPI (0V)	Output
H5	UART6	uart_cts_b	ECSPI1_SS0	NVCC_SPI (0V)	Output
E20	ELCDIF	lcd_clk	LCD1_CLK	NVCC_LCD (0V)	Input
F25	ELCDIF	lcd_enable	LCD1_ENABLE	NVCC_LCD (0V)	Input/Output
E25	ELCDIF	lcd_hsync	LCD1_HSYNC	NVCC_LCD (0V)	Input
F24	ELCDIF	lcd_vsync	LCD1_VSYNC	NVCC_LCD (0V)	Input
C21	ELCDIF	lcd_rs	LCD1_RESET	NVCC_LCD (0V)	Output
D21	ELCDIF	lcd_data, 00	LCD1_DATA00	NVCC_LCD (0V)	Input/Output
A22	ELCDIF	lcd_data, 01	LCD1_DATA01	NVCC_LCD (0V)	Input/Output
B22	ELCDIF	lcd_data, 02	LCD1_DATA02	NVCC_LCD (0V)	Input/Output
A23	ELCDIF	lcd_data, 03	LCD1_DATA03	NVCC_LCD (0V)	Input/Output
C22	ELCDIF	lcd_data, 04	LCD1_DATA04	NVCC_LCD (0V)	Input/Output
B23	ELCDIF	lcd_data, 05	LCD1_DATA05	NVCC_LCD (0V)	Input/Output
A24	ELCDIF	lcd_data, 06	LCD1_DATA06	NVCC_LCD (0V)	Input/Output
F20	ELCDIF	lcd_data, 07	LCD1_DATA07	NVCC_LCD (0V)	Input/Output
E21	ELCDIF	lcd_data, 08	LCD1_DATA08	NVCC_LCD (0V)	Input/Output
C23	ELCDIF	lcd_data, 09	LCD1_DATA09	NVCC_LCD (0V)	Input/Output
B24	ELCDIF	lcd_data, 10	LCD1_DATA10	NVCC_LCD (0V)	Input/Output
G20	ELCDIF	lcd_data, 11	LCD1_DATA11	NVCC_LCD (0V)	Input/Output
F21	ELCDIF	lcd_data, 12	LCD1_DATA12	NVCC_LCD (0V)	Input/Output
E22	ELCDIF	lcd_data, 13	LCD1_DATA13	NVCC_LCD (0V)	Input/Output
D23	ELCDIF	lcd_data, 14	LCD1_DATA14	NVCC_LCD (0V)	Input/Output

表 8. i.MX 7D Pin Mapping (continued)

PIN	PERIPHERAL	SIGNAL	ROUTE TO	POWER GROUP	DIRECTION
C24	ELCDIF	lcd_data, 15	LCD1_DATA15	NVCC_LCD (0V)	Input/Output
B25	ELCDIF	lcd_data, 16	LCD1_DATA16	NVCC_LCD (0V)	Input/Output
G21	ELCDIF	lcd_data, 17	LCD1_DATA17	NVCC_LCD (0V)	Input/Output
E23	ELCDIF	lcd_data, 18	LCD1_DATA18	NVCC_LCD (0V)	Input/Output
D24	ELCDIF	lcd_data, 19	LCD1_DATA19	NVCC_LCD (0V)	Input/Output
C25	ELCDIF	lcd_data, 20	LCD1_DATA20	NVCC_LCD (0V)	Input/Output
E24	ELCDIF	lcd_data, 21	LCD1_DATA21	NVCC_LCD (0V)	Input/Output
D25	ELCDIF	lcd_data, 22	LCD1_DATA22	NVCC_LCD (0V)	Input/Output
G23	ELCDIF	lcd_data, 23	LCD1_DATA23	NVCC_LCD (0V)	Input/Output
E3	uSDHC2	sd_clk	SD2_CLK	NVCC_SD2 (0V)	Output
F6	uSDHC2	sd_cmd	SD2_CMD	NVCC_SD2 (0V)	Input/Output
E4	uSDHC2	sd_data, 0	SD2_DATA0	NVCC_SD2 (0V)	Input/Output
E5	uSDHC2	sd_data, 1	SD2_DATA1	NVCC_SD2 (0V)	Input/Output
F5	uSDHC2	sd_data, 2	SD2_DATA2	NVCC_SD2 (0V)	Input/Output
E6	uSDHC2	sd_data, 3	SD2_DATA3	NVCC_SD2 (0V)	Input/Output
D3	uSDHC2	sd_cd_b	SD2_CD_B	NVCC_SD2 (0V)	Input
C1	uSDHC3	sd_clk	SD3_CLK	NVCC_SD3 (0V)	Output
E1	uSDHC3	sd_cmd	SD3_CMD	NVCC_SD3 (0V)	Input/Output
B2	uSDHC3	sd_data, 0	SD3_DATA0	NVCC_SD3 (0V)	Input/Output
A2	uSDHC3	sd_data, 1	SD3_DATA1	NVCC_SD3 (0V)	Input/Output
G2	uSDHC3	sd_data, 2	SD3_DATA2	NVCC_SD3 (0V)	Input/Output
F1	uSDHC3	sd_data, 3	SD3_DATA3	NVCC_SD3 (0V)	Input/Output
F2	uSDHC3	sd_data, 4	SD3_DATA4	NVCC_SD3 (0V)	Input/Output
E2	uSDHC3	sd_data, 5	SD3_DATA5	NVCC_SD3 (0V)	Input/Output
C2	uSDHC3	sd_data, 6	SD3_DATA6	NVCC_SD3 (0V)	Input/Output
B1	uSDHC3	sd_data, 7	SD3_DATA7	NVCC_SD3 (0V)	Input/Output
J1	uSDHC3	sd_strobe	SD3_STROBE	NVCC_SD3 (0V)	Output
G1	uSDHC3	sd_reset_b	SD3_RESET_B	NVCC_SD3 (0V)	Output
K24	GPIO2	gpio_io, 28	EPDC1_BDR0	NVCC_EPDC2 (0V)	Not Specified
D15	SAI1	sai_tx_bclk	ENET1_RX_CLK	NVCC_ENET1 (0V)	Output
D16	SAI1	sai_rx_data	ENET1_TX_CLK	NVCC_ENET1 (0V)	Input
D19	SAI1	sai_tx_data	ENET1_COL	NVCC_ENET1 (0V)	Output
E19	SAI1	sai_tx_sync	ENET1_CRS	NVCC_ENET1 (0V)	Input/Output
E10	SAI1	sai_mclk	SAI1_MCLK	NVCC_SAI (0V)	Output
J2	I2C1	i2c_scl	I2C1_SCL	NVCC_I2C (0V)	Input/Output
K1	I2C1	i2c_sda	I2C1_SDA	NVCC_I2C (0V)	Input/Output
K2	I2C2	i2c_scl	I2C2_SCL	NVCC_I2C (0V)	Input/Output
K3	I2C2	i2c_sda	I2C2_SDA	NVCC_I2C (0V)	Input/Output
K5	I2C3	i2c_scl	I2C3_SCL	NVCC_I2C (0V)	Input/Output
K6	I2C3	i2c_sda	I2C3_SDA	NVCC_I2C (0V)	Input/Output
B8	USB	usb_otg1_dp	USB_OTG1_DP	USB_OTG1_VDDA_3P3 (0V)	Input/Output
A8	USB	usb_otg1_dn	USB_OTG1_DN	USB_OTG1_VDDA_3P3 (0V)	Input/Output
B7	USB	usb_otg1_id	USB_OTG1_ID	USB_OTG1_VDDA_3P3 (0V)	Input
C7	USB	usb_otg1_chd_b	USB_OTG1_CHD_B	USB_OTG1_VDDA_3P3 (0V)	Input/Output
A7	USB	usb_otg1_rext	USB_OTG1_REXT	USB_OTG1_VDDA_3P3 (0V)	Input/Output
B10	USB	usb_otg2_dp	USB_OTG2_DP	USB_OTG2_VDDA_3P3 (0V)	Input/Output
A10	USB	usb_otg2_dn	USB_OTG2_DN	USB_OTG2_VDDA_3P3 (0V)	Input/Output

表 8. i.MX 7D Pin Mapping (continued)

PIN	PERIPHERAL	SIGNAL	ROUTE TO	POWER GROUP	DIRECTION
B11	USB	usb_otg2_id	USB_OTG2_ID	USB_OTG2_VDDA_3P3 (0V)	Input
A11	USB	usb_otg2_rext	USB_OTG2_REXT	USB_OTG2_VDDA_3P3 (0V)	Input/Output
A12	USB	usb_h_data	USB_H_DATA	USB_H_VDD_1P2 (0V)	Input/Output
B12	USB	usb_h_strobe	USB_H_STROBE	USB_H_VDD_1P2 (0V)	Input/Output
T6	FLEXCAN2	flexcan_tx	GPIO1_IO15	NVCC_GPIO2 (0V)	Output
T5	FLEXCAN2	flexcan_rx	GPIO1_IO14	NVCC_GPIO2 (0V)	Input
L20	GPIO2	gpio_io, 14	EPDC1_DATA14	NVCC_EPDC1 (0V)	Not Specified
P20	QSPI	qspi_a_data, 0	EPDC1_DATA00	NVCC_EPDC1 (0V)	Input/Output
AC10	PCIE	pcie_refclkout_n	PCIE_REFCLKOUT_N	PCIE_VPH (0V)	Output
AB10	PCIE	pcie_refclkout_p	PCIE_REFCLKOUT_P	PCIE_VPH (0V)	Output
AD10	PCIE	pcie_refclkin_p	PCIE_REFCLKIN_P	PCIE_VPH (0V)	Input
AE10	PCIE	pcie_refclkin_n	PCIE_REFCLKIN_N	PCIE_VPH (0V)	Input
AD11	PCIE	pcie_rx_p	PCIE_RX_P	PCIE_VPH_RX (0V)	Input
AE11	PCIE	pcie_rx_n	PCIE_RX_N	PCIE_VPH_RX (0V)	Input
AB11	PCIE	pcie_tx_p	PCIE_TX_P	PCIE_VPH_TX (0V)	Output
AC11	PCIE	pcie_tx_n	PCIE_TX_N	PCIE_VPH_TX (0V)	Output
AA13	PCIE	pcie_rext	PCIE_REXT	PCIE_VPH (0V)	Input/Output
B15	MIPI_CSI2	mipi_csi_clk_p	MIPI_CSI_CLK_P	MIPI_VDDA_1P8 (0V)	Input/Output
A15	MIPI_CSI2	mipi_csi_clk_n	MIPI_CSI_CLK_N	MIPI_VDDA_1P8 (0V)	Input/Output
B16	MIPI_CSI2	mipi_csi_d0_p	MIPI_CSI_D0_P	MIPI_VDDA_1P8 (0V)	Input/Output
A16	MIPI_CSI2	mipi_csi_d0_n	MIPI_CSI_D0_N	MIPI_VDDA_1P8 (0V)	Input/Output
B14	MIPI_CSI2	mipi_csi_d1_p	MIPI_CSI_D1_P	MIPI_VDDA_1P8 (0V)	Input/Output
A14	MIPI_CSI2	mipi_csi_d1_n	MIPI_CSI_D1_N	MIPI_VDDA_1P8 (0V)	Input/Output
AE6	XTALOSC	rtc_xtali	RTC_XTALI	VDD_SNVS_1P8_CAP (0V)	Input
AD6	XTALOSC	rtc_xtalo	RTC_XTALO	VDD_SNVS_1P8_CAP (0V)	Output
V1	XTALOSC	xtali	XTALI	VDDA_1P8 (0V)	Input
V2	XTALOSC	xtalo	XTALO	VDDA_1P8 (0V)	Output
AC8	XTALOSC	onoff	ONOFF	VDD_SNVS_IN (0V)	Input
AE4	TEMPSENSOR	rext	TEMPSENSOR_REXT	VDD_TEMPSENSOR_1P8 (0V)	Input
D12	I2C4	i2c_sda	SAI1_RXC	NVCC_SAI (0V)	Input/Output
C12	I2C4	i2c_scl	SAI1_RXFS	NVCC_SAI (0V)	Input/Output
G3	GPIO5	gpio_io, 11	SD2_RESET_B	NVCC_SD2 (0V)	Not Specified
C3	GPIO5	gpio_io, 10	SD2_WP	NVCC_SD2 (0V)	Not Specified
N1	GPIO1	gpio_io, 00	GPIO1_IO00	NVCC_GPIO1 (0V)	Not Specified
N2	GPIO1	gpio_io, 01	GPIO1_IO01	NVCC_GPIO1 (0V)	Not Specified
N3	GPIO1	gpio_io, 02	GPIO1_IO02	NVCC_GPIO1 (0V)	Not Specified
J6	GPIO4	gpio_io, 23	ECSPI2_SS0	NVCC_SPI (0V)	Not Specified
G6	GPIO4	gpio_io, 21	ECSPI2_MOSI	NVCC_SPI (0V)	Not Specified

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265