参考資料

デザイン・ガイド：TIDA-00300
通信およびアナログ I/O モジュール用絶縁型電源アーキテクチャのリファレンス・デザイン

概要

このリファレンス・デザインでは、各種保護リレー・モジュール用絶縁型電源を生成する複数の方法を説明します。アナログ入力、バイナリ入力、通信モジュール用の絶縁型電源は、LDO に接続するための出力ヘッドルームと構成可能な出力を備えた絶縁型 DC/DC コンバータを使用して生成します。またこのリファレンス・デザインでは、電源レギュレーション用の LDO、電圧検出器を使用した DC 電圧状態の監視、負荷スイッチを使用した入出力過負荷保護についても紹介します。

リソース

TIDA-00300	デザイン・フォルダ
UCC12050、TPS782、TPS760、TLV713	プロダクト・フォルダ
SN6505B、SN6501、TPS709、TPS61220	プロダクト・フォルダ
ISOW7841、TPS763、TPS22944、TLV3012	プロダクト・フォルダ
REF3025、LM5017、TPS7A47、TPS7A16	プロダクト・フォルダ
ISO7741、ISO1541、TPS55010、TVS3300	プロダクト・フォルダ
DCH010515D、DCH010505S、REF3425	プロダクト・フォルダ

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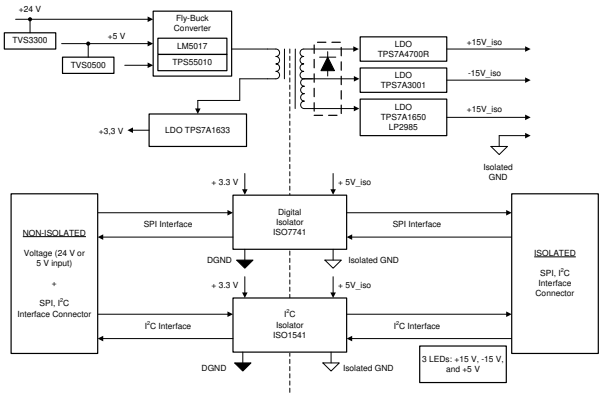
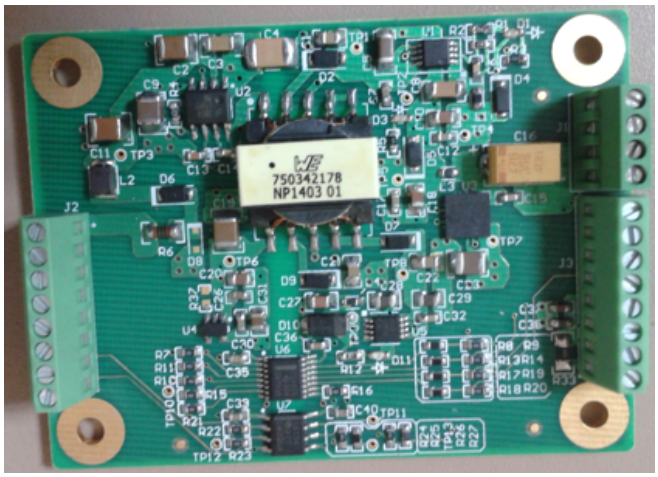
特長

- トランス・ドライバ、パワー・モジュール、絶縁型 DC/DC を使用して、アナログ入力、バイナリ入力、通信モジュール用の絶縁型電源を生成する複数の方法
- 絶縁型 DC/DC コンバータを使用することで簡単なシステム設計、柔軟な出力構成、高い信頼性を実現
- DC/DC コンバータと LDO を使用した分割レール電源、Fly-Buck™コンバータ、分割レール DC/DC、LDO を含む、アナログ入出力モジュール用絶縁型電源を生成する複数の方法
- デジタル・アイソレータを使用した同期整流 SPI インターフェイスと、双方向 SDA と単方向 SCL を備えたデジタル・アイソレータを使用した I^2C インターフェイス
- 基板は、TIDA-00227 デザインに接続することで EMI/EMC プリコンプライアンス要件を満たすことをテスト済み

アプリケーション

- AC アナログ入力モジュール
- 通信モジュール
- マルチファンクション・リレー





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TIDU562 翻訳版 — 最新の英語版資料 http://www-s.ti.com/sc/techlit/TIDU562

1 リソース (続き)

TLV742P、TLV704、TPS22960、SN74LVC1G14	プロダクト・フォルダ
TPS62821、DCR010505、LP2985-N、TPS3897	プロダクト・フォルダ
TPS3895、TPS7A39、DCP010505B、TPS7A3001-EP	プロダクト・フォルダ
LM5160、TPS65130、LM27762、REF3025	プロダクト・フォルダ
OPA2376、REF5025、LM4040、TPS22917	プロダクト・フォルダ

2 System Description

2.1 Need for Isolation

Industrial electronic equipment commonly uses galvanic isolators to protect systems and users from potentially hazardous voltages. Industrial equipment must operate reliably in the harshest environments, where strong electromagnetic fields, surges, fast transients, and high noise floors are normal. This environment presents challenges for designing reliable isolation circuits that deliver error-free operation over long equipment lifetimes. Over many decades, optocouplers have been the default signal isolation device, but recent breakthroughs in silicon isolation technology have spawned smaller, faster, and more reliable and cost-effective solutions that have already begun supplanting optocouplers in many end applications.

Benefits of Digital Isolators

- Higher integration: smaller size and lower cost per channel on multi-channel versions
- Higher performance: faster, tighter timing, and substantially lower power
- Longer service life: no wear-out mechanisms as in optocouplers
- Higher reliability: operating parameters remain stable over VDD, temperature, and device age
- High CMTI: an isolation signal path that is fully differential and a high receiver selectivity for CMTI greater than 15 kV/μs
- Low EMI
- High electric-field immunity: >20 V/m, as measured by independent laboratories
- Industry-leading ESD tolerance: 3-kV HBM on all devices
- Lower external bill-of-materials
- Easy to use: single-chip, complete isolation solution

2.2 I/Os in Smart Grid

A number of IEDs or protection relays are used in smart grid and protection systems. These IEDs and protection relays have following I/Os:

- RTD inputs
- DC voltage transducers (0 to 10 V)
- DC current transducers (4 to 20 mA)
- Binary inputs and outputs

The number of inputs vary depending on the application. If the application requires more I/Os and protection relay has a limited number of I/Os, external expansion modules are used to increase the number of I/Os.

Isolation In Smart Grid

The previously-described external expansion modules are standalone devices that sense any of the listed inputs and provide the information to the IED and protection relay through RS-485 communication. These expansion devices need the following isolation:

- Communication
- Power supply, as they are operated from an auxiliary DC input
- Isolation for the previously mentioned I/Os

The required number of I/Os also varies with application and vary from 8 to 16. To control each I/O, an individual isolated channel is required. Alternative to isolating individual channel is to use serial communication with expansion options on the non-isolated side. I2C, a 2-wire communication technology, is commonly used for such applications. Many I2C expanders are available as part of the TI expander portfolio for this kind of application.

I2C is a simple, low-bandwidth, short-distance protocol. Most available I2C devices operate at speeds up to 400 Kbps, with some venturing up into the low megahertz range. I2C can easily link multiple devices together because it has a built-in addressing scheme.

I2C advantages are:

- Requires only two bus lines (SDA and SCL)
- No strict baud rate requirements, the master generates a bus clock
- Simple master/slave relationships between all components
- Each device connected to the bus is software-addressable by a unique address
- A true multi-master bus providing arbitration and collision detection

Analog inputs are interfaced with analog-to-digital converters (ADCs), and analog outputs are generated through digital-to-analog converters (DACs). Most of the ADCs and DACs are available with SPI.

SPIs can daisy chain multiple devices. An advantage of daisy chaining is the reduced requirement for number of chip selects. Many SPI-based ADCs and DACs are available as part of TI's portfolio.

In most applications, these modules work on auxiliary supply. The available auxiliary input for smart grid applications is 24 V. For safety reasons, isolate the auxiliary modules. To generate the required supply voltages, a switching regulator is used. When digital isolators are used to isolate SPI and I2C as previously described, an isolated and a non-isolated supply are required to function.

To generate both the isolated and non-isolated supply, a synchronous buck regulator with Fly-Buck topology can be used. The Fly-Buck topology can generated both isolated and non-isolated voltages with good regulation.

The ADC and DAC require different supply voltages to operate. Most common supply voltages used are ±15 V, 5 V, 3.3 V. The output of the Fly-Buck is an unregulated output. LDOs are used to regulate voltages to the required levels.

An isolated buck converter (Fly-Buck) uses a synchronous buck converter with coupled inductor windings to create isolated outputs. Isolated converters utilizing Fly-Buck topology use a smaller transformer for an equivalent power transfer as the transformer primary and secondary turns ratios are better matched. An optocoupler or auxiliary winding is not needed as the secondary output closely tracks the primary output voltage, resulting in a smaller solution size and cost.

2.3 Isolation Types

The signal isolation can be achieved by:

- Optical coupling: The transmission of light across a transparent nonconductive barrier, such as an air gap, to achieve isolation. The main benefits of optical coupling (optocoupling) are that light is inherently immune to external electric or magnetic fields, and optical coupling allows for transfer of steady-state information. The disadvantages of optocouplers include speed limitations, power dissipation, and the degradation of the LED. The advantage of inductive coupling is the possible difference in common-mode and differential transfer characteristics
- Inductive coupling: Uses a changing magnetic field between two coils to communicate across an isolation barrier. The most common example is the transformer where the strength of the magnetic field depends on the coil structure (number of turns/unit length) of the primary and secondary windings, the permittivity of the magnetic core, and the current magnitude.
- Capacitive coupling: Uses a changing electric field to transmit information across the isolation barrier. The material between the capacitor plates is a dielectric insulator and forms the isolation barrier. The plate size, the distance between the plates, and the dielectric material determine the electrical properties. The benefits of using a capacitive isolation barrier are efficiency, in both size and energy transfer, and immunity to magnetic fields.

2.4 Digital Isolator

Digital isolators use innovative circuitry to isolate standard digital signals at signaling rates of DC to over 100 Mbps. The TI family of isolators use capacitive coupling. The capacitive coupling solution uses proven and cost-effective manufacturing processes and provides an inherent immunity to magnetic fields.

Device Selection

System performance requirements have the most impact on the selection of an isolation device. Other considerations include space constraints and cost.

Data Rate Requirements

System data rate requirements are likely to be the single most important parameter for device selection. If a system uses high data rates, such as the high speed PROFIBUS protocol, the minimum data rate speed requirement of 9.6 Mbps narrows the device selection to the high performance products available. Conversely, if the RS-485 network runs at much lower data rate speeds, the possible device selection options widens.

Device costs typically rise in proportion to data rate performance. Therefore, a designer must take care not to specify a device with more performance than is required. However, low performance device selection can make future system performance upgrades more costly and involved, because all devices not compatible with upgraded system data speeds require replacement.

Space Requirements

Space constraints are a second area of concern that can also limit a designer’s choices. Maximum dimension requirements are a concern for virtually all applications. However, some implementations can be severely space-limited. Fortunately, there are solutions for these situations.

Cost Requirements

Cost constraints and concerns are a reality in virtually all system design work, and therefore must be considered. Cost considerations can have an effect on the design choices for a system. As noted previously, isolator device cost rises in proportion with data rate performance. Specifying a device with only the system performance required can reduce costs. Other cost issues include a consideration of the number of devices used.

Additional cost benefits of integrating as many channels into one device include reduction in board space and assembly costs. A lower device count results in smaller boards. Also, lower device count typically results in a less complex board layout. The combination of smaller boards and less complex layout reduces board costs. In addition, circuit board assembly costs typically decrease proportionally as the number of devices required for the board assembly process decreases. Therefore, designing with fewer devices results in lower manufacturing costs.

表 1. Comparison of Different Signal Isolation Techniques

PARAMETER	OPTO	MAGNETIC	CAPACITIVE
Sampling rate (Mbps)	50	150	150
Propagation delay time (ns)	20	32	12
Pulse width distortion (ns)	2	2	1.5
Channel-to-channel skew (ns)	16	2.0	1.6
Part-to-part skew (ns)	20	10	2
ESD on all pins (kV)	±2	±2	±4
CM transient immunity (kV/µs)	20	25	25
Temperature (°C)	–45 to 125	–40 to 125	–55 to 125
MTTF at 125°C, 90% confidence	8	1746	2255
FIT at 125°C, 90% confidence	14391	65	50
Magnetic immunity at 1 kHz (Wb/m^2)	—	10^2	10^8
Radiated electromagnetic field immunity			
IEC61000-4-3 (80 to 1000 MHz)	—	Fails	Complies
MIL-STD 461E RS-103 (30 to 1000 MHz)	—	Fails	Complies
High-voltage lifetime expectancy (years)	<5	<10	>28

2.5 Isolation Communication Module

TI has a large portfolio of isolators that gives flexibility to select the isolator based on some of the previously mentioned selection criteria.

This design guide demonstrates using TI devices for the following applications:

- Isolation of I2C interface
- Isolation of SPI
- Power Supply Isolation
- LDOs to regulate the supply voltages

TI has a large portfolio of isolation devices for power and signal isolation. TI also has a large portfolio of linear dropout regulators. All the relevant design files like schematics, BOM, layer plots, Altium files, and Gerber files have also been provided to the user (see 10).

The following care has to be taken while using this design:

- Power Supply outputs: The power supply outputs are not protected. A suitable SMD fuse can be used based on the application need. This design provides options to mount the SMD fuse.
- Surge protection: This reference design is a sub-system and is expected to be an integral part of expansion module. So, no surge protection is provided.
- A high-voltage isolation test has not been performed. All the devices and PCB design are done considering the required isolation.

2.6 Isolated DC-DC Converter UCC12050 Advantages

Some of the advantages of using an isolated DC/DC converter include:

- Fully integrated high-efficiency isolated DC-DC converter
- Regulated 5.0-V or 3.3-V output with selectable 400-mV headroom voltage to power an LDO
- Extended ambient temperature range: –40ºC to +125ºC
- Short circuit tolerant and provides thermal shutdown
- Extended ambient temperature range: –40ºC to +125ºC

  The UCC12050 provides extra features such as an enable pin, synchronization of switching frequency among multiple devices, and selection of isolated output voltages.

3 Design Features

The primary objective is to create a reference design platform to showcase different approaches to generation of isolated power-supply rails including a split-rail supply required for communication, analog input, and analog output modules from 24-V or 5-V DC input using a DC/DC converter with integrated FET, split-rail DC/DC converter, isolated power module, and transformer driver. The design additionally features generation of a stable reference using low drift references, diagnostics of input voltage, synchronous communication using digital isolators, and input protection using load switches. 表 2 lists the typical requirements:

表 2. System Specifications for TIDA-00300

PART NUMBER	NAME	DESCRIPTION
1	SPI interface	4-wire , up to 4Mbps
2	I2C interface	Bidirectional data , unidirectional clock , up to 100 Kbps
3	Fly-Buck converter Output voltages	Isolated: > 18 V, < –18 V, > 7 V Non-isolated > 9 V
4	Input voltage, connection	24-V DC nominal input, screw-type terminal
5	Regulators (LDOs)	Isolated: 15 V, –15 V, 5 V; Non-isolated: 3.3 V
6	Protection	Undervoltage lockout for Fly-Buck converter Supply input reversal
7	Host input connection	8-pin screw type terminal block
8	Output connection	8-pin screw type terminal block for signal 4-pin screw type terminal block for power
9	Indication	LED indications for 15-V, –15-V, and 5-V isolated power supplies
10	Generation of isolated supplies using DC/DC power module	±15 V , 6 V, 5 V , 3.3 V
11	Generation of isolated supplies using transformer driver and LDO	±13 V , ±12 V, 6 V, 5 V, 3.3 V
12	Generation of isolated supplies using isolated DC/DC with configurable outputs	5.4 V, 5 V , 3.7 V, 3.3 V
13	Generation of isolated supplies using digital isolator with integrated power	5.4 V, 5 V , 3.3 V
14	Generation of split-rail supplies using isolated DC/DC converter with integrated FETS	±15 V, 5 V
15	Generation of isolated split rail using wide input synchronous buck, Fly-Buck converter	±18 V, ±15 V, 5 V
16	Generation of stable reference output using series or shunt reference	2.5 V

4 TI Device Mapping to Reference Design Functionalities

This section provides details of device mapping to functionalities for the following boards:

- Isolated power supply for communication module
- Isolated power supply for analog IO module
- Isolated synchronous communication with split-rail power supplies

4.1 Isolated Power Supply for Communication Module

表 3 provides details of the TI devices and functionalities implemented in this reference design for generating isolated power supplies for the communication module.

表 3. Details of Functions and Devices Used for Implementing Power Supplies for Communication Module

FUNCTION	DEVICES	DESCRIPTION
Isolated 5-V and 3.3-V supply generation using power module	DCR010505P, DCP010505BP, LP2985AIM5-3.3, TPS78233	Generation of isolated, regulated and unregulated DC supply using isolated DC/DC converter modules and LDOs
Isolated 5-V, 3.3-V, and ±12-V supply generation using transformer driver	SN6505B, SN6501, TPS70933, TPS76050, TPS7A3901	Generation of isolated supply including split-rail power supply for analog input module using transformer driver and LDOs
Isolated 5.4-V, 5-V, and 3.3-V supply using digital isolator with integrated power	ISOW7841, TPS22944, TPS61220, TPS76350, TPS62821	Generation of isolated using digital isolator with integrated power, DC/DC converter to boost the output and LDOs to regulate the output
Generation of regulated DC supplies with diagnostics	UCC12050, SN74LVC1G14, SN74LVC1G14, CSD17571Q2, TPS22960, TLV74233, TLV70450, TLV71333, TPS3897, SN74LVC1G17	Generation of isolated power supplies with configurable output and regulating the output using LDOs including 5-V and 3.3-V output with input overload protection, voltage level detection and voltage status indication

4.2 Wide Input Isolated Power Supply for Analog IO Modules

表 4 provides details of the TI devices and functionalities implemented in this reference design for generating isolated power supplies for analog IO modules.

表 4. Details of Functions and Devices Used for Implementing Power Supply for Analog IO Modules

FUNCTION	DEVICES	DESCRIPTION
Generation of isolated 5 V and ±15 V using DC/DC, split-rail DC/DC, and power module	TVS3300, LM5160, TVS0500, TPS22917, SN6505B, TPS2400, DCH010515D, DCH010505S, TPS65130	Generation of split-rail power supply for analog input and analog output from 24-V or 5-V DC input with input protection
Generation of regulated 3.3 V, ±5 V and ±12 V using LDOs	LM27762, TPS7A3901, TLV70433, TVS1400	Generation of regulated split-rail supplies from unregulated split-rail supplies
Generation of stable reference	REF5025, REF3025A, REF3425, OPA2376, LM4040AIM3-2.5	Generation of stable reference using series or shunt reference

4.3 Isolated Synchronous Communication With Split-Rail Power Supplies

表 5 provides details of the TI devices and functionalities implemented in this reference design for generating isolated power supplies for analog IO module and isolated synchronous communication.

表 5. Details of Functions and Devices Used for Implementing Power Supply and Synchronous Communication

FUNCTION	DEVICES	DESCRIPTION
Generation of 5 V and ±15 V from 24-V input using DC/DC	TVS3300, LM5017, TPS70933, TPS7A4700, TPS7A3001, TPS7A1650	Generation of split-rail power supply output from 12- or 24-V input using isolated DC/DC converter with integrated switch
Generation of 5 V and ±15 V from 5-V input using DC/DC	TPS55010, TVS0500, LP2985-	Generation of split-rail power supply output from a 5-V input using isolated DC/DC converter with integrated switch
Isolated SPI interface	ISO7741, ISO7141	Digital isolator with basic or reinforced isolation to implement SPI with varying speed
Isolated I2C interface	ISO1541D	Digital isolators to implement I2C interface with varying speed

5 System Overview

Some of the key requirements for designing the isolated power architecture for protection relay modules include:

1. Generation of isolated 5 V or 3.3 V with output headroom allowing usage of LDOs for applications in an analog input module or communication module
2. Generation of the required supply rails (5 V to ±14 V, ±14 V to ±12 V, 5 V to ±5 V for analog IO and 5 V and 3.3 V for communication) with high efficiency and scalable load current using 5-V, 12-V, or 24-V input
3. Operation of the supply over wide range for applications using external auxiliary supply
4. Generation of isolated power supplies with high efficiency
5. Generation of stable reference (Series or Shunt) with buffer and low temperature drift
6. Isolation of SPI signals with varying speed and low current consumption
7. Isolation of I2C interface signals with varying speed
8. Generation of isolated power supplies with low EMI for ease of design
9. Diagnostics including LEDs and voltage detection

The TIDA-00300 reference design provides solutions to the previous requirements and also solves some of the design challenges associated with the design of isolated power architecture for protection relay modules.

5.1 Block Diagram

Block diagram for the boards used for generating power supplies used for isolated communication and isolated IO modules are discussed in this section.

5.1.1 Isolated Power Supply for Communication Module

図 1 shows multiple approaches to generation of isolated power supply for low-speed wired communication modules.

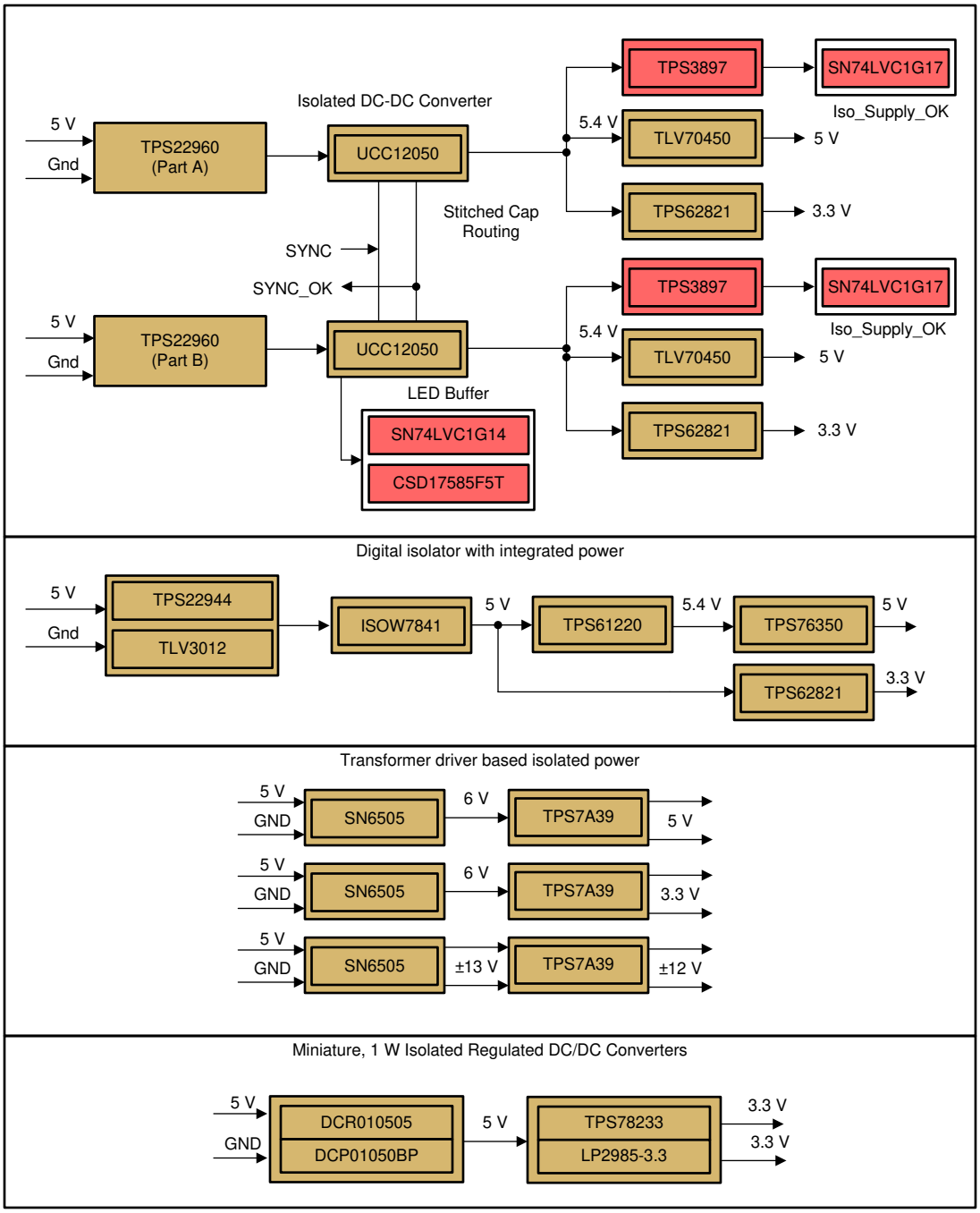

図 1. Isolated Power Supply Architecture for Communication Modules

5.1.1.1 Generation of Isolated 5-V, 5.4-V, 3.3-V, or 3.7-V Supply Using Isolated DC/DC With Protection and Diagnostics

This design has the following functionality:

- Configuration of output voltage using output select pin and resistors
- Generation of regulated 5-V and 3.3-V supplies
- Protection of 5-V input using a load switch
- Voltage detector to indicate the isolated supply status

5.1.1.2 Isolated 5-V and 3.3-V Supply Generation Using Power Module

This design has the following functionality:

- Generation of 5-V DC power supply from 5-V input using an unregulated power module
- Generation of 5-V DC power supply from 5-V input using a regulated power module
- Generation of regulated 3.3-V output using LDO

5.1.1.3 Isolated 5-V, 3.3-V and ±12-V Supply Generation Using Transformer Driver

This design has the following functionality:

- Generation of isolated 3.3 V or 5 V from 5-V input using a transformer driver
- Generation of split-rail ±12-V supply from 5-V input using a transformer driver

5.1.1.4 Isolated 5.4-V, 5-V and 3.3-V Supply Using Digital Isolator With Integrated Power

This design has the following functionality:

- Generation of isolated 5 V from 5-V input using digital isolators with integrated power
- Generation of isolated 5.4 V, regulated 5 V, 3.3 V from 5 V

5.1.2 Wide Input Isolated Power Supply for Analog IO Modules

図 2 shows multiple approaches to generation of isolated power supply for analog input/output modules.

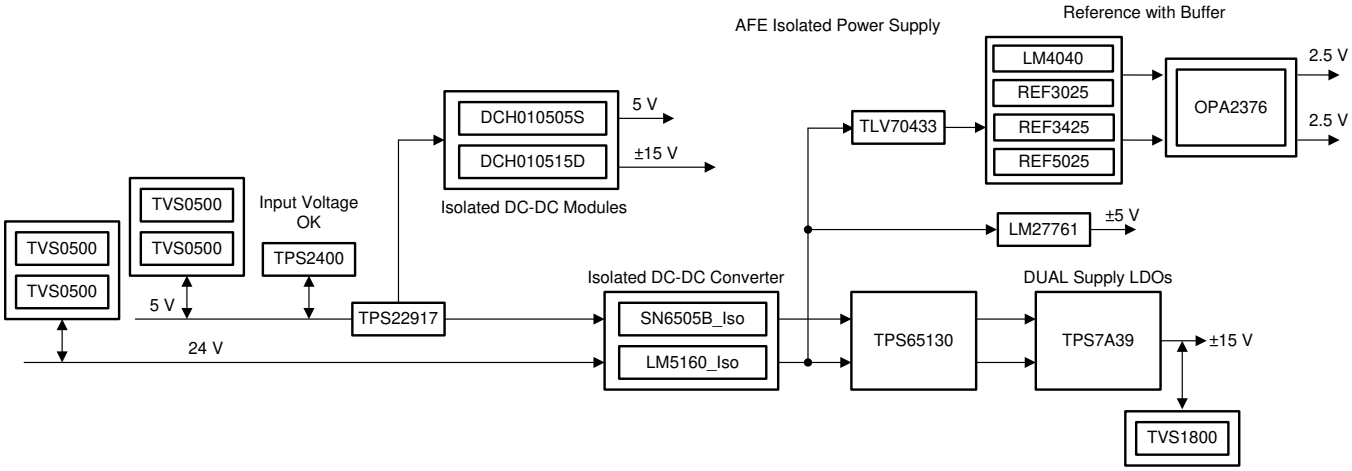

図 2. Wide Input Isolated Power Supply Architecture for Analog IO Modules

5.1.2.1 Generation of Isolated 5 V and ±15 V With Protection

This design has the following functionality:

- Generation of isolated split-rail supplies using DC/DC converter with integrated switch from 24-V input
- Generation of isolated split-rail supplies using isolated power module from 5-V input
- Input protection against overload using a load switch
- Input protection against transients using a flat clamp TVS

5.1.2.2 Generation of Regulated 3.3-V, ±5-V and ±12-V Supplies Using LDOs

This design has the following functionality:

- Generation of regulated split-rail supply using a dual LDO
- Generation of 5 V and 3.3 V using LDOs

5.1.2.3 Generation of Stable Reference

This design has the following functionality:

- Generation of stable reference using shunt reference with buffer
- Generation of stable reference using series reference with buffer

5.1.3 Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power

図 3 shows multiple approaches to the generation of isolated power supply for synchronous communication and analog IO modules with protection.

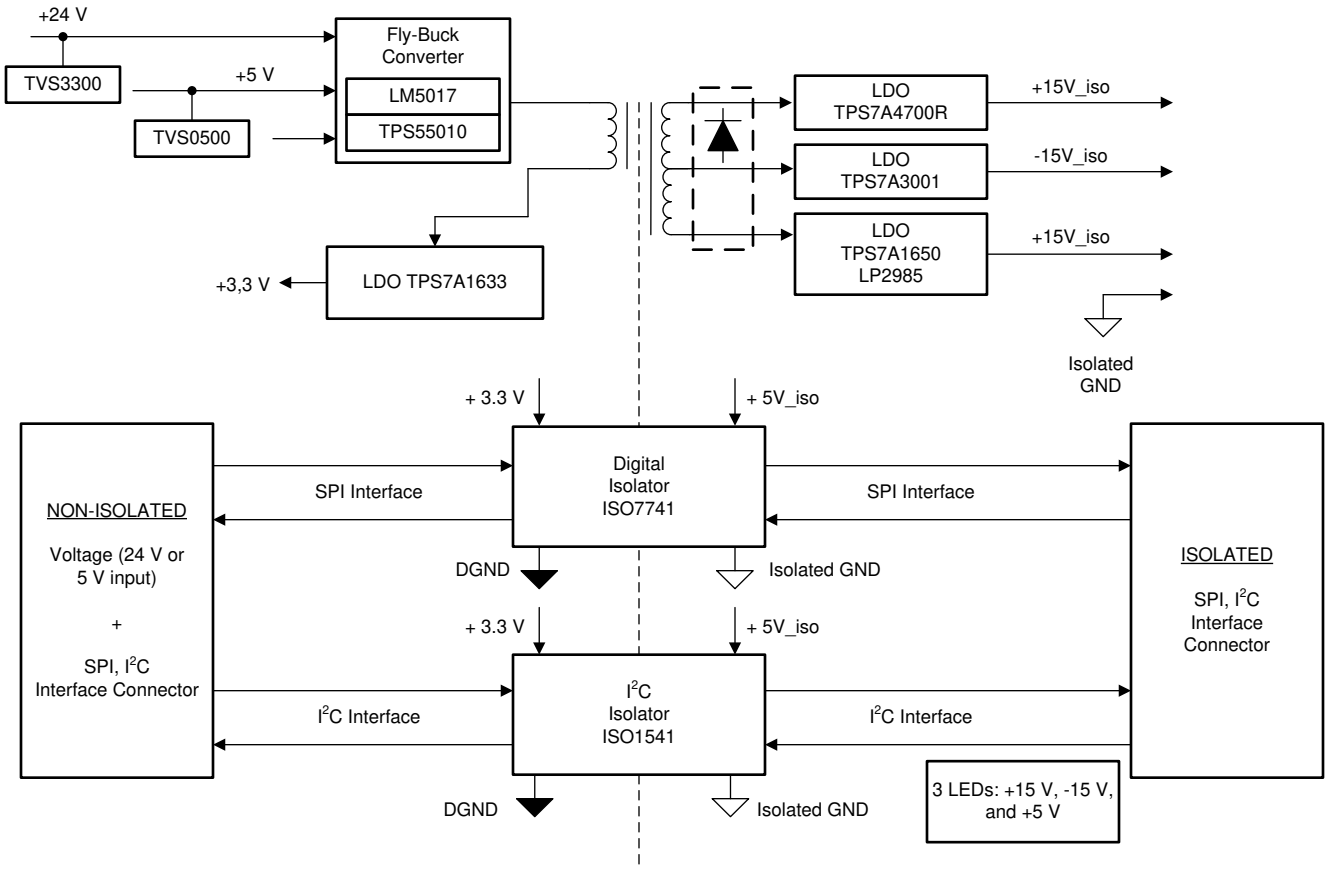

図 3. Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power

5.1.3.1 Generation of 5 V and ±15 V from 24 V

This design showcases the following:

- Generation of split-rail supply from 24-V input using a DC/DC converter
- Generation of regulated split-rail supply using LDOs
- Input transient protection using a flat clamp TVS

5.1.3.2 Generation of 5 V and ±15 V from 5-V input

This design has the following functionality:

- Generation of split-rail supply from 5-V input using a DC/DC converter
- Generation of 5 V using LDO
- Input transient protection using flat clamp

5.1.3.3 Isolated Synchronous Interface

This design has the following functionality:

- SPI using digital isolator
- I2C interface using digital isolators

5.2 Highlighted Products

This section provides details of some of the focus TI products used in this reference design for generation of required power supplies for protection relay modules.

5.2.1 Isolated Power Supply for Communication Module

This section provides details of the devices used to generate the required isolated power supplies for the communication module:

5.2.1.1 Generation of Isolated 5-V, 5.4-V, 3.3-V, or 3.7-V Supply Using Isolated DC/DC With Protection and Diagnostics

This design has the following functionality:

- UCC12050, 500-mW, high-efficiency, 5-kVRMS isolated DC-DC converter
- TPS22960, 5.5-V, 0.5-A, 435-mΩ, 2-channel load switch with quick output discharge
- TLV74233, 200-mA small-size low-dropout (LDO) linear voltage regulator
- TLV70450, 24-V input voltage, 150-mA, ultra-low I_Q low-dropout (LDO) regulators
- TLV713, 150-mA low-dropout (LDO) regulator with fold-back current limit for portable devices
- TPS3897, single-channel ultra-small adjustable supervisory circuit with active-high, open-drain output
- SN74LVC1G14, single Schmitt-trigger inverter
- SN74LVC1G17, single Schmitt-trigger buffer
- CSD17571Q2, 30-V N-channel NexFET™ power MOSFETs

5.2.1.2 Isolated 5-V and 3.3-V Supply Generation Using Power Module

This design has the following functionality:

- DCR010505P, miniature, 1-W isolated unregulated DC/DC converters

- DCP010505BP, miniature, 1-W isolated unregulated DC/DC converters in a PDIP package
- LP2985AIM5-3.3, 150-mA low-noise low-dropout regulator with shutdown
- TPS78233, 3.3-V, 150-mA, ultra-low quiescent current (500 nA) low-dropout linear regulator

5.2.1.3 Isolated 5-V, 3.3-V and ±12-V Supply Generation Using Transformer Driver

This design has the following functionality:

- SN6505B, low-noise 1-A, 420-kHz transformer driver for isolated power supplies
- SN6501, low-noise, 350-mA, 410-kHz transformer driver for isolated power supplies
- TPS70933, 3.3-V, 150-mA 30-V ultra-low I_Q wide-input low-dropout (LDO) regulator with reverse current protection
- TPS76050, 5-V output, 16-V, 50-mA, low I_Q, low-dropout linear regulator
- TPS7A3901, dual, 150-mA, wide-V_{IN}, positive and negative low-dropout (LDO) voltage regulator

5.2.1.4 Isolated 5.4-V, 5-V, and 3.3-V Supply Using Digital Isolator With Integrated Power

This design has the following functionality:

- TPS22944, 5.5-V, 0.2-A, 500-mΩ, 100-mA current-limit load switch
- ISOW7841, high-efficiency, low-emissions, reinforced digital isolator with integrated power
- TPS61220, low input voltage, 0.7-V boost converter with 5.5-μA quiescent current
- TPS76350, low I_Q, 150-mA, low-dropout linear regulators
- TPS62821, 1-A step-down converter with 1% accuracy

5.2.2 Wide Input Isolated Power Supply for Analog IO Modules

This section provides details of the devices and configurations used to generate the required isolated power supplies for an analog IO module.

5.2.2.1 Generation of Isolated 5-V and ±15-V With Protection

This design has the following functionality:

- LM5160, wide input 65-V, 2-A synchronous buck or Fly-Buck converter
- TPS22917, ultra-low leakage, 5.5-V, 2-A, 80-mΩ on-resistance load switch
- SN6505B, low-noise 1-A, 420-kHz transformer driver for isolated power supplies
- TPS2400, 5.5-V overvoltage protection controller with 100-V input transient protection
- DCH010515D, miniature, 1-W, 3-kV DC isolated DC/DC converters with dual output
- DCH010505S, miniature, 1-W, 3-kV DC isolated DC/DC converters
- TPS65130, split-rail converter with dual, positive and negative outputs (300 mA typ)
- TPS65130, split-rail converter with dual, positive and negative outputs (300 mA typ)
- TVS0500, 5-V flat-clamp surge protection device

5.2.2.2 Generation of Regulated 3.3-V, ±5-V and ±12-V Supplies Using LDOs

This design has the following functionality:

- TPS7A3901, dual, 150-mA, wide-V_{in}, positive and negative low-dropout (LDO) voltage regulator
- LM27762, low-noise positive- and negative-output charge pump with integrated LDO
- TLV70433, 24-V input voltage, 150-mA, ultra-low I_Q low-dropout (LDO) regulators
- TVS1400, 14-V flat-clamp surge protection device

5.2.2.3 Generation of Stable Reference

This design has the following functionality:

- REF5025, 3-µVpp/V, noise, 3 ppm/°C drift precision series voltage reference
- REF3025, 2.5-V, 50-ppm/°C, 50-µA in SOT23-3 series (Bandgap) voltage reference
- REF3425, 2.5-V, low-drift low-power small-footprint series voltage reference
- LM4040AIM3-2.5, precision micropower shunt voltage reference
- OPA2376, precision, low noise, low quiescent current operational amplifier

5.2.3 Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power

This section provides details of the devices used to generate the required isolated power supplies for analog IO module and digital isolators used for isolated synchronous communication.

5.2.3.1 Generation of 5 V and ±15 V from 24-V input

This design has the following functionality:

- LM5017, 7.5 V–100 V wide V_{IN}, 600-mA constant on-time synchronous buck
- TPS7A4700, 36-V, 1-A, 4.17-μV_{RMS}, RF low-dropout (LDO) voltage regulator
- TPS7A3001, V_{IN}, –3 V to –36 V, –200 mA, ultra-low noise, high-PSRR, low-dropout (LDO) linear regulator
- TPS7A1650, 60-V, 5-µA I_Q, 100-mA, low-dropout (LDO) voltage regulator with enable and power good
- TPS70933, 150-mA 30-V ultra-low I_Q wide-input low-dropout (LDO) regulator with reverse current protection
- TVS3300, 33-V flat-clamp surge protection device

5.2.3.2 Generation of 5 V and ±15 V from 5-V input

This design showcases the following functionality:

- TPS55010, 2.95-V to 6-V input, 2-W, isolated DC/DC converter with integrated FETS
- LP2985-50, 150-mA low-noise low-dropout regulator with shutdown
- TVS0500, 5-V flat-clamp surge protection device

5.2.3.3 Isolated Synchronous Interface

This design has the following functionality:

- ISO7741, high-speed, low-power, robust EMC quad-channel digital isolator
- ISO7141, 4242-V_{PK} small-footprint and low-power 3/1 quad-channel digital isolator with noise filter
- ISO1541D, 2.5-kV_{RMS} isolated unidirectional clock, bidirectional I2C isolators

5.2.4 System Design

The design is split into multiple boards as described in this section:

1. Isolated power supply for communication module
2. Wide input isolated power supply for analog IO modules
3. Isolated synchronous communication with split-rail Fly-Buck power

5.2.4.1 Isolated Power Supply for Communication Module

This section provides details of the devices used to generate the required power supplies for isolated communication module.

5.2.4.1.1 Isolated 5-V and 3.3-V Supply Generation Using Power Module

This design features the following functionality and is configured as detailed in the following section:

- DCR010505P, 5-V output configuration loaded for 100 mA and connected to LDO
- DCP010505BP, 5-V output configuration loaded for 100 mA in PDIP package and connected to LDO
- LP2985AIM5-3.3, generation of fixed and regulated 3.3-V output loaded to 50 mA

5.2.4.1.2 Isolated 5-V, 3.3-V, and ±12-V Supply Generation Using Transformer Driver

This design features the following functionality and is configured as detailed in the following section:

- SN6505B, 6-V output loaded to 200 mA and connected to LDO
- SN6501, 6-V output loaded to 100 mA and connected to LDO
- TPS70933, generation of fixed and regulated 3.3-V output loaded to 50 mA
- TPS70950, generation of fixed and regulated 5-V output loaded to 50 mA
- TPS7A3901, configured to generate regulated dual ±12-V output loaded to 100 mA for each output

5.2.4.1.3 Isolated 5.4-V, 5-V, and 3.3-V Supply Using Digital Isolator With Integrated Power

This design showcases the following functionality and is configured as detailed in the following section:

- TPS22944, for overload protection of 5-V input to ISOW7841
- ISOW7841, configured for 5-V output loaded to 100 mA
- TPS76350, generation of fixed and regulated 5-V output loaded to 50 mA
- TPS62821, 5-V to 3.3-V conversion output loaded to 100 mA

5.2.4.1.4 Generation of Regulated DC Supplies With Protection and Diagnostics

This design showcases the following functionality and is configured as detailed in the following section:

- UCC12050, can be configured (using resistor) to generate 5.4-V, 5-V, 3.7-V or 3.3-V
- TPS22960, for overload protection of input voltage
- TLV74233, generation of fixed and regulated 3.3-V output loaded to 50 mA
- TLV70450, generation of fixed and regulated 5-V output loaded to 50 mA
- TPS3897, for monitoring of 5.4-V output voltage
- SN74LVC1G14, single Schmitt-trigger inverter for status indication
- SN74LVC1G17, single Schmitt-trigger buffer for status indication
- CSD17571Q2, 30-V N-channel NexFET power MOSFETs for driving the LEDs

The UCC12050 is a high isolation voltage DC/DC converter designed to provide efficient isolated power to isolated circuits that require well-regulated supply voltages. The UCC12050 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high efficiency with very low emissions. The UCC12050 provides 500 mW (typical) of isolated output power at high efficiency. Requiring a minimum of external components and including on-chip device protection, the UCC12050 provides extra features such as an enable pin, synchronization of switching frequency among multiple devices, and selection of isolated output voltages.

5.2.4.2 Wide Input Isolated Power Supply for Analog IO Modules

This section provides details of the devices used and configurations to generate required isolated power supplies for analog IO module.

5.2.4.2.1 Generation of Isolated 5 V and ±15 V With Protection

This design showcases the following functionality and is configured as detailed in the following section:

- LM5160, configured for generating of isolated 5-V output loaded to 250 mA
- TPS22917, overload protection of 5-V input to SN6505B
- SN6505B, configured for generation of isolated 5-V output from 5-V input
- TPS2400, used for diagnostics to indicate 5-V input voltage status
- DCH010515D, generation of isolated split-rail supply ±15 V loaded to 25 mA
- DCH010505S, generation of isolated split-rail supply 5 V loaded to 100 mA
- TPS65130, generation of isolated split-rail supply ±15 V loaded to 100 mA
- TVS3300, protection of LM5160 with 24-V input against
- TVS0500, protection of TPS22917 with 5-V input against transients

5.2.4.2.2 Generation of Regulated 3.3-V, ±5-V, and ±12-V Supplies Using LDOs

This design showcases the following functionality and is configured as detailed in the following section:

- TPS7A3901, generation of regulated split-rail supply ±12 V loaded to 100 mA
- LM27762, generation of regulated split-rail supply ±5 V loaded to 100 mA
- TLV70433, generation of fixed and regulated 3.3 V for generation of reference
- TVS1400, protection of split-rail supply voltage against transients

5.2.4.2.3 Generation of Stable Reference

This design showcases the following functionality and is configured as detailed in the following section:

- REF5025, generation of 2.5-V reference from 3.3-V input
- REF3025, generation of 2.5-V reference from 3.3-V input
- REF3425, generation of 2.5-V reference from 3.3-V input
- LM4040AIM3-2.5, generation of 2.5-V reference from 3.3-V input
- OPA2376, for buffering the reference output

5.2.4.3 Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power

This section provides details of the devices used and configuration to generate the required isolated power supplies for analog IO module and digital isolators used for synchronous communication.

5.2.4.3.1 Generation of 5 V and ±15 V From 24-V input

This design showcases the following functionality and is configured as detailed in the following section:

- LM5017, generation of isolated split-rail ±17-V power supply
- TPS7A4700, generation of regulated 15 V loaded to 100 mA
- TPS7A3001, generation of regulated –15 V loaded to 100 mA

- TPS7A1650, generation of regulated 5 V loaded to 100 mA
- TPS70933, generation of fixed and regulated 3.3 V loaded to 50 mA
- TVS3300, protection of LM5017 DC/DC with 24-V input against transients

5.2.4.3.2 Generation of 5 V and ±15 V From 5-V input

This design showcases the following functionality and is configured as detailed in the following section:

- TPS55010, generation of isolated split-rail ±15-V power supply
- LP2985-50, generation of fixed and regulated 5 V loaded to 50 mA
- TVS0500, protection of TPS55010 DC/DC with 5-V input against transients

5.2.4.3.3 Isolated Synchronous Interface

This design showcases the following functionality and is configured as detailed in the following section:

- ISO7741, implementing SPI from host
- ISO7141, implementing SPI from host
- ISO1541D, implementing I2C interface from host

5.2.4.4 Enhancements

There are multiple approaches to the generation of isolated split-rail power supplies based on load current and EMI performance for analog IO modules. These are summarized in 表 6.

表 6. Isolated Split-Rail Supply Generation

OPTIONS	ANALOG SUPPLY RANGE	SWITCHER, DC/DC	LDO	COMMENTS
1	±5 V (100 mA)	NA	LM27762	No additional inductor or diodes required
2	±5 V (50 mA)	TPS60403	LP2951, LM337	No additional inductor or diodes required
3	±5 V (25 mA)	TPS61040	LP2951, LM337	Need inductor, diodes
4	±10 V (25 mA)	TPS61040	LP2951, LM337	Need inductor, diodes
5	±10 V (50–100 mA)	SN6505 or SN6501	TPS7A3901	Need transformer, diodes
6	±10 V (50–100 mA)	SN6505 or SN6501	TPS7A4901, TPS7A3001	Need transformer, diodes
7	±10 V (20 ma)	Power module (isolated DC/DC)	TPS7A4901, TPS7A3001	No additional inductor or diodes required
8	±10 V (150 mA)	TPS65131	TPS7A3901	Need inductor, diodes
9	±10 V (150 mA)	TPS65131	TPS7A4901, TPS7A3001	Need inductor, diodes
10	±10 V (150 mA)	LM5017	TPS7A4901, TPS7A3001	Need transformer, diodes
11	±10 V (60 mA)	LM5002	NA	Need transformer, inductors, diodes
12	±15 V (100 mA)	TPS55010	NA	Need transformer, diodes

5.2.5 Design Guidelines

This section provides generic guidelines for designing the isolated power supply modules.

- Refer to the product data sheet for layout guidelines for the devices used in this reference design.
- Refer to the product data sheet and the EVMs for configuring the required outputs.

- The selection of the transformer plays an important role in providing the required isolation and output current.

6 Design Details for Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power-Supply Board

This section provides implementation details for Isolated synchronous communication with split-rail Fly-Buck power supply board.

6.1 Power Supply

6.1.1 DC/DC Converter for Generation of Output Voltages

In industrial systems, signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. Isolation also avoids ground loop. The LM5017 is a synchronous buck regulator with integrated MOSFET.

This design uses the LM5017 configured in Fly-Buck mode for converting the 24-V DC input to the required output voltage. The Fly-Buck converter generates the following voltages:

- Isolated voltages: 18 V, –18 V, and 7 V
- Non-isolated voltages: 9 V (ratio of input voltage)

注: The output voltages are unregulated outputs and may vary with the input voltage.

6.1.2 Isolated Output Voltage Regulator

Isolated voltages are used for

- I2C and SPI isolators
- Interfaced to the connectors for powering external devices like ADC, DAC, and I2C expanders

The unregulated isolated voltage outputs of the Fly-Buck converter are regulated using the LDO. The following regulators are used in this design:

- 15 V → LDO TPS7A4700
- –15 V → Linear Regulator TPS7A3001
- 5 V → Linear Regulator TPS7A1650

6.1.3 Non-isolated Output Voltage Regulator

Non-isolated voltages are used for I2C and SPI isolators. This supply can be used to power low-power microcontrollers based on the application.

The following non-isolated supply is generated in design:

- 3.3 V at 25 mA → Linear Regulator TPS70933

The isolated voltages are protected against overvoltage with Zener diodes . These Zener diodes provide additional protection for ESD .

6.2 Signal Isolation

CAUTION

Although these devices provide galvanic isolation of up to 5000 V_{RMS}, this reference design is not recommended for isolation voltage testing. The reference design is designed for the evaluation of device operating parameters only and may be damaged if a voltage exceeding 32-V DC is applied anywhere in the circuit.

6.2.1 Serial Peripheral Interface (SPI)

ISO7141CC (or ISO7741) , a low-power 3/1 quad-channel digital isolator with noise filter, is used to isolate SPI signals. This design is tested up to 4Mbps.

6.2.2 I2C Interface

ISO1541, a low-power, bidirectional I2C isolator, is used to isolate I2C signals.

The I2C is open-drain topology, requiring two lines, serial data (SDA), and serial clock (SCL), to be connected to VDD by pullup resistors. To have logic Zero online, pull the line to ground (an operating MOSFET). To have logic One, let the line float (a not-operating MOSFET) to make it High due to the pullup resistor.

Pullup resistors are selected based on recommended drain currents. This design uses 1.5-kΩ pullup resistors and is tested at 100 Kbps.

6.3 LED Indicators

LED indications for 15-V, –15-V, and 5-V isolated power supplies are provided in this design.

6.4 Input and Output Connectors

Input connector:

- 8-pin screw type terminal blocks for interfacing non-isolated SPI, I2C, and input power

Output connectors:

- 8-pin screw type terminal block for interfacing isolated SPI and I2C
- 4-pin screw type terminal block for isolated voltage outputs

7 Circuit Design for Isolated Synchronous Communication With Split Rail Fly-Buck™ Power-Supply Board

7.1 Power Supply

7.1.1 DC/DC Converter for Generation of Output Voltages

The Fly-Buck converter is evolved from a synchronous buck converter by adding coupled windings to the inductor to have flyback-like isolated outputs. The isolated outputs can be multiple by adding more secondary windings to the transformer.

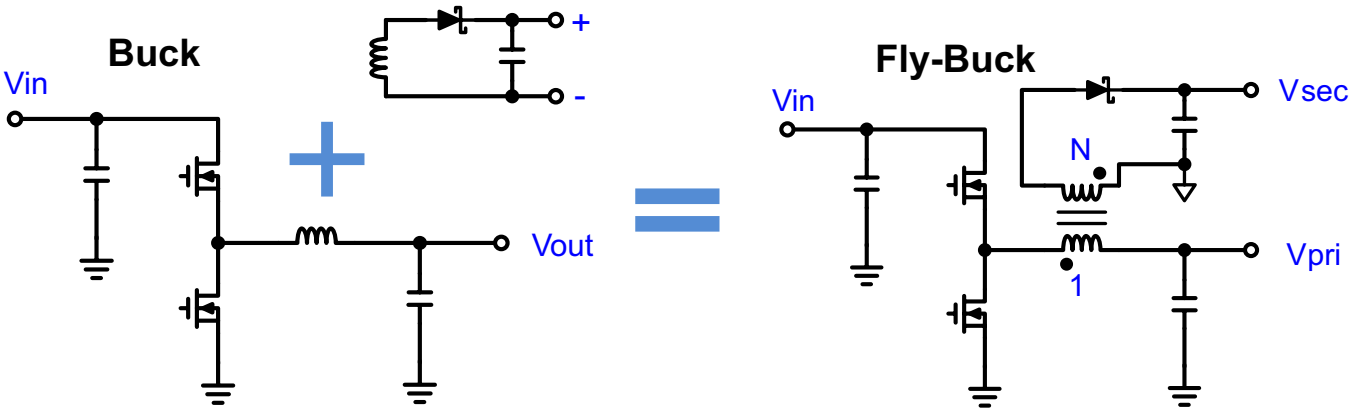

図 4. Fly-Buck™ Topology Basics

The Fly-Buck is capable of generating multiple isolated and negative outputs. Fly-Buck topology has better regulation, better efficiency, and lower cost compared to flyback topology.

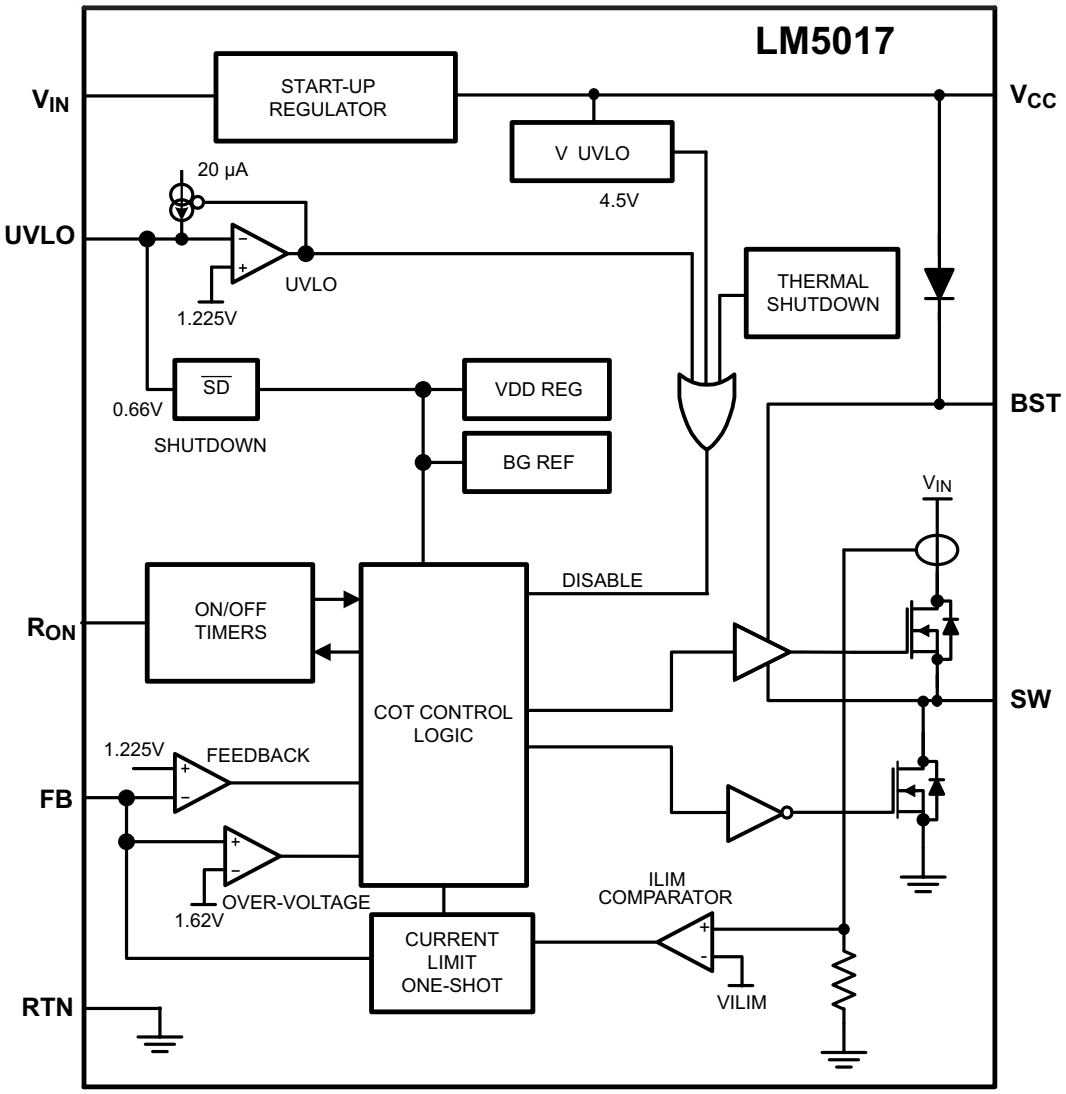

図 5. LM5017 Functional Block Diagram

The LM5017 is configured in Fly-Buck topology to generate non-isolated 3.3 V and isolated 5, 15, and –15 V from 24-V DC. An isolated Fly-Buck converter uses a coupled inductor windings to generate isolated outputs. Flyback topology does not need for an optocoupler or auxiliary winding as the secondary output closely tracks the primary output voltage, resulting in a cost effective and smaller-sized solution.

表 7. Power-Supply Specifications

INPUT — DC NOMINAL	OUTPUTS ISOLATED — DC		OUTPUT NON-ISOLATED — DC	
	VOLTAGE	LOAD	VOLTAGE	LOAD
24 V	15 V	50 mA	3.3 V	25 mA
	–15 V	50 mA		
	5 V	100 mA		

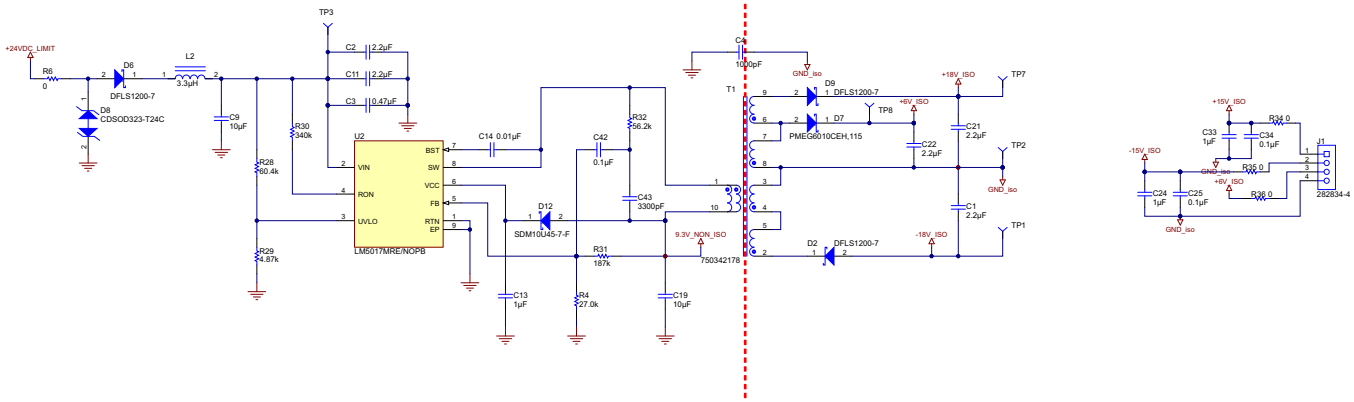

図 6. Fly-Buck™ Power-Supply Schematic

表 8. LM5017 Fly-Buck™ Calculation

SPECIFICATIONS			NOTE
NAME	(V)	(A)	
Vin_min	17		
Vin_max	32		
Vopri	7.9	0	
Vosec1	5	0.1	
Vosec2	5	0.1	
Vosec3	15	0.05	
Vosec4	15	0.05	
η	0.85		Assumed efficiency
fsw	270	kHz	
Ron	344.23	kΩ	
Dmax	0.55		
Dmin	0.29		
Toff_min	1.68	µs	Toff_min > 0.144 µs
Vdiode	0.3	V	Rectifier diode voltage drop
Nsec1/Npri	0.67		
Nsec2/Npri	0.67		
Nsec3/Npri	1.94		
Nsec4/Npri	1.94		

表 9. Peak Current

NAME	VALUE	UNIT	NOTE
IL (avg)	0.328	A	
Lpri	50	µH	
ΔIL	0.441	A	
IL_peak	0.548	A	IL_peak < 0.7 A

表 10. Transformer Design

NAME	VALUE	DESCRIPTION
CORE SELECTION		
Pout_total	2.5 W	
Ae	19.5 mm^2	Effective core area
Ie	24.2 mm	Effective core length
Ve	472 mm^3	Effective core volume
NUMBER OF TURNS		
Bmax	250 mT	Assumed max flux density in steady state
Npri_min	6	Min prim. turns based on Bmax and peak currents
Npri	15	Actual prim. turns (Npri > Npri_min)
Nsec1	10	
Nsec1	10	
Nsec1	29	
Nsec1	29	
FLUX DENSITY CHECK		
Ilim_max	1.3 A	Max current limit
Bsat	350 mT	Saturation flux density
Bmat_sc	222 mT	Max flux density in short circuit Check Bmax_sc < Bsat, otherwise increase Npri
AIR GAP ESTIMATION (FOR SMALL GAP)		
µ0	1.257E-06 H/m	Vacuum permeability
µe	219	Effective permeability
Ie/µe	0.110 mm	
ROUND CENTER POLE (LIKE E CORE)		
Dcp	4.5 mm	Center pole diameter
lg	0.116 mm	Air gap length
RECTANGULAR CENTER POLE (LIKE E CORE)		
a	3 mm	Center pole width
b	4 mm	Center pole length
lg	0.118 mm	Air gap length
CORE LOSS		
fsw	270.00 kHz	
ΔB	38 mT	
Pv	50 kW/m^3	Look up Pv in core material chart based on fsw and ΔB
Pcore	24 mW	Core loss

7.1.2 UV Protection

The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed.

$$V_{IN}\ (UVLO, rising) = 1.225 \times \left(\frac{R28}{R29} + 1 \right)$$

where

- R28 = 60.4 kΩ
- R29 = 4.87 kΩ

(1)

Then, V_{IN} (UVLO, rising) = 16.46 V.

$$V_{IN}\ (HYS) = I_{HYS} \times R28$$

where

- I_{HYS} = 0.02 mA

(2)

Then, V_{IN} (HYS) = 1.208 V.

7.1.3 Isolated Output Voltage Regulators

7.1.3.1 Isolated 15 V

The TPS7A4700 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature is a must for powering operational amplifiers, ADCs, DACs, and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

In addition, the TPS7A4700 is ideal for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversions, maximum system performance is ensured in sensitive instrumentation, test-and-measurement, audio, and RF applications.

Output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

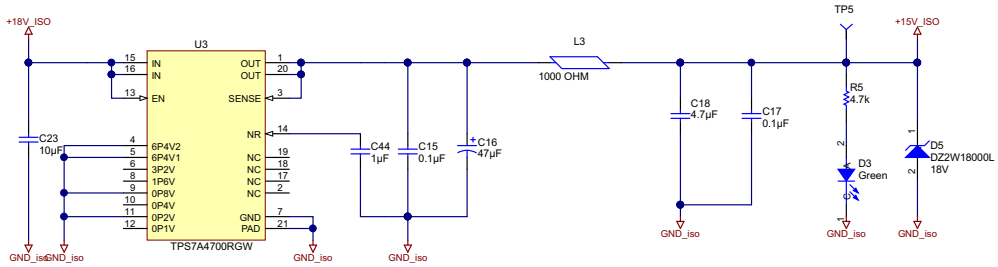

図 7. TPS7A4700 15-V Regulator

表 11. TPS7A4700 Critical Parameters

PARAMETER	TPS7A4700
Output options	Programmable output
V_{IN} (Min) (V)	3
V_{IN} (Max) (V)	36
V_{OUT} (Min) (V)	1.4
V_{OUT} (Max) (V)	20.5
Iq (Typ) (mA)	0.58
Vdo (Typ) (mV)	216
Accuracy (%)	2.5
Noise (μV_{RMS})	4
PSRR at 100 kHz (dB)	68

7.1.3.2 Isolated –15 V

The TPS7A3001 is a negative, high-voltage (–36 V), ultra low-noise (15.1 μV_{RMS}, 72 dB PSRR) linear regulator. TPS7A3001 includes a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design is an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A3001 linear regulator is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

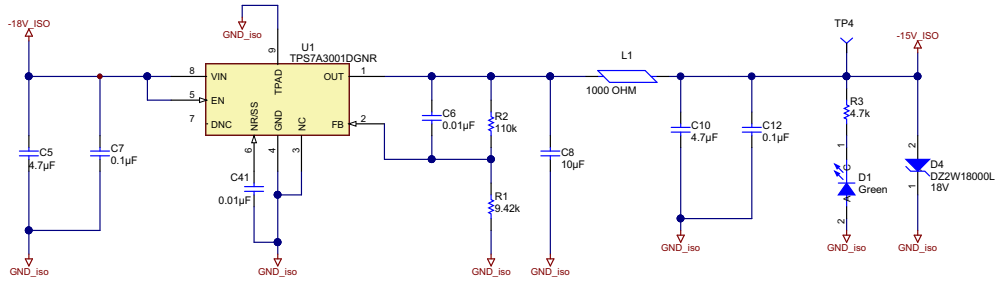

図 8. TPS7A3001 –15-V Regulator

表 12. TPS7A3001 Critical Parameters

PARAMETER	TPS7A3001
Output options	Adjustable output Negative output
V_{IN} (Min) (V)	–36
V_{IN} (Max) (V)	–3
V_{OUT} (Min) (V)	–33
V_{OUT} (Max) (V)	–1.2
Iq (Typ) (mA)	0.05
Vdo (Typ) (mV)	216
Accuracy (%)	2.5
Noise (μV_{RMS})	15
PSRR at 100 kHz (dB)	55

7.1.3.3 Isolated 5 V

An isolated 5 V is generated using TPS7A1650 linear regulator.

The TPS7A1650 is ultra-low power, low-dropout (LDO) voltage regulator, which offers the benefits of ultra-low quiescent current, high input voltage and miniaturized, high thermal-performance packaging.

The TPS7A1650 is designed for continuous or sporadic (power backup) battery-powered applications where ultra-low quiescent current is critical to extending system battery life.

The TPS7A1650 offers an enable pin (EN) compatible with standard CMOS logic and an integrated open drain active-high power good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power rail sequencing is required.

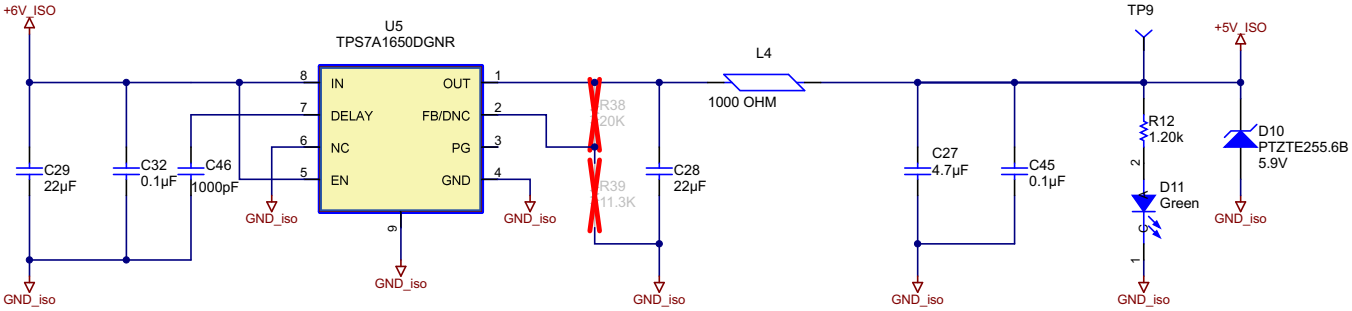

図 9. TPS7A1650 5-V Regulator

表 13. TPS7A1650 Critical Parameters

PARAMETER	TPS7A1650
Output options	Fixed output
V_{IN} (Min) (V)	3
V_{IN} (Max) (V)	60
Fixed Output Options (V)	5
V_{OUT} (Min) (V)	5
V_{OUT} (Max) (V)	5
I_Q (Typ) (mA)	0.005
Vdo (Typ) (mV)	60
Accuracy (%)	2
PSRR at 100 kHz (dB)	26

The isolated SPI and I2C are interfaced with external devices. These external devices can operate on 3.3 V or 5 V. Currently, the levels are configured for external devices operating at 5 V . When the slave devices are operating at 3.3 V, change the following to configure the interface signals to 3.3 V:

1. Change U5: Use TPS7A1501 instead of TPS1650.
2. Populate R38 and R39 with values shown in the schematic and BOM. Currently, R38 and R39 are shown as do not populate.

The Fly-Buck design can generate –5 V. There is no requirement for –5 V in the designs this module is targeted to interface with; therefore, the design does not have the –5-V output regulator.

7.1.4 3.3-V Non-isolated Output Voltage

VCC_NON_ISO is applied to TPS70933 linear regulator that generates 3.3 V_NON_ISO. The 3.3 V_NON_ISO is used to power-up SPI and I2C digital isolators.

The TPS70933 linear regulator is an ultra-low, quiescent current device designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1 µA makes TPS70933 ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. TPS70933 have thermal-shutdown, current-limit, and reverse-current protections for added safety.

This regulator can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typically.

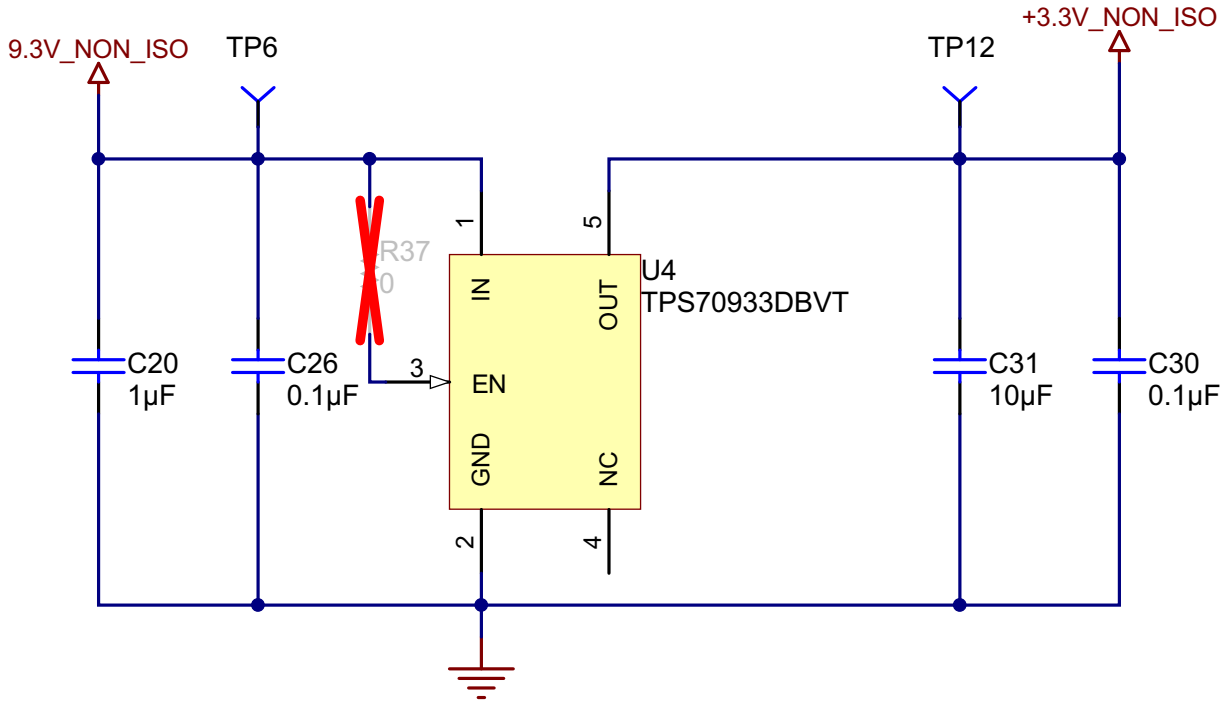

図 10. TPS70933 3.3-V Regulator

表 14. TPS70933 Critical Parameters

PARAMETER	TPS70933
Output options	Fixed output
V_{IN} (Min) (V)	2.7
V_{IN} (Max) (V)	30
Fixed Output Options (V)	3.3
V_{OUT} (Min) (V)	3.3
V_{OUT} (Max) (V)	3.3
Iq (Typ) (mA)	0.001
Vdo (Typ) (mV)	300
Accuracy (%)	2
PSRR at 100kHz (dB)	26

7.1.5 Power-Supply Performance

表 15. Current Consumption for SPI and I2C Isolators

DEVICE	NON-ISOLATED SIDE — CURRENT AT 3.3 V	ISOLATED SIDE — CURRENT AT 5 V
SPI	3.5 mA	9.6 mA
I2C	3.5 mA	3.5 mA

表 16. Maximum Power on Output Voltages

OUTPUT VOLTAGE	POWER
15 V	0.8 W
–15 V	0.8 W
5 V	0.55 W
3.3 V	0.1 W

表 17. Efficiency Calculation

NAME	VALUE
Output power	2.25 W
Input power	3.1 W
Efficiency	>72%

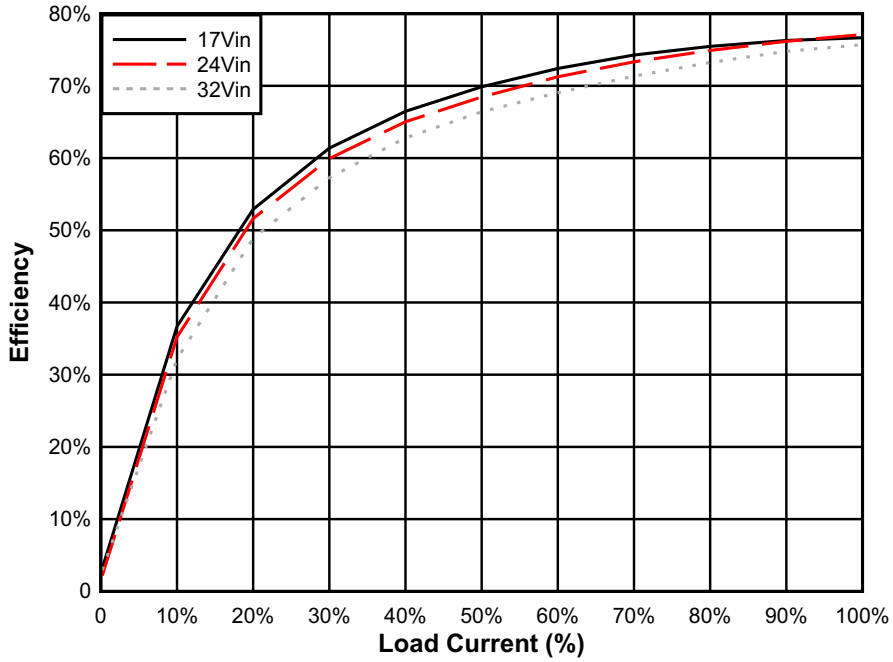

図 11. Efficiency Plot

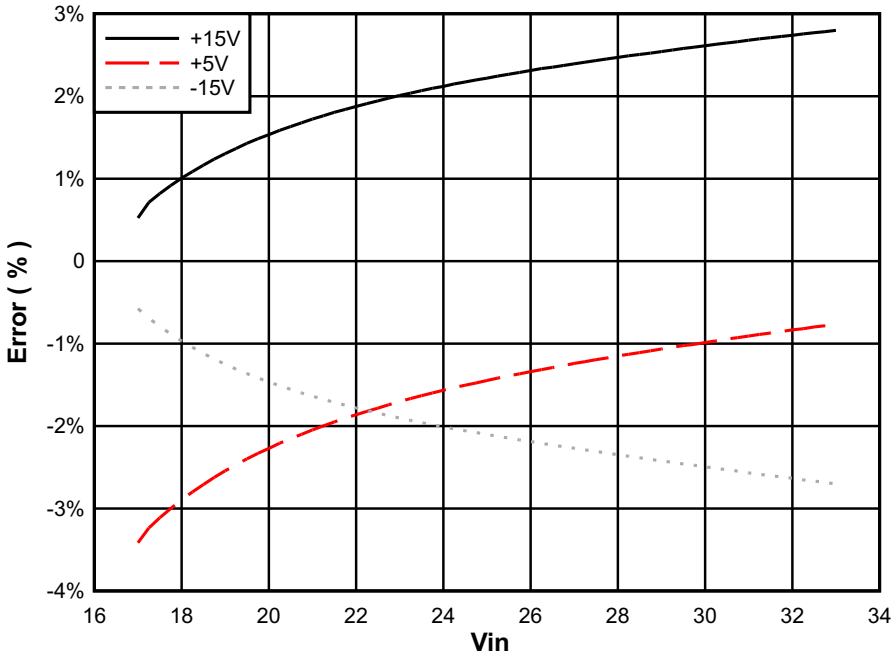

図 12. Line Regulation at 100% Load

7.1.6 Recommendations for Power Supply

1. Power supply must be on before SPI or I2C communication is initiated.
2. Do not hot swap the input and output power.
3. Do not apply overvoltage >30 V at the input.

7.2 Signal Isolation

7.2.1 Serial Peripheral Interface (SPI)

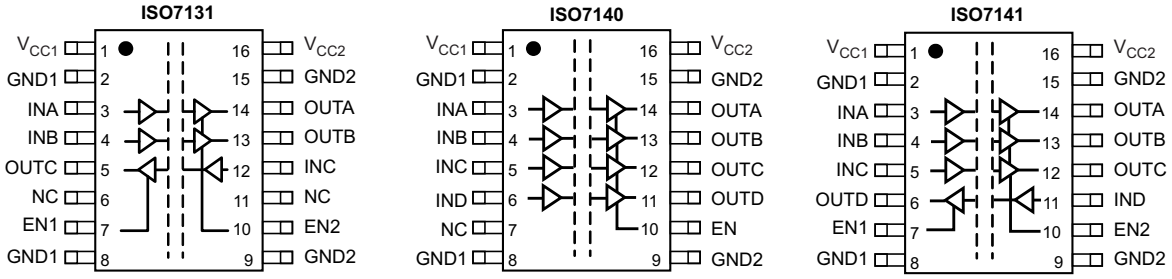

図 13. Pin Configuration for ISO7141CC (Top View)

表 18. Output — High and Low Levels for ISO7141CC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	V_{CCx} (1) – 0.5	4.8		V
		I_{OH} = –20 µA	V_{CCx} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.2	0.4	V
		I_{OL} = 20 µA		0	0.1	

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

表 19. Input Levels for ISO7141CC

PARAMETER		MIN	TYP	MAX	UNIT
I_{OH}	High-level output current (V_{CC} ≥ 3.0 V)	–4			mA
	High-level output current (V_{CC} < 3.0 V)	–2			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V

This design is tested for the application requirement speed up to 4 Mbps.

ISO7141CC provide galvanic isolation up to 2500 V_{RMS} for one minute per UL and 4242 V_{PK} per VDE. ISO7141 is quad-channel isolator with three forward and one reverse-direction channels. ISO7141CC is capable of a 50-Mbps maximum data rate with a 5-V supply and a 40-Mbps maximum data rate with a 3.3-V or 2.7-V supply, with integrated filters on the inputs for noise-prone applications. The default output state is high as required for SPI.

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The device has TTL input thresholds and can operate from 2.7-V, 3.3-V, and 5-V supplies. All inputs are 5-V tolerant when supplied from a 2.7-V or 3.3-V supply.

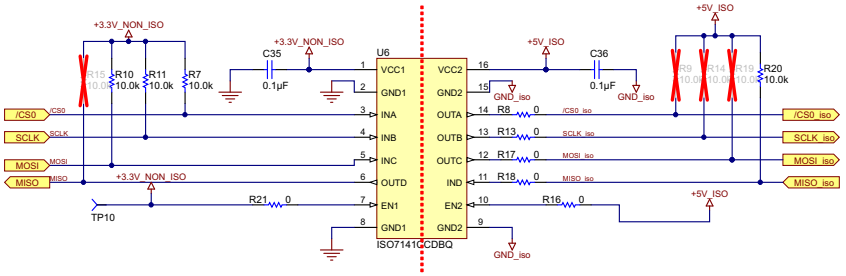

図 14. ISO7141CC — SPI Isolator Section

表 20. ISO7141CC Critical Parameters

PARAMETER	ISO7141CC
UL 1577 isolation voltage (single) (kV_{RMS})	2500
VDE DIN EN 60747-5-5 basic transient overvoltage rating (kVpk)	4200
VDE DIN EN 60747-5-5 basic surge voltage rating (kVpk)	4000
VDE DIN EN 60747-5-5 basic working voltage rating (kVpk)	566
Number of channels	4
Forward/reverse channels	3/1
Supply voltages (V)	2.7, 3.3, 5
Default output	High
CSA 60950-1 basic working (V_{RMS})	370
CSA 60950-1 reinforced working (V_{RMS})	185
CSA 61010-1 basic working (V_{RMS})	300
CSA 61010-1 reinforced working (V_{RMS})	150
CSA Isolation Rating (V_{RMS})	3000
TTL/CMOS input threshold	TTL, CMOS
Propagation delay (ns)	23

注: Alternatively, use a ISO7741 digital isolator. The ISO7741 device has low power consumption, typical 1.5-mA per channel at 1Mbps, and low propagation delay: 10.7 ns typical at 5 V. Other advantages include robust electromagnetic compatibility (EMC) including system-level ESD, EFT, and surge immunity and low emissions.

7.2.2 I2C Interface

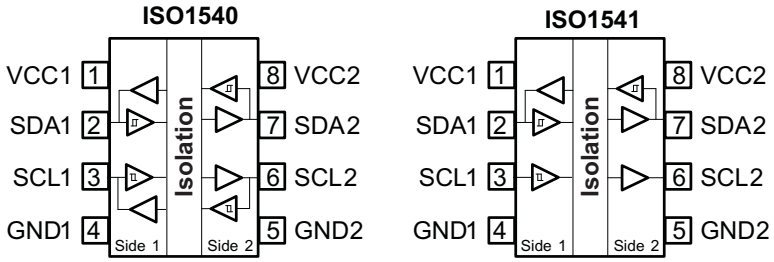

図 15. Pin Configuration for ISO1540 and ISO1541

表 21. Input and Output Levels for ISO1541

PARAMETER		MIN	NOM	MAX	UNIT
VCC1, VCC2	Supply voltage	3		5.5	V
VSDA1, VSCL1	I/O signal voltages, side 1	0		VCC1	
VSDA2, VSCL2	I/O signal voltages, side 2	0		VCC2	
VIL1	Low-level input voltage, side 1	0		0.5	
VIH1	High-level input voltage, side 1	0.7 × VCC1		VCC1	
VIL2	Low-level input voltage, side 2	0		0.3 × VCC2	
VIH2	High-level input voltage, side 2	0.7 × VCC2		VCC2	

The ISO1541 is a low-power, bidirectional isolator that is compatible with I2C interfaces. This device has logic input and output buffers separated by TI's capacitive isolation technology using a SiO2 barrier. When used in conjunction with isolated power supplies, this device blocks high voltages, isolates grounds, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1541 enable a complete isolated I2C interface to be implemented within a small form factor.

The ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within ISO1541 by offsetting the side one low-level output voltage to a value greater than the side one high-level input voltage thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

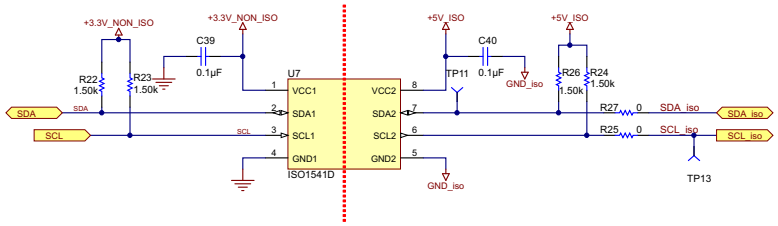

図 16. ISO1541 — I2C Isolator

表 22. ISO1541 Critical Parameters

PARAMETER	ISO1541
UL 1577 isolation voltage (single) (kV_{RMS})	2.5
VDE DIN EN 60747-5-5 basic transient overvoltage rating (kVpk)	4.3
VDE DIN EN 60747-5-5 basic surge voltage rating (kVpk)	4
VDE DIN EN 60747-5-5 basic working voltage rating (kVpk)	0.0566
CSA isolation rating (V_{RMS})	2.8
CSA 60950-1 basic working (V_{RMS})	390
CSA 61010-1 basic working (V_{RMS})	300
CSA 61010-1 reinforced working (V_{RMS})	150
Data rate (Mbps)	1
Number of channels	2
Serial clock	Unidirectional
Serial data	Bidirectional

表 23. Pullup Recommendations for I2C Interface(1)

POWER STATE	INPUT	OUTPUT
VCC1 or VCC2 < 2.1 V	X	Z
VCC1 and VCC2 > 2.8 V	L	L
VCC1 and VCC2 > 2.8 V	H	Z
VCC1 and VCC2 > 2.8 V	Z(2)	?

(1) H = High level; L = Low level; Z = High impedance or float; X = Irrelevant; ? = Indeterminate.
(2) Invalid input condition as an I2C system requires that a pullup resistor to VCC is connected.

For I2C interface, a pullup on the input side and the output side of the isolator is recommended.

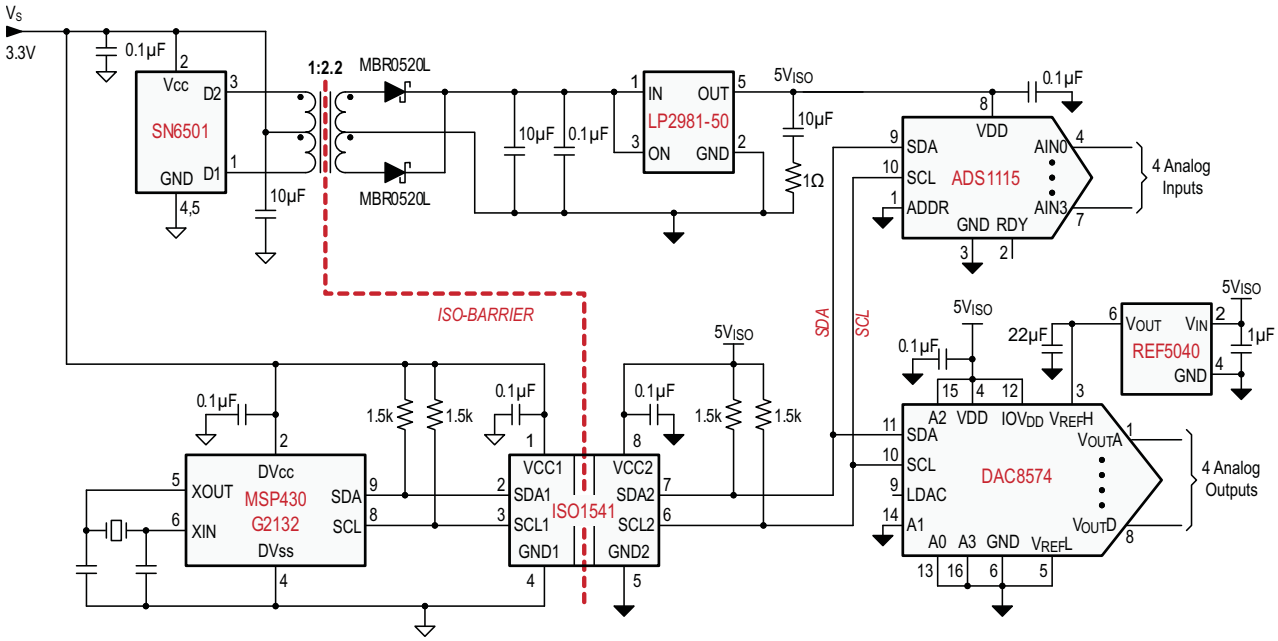

図 17. Illustration for I2C Interface With Pullups

In 図 17, the ultra low-power microcontroller MSP430G2132 controls the I2C data traffic of configuration data and conversion results for the analog inputs and outputs (see datasheet). Low-power data converters build the analog interface to sensors and actuators. The ISO1541 provides the necessary isolation between different ground potentials of the system controller, remote sensor, and actuator circuitry to prevent ground loop currents that otherwise may falsify the acquired data.

The entire circuit operates from a single 3.3-V supply. A low-power push-pull converter, SN6501, drives a center-tapped transformer whose output is rectified and linearly regulated to provide a stable 5-V supply for the data converters.

7.3 LED Indicators

The LEDs are provided for indicating the status of the output voltages. SMD LEDs are used for indication purpose. These LEDs are continuously ON when output voltages are present.

7.4 Input and Output Connectors

Input Connector

8-pin screw type terminal blocks are used for interfacing non-isolated SPI, I2C, and input power.

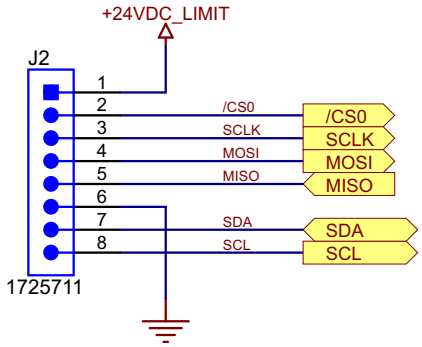

図 18. Non-isolated SPI, I2C, and Power Input Connector

Output Connector

An 8-pin screw type terminal block is used for interfacing isolated SPI and I2C.

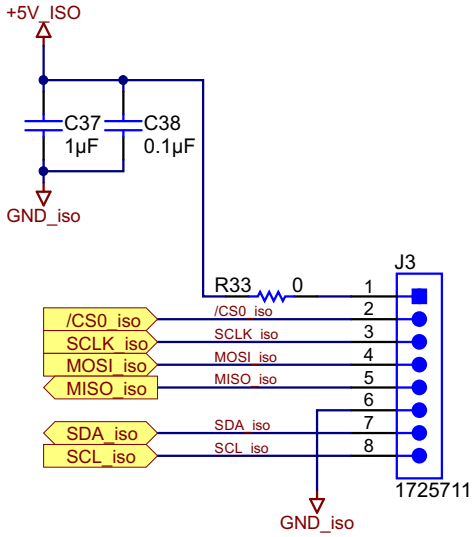

図 19. Isolated SPI and I2C Output Connector

A 4-pin screw type terminal block is used for isolated voltage outputs.

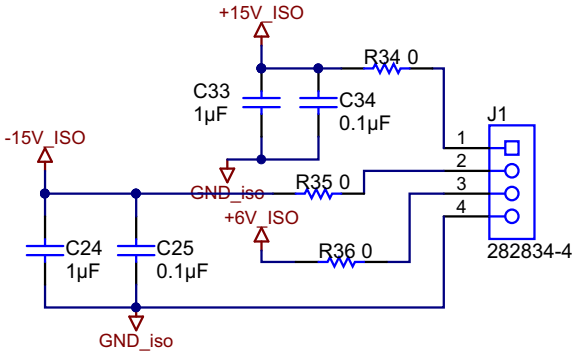

図 20. Isolated Output Voltage Connector

7.5 PCB Design Guidelines and Dimensions

- Apply creepage and clearance requirements according to the specific application isolation standards. Take care to maintain these distances on a board design to ensure that the mounting pads for the isolator do not reduce this distance. Creepage and clearance on the printed-circuit board become equal in certain cases. Use techniques such as inserting grooves and ribs on the PCB to help increase these specifications.
- Use an SMD ceramic bypass capacitor of approximately 0.1 μF in value.
- Use a continuous ground plane to provide a low-impedance signal return path as well as generating the lowest EMI signature by reducing phenomena such as unintended current loops.
- PCB material: Standard FR-4 epoxy-glass as PCB material is preferred for industrial applications with a speed less than 100 MHz I. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0 and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing, flammability characteristics.
- Trace Routing: Use 45° bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width and thus the trace impedance. This creates additional impedance mismatch, which may lead to higher reflections.

注: The PCB is designed as a small add-on board. This board has provision for isolated power supply, SPI, and I2C interface. There may be some applications where 15- and –15-V isolated power supplies are available. In this case, the LM5017 Fly-Buck part may not be required.

7.6 Tiva™ C Series LaunchPad™ Interface

The Tiva C Series LaunchPad (EK-TM4C123GXL) is a low-cost evaluation platform for Arm® Cortex®-M4F-based microcontrollers. The Tiva C Series LaunchPad design highlights the TM4C123GH6PMI microcontroller USB 2.0 device interface, hibernation module, and motion control pulse-width modulator (MC PWM) module. The Tiva C Series LaunchPad also features programmable user buttons and an RGB LED for custom applications. The stackable headers of the Tiva C Series LaunchPad BoosterPack XL interface demonstrate how easy it is to expand the functionality of the Tiva C Series LaunchPad when interfacing to other peripherals on many existing BoosterPack add-on boards as well as future products. 図 21 shows a photo of the Tiva C Series LaunchPad.

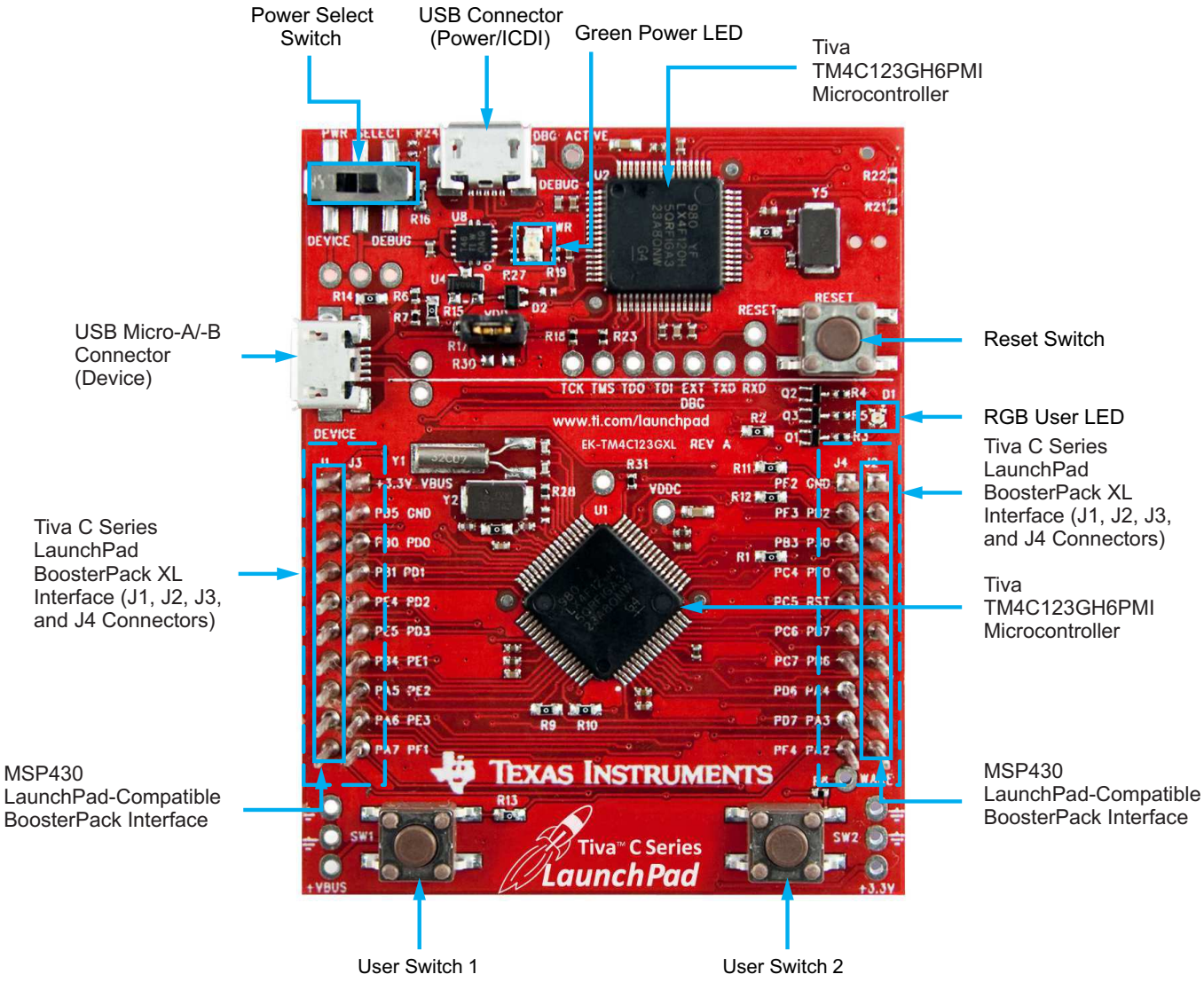

図 21. Tiva™ C Series TM4C123G LaunchPad™ Evaluation Board

8 Software Description

The code was developed, compiled, and tested in a CCS environment.

8.1 I2C Communication Interface Between Master and Slave

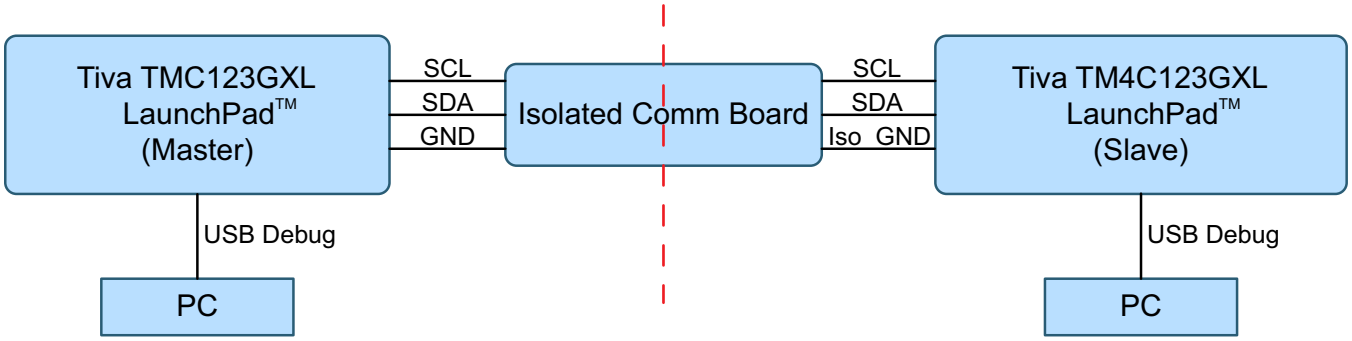

図 22. I2C Communication Test Setup

I2C uses one bi-directional pin serial data line (SDA) and one unidirectional serial clock line (SCL):

- Master node — generates the clock and initiates communication with slaves
- Slave node — receives the clock and responds when addressed by the master

8.1.1 I2C Master

Initializing I2C Master

To initialize the I2C master functionality:

1. Enable the I2C peripheral.
2. Enable the clock gating to the SDA and SCL pins.
3. Choose the pin configuration for SCL and SDA pins.
4. If the I2C device is a master, then enable the master functionality, clock source, and speed of communication.
5. Internal pull up resistors are required when external pull up resistors are not available for SCL and SDA pins.

Depending on the processor platform, the pin mapping would change. 図 23 is an example code snippet for I2C initialization.

```
void I2C1_Init(void)
{
      unsigned int Status=0;

      SysCtlPeripheralEnable(SYSCTL_PERIPH_I2C1);   //Enable the I2C peripheral
      SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA);  //Enable GPIOA

      SysCtlPeripheralClockGating(true);
      SysCtlDelay(2);

      GPIOPinConfigure(GPIO_PA6_I2C1SCL);           //Choose the pin mux for I2C pins
      GPIOPinConfigure(GPIO_PA7_I2C1SDA);
      SysCtlDelay(2);

      GPIOPinTypeI2CSCL(GPIO_PORTA_BASE, GPIO_PIN_6);       //SCL clock pin configuration
      GPIOPinTypeI2C(GPIO_PORTA_BASE, GPIO_PIN_7);          //SDA pin configuration
      SysCtlDelay(2);

      ROM_I2CMasterInitExpClk(I2C1_BASE, SYS_CLOCK, false); //Master init at 100kbps
      SysCtlDelay(2);

      HWREG(GPIO_PORTA_BASE + GPIO_O_PUR) |= 0xC0;   //Enable internal Pull up resistors

      Status=I2CMasterLineStateGet(I2C1_BASE);
}
```

図 23. I2C Master Initialization Code

Sending Data on I2C

To send data on I2C:

1. Set the slave address with whom the master would like to communicate.
2. Set the data.
3. Set the master to transmit mode (single-byte or a multiple-byte stream).
4. Wait until the master completes sending the data.

図 24 shows an example of I2C master data sending.

```
Unsigned int Error_Status=0;

I2CMasterSlaveAddrSet(I2C1_BASE, I2C_SLAVE_ADDR, false);

I2CMasterDataPut(I2C1_BASE, 0x03);
I2CMasterControl(I2C1_BASE, I2C_MASTER_CMD_SINGLE_SEND);

while(I2CMasterBusBusy(I2C1_BASE));    //Loop until the bus is no longer busy

Error_Status = ROM_I2CMasterErr(I2C1_BASE);   //check for errors
```

図 24. I2C Master Data Sending Code

Receiving Data on I2C

To receive data on I2C bus:

1. Set the slave address which sends the data.
2. Set the master to receive mode (could be single byte or a burst stream)
3. Receive the data.
4. Check for errors.

図 25 is a code snippet for receiving data on I2C:

```
uint32_t g_ui32DataRx;
I2CMasterSlaveAddrSet(I2C0_BASE, I2C_SLAVE_ADDRESS, false);
I2CMasterControl(I2C0_BASE, I2C_MASTER_CMD_SINGLE_RECEIVE);
g_ui32DataRx = I2CSlaveDataGet(I2C0_BASE);
```

図 25. I2C Master Receiving Code

Optionally, interrupts can be used to receive data.

8.1.2 I2C Slave

Initializing I2C Slave

To initialize the I2C slave functionality:

1. Enable the I2C peripheral.
2. Enable the clock gating to the SDA and SCL pins.
3. Choose the pin configuration for SCL and SDA pins.
4. Use internal pull up resistors when external pullup resistors are not available for SCL and SDA pins. (Since the Tiva Microcontroller is used as the I2C slave, use an external pull up on the slave side as well.)
5. Select *Slave Enable.*

Depending on the processor platform, the pin mapping changes. 図 26 is an example code snippet for I2C initialization.

```
void I2C0_init(void)
{
    uint32_t Status;

    SysCtlPeripheralEnable(SYSCTL_PERIPH_I2C0);
    SysCtlPeripheralReset(SYSCTL_PERIPH_I2C0);

    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB);
    SysCtlDelay(2);

    GPIOPinConfigure(GPIO_PB2_I2C0SCL);
    GPIOPinConfigure(GPIO_PB3_I2C0SDA);
    SysCtlDelay(2);
    //
    // Select the I2C function for these pins.  This function will also
    // configure the GPIO pins pins for I2C operation, setting them to
    // open-drain operation with weak pull-ups.  Consult the data sheet
    // to see which functions are allocated per pin.
    //
    GPIOPinTypeI2CSCL(GPIO_PORTB_BASE, GPIO_PIN_2);
    GPIOPinTypeI2C(GPIO_PORTB_BASE, GPIO_PIN_3);
    SysCtlDelay(2);

    I2CSlaveInit(I2C0_BASE, SLAVE_ADDRESS);
    I2CSlaveEnable(I2C0_BASE);

    Status=I2CMasterLineStateGet(I2C0_BASE);
}
```

図 26. I2C Slave Initialization Code

Sending Data on I2C

To send data on I2C bus: I2CSlaveDataPut(I2C0_BASE, ui32DataTx);

Checking the Slave Status

To check the slave status: Error_Status = I2CSlaveStatus(I2C0_BASE);

Receiving Data on I2C

To receive data from master on I2C bus: first_byte = I2CSlaveDataGet(I2C0_BASE);

8.2 SPI Communication Interface Between Master and Slave

The Tiva LaunchPad is used as master and slave. The SPI is configured to work up to 4Mbps. The SPI communication uses the following pins:

- /CS: Chip select used by the master to select the slave to initiate the communication
- SCLK: Clock generated by the master
- MISO: Pin used by the slave to transmit data and the master to receive
- MOSI: Pin used by the master to transmit data and the slave to receive

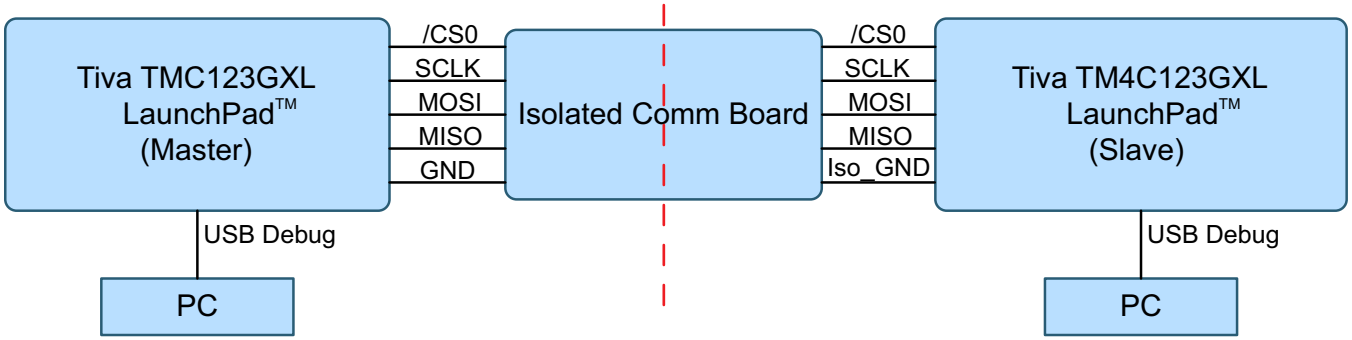

図 27. SPI Communication Test Setup

注: Host can also be referred as Master.

8.2.1 Initializing the SPI

To initialize the SPI:

1. Choose master or slave through the macro.
2. Enable clock gating to the SPI peripheral.
3. Enable and configure the GPIO peripheral pins for SPI mode (clock, chip select, RX and TX).
4. Set the SPI to master or slave mode and select the speed.
5. Enable the SPI module.

```
void SPI_Init(void)
{
    uint32_t pui32DataTx[NUM_SSI_DATA];
    uint32_t pui32DataRx[NUM_SSI_DATA];
    uint32_t ui32Index;

    SysCtlPeripheralEnable(SYSCTL_PERIPH_SSI0);
    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA);

    GPIOPinConfigure(GPIO_PA2_SSI0CLK);
    GPIOPinConfigure(GPIO_PA3_SSI0FSS);
    GPIOPinConfigure(GPIO_PA4_SSI0RX);
    GPIOPinConfigure(GPIO_PA5_SSI0TX);

    GPIOPinTypeSSI(GPIO_PORTA_BASE, GPIO_PIN_5 | GPIO_PIN_4 | GPIO_PIN_3 |
                   GPIO_PIN_2);

#ifdef MASTER
    SSIConfigSetExpClk(SSI0_BASE, SysCtlClockGet(), SSI_FRF_MOTO_MODE_0,
                       SSI_MODE_MASTER, 4000000, 8);
    Set_CS_Low(0);

#else
    SSIConfigSetExpClk(SSI0_BASE, SysCtlClockGet(), SSI_FRF_MOTO_MODE_0,
                               SSI_MODE_SLAVE, 1000000, 8);
#endif

    SSIEnable(SSI0_BASE);

// Receive data

    while(SSIDataGetNonBlocking(SSI0_BASE, &pui32DataRx[0]))
    {
    }
}
```

図 28. SPI Initialization Code

8.2.2 Sending Data on SPI

To send data on the SPI:

1. Ensure the slave chip select is enabled.
2. Send the data.
3. Wait until the data is transmitted.

```
// Initialize the data to send.

    pui32DataTx[0] = 's';
    pui32DataTx[1] = 'p';
    pui32DataTx[2] = 'i';


// Send 3 bytes of data.

    for(ui32Index = 0; ui32Index < NUM_SSI_DATA; ui32Index++)
    {
        // Send the data using the "blocking" put function.  This function
        // will wait until there is room in the send FIFO before returning.
        // This allows you to assure that all the data you send makes it into
        // the send FIFO.
        //
        SSIDataPut(SSI0_BASE, pui32DataTx[ui32Index]);
    }

    //
    // Wait until SSI0 is done transferring all the data in the transmit FIFO.
    //
    while(SSIBusy(SSI0_BASE))
    {
    }
```

図 29. SPI Data Sending Code

8.2.3 Receiving Data on SPI

To receive data on SPI, use the receive routine. Data can be received by either polling (in a blocking or non-blocking way) or using interrupts. 図 30 demonstrates blocking receive function.

```
//
// Receive 3 bytes of data.
//
for(ui32Index = 0; ui32Index < NUM_SSI_DATA; ui32Index++)
{
    //
    // Receive the data using the "blocking" Get function. This function
    // will wait until there is data in the receive FIFO before returning.
    //
    SSIDataGet(SSI0_BASE, &pui32DataRx[ui32Index]);

    //
    // Since we are using 8-bit data, mask off the MSB.
    //
    pui32DataRx[ui32Index] &= 0x00FF;


}
```

図 30. SPI Blocking Receive Function Code

9 Hardware, Testing Requirements, and Test Results

This section provides details of the setup and testing done on the TIDA-00300 reference design to validating the performance:

- Required hardware connection
- Test setup
- Functional testing and performance testing
- Waveforms

9.1 Required Hardware Connection

The following boards and equipment are required for validating the functionality and performance:

- TIDA-00300 power supply board for IO and communication modules with basic functional tests completed
- Programmable DC voltage source capable of varying the voltage between 5 V to 30 V with a programmable current limit up to 1 A
- Electronic load for testing the power-supply outputs
- Digital multimeter with sufficient resolution for measuring the DC output voltages

9.2 Test Setup for Synchronous Communication Board

Use the following setup to test the isolated and non-isolated power supply performance (see 図 31). DC power supply, electronic loads, multimeter, and CROs are used to check the power supply performance.

図 31. Test Setup for TIDA-00300

9.3 Testing and Results

Testing of the design includes the following:

- Functional testing
- Performance testing

9.3.1 Functional Testing

This section provides details of the functional tests performed, including observations.

9.3.1.1 Isolated Power Supplies for Communication Module

This section provides details of the tests done and the test observations for isolated power supplies using the DC/DC power module, transformer driver, and digital isolator with integrated power from a 5-V input

表 24. Isolated Power Supply for Communication Connection Details and Measurements

POWER SUPPLY INPUT	INPUT CONNECTOR	OUTPUT	MEASUREMENT (V)
5-V DC input	J7-1: input	C104: 5 V	5.15
	J7-2: Ground	TP51: 5 V	4.97
		TP53: 3.3 V	3.26
		TP52: Gnd	
	J1-1: input	TP2: 6 V	6.3
	J1-2: Ground	TP7: 3.3 V	3.255
		TP6: Gnd	
	J2-1: input	TP1: 6 V	6.1
	J2-2: Ground	TP8: 5 V	4.93
		TP5: Gnd	
	J8-1: input	TP55: P_13	13.1
	J8-2: Ground	TP59: N_13	13.1
		TP56: P_12	12.15
		TP60: N_12	12.08
		TP58: Gnd	
	J4-2: input	TP29: LS output	4.88
	J4-1: Ground	TP12: 5.4 V	5.42
		TP28: 5 V	5.02
		TP19: 3.3 V	3.31
	J6-1, J5-2: input	TP36: LS_Out	4.78
	J6-2: Ground	TP39: LS_Out1	4.78
		TP24: 5.4 V	5.38
		TP25: 5.4 V	5.38
		TP30: 3.3 V	3.28
		TP38: 3.3 V	3.28
		TP33: 5 V	5.01
		TP41: 5 V	4.95
		LED_23	OK
		LED_24	OK

9.3.1.1.1 Testing Isolated DC/DC Converter Functional Modes

This section provides details of different functional modes configured for isolated DC/DC converter UCC12050 and the observations.

表 25. Device Functional Modes and Observations

EN	SEL	ISOLATED SUPPLY OUTPUT VOLTAGE (VISO) SET POINT	LOAD CURRENT	INPUT CURRENT	MEASURED VOLTAGE
HIGH	Shorted to VISO	5.0 V	100	173	4.98
HIGH	Shorted to VISO	5.0 V	150	281	3.71
HIGH	100 kΩ to VISO	5.4 V	100	206	5.37
HIGH	100 kΩ to VISO	5.4 V	10	55	5.37
HIGH	100 kΩ to VISO	5.4 V	5	49	5.37
HIGH	Shorted to GNDS	3.3 V	100	152	3.28
HIGH	100 kΩ to GNDS	3.7 V	100	149	3.67
HIGH	OPEN	UNSUPPORTED			
LOW	X	0 V		0	0

9.3.1.1.2 Additional Isolated DC/DC Converter Testing

This section provides details of the tests performed on the isolated DC/DC using a current limited source.

表 26. Testing With Current Controller Source

INPUT VOLTAGE	CURRENT LIMIT (mA)	INPUT CURRENT (mA)	OUTPUT SELECTION	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)
5	50	.049	5	4.97	No load
5	50	.044	5.4	5.37	No load
5	120	.098	5	4.97	50
5	150	.101	5.4	5.37	50
5	230	.169	5	4.98	100
5	250	.194	5.4	5.37	100
5	230	.181	5	3.18	200
5	400	.242	5	0.05	short
5	400	.242	5.4	0.05	short

9.3.1.1.3 Testing Protection

This section provides details of the tests done for checking protection against input voltage variation.

表 27. Testing UVLO

ISOLATED SUPPLY OUTPUT VOLTAGE (VISO) SET POINT	MEASURED VOLTAGE
5.0 V	4.98
5.4 V	5.37
UVLO – rising	4.3
UVLO – falling	3.7

9.3.1.2 Wide Input Isolated Power Supply for Analog IO Modules

This section provides details of the tests done and the test observations for the split-rail power supplies generated using DC/DC from 24-V or 5-V input.

表 28. Isolated Power Supply for IO Connection Details and Measurements

POWER SUPPLY INPUT	INPUT	OUTPUT	MEASUREMENT (V)
5-V DC input	J1-1: Input	TP43: 5 V	4.996
	J1-2: Ground	J6-1: Ground	
24-V input DC/DC	J4-1: input	J6-2: 5 V	5.126
	J4-2: Ground	J6-1: Ground	
		TP1: +14 V	14.8
		TP2: –14 V	14.91
		TP29: +12 V	12.08
		TP31: –12 V	12.28
		R23: LDO+5 V	5.11
		R40: LDO-5 V	4.996
		TP6: REF_2.5V_A	2.501
		TP5: REF_2.5 V	2.494
		TP49: +3.3 V	3.288

9.3.1.3 Isolated Synchronous Communication With Split-Rail Fly-Buck™ Power

This section provides details of the tests done and the test observations for supply rails generated using 24-V input with DC/DC configured in Fly-Buck configuration.

表 29. Fly-Buck™ Test Results at 24-V and 5-V Input

POWER SUPPLY INPUT	INPUT	OUTPUT	MEASUREMENT (V)
24-V input	J2-1: input	J1-1: Iso_P_15V	15.27
	J2-6: Ground	J1-2: Iso_M_15V	14.87
		J1-3: Iso_P_5V	4.959
		TP10: Non_Iso_3.3V	3.22
		J1-4: Gnd	
	J2-2: /CS0	J3-2: /CS0_Iso	OK
	J2-3: SCLK	J3-3: SCLK_Iso	OK
	J2-4: MOSI	J3-4: MOSI_Iso	OK
	J2-5: MISO	J3-5: MISO_Iso	OK
	J2-7: SDA	J3-4: SDA_Iso	OK
	J2-8: SCL	J3-5: SCL_Iso	OK
5-V input DC/DC	J4-1: input	TP15: Iso1_P_15V	15.7
	J4-2: Ground	TP17: Iso1_N_15V	15.7
		TP20: Iso1_P_5V	5.06
		C58: Gnd_Iso1	

9.3.2 Performance Testing

This section provides details of the performance tests including EMI tests that were performed using TIDA-00300.

9.3.2.1 EMI Performance of DC/DC Converters With 24-V Input

The radiated emission for the DC/DC converter with the following configuration and 24-V input was tested:

- LM5160 configured to generate ±15 V and 5 V using the PMP10532 device
- LM5017 configured to generate ±15 V and ±5 V using the PMP7993 device

図 32 shows the radiated emission plot.

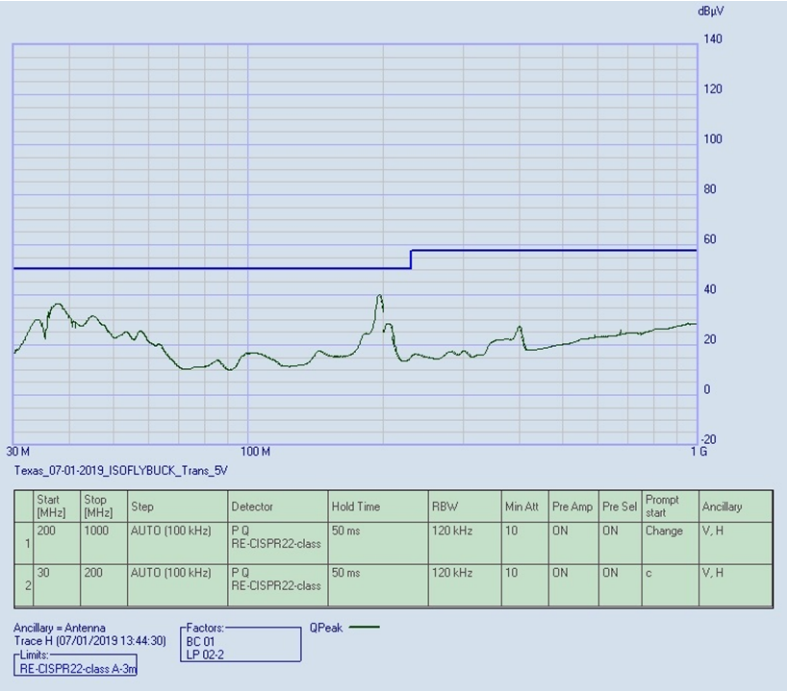

図 32. Wide Input DC/DC With Split-Rail EMI Plot

9.3.2.2 EMI Performance of DC/DC Converters With 5-V input Connected to J1, J2, J7

The radiated emission using a DC/DC converter with the following configuration was tested:

- DCR010505P configured for 5-V output loaded to 100-mA load
- DCP010505BP configured for 5-V output loaded to 100-mA load
- LP2985AIM5-3.3 configured for 3.3-V output loaded to 50-mA load
- SN6505B configured for 6-V output loaded to 200-mA load
- SN6501 configured for 6-V output loaded to 100-mA load
- TPS70933 configured for 3.3-V output and loaded to 50 mA
- TPS70950 configured for 5-V output and loaded to 50 mA

図 33 shows the radiated emission plot.

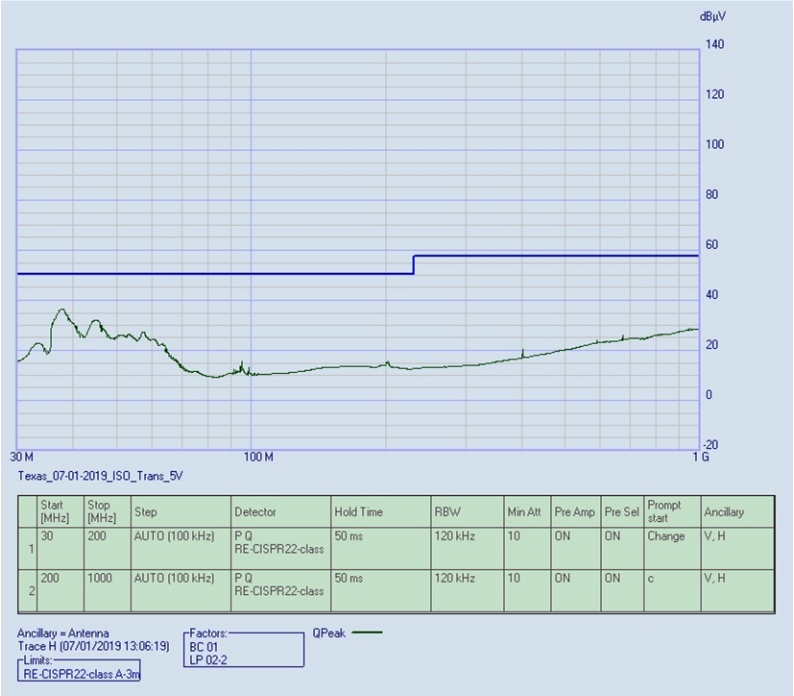

図 33. SN6505B + SN6501 + DCR010505 + LDO + RE

9.3.2.3 EFT and Surge Test Setup, TIDA-00300 Boards Test Method, Acceptance Criteria and Results

EFT and surge testing was done on the TIDA-00300 boards with the following test conditions:

- 240-V AC supply connected to the TIDA-00227 and TIDA-00227 reference design power-supply output connected to the TIDA-00300 boards

表 30 summarizes surge and EFT test results for TIDA-00300 boards connected to the output of the TIDA-00227 power supply with 240-V AC input.

表 30. Test Results for TIDA-00300 Boards Connected to TIDA-00227

TEST TYPE AND STANDARD	VOLTAGE LEVEL	MEASUREMENT BEFORE TEST	MEASUREMENT AFTER TEST
EFT IEC61000-4-4	±1 kV, 5 kHz, 100 kHz	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V
EFT IEC61000-4-4	±2 kV, 5 kHz, 100 kHz for 1 minute	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V
EFT IEC61000-4-4	±2.5 kV, 5 kHz, 100 kHz for 1 minute	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V
Surge, IEC61000-4-5	±1 kV, 2Ω, 5 pulses	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V
Surge, IEC61000-4-5	±2 kV, 2Ω, 5 pulses	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V
Surge, IEC61000-4-5	±2.5 kV, 2Ω, 5 pulses	12 V: 12.06 V, Iso_P_15V: 15.27 V	12 V: 12.06 V, Iso_P_15V: 15.27 V

9.3.2.4 Split-Rail Supply Output Testing With TIDA-00834 and TIDA-01633

A split-rail power supply of ±12 V is generated using the TPS65130 or SN6505B and TPS7A3901 devices. The power supply output was tested for performance in analog input module applications using the following setup:

- TIDA-00834 reference design board
- ADS8588SEVM-PDK

- Split-rail power supply board for analog IO module

Accuracy tests were performed using the split-rail power supply on the TIDA-00834 board, initially. The split-rail power supply was connected to the TIDA-00834 board and accuracy measurements were repeated. There was no variation in measurements. 表 31 provides the accuracy measurements with the supply from the power-supply board connected.

表 31. ADS8588S ADC-Based TIDA-00834 and TIDA-00300 Split-Rail Power Accuracy Test Results

CURRENT A	ADC INPUT (mV)	ACI-6 MEASUREMENT (mV)	ACI-6 % ERROR
0.2003	10.9609	10.970	0.081
0.5003	27.3775	27.395	0.065
1	54.7222	54.788	0.119
2.5	136.8056	136.961	0.114
5	273.6112	274.065	0.166
10	547.2224	547.771	0.100
20	1094.4449	1096.093	0.151
50	2736.1122	2739.645	0.129
80	4377.7795	4382.236	0.102
100	5472.2244	5480.198	0.146
120	6566.6693	6577.257	0.161
125	6840.2805	6849.696	0.138

The split-rail power supply output generated using the TPS65130 and TPS7A3901 devices was modified to generate ±13.5 V. The power-supply output was tested for performance in analog output module applications using the following setup:

- TIDA-01633 reference design board
- Power-supply board for analog IO module

Accuracy tests were done using external split-rail power supply on the TIDA-01633 board, initially. The split-rail power supply of the analog IO power supply board was connected to the TIDA-01633 board and accuracy measurements were repeated. There was no variation observed in measurements. 表 32 provides the accuracy measurements with the supply from the analog IO power-supply board connected

表 32. TIDA-01633 + TIDA-00300 Analog IO Power Interface

XTR305_Vout EXPECTED (V)	XTR305_Vout MEASURED (V)
–10.098	–10.081
–7.069	–7.057
–5.050	–5.042
–2.020	–2.017
–1.011	–1.009
0.000	0.000
1.010	1.008
2.019	2.015
5.049	5.039
8.077	8.062
10.097	10.078

9.3.2.5 Isolated Low-Speed Wired Communication Interface Testing

A communication test for RS-232, RS-485, and CAN interface was tested using EVMs, an MSP432 LaunchPad, and the Tera Term terminal emulator. Testing was done using a loop-back approach or by configuring one of the MSP432 LaunchPads as a transmitter and the other MSP432 LaunchPad as receiver. The 5-V or 3.3-V output from the isolated power supply for the communication module board was connected to the different EVMs and devices listed in 表 33 and tested for communication performance.

表 33. EVMs Used for Isolated Interface Testing and Observations

COMMUNICATION INTERFACES TESTED	EVMs USED	DEVICES	OBSERVATION
Isolated RS-485 half duplex interface	RS485-HF-DPLX-EVM , ISO7741EVM , ISO1410DWEVM, ISO1412DWEVM, ISO1500DBQEVM, MSP-EXP432P401R, UCC12050EVM-022 and isolated supply output from ISOW7841, SN6501, SN6505B, DCR010505, DCP010505, UCC12050 for communication module board	THVD1419, THVD1429, THVD1450, THVD1510, THVD1410, ISO1430, ISO1432, ISO1450, ISO1452 ,ISO1412, ISO1500	Testing done using all these transceivers listed and tested for communication performance at 9600 bps and 115000 bps and observed for communication error. No errors observed for 1500 8-byte packet transmission using byte checksum.
Isolated RS-485 full duplex interface	RS485-FL-DPLX-EVM, ISO7741EVM, MSP-EXP432P401R, UCC12050EVM-022 and isolated supply output from ISOW7841, SN6501, SN6505B, DCR010505, DCP010505, UCC12050 for communication module board	THVD1452, SN65HVD73, SN65HVD1470	Testing done using all these transceivers listed and tested for communication performance at 9600 bps and 115000 bps and observed for communication error. No errors observed for 1500 8-byte packet transmission using byte checksum.
Isolated CAN interface	TCAN1042DEVM, ISO7741EVM, ISO1042DWEVM, MSP-EXP432P401R, UCC12050EVM-022 and Isolated supply output from ISOW7841, SN6501, SN6505B, DCR010505, DCP010505, UCC12050 for communication module board	ISO1042, ISO1050, TCAN1042D, SN65HVD255, TCAN1051	Testing done using all these transceivers listed and tested for communication performance at 9600 bps and 115000 bps and observed for communication error. No errors observed for 1500 8-byte packet transmission using byte checksum.
Isolated RS-232	TRS3122E, EVM ISO7742EVM, TIDA-00557, MSP-EXP432P401R, UCC12050EVM-022 and Isolated supply output from ISOW7841, SN6501, SN6505B, DCR010505, DCP010505, UCC12050 for communication module board	TRS3122E, MAX3232, TRS3232, MAX202, TRSF3238, TRS3243E	Testing done using all these transceivers listed and tested for communication performance at 9600 bps and 115000 bps and observed for communication error. No errors observed for 1500 8 byte packet transmission using byte checksum.

9.4 Power Supply Test Results and Waveforms

9.4.1 Isolated Power Supply

表 34. Output Voltage Measurement

INPUT VOLTAGE	VOLTAGE (V)	LOAD CURRENT (mA)	MEASURED VOLTAGE (V)
24-V DC	Isolated 15	50	15.27
	Isolated –15	50	–14.87
	Isolated 5	100	4.959
	Non-isolated 3.3	10	3.2

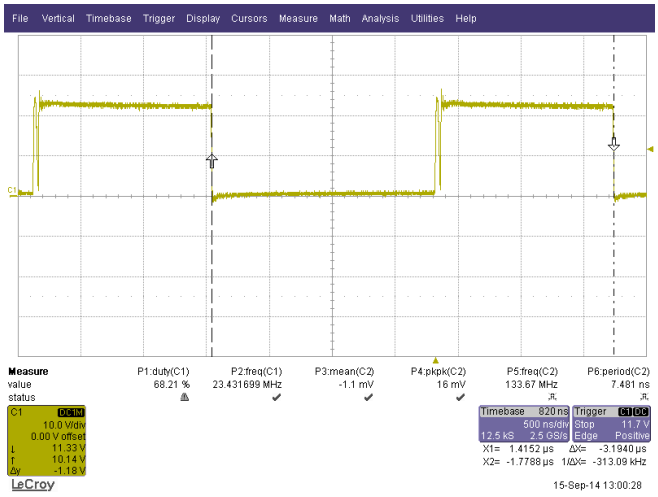

図 34. Full Load Switching Frequency

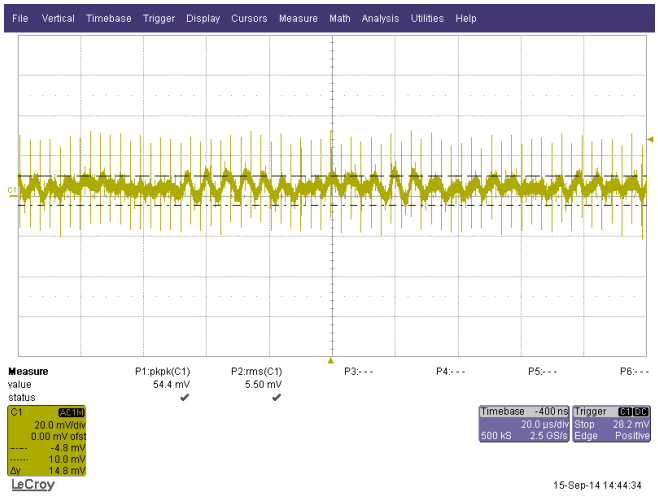

図 35. 15-V Ripple Full Load

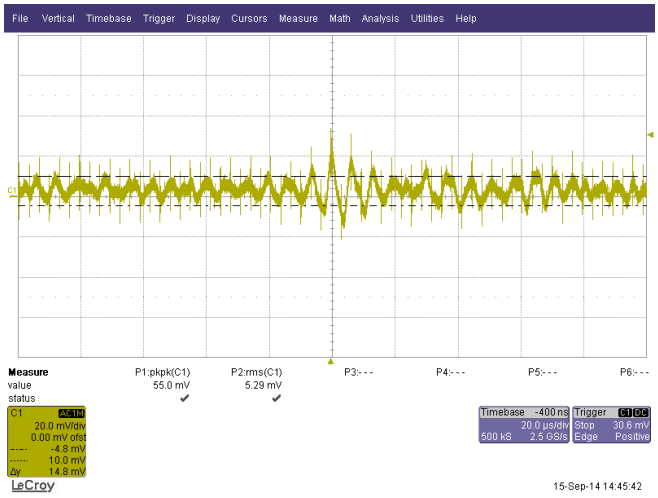

図 36. –15-V Ripple Full Load

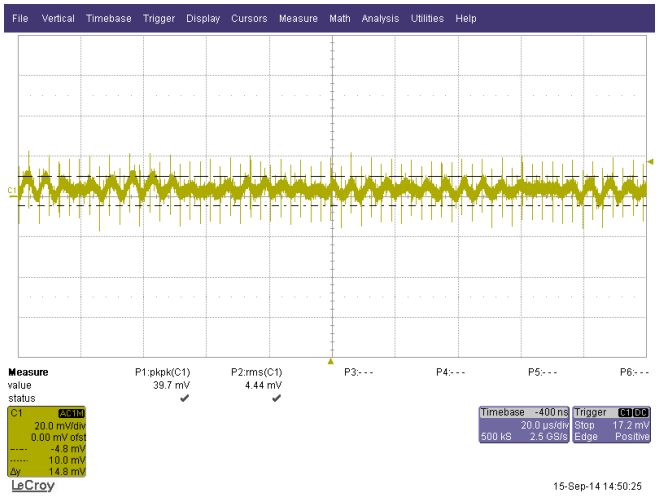

図 37. 5-V Ripple Full Load

9.5 Isolated SPI Communication Test Results

Both master and slave are set up (as shown previously). Data is transmitted by the SPI master and received by the SPI slave. The data speeds are configured as shown in 表 35. The sent and received data are the same.

表 35. SPI Test Result

SPEED	DATA COMMUNICATION RESULT
1 MHz	OK; No failure observed for > 50 transfer cycles
2 MHz	OK; No failure observed for > 100 transfer cycles
4 MHz	OK; No failure observed for > 100 transfer cycles

The design is successfully tested up to 4-Mbps speeds.

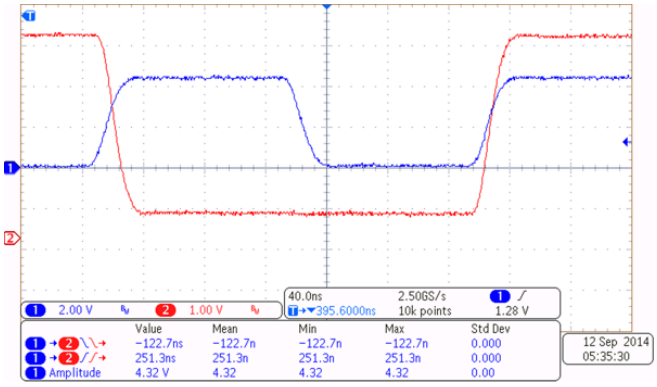

図 38. SPI: 4-Mbps Isolated — CLK (Blue) and MOSI (Red)

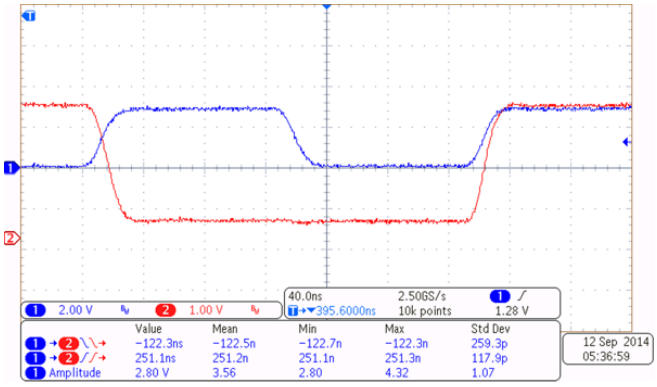

図 39. SPI: 4-Mbps Non-isolated — CLK (Blue) and MOSI (Red)

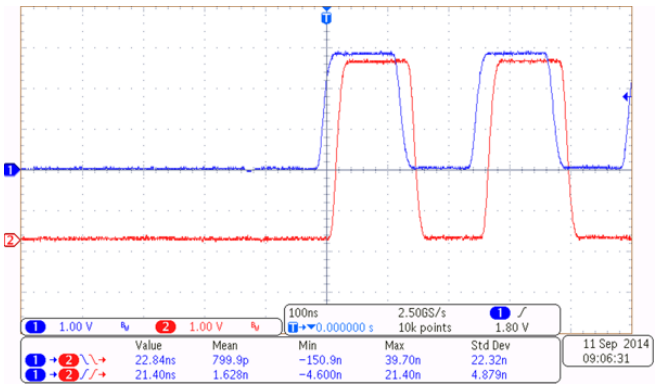

図 40. SPI Clock: Non-isolated (Blue) and Isolated (Red)

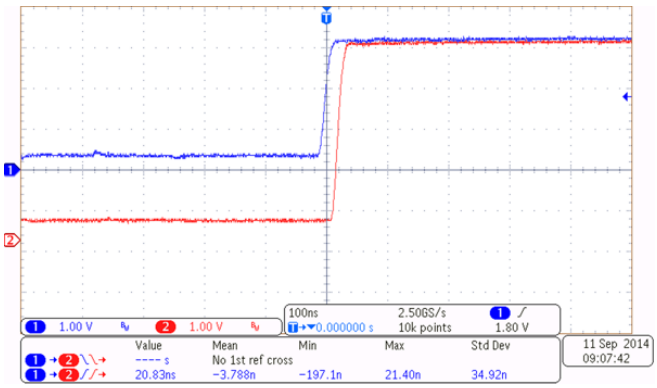

図 41. SPI SS: Non-isolated (Blue) and Isolated (Red)

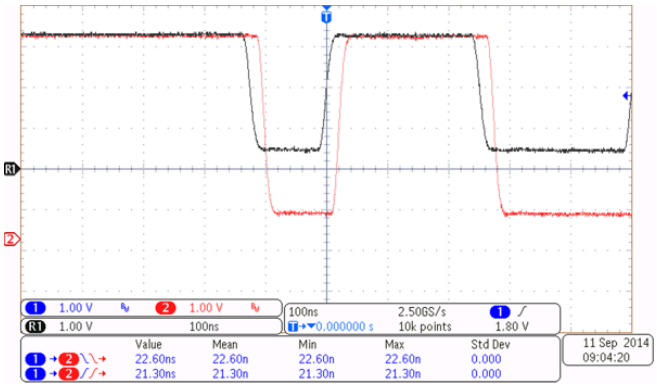

図 42. SPI MOSI: Non-isolated (Blue) and Isolated (Red)

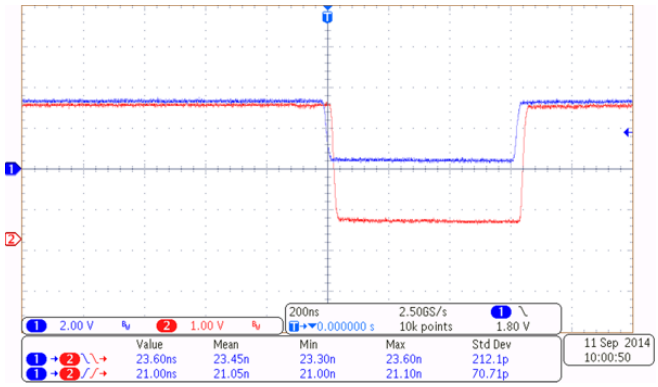

図 43. SPI MISO: Isolated (Blue) and Non-isolated (Red)

9.6 Isolated I2C Communication

Both master and slave are set up (as previously shown). Data is transmitted by the I2C master and received by the I2C slave without errors. The clock and data is observed on the oscilloscope. The sent and received data are the same.

表 36. I2C Test Result

SPEED	DATA COMMUNICATION RESULT
100 khz	OK; No failure observed for > 50 transfer cycles

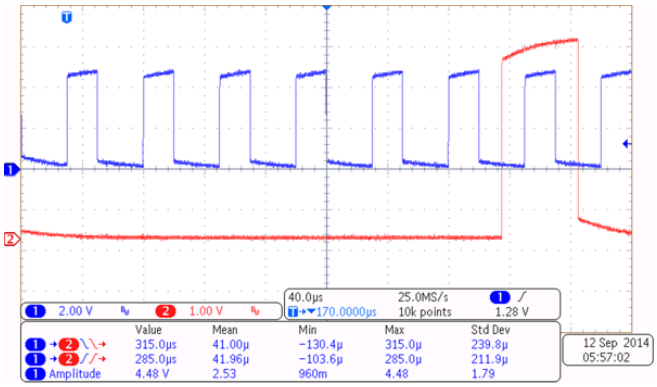

図 44. I2C 100 Kbps: Isolated SCL (Blue) and SDA (Red)

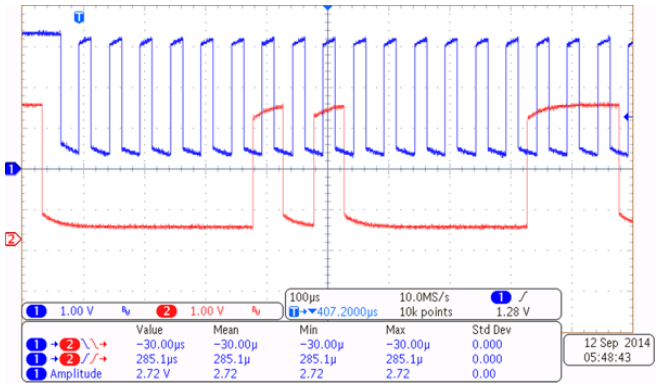

図 45. I2C 100 Kbps: Non-isolated SCL (Blue) and SDA (Red)

9.7 Summary of Test Results

This section summarizes the tests that were performed on the reference design and the observation of the tests

表 37. Summary of the Tests Performed and Observations

SERIAL NUMBER	PARAMETERS	OBSERVATION
1	Isolated split-rail supply output with DC/DC configured as Fly-Buck and 24-V input	OK
2	Isolated split-rail supply output using isolated DC/DC converter with 5-V input	OK
3	Isolated 5..4 V, 5 V, 3.7 V, 3.3 V and regulated 5 V and 3.3 V	OK
4	Isolated 5 V and 3.3 V using isolated DC/DC power module, transformer driver and digital isolator with integrated power	OK
5	Isolated power supply using a wide-input DC/DC, split-rail DC/DC and dual LDO	OK
6	Power supply diagnostics and indication	OK
7	Pre-compliance EMI/EMC testing as per CISPR22 and IEC61000-4-4, IEC61000-4-5	OK

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00300.

10.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00300.

10.3 Layer Plots

To download the layer plots for each board, see the design files at TIDA-00300.

10.4 Altium Project

To download the Altium Designer® project files for each board, see the design files at TIDA-00300.

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00300.

10.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00300.

11 Related Documentation

Texas Instruments, Digital Isolator Design Guide Developer's Guide

Texas Instruments, *Fly-Buck™ converter provides EMC and isolation in PLC applications analog applications journal*

Texas Instruments, *Overvoltage Protection for Isolated DC/DC Converter Tech Note*

Texas Instruments, *How to use isolation to improve ESD, EFT and surge immunity in industrial systems analog applications journal*

11.1 Related Reference Designs

Texas Instruments, *Small Form Factor 12W Ultra Wide Range Power Supply for Protection Relays - Reference Design*

11.2 商標

E2E, Fly-Buck, NexFET, Tiva, LaunchPad are trademarks of Texas Instruments.
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12 About the Author

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (June 2019) から **Revision B** に変更 **Page**

- 「*概要*」セクションを 変更 1
- 「*リソース*」セクションの製品を 変更 1
- 「*特長*」セクションを 変更 1
- *Isolated DC-DC Converter UCC12050 Advantages* section 追加 7
- information in *System Specifications for TIDA-00300* table 変更 8
- information in *Details of Functions and Devices Used for Implementing Power Supplies for Communication Module* table 変更 9
- a key requirement for designing the isolated power architecture for protection relay modules 追加 10
- *Isolated Power Supply Architecture for Communication Modules* image 変更 11
- *Generation of Isolated 5-V, 5.4-V, 3.3-V, or 3.7-V Supply Using Isolated DC/DC With Protection and Diagnostics* section 追加 12
- *Generation of Regulated DC Supplies With Protection and Diagnostics* section 削除 12
- *Generation of Isolated 5-V, 5.4-V, 3.3-V, or 3.7-V Supply Using Isolated DC/DC With Protection and Diagnostics* section 追加 15
- design functionality to *Isolated 5-V and 3.3-V Supply Generation Using Power Module* section 追加 15
- design functionality in *Isolated 5-V, 3.3-V and ±12-V Supply Generation Using Transformer Driver* section 変更 16
- design functionality and information to *Generation of Regulated DC Supplies With Protection and Diagnostics* section 追加 20
- information to *Isolated Power Supply for Communication Connection Details and Measurements* table 追加 52
- *Testing Isolated DC/DC Converter Functional Modes* section 追加 53
- *Additional Isolated DC/DC Converter Testing* section 追加 53
- *Testing Protection* section 追加 53
- information in *EVMs Used for Isolated Interface Testing and Observations* table 変更 58
- information in *Summary of the Tests Performed and Observations* table 変更 62

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- 「*概要*」セクションを 変更 1
- 「*リソース*」セクションの製品を 変更 1
- 「*特長*」セクションを 変更 1
- 「*アプリケーション*」セクション 変更 1
- a paragraph to the *Design Features* section. 追加 8
- the *TI Device Mapping to Reference Design Functionalities* section. 追加 9
- the *System Overview* section. 追加 10
- ISO7741 to the *Serial Peripheral Interface (SPI)* section. 追加 25
- a **NOTE** after the *ISO7141CC Critical Parameters* table. 追加 38
- content and several sections to the *Hardware, Testing Requirements, and Test Results* section. 追加 51

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