参考資料

デザイン・ガイド: TIDA-010056
3 相 BLDC 駆動用 54V、1.5kW、効率 99% 超、70×69mm^2 電力段のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このデザイン・ガイドでは、コードレス・ツールで 3 相のブラシレス DC モータを 15 セルのリチウムイオン・バッテリから最高 63V の電圧で駆動する、1.5kW 電力段を紹介します。この 70mm x 69mm の小型ドライブは、スイッチング周波数 20kHz、ヒートシンクなし、自然対流で 25A RMS の連続電流を供給し、センサによる台形波制御を実現します。MOSFET と PCB を最適化したスマート・ゲート・ドライバを使用することで、MOSFET のスイッチング損失と EMI を最適化できます。また、VDS 監視による MOSFET の過電流およびシュートスルー保護、ゲート保護、スルーレート制御によるスイッチング電圧スパイクの最適化、過熱保護など、強化された保護機能により、MOSFET が安全動作領域内で動作できます。

リソース

TIDA-010056	デザイン・フォルダ
DRV8350R	プロダクト・フォルダ
CSD19536KTT	プロダクト・フォルダ
INA180	プロダクト・フォルダ
MSP430FR2355	プロダクト・フォルダ
TMP235	プロダクト・フォルダ
TPS709	プロダクト・フォルダ

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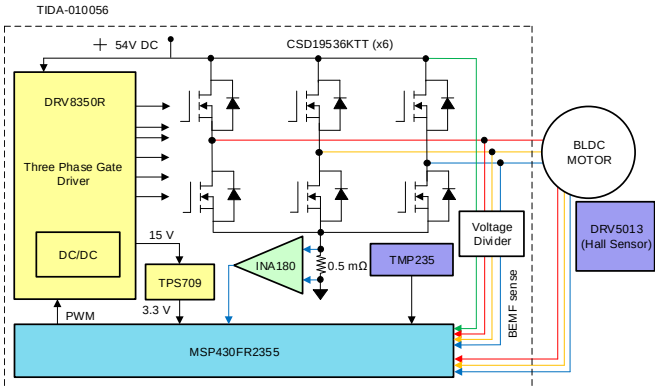
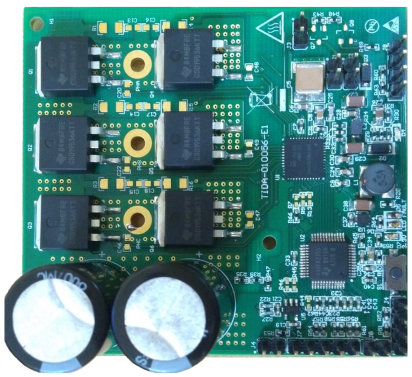
特長

- 9V～63V (15 セル・リチウムイオン・バッテリ) の電圧範囲で動作し、25A$_{RMS}$ の連続電流、400A のピーク電流を供給
- 70mm x 69mm の小型の PCB、ヒートシンクなしで 54V/1.5kW、25A$_{RMS}$ をサポート
- センサあり/センサなし両方の台形波制御をサポートする設計
- 54V/1.5kW で 99% 超の効率により、20kHz のユニポーラ台形波制御を実現
- VDS センシングによる、応答時間 1µs 未満、グリッチ除去時間 4µs の MOSFET 過電流保護で誤トリップを防止
- VGS 低電圧、過電圧、ゲート・ソース間短絡、および開回路保護といった強化された MOSFET ゲート保護機能
- 動作周囲温度:-20℃～55℃

アプリケーション

- コードレス電動工具
- コードレス・ハンドヘルド園芸用器具
- 電動自転車
- 芝刈り機





1 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors.

Cordless tools use battery power to drive DC motors. Most cordless tools use lithium-ion batteries, the most advanced in the industry offering high-energy density, low weight, and greater life. Power tools are available in different power levels and battery voltage levels. High power tools like chain saws, circular saws, high torque drills, garden tools, and lawn mowers often use up to 15-cell Li-ion pack battery to enable high power capability.

Cordless tools use brushed or brushless DC (BLDC) motors. The BLDC motors are more efficient and have less maintenance, low noise, and longer life. Power tools have requirements on form factor, efficiency, peak current, reliability, and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. The small form factor of the power stage enables flexible mounting, better PCB layout performance, and low-cost design. High efficiency provides maximum battery duration and reduces cooling efforts. The high-efficiency requirement in turn asks for switching devices with a low drain-to-source resistance (RDS_ON). The power stage must also take care of protections like motor stall or any other chances of high current.

This design guide uses the CSD19536KTT NexFET™ featuring a very low R_{DS_ON} of 2 mΩ in D2PAK package with an optimized gate charge and switching performance. The three-phase gate driver DRV8350R is used to drive the three-phase MOSFET bridge, which can operate from 9 to 100 V and support programmable gate current with maximum setting of 2-A sink / 1-A source. The DRV8350R uses smart gate drive (SGD) architecture to decrease the number of external components that are typically necessary for MOSFET slew rate control and protection circuits. The DRV8350R devices integrate a 350-mA buck regulator.

The INA180A3 integrated current sense amplifier is used to sense the low side DC bus current, at a gain of 100V/V with very low gain error. The TMP235 temperature sensor is used to sense the FET temperature. The MSP430FR2355 microcontroller is used to implement the control algorithm. The design has motor back emf sensing circuits and DC bus voltage sensing circuit for sensorless control using the smart analog combo of MSP430FR2355.

The test report evaluates the RMS current capability, peak current capability, efficiency and thermal performance of the board, FET switching waveforms, and over current protection

1.1 Key System Specifications

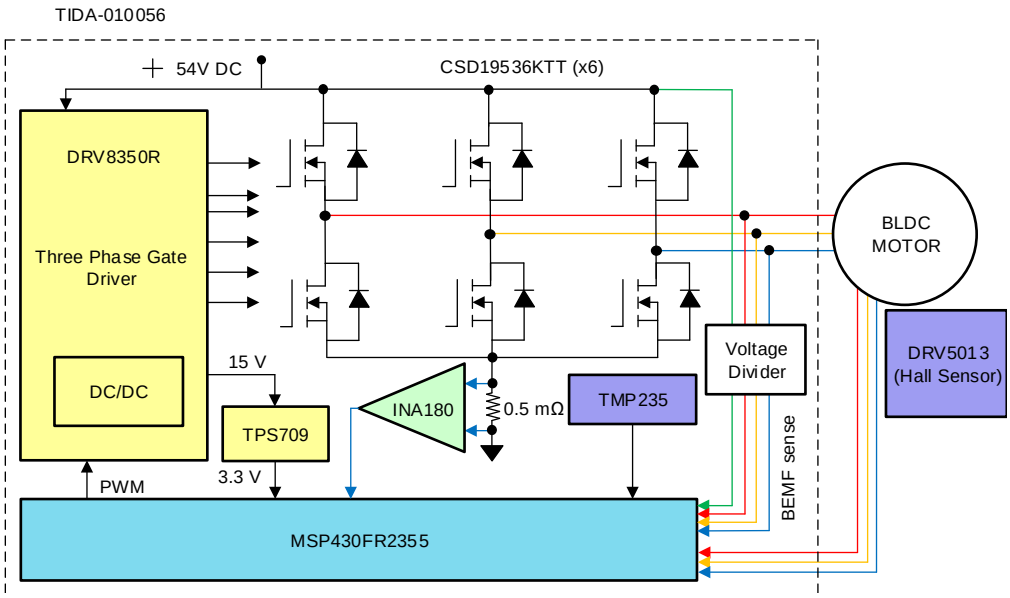
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	54-V typ (9-V min to 63-V max)
Rated output power	1.5-kW
RMS winding current	27-A (20-kHz switching)
Peak winding current	400-A
Inverter switching frequency	20-kHz (Tunable for 5-100kHz)
Operating ambient	–20 ^{O}C to 55^{O}C
Efficiency	>99% at 54-V, 1.5-kW, 20-kHz unipolar trapezoidal PWM
Board specification	70mm x 69mm, 4-layer, 2-Oz copper
Feedback signals	DC bus voltage, Motor phase voltages, Motor position Hall sensors, Low side DC bus current
Protections	Cycle-by-cycle over current, input under-voltage, over temperature, MOSFET gate-source open circuit and short circuit
Cooling	Natural cooling only, no heat sink
Control method	Sensor-based & sensorless trapezoidal

2 System Overview

2.1 Block Diagram

図 1. TIDA-010056 Block Diagram



2.2 Design Considerations

This reference design implements a 54-V, 1.5-kW three-phase inverter with smart gate driver for cordless tools, lawn mowers and e-bikes. The design is done and tested up to 1.5kW with 54-V DC input by driving a BLDC motor at 20 kHz PWM cycle.

The reference design has the following sub-blocks.

- Three-phase power stage including gate drivers and FETs
- Motor Position sensor (three hall latches) interface for sensored trapezoidal control
- DC bus voltage sensing and all the three phase node voltage sensing circuit to implement sensorless trapezoidal control
- DC bus low side current sensing for torque control and software current limit by MCU
- Board power supply generation including 15 V and 3.3 V from the 54 V line
- MOSFET temperature sensing using on board temperature sensor
- Host controller to implement the necessary motor control algorithms, sensing and protections

For detailed design considerations and calculations refer 2.4

2.3 Highlighted Products

2.3.1 DRV8350R

The key requirements in selecting the gate driver are:

- Three-phase gate driver with a high level of integration to reduce the PCB form factor and hence PCB parasitics and cost
- Sufficient gate source and sink current to reduce the switching losses

- Sufficiently high gate drive voltage to enable the MOSFET conducts at the minimum R_{DS_ON}
- High level of overcurrent and other protections to enable a reliable system operation under worst case conditions like motor stall, short circuit, and so on

The 9- to 100-V three phase half bridge gate driver DRV8350R three-phase gate driver can be used to meet these requirements. The device provides three half-bridge drivers, each capable of driving one high-side and one low-side N-channel MOSFET. The DRV8350R generates the proper gate voltage drive for both the high-side and low-side FETs using a charge pump. The DRV8350R supports up to a 1-A source and 2-A sink peak gate drive current capability. The DRV835x uses smart gate drive (SGD) architecture to decrease the number of external components that are typically necessary for MOSFET slew rate control and protection circuits. The SGD architecture also optimizes dead time to prevent shoot-through conditions, provides flexibility in decreasing electromagnetic interference (EMI) by MOSFET slew rate control, and protects against gate short circuit conditions through VGS monitors. A strong gate pulldown circuit helps prevent unwanted dV/dt parasitic gate turn on events. The DRV8350 protects against external MOSFET over current and short circuit by sensing the drain to source voltage (VDS) of all the MOSFETs. The gate driver supports 100% duty cycle. The DRV8350R devices integrate a 350-mA buck regulator that can be used to power an external controller or other logic circuits. The buck regulator is implemented as a separate internal die that can use either the same or a different power supply from the gate driver.

2.3.2 CSD19536KTT

The key requirements in selecting the MOSFET include:

- High efficiency (MOSFET with low losses under operating conditions)
- Small size to reduce the solution form factor
- Better heat dissipation
- High peak current capability
- Better switching performance to ensure reliable operation under short circuit or worst case switching conditions

The design guide uses six CSD19536KTT MOSFETs to implement the three phase inverter meeting the said requirements. The MOSFET is rated up to 100-V, having a very low R_{DS_ON} of 2-mΩ in a D2PAK (TO-263).

2.3.3 INA180

The design requirements in selecting the current sense amplifier are:

- The current sense amplifier (CSA) should be designed for high gain to reduce the shunt resistor value and hence the shunt resistor losses
- The CSA should have enough bandwidth and slew rate to enable fast output voltage settling for the designed gain. The design targets for less than 5-µs full swing settling time for DC bus current sensing in BLDC trapezoidal control with 20kHz PWM frequency
- The CSA should have very low gain error, offset error and offset drift to ensure that the output error is low enough to get a torque control (current control) error less than 1%.
- The CSA circuit should take only small PCB area to help in PCB size reduction

This reference design uses the integrated current sense amplifier INA180A3 with a gain of 100 V/V with a bandwidth of 150 kHz. The device has a very low gain error less than ±1%, offset voltage of <±150 µV at VCM = 0 V and less than 1-µV/°C offset drift.

The INA180, INA2180, and INA4180 (INAx180) current sense amplifiers are designed for cost-optimized applications. These devices are part of a family of current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to +26 V, independent of the supply voltage. The INAx180 integrate a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift. All these devices operate from a single 2.7-V to 5.5-V power supply. The INA180 is available in a 5-pin, SOT-23 package with two different pin configurations. All device options are specified over the extended operating temperature range of –40°C to +125°C.

2.3.4 TPS709

The key requirements in selecting the linear regulator are:

- Support wide input voltage to support 15V to 3.3V conversion.
- Average current support of more than 50mA, thermal pad package for better heat dissipation.
- Ultra low Iq (1uA) to enable the use in battery powered applications

The design uses the 3.3V output linear regulator TPS70933, with a rated input voltage up to 30V. The TPS709xx series of linear regulators are ultra-low, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical. The TPS709xx series is available in WSON-6 and SOT-23-5 packages.

2.3.5 TMP235

The reference design uses TMP235A4 analog output low cost temperature sensor supporting wide temperature measurement range: – 40°C to +150°C with a typical accuracy of ±1°C. The TMP23x devices are a family of precision CMOS integrated-circuit linear analog temperature sensors with an output voltage proportional to temperature. These temperature sensors are more accurate than similar pin-compatible devices on the market, featuring typical accuracy from 0°C to +70°C of ±0.5°C and ±1°C. The TMP235 device provides a positive slope output of 10 mV/°C over the full –40°C to +150°C temperature range and a supply range from 2.3 V to 5.5 V. The higher gain TMP236 sensor provides a positive slope output of 19.5 mV/°C from –10°C to +125°C and a supply range from 3.1 V to 5.5 V. The 9-µA typical quiescent current and 800-µs typical power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered devices. A class-AB output driver provides a strong 500-µA maximum output to drive capacitive loads up to 1000 pF and is designed to directly interface to analog-to-digital converter sample and hold inputs. With excellent accuracy and a strong linear output driver, the TMP23x analog output temperature sensors are cost-effective alternatives to passive thermistors.

2.3.6 MSP430FR2355

MSP430FR215x and MSP430FR235x microcontrollers (MCUs) are part of the MSP430™ MCU value line portfolio of ultra-low-power low-cost devices for sensing and measurement applications. MSP430FR235x MCUs integrate four configurable signal-chain modules called smart analog combos, each of which can be used as a 12-bit DAC or a configurable programmable-gain Op-Amp to meet the specific needs of a system while reducing the BOM and PCB size. The device also includes a 12-bit SAR ADC and two

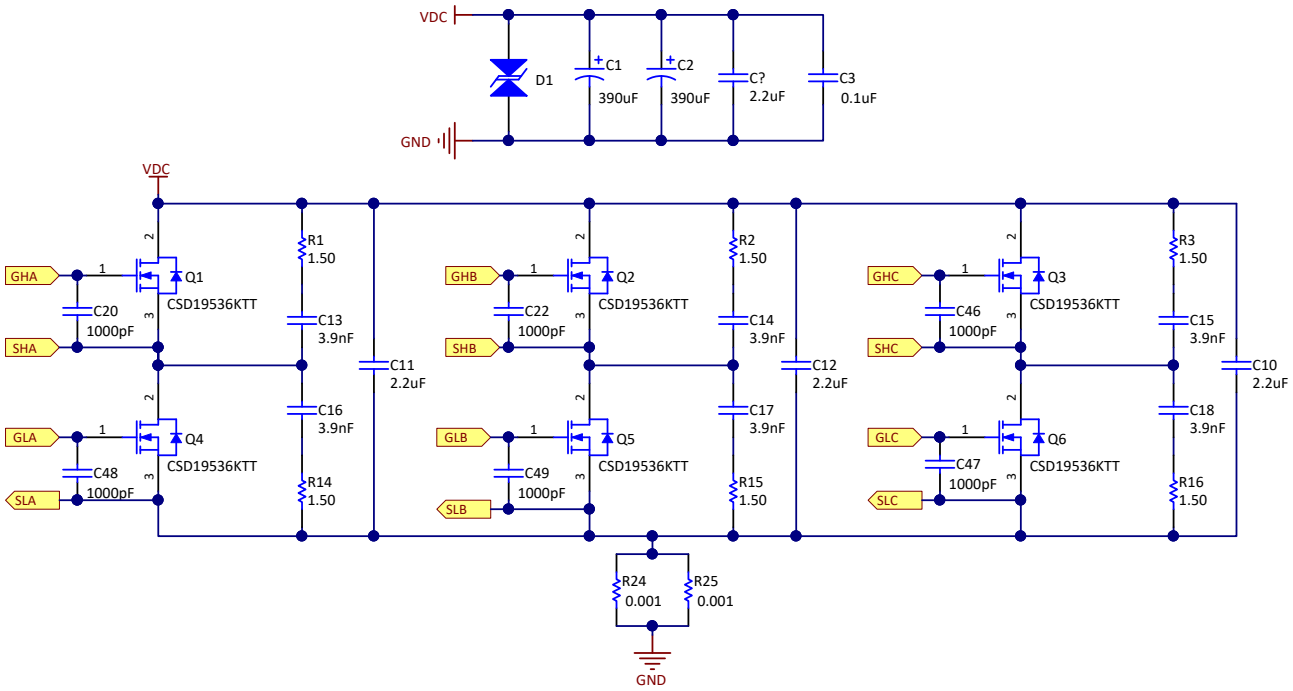
comparators. The MSP430FR215x and MSP430FR235x MCUs all support an extended temperature range from –40° up to 105°C, so higher temperature industrial applications can benefit from the devices' FRAM data-logging capabilities. The extended temperature range allows developers to meet requirements of applications such as smoke detectors, sensor transmitters, and circuit breakers. The MSP430FR215x and MSP430FR235x MCUs feature a powerful 16-bit RISC CPU, 16-bit registers, and a constant generator that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode typically in less than 10 µs. The MSP430 ultra-low-power (ULP) FRAM microcontroller platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

2.4 System Design Theory

2.4.1 Power Stage Design: Three-Phase Inverter

The three-phase inverter is realized using six D2PAK MOSFETs CSD19536KTT as shown in 図 2. The MOSFET is rated for a maximum drain to source voltage of 100V and a peak current of 400A. The design has provision to use RC snubber across all the FETs. The design is tested with synchronous unipolar trapezoidal PWM as shown in 図 25. The voltage ringing is expected to be maximum across the FETs due to diode reverse recovery. With unipolar trapezoidal control we may not need snubber across all the FETs and the need depends on the current direction, PWM strategy and diode reverse recovery. For more details refer 3.2.2.6.

図 2. Schematic of Three-Phase MOSFET Inverter



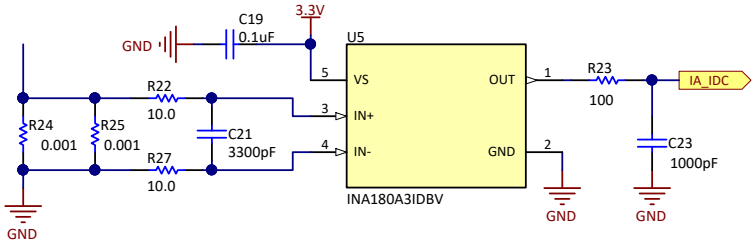
The snubber capacitor is selected as approximately two times the output capacitance of the FET. The snubber resistor value is tuned during board testing to sufficiently damp the VDS switching over shoot ringing during switching. C10, C11 and C12 are decoupling capacitors between the VDC input and the source terminal of bottom FET of each leg. This decoupling capacitor reduces the ringing in the supply lines caused due to the parasitic inductance added by the sense resistor and the power track. The design also have optional external capacitance between the gate to source of each FET, to reduce the gate pick up or gate ringing during switching. However this capacitors are not mounted during testing with the help from the smart gate drive architecture of DRV8350R.

注: Connect the RC snubber components very close to each FET in the same PCB layer as the FET, to ensure best snubbing action. Similarly place the decoupling capacitors very near to the corresponding MOSFET legs for better decoupling, ideally in the same layer. An improper layout or position of the snubber and decoupling capacitors can cause undesired VDS switching voltage spikes.

2.4.2 Current Sense Amplifier

The design uses the low side DC bus leg current sensing using the current sense amplifier INA180A3. 図 3 shows the current sense amplifier circuit.

図 3. Current Sense Amplifier Circuit



R24 and R25 in parallel forms the sense resistors. The power dissipation, amplifier gain bandwidth product (required settling time) and the input offset error voltage of the op amps are important in selecting the sense resistance values. The sense resistors are designed to carry a total nominal RMS current of 30 A with a peak current of 60 A for 2 seconds. A lower gain of the amplifier asks for high sense resistance value causing increased power loss in the resistors.

INA180 offers a very low offset voltage of ±150 µV (max) at VCM = 0 V. The gain error is ±1% gain error (max) with 1-µV/°C offset drift (max). The low offset voltage, low gain error and low drift allow to design the current sense amplifier at very high gain (ex: 100V/V) with very minimum amplifier output steady state error. INA180A3 offers a bandwidth of 150kHz at a gain of 100V/V, along with a slew rate of 2V/us ensure that for a full swing step change in current through the sense resistor (during FET switching), the transient settling time of the current sense amplifier is less than 5us.

The high gain of 100V/V with minimum output error helps to use a very low value sense resistor with low power loss. The design guide uses 0.5-mΩ sense resistor (two 1-mΩ in parallel) to enable unipolar current sense range of 0 - 66A peak for a full swing voltage of 3.3V using 式 1.

With gain = 100V/V, R_{SENSE} = 0.5 mΩ, V_{SCALE} = 3.3V, I_{SCALE} = 66A.

$$V_{OUT} = I_{SENSE} \times R_{SENSE} \times A_{GAIN} \quad (1)$$

The power loss in the sense resistor can be calculated using 式 2.

$$P_{LOSS} = I_{SENSE,RMS}^{2} \times R_{SENSE} \quad (2)$$

At 30ARMS current, P_{LOSS} = 0.45 W

注: If faster settling time is required, INA180A2 can be used (with a bandwidth of 210kHz, and slew rate of 2V/us) having a gain of 50V/V. With INA180A2, increase the sense resistor value to utilize the available full swing voltage capability of INA180A2 and the ADC.

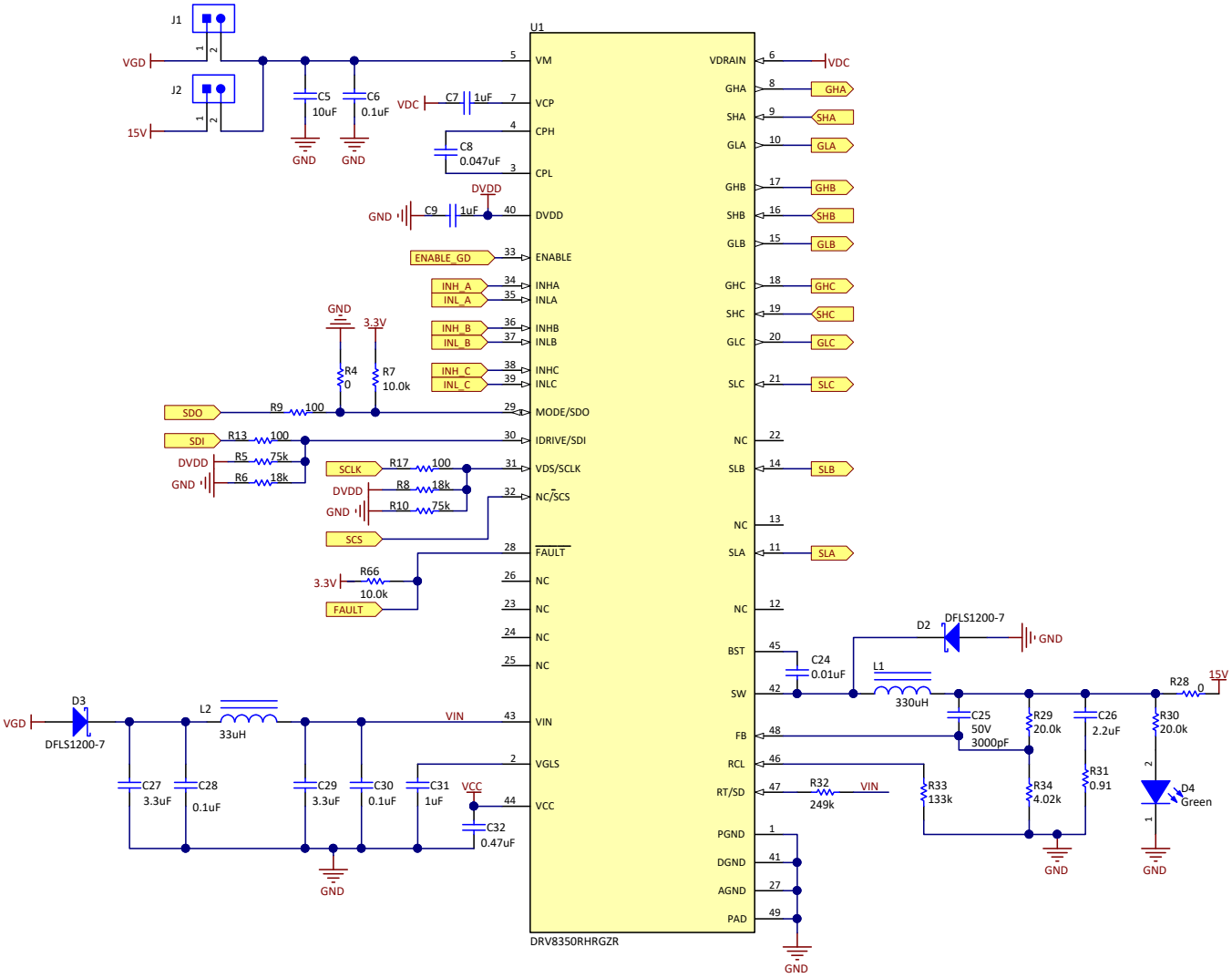
The input filter resistors R22 and R27 can create a small gain error in the amplifier circuit as these resistors add to the input resistance of amplifier. The gain error has to be taken in to account while selecting the filter resistor values.

2.4.3 Power Stage Design: DRV8350R Gate Driver

図 4 shows the schematic of the DRV8350R gate driver circuit. C5 and C6 are the ceramic capacitors at the gate driver power supply input, as recommended by the data sheet. The DRV835x gate drivers can operate in either a single or dual supply architecture. In the single supply architecture, VM can be tied to VDRAIN and is regulated to the correct supply voltages internally. In the dual supply architecture, VM can be connected to a lower voltage supply from a more efficient switching regulator to improve the device efficiency. VDRAIN stays connected to the external MOSFETs to set the correct charge pump and overcurrent monitor reference. This design guide uses the dual supply architecture, where the VM supply of DRV8350R is powered from 15V generated by the integrated DC/DC converter (LM5008A) of DRV8350R. Any one of the jumpers J1 or J2 can be closed externally to select the gate driver power supply. The maximum allowed gate power supply voltage is 80V. The design is tested with15V as the gate driver power supply, which will ensure that the quiescent current consumption is minimum compared to powering up the VM pin with DC input (specified for a maximum of 63V).

The capacitors C7, C8, C9 and C31 are the recommended capacitors at the charge pump pins, DVDD and VGLS pins.

図 4. Schematic of DRV8350R Gate Driver Circuit



2.4.3.1 *Average gate current calculation*

The average current from the high side pump charge pump (VCP) and the low side gate drive regulator power supply (VGLS) can be calculated using 式 3, applicable for 120 degree conduction trapezoidal control.

$$I_{VCP/VGLS} = Q_G \times f_{PWM} \quad (3)$$

Where, Q_G = 118 nC (Total gate charge of the MOSFET used (CSD19536KTT))

f_{PWM} = 20kHz (switching frequency), I_{VCP}/V_{GLS} > 118 nC x 20 kHz = 2.36mA

The charge pump and VGLS regulator power supply average current is well below the data sheet specified value of 25mA at a V_{VM} of 15V. If using 100 kHz PWM, the average current is 11.8 mA.

2.4.3.2 Gate driver peak source and sink current calculation

IDRIVE needs to be tuned in the application based on the required VDS slew rate. The MOSFET CSD19536KTT has a gate to drain gate charge (Q_{GD}) of 17 nC. The peak gate source current (IDRIVEP) to get a rise time trr, can be calculated as IDRIVEP > Q_{GD}/trr. To get a rise time of 50ns to 200ns, the IDRIVEP has to selected to be between 340mA and 85 mA. The gate drive sink current IDRIVEN for the required MSOFET switching fall time can be calculated in a similar way.

2.4.3.3 Selecting the current limit threshold using VDS protection

The VDS monitors are configured based on the worst-case motor current and the R_{DS_ON} of the external MOSFETs as shown in 式 4.

$$V_{DS\_OCP} > I_{max} \times R_{DS\_ON(max)} \quad (4)$$

As per the CSD19535KTT data sheet, the R_{DS_ON} value is approximately 1.6 times higher at 120°C compared to that at 25°C, and the maximum R_{DS_ON} value at a VGS of 10 V is 2.4 mΩ at T_A = 25°C. From these values, the approximate worst-case value of R_{DS_ON} is 1.6 × 2.4 mΩ = 3.84 mΩ. In order to get an over current threshold of 100A, the required VDS monitor trip point can be calculated using 式 4. V_{DS_OCP} > 100 A x 3.84 mΩ = 0.384 V.

The design guide provides provision for selecting different VDS monitor trip values.

2.4.3.4 DRV8350 Power Loss Calculation

The internal power dissipation of DRV8350 has four primary components:

- VCP Charge pump power dissipation (P_{VCP})
- VGLS low-side regulator power dissipation (P_{VGLS})
- VM device nominal power dissipation (P_{VM})
- VIN buck regulator power dissipation (P_{BUCK})

The value of P_{VCP} and P_{VGLS} can be approximated calculated by first calculating the I_{VCP} and I_{VGLS} required for the external MOSFET and then using 式 5 and 式 6.

$$P_{VCP} = I_{VCP} \times \left(V_{VM} + V_{VDRAIN}\right) \quad (5)$$

$$P_{VGLS} = I_{VGLS} \times V_{VM} \quad (6)$$

The value of P_{VM} can be calculated by referring to the data sheet parameter for I_{VM} current and 式 7.

$$P_{VM} = I_{VM} \times V_{VM} \quad (7)$$

The value of P_{BUCK} can be calculated with the buck output voltage (V_{VCC}), buck output current (I_{VCC}), and by referring to the typical characteristic curve for efficiency (η) in the LM5008A data sheet using 式 8.

$$P_{BUCK} = \left(P_O / \eta\right) - P_O \quad (8)$$

The total power dissipation is then calculated by summing the four components as shown in 式 9.

$$P_{tot} = P_{VCP} + P_{VGLS} + P_{VM} + P_{BUCK} \quad (9)$$

Use 式 5, 式 6, 式 7, 式 8, and 式 9 to calculate the value of P_{tot} for V_{VM} = 15V, V_{VDRAIN} = 54 V, I_{VM} = 9.5 mA, I_{VCP} = 2.36 mA, I_{VGLS} = 2.36 mA, V_{VCC} = 15 V, I_{VCC} = 100 mA, and η = 86 %.

P_{VCP} = 162.84 mW, P_{VGLS} = 35.4mW, P_{VM} = 142.5 mW, P_{BUCK} = 210mW

P_{tot} = 550.74 mW

The device junction temperature can be estimated by referring to the Thermal Information and 式 10.

$$T_{Jmax} = T_{Amax} + \left(R_{\theta JA} \times P_{tot}\right) \quad (10)$$

T_{Amax} is the maximum ambient temperature, $R_{\theta JA}$ is the junction to ambient thermal resistance of the DRV8350R package. Use 式 10 to calculate the value of T_{Jmax} for T_{Amax} = 55°C, $R_{\theta JA}$ = 26.6°C/W for the RGZ package, and P_{tot} = 0.551 W

T_{Jmax} = 55 + (26.6 x 0.551) = 69.65°C

2.4.3.5 Step-Down Buck Regulator of DRV8350

The DRV8350R have an integrated buck regulator (LM5008A) to supply power for an external controller or system voltage rail. This design uses the integrated buck regulator to generate 15 V from battery input supply. The diode D3 ensures that the battery voltage dips during load transients will not affect the performance of the integrated DC/DC converter of DRV8350R. The LM5008A regulator is an easy-to-use buck (step-down) DC-DC regulator that operates from 6-V to 95-V supply voltage. With integrated buck power MOSFET, the LM5008A delivers up to 350-mA DC load current with exceptional efficiency and low input quiescent current in a very small solution size. The DC/DC incorporates other features for comprehensive system requirements, including VCC undervoltage lockout (UVLO), gate drive undervoltage lockout, maximum duty cycle limiter, intelligent current limit off-timer, a pre-charge switch, and thermal shutdown with automatic recovery.

表 2 shows the design specification of the DC/DC for this design guide.

表 2. Specification of Buck Converter

CONDUCTION MODE	FIXED FREQUENCY PWM CONTROL
Output Voltage	15 V
Input Voltage	6 - 72 V
Transient Response 50 to 150mA load step	ΔVOUT = 4%
Maximum Output Current	150 mA
Output Voltage Ripple	0.5% of VOUT
Switching Frequency	500kHz

The LM5008A operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. At light loads, the conversion efficiency is kept because the switching losses decrease with the reduction in load and frequency. The discontinuous operating frequency can be calculated with 式 11.

$$F = \left(\frac{V_{OUT}^{2} \times L \times 1.04 \times 10^{20}}{R_L \times \left(R_T\right)2} \right) \quad (11)$$

where, RL = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. The approximate continuous mode operating frequency can be calculated with 式 12.

$$F = \left(\frac{V_{OUT}}{1.385 \times 10^{-10} \times R_T} \right) \quad (12)$$

The output voltage (V_{OUT}) is programmed by two external resistors (R29 and R34 shown in 図 4). The regulation point can be calculated with 式 13.

$$V_{OUT} = 2.5 \times \left(R_{FB1} + R_{FB2}\right) / R_{FB1} \quad (13)$$

The on-time for the LM5008A is determined by the RT resistor and is inversely proportional to the input voltage (V_{IN}), resulting in an almost constant frequency as V_{IN} is varied over its range. The on-time for the LM5008A is calculated with 式 14.

$$T_{ON} = 1.385 \times 10^{-10} \times R_T / V_{IN} \quad (14)$$

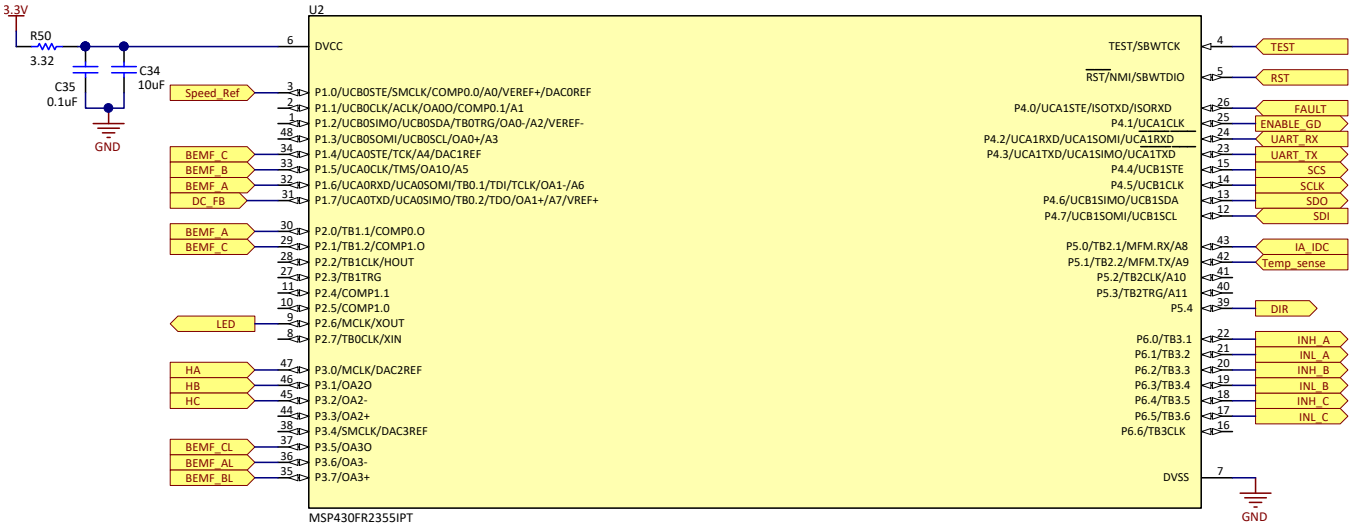
RT must be selected for a minimum on-time (at maximum V_{IN}) greater than 400 ns, for correct current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}. The LM5008A has an intelligent current limit OFF timer. If the current in the Buck switch exceeds 0.51 A the present cycle is immediately terminated and a non-resetable OFF timer is initiated. The length of off-time is controlled by an external resistor (RCL) and the FB voltage. When FB = 0 V, a maximum off-time is required, and the time is preset to 35 µs. This condition occurs when the output is shorted and during the initial part of start-up. This amount of time makes sure that safe short-circuit operation occurs up to the maximum input voltage of 95 V. In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is less than 35 µs. Reducing the off-time during less severe overloads decreases the amount of foldback, recovery time, and the start-up time.

2.4.4 Power Stage Design – Microcontroller MSP430

図 5 shows the schematic for configuring the MSP430FR2355 MCU. The resistor R50 is used to limit the dV/dt at the supply pin of the MSP430FR2355. The design guide uses 10-µF decoupling capacitors. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency. The Timer B of the MCU is used for PWM generation.

図 5 shows all of the feedback signal voltages including the DC bus voltage, current sense amplifier output, potentiometer voltage for speed control, and temperature sensor output interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The phase node voltages of A, B and C phases are measured to implement the sensorless control algorithm.

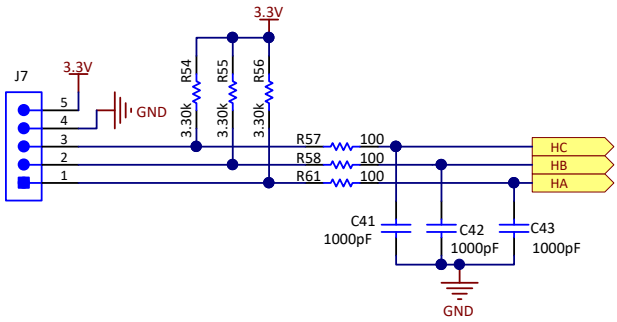
図 5. MSP430FR2355 Schematic



2.4.5 Power Stage Design – Hall Sensor Interface

図 6 shows the Hall sensor interface from the motor to the board. The 3.3 V is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R54, R55, and R56 are used as the pull-up resistors. R57, R58, and R61, along with C41, C42, and C43, form noise filters at the Hall sensor signal.

図 6. Schematic of Hall Sensor Interface

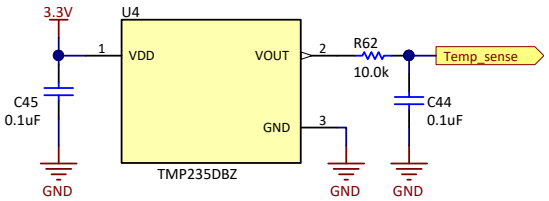


注: The Hall sensor connection should match with the motor winding connection for proper operation of the BLDC motor for sensor based trapezoidal control.

2.4.6 Temperature Sensing

図 7 shows the schematic of temperature sensor circuit. The temperature sensor is placed close to the MOSFET. The thermal gradient across the board need to be considered while calibrating the temperature measurement for all the MOSFETs. The design uses the analog output temperature sensor TMP235A4, supporting wide temperature measurement range: – –40°C to +150°C with a typical accuracy of ±1°C.

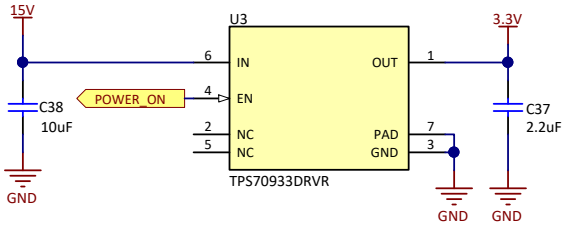
図 7. Schematic of Temperature Sensor



2.4.7 LDO Circuit to Generate 3.3V Supply

図 8 shows the regulator circuit to generate the 3.3V from the 15V input. The reference design uses the ultra-low quiescent current, linear regulator TPS709 to generate the 3.3-V power supply from the input voltage of 15 V. The selection of regulator depends on the wide input voltage support (in this design up to 15V), the load current, and power dissipation. Power dissipation (Pdiss) is equal to the product of the output current and the voltage drop across the output pass element. Assuming a nominal load current of 30 mA, the power dissipation at VIN = 15 V can be calculated as: Pdiss = (15 – 3.3) × 0.03 = 0.351 W. The design uses the thermal pad of the TPS709 package to dissipate heat to the PCB. The POWER_ON signal is an external signal to keep the regulator in sleep mode when the drive is not in use.

図 8. Voltage Regulator Circuit to Generate the 3.3V Supply



2.4.8 Back EMF and VDC Input Voltage Sensing Circuit

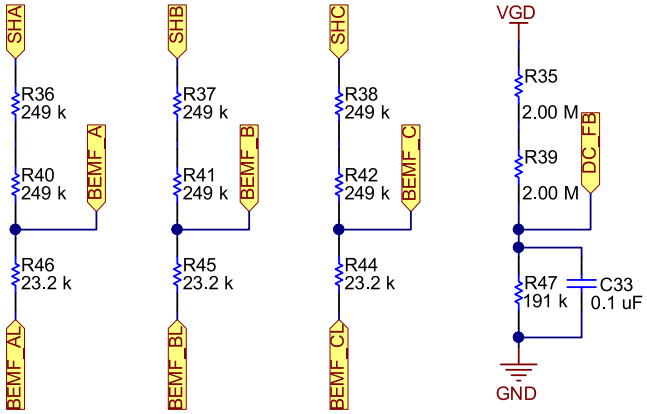
The input supply voltage VDC is scaled using the resistive divider network, which consists of R35, R39, R47, and C33, and fed to the MCU as shown in 図 9. The resistance values are selected high enough to reduce the current consumption. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in 式 15.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(191\,k\Omega + 4000\,k\Omega)}{191\,k\Omega} = 3.3 \times \frac{(191\,k\Omega + 4000\,k\Omega)}{191\,k\Omega} = 72.4\ V \quad (15)$$

Considering a 10% headroom for this value, the maximum recommended voltage input to the system is 72.4 × 0.9 = 65.16. For a power stage with maximum operating voltage of 63 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 15 to 63 V.

The phase node voltages SHA, SHB and SHC are scaled using similar resistive divider network as the VDC sensing. The scaling circuit is shown in 図 9. The scaling factor is the same as the VDC sensing divider circuit to use the full ADC voltage range. The divider circuit uses lower resistance to make sure that the total RC delay due to the ADC sampling capacitor through the resistive divider is less than 10-µs.

図 9. Back EMF Sensing Voltage Divider Circuit



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

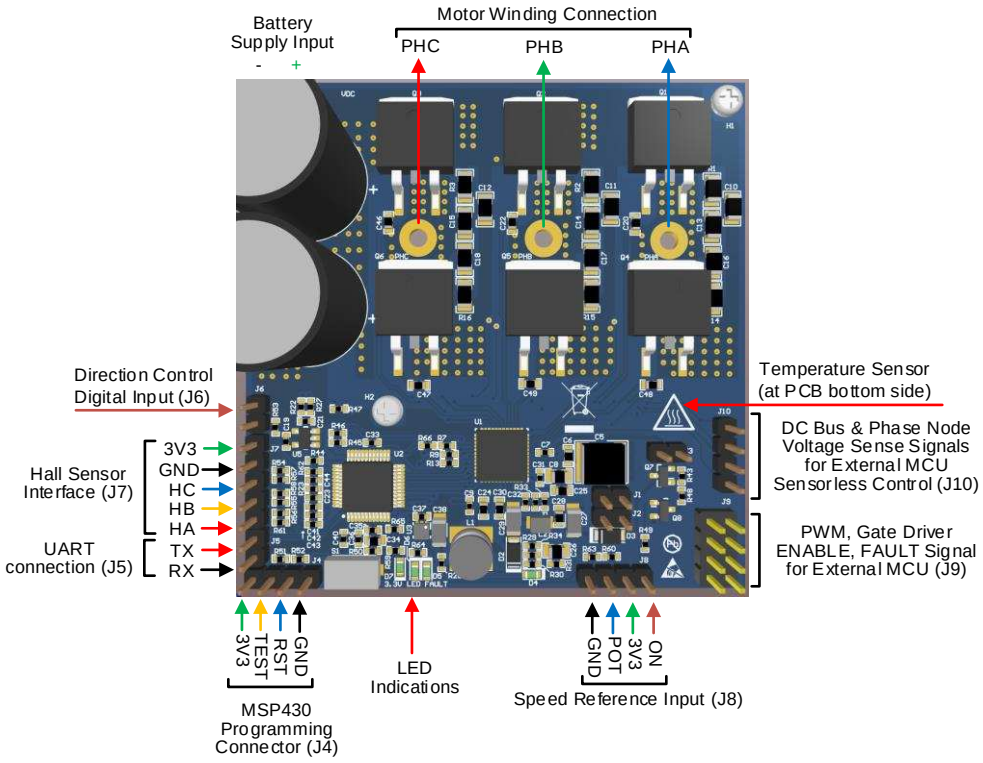
3.1.1 Hardware

3.1.1.1 Connector Configuration of TIDA-010056

図 10 shows the connector configuration of the reference design board, which features the following:

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in 図 10.
- Three-terminal output for motor winding connection: The phase output connections for connecting to the three-phase BLDC motor winding, marked as PHA, PHB, PHC.
- 4-pin connector J8: This connector can be used to interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer should be connected to 3V3 pin and GND pin. The mid-point of the potentiometer must be connected to the POT pin of the connector. The pin marked POWER_ON (ON) is an external two state signal of 0V (low) or 3.3 V (high) to control the on/off of the complete power stage. If the POWER_ON signal is low, then the complete power stage goes to sleep mode with sleep current less than 40 µs.
- 2-pin connector J6: This connector is used for the motor direction change. Externally shorting or opening this connector changes the direction of rotation of the motor.
- 4-pin connector J4: This is the programming connector for the MSP430FR2355 MCU.
- 5-pin connector J5: This is the interface for connecting the Hall position sensors from the motor.
- 2-pin connector J5: This connector is used for external UART communication interface. The RX and TX pins are available enabling the communication with external Bluetooth® low energy or Wi-Fi® module or for communication to the battery pack.
- Two pin jumpers J1 and J2: Close the jumper J1 or J2 to select between single supply mode or dual supply mode for DRV8350R. Close the jumper J2 to connect 15V to the DRV8350R VM supply to enable dual supply mode. Close the jumper J1 to connect VDC input supply to the DRV8350R VM supply to enable single supply mode. This design is tested and validated using dual supply mode.
- J9 and J10: The multi-pin connectors with all the six PWM signals, gate driver ENABLE, gate driver FAULT, DC bus and phase voltage sensing signals, to enable control from an external MCU if required.

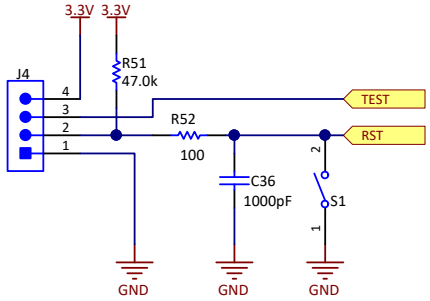
図 10. TIDA-010056 Board Connectors



3.1.1.2 *Programming the MSP430*

The two-wire Spy-Bi-Wire protocol is used to program the MSP430FR2355 MCU. 図 11 shows the four pin programming connector provided in the design board.

図 11. Schematic of MSP430FR2355 Programming Connector



See the MSP430FR2355 development tools for programming options with an external JTAG interface.

Use the following steps to program the MSP430FR2355 MCU when the programming supply voltage is provided by the board itself:

- Remove the motor connections from the board, and power on the input DC supply. Make sure that a minimum of 15-V DC input is applied and 3.3 V is generated in the board.
- Connect the programmer to the board.
- Open the CCS software, and then build and debug the code to program the MCU.

3.1.1.3 Procedure for Board Bring-up and Testing

Follow this procedure for board bring-up and testing:

- Remove the motor connections from the board, and power on the input DC supply. Make sure that a minimum of a 15-V DC input is applied and the 3.3 V is generated in the board.
- Program the MCU as detailed in 3.1.1.2.
- Remove the programmer, and switch off the DC input supply.
- Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs, and make sure that the winding connection and Hall sensor connections match.
- Connect the POT at the interface J8 and set the speed reference.
- Use a DC power supply with current limit protection and apply 15-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence, then the motor starts running at a speed set by the POT.
- If the motor is not rotating and takes high current, or rotates and draws a distorted peak winding current waveform, then check the winding and Hall sensor connection matching and, if wrong, correct the connection sequence to match.
- Adjust the POT voltage for change in speed.
- To change direction, switch off the DC input, close the jumper J6, and switch on the DC input.

3.1.2 Software

The firmware of this design guide offers the following features and user controllable parameters:

- Trapezoidal control of BLDC motor using digital position Hall sensor feedback
- Option for sensorless trapezoidal control by back EMF sensing.
- Option to use DRV8350RS, the SPI version of three phase gate driver.
- Overcurrent cycle-by-cycle protection and latch protection using the VDS sensing feature of the DRV8350R

The firmware system components of this design are listed in 表 3.

表 3. TIDA-010056 Firmware System Components

SYSTEM COMPONENT	DESCRIPTION
Development and emulation	Code Composer Studio v8.3.0
Target controller	MSP430FR2355
PWM frequency	20-KHz PWM (default), programmable for higher and lower frequencies
PWM mode	Asymmetrical
Interrupts	Port 3 Interrupt for hall sensor change. CPU Timer D – Implements 20-KHz ISR execution rate. ADC interrupt
PWM Generation: Timer Configuration	TIMER: TB3.1 –TB.6, Clock = 25 MHz, PWM frequency set for 20 kHz
Position Feedback -Hall sensor Signals	P3.0 → HA P3.1 → HB P3.2 → HC

表 3. TIDA-010056 Firmware System Components (continued)

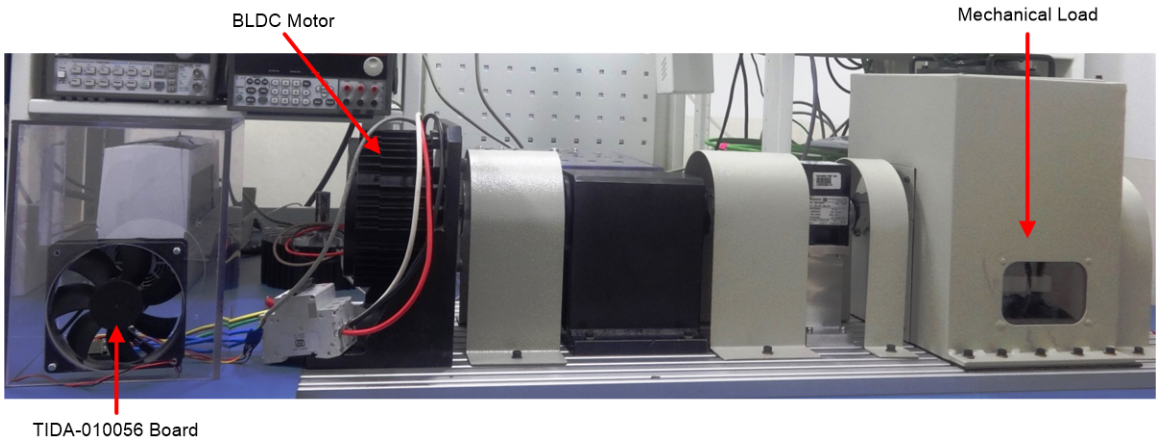
SYSTEM COMPONENT	DESCRIPTION
ADC channel assignment	A0 → Speed reference from the external potentiometer/trigger A6→ Phase A back EMF sensing for sensorless A5 → Phase B back EMF sensing for sensorless A4 → Phase C back EMF sensing for sensorless A7 → DC bus voltage sensing A8 →Low-side DC bus current sensing A9 → PCB or FET temperature feedback
Comparator configuration for back EMF zero crossing detection	COMP0.O (P2.0) – Phase A back EMF zero cross comparator COMP1.O(P2.1) – Phase C back EMF zero cross comparator OA1O (P1.5) - Phase C back EMF zero cross comparator. The opamp of smart compo module is configured as a comparator
DRV8350RS - SPI programming pins connection	P4.4 → SCS P4.5 → SCLK P4.6 → SDO P4.7 → SDI
UART communication	P4.2 → UART RX pin P4.3 → UART TX pin
MCU Digital Inputs/Output	P5.4 → Direction of motor rotation P4.1 → ENABLE connection for DRV8350R P4.0 → FAULT pin connection from DRV8350R P2.6 → LED output

3.2 Testing and Results

3.2.1 Test Setup

図 12 shows the load setup used to test the motor. The load is an electrodynamometer-type load by which the load torque applied to the motor can be controlled.

図 12. Board and Motor Test Setup



3.2.2 Test Results

3.2.2.1 DRV8350R DC/DC Regulator Performance

The internal DC/DC regulator of the DRV8350R is configured to generate 15 V output. The 15 V powers the VM pin of DRV8350R and the input of the 3.3 V regulator. The 15V DC/DC regulator output is specified to deliver 50mA average nominal current with less than 1% voltage ripple. 図 13 shows the peak to peak ripple of the 15 V output, when the 15 V powers the VM line of DRV8350R and the 3.3 V regulator input (an average load of 50mA on the 15 V line). The peak to peak ripple is less than 20 mV.

図 13. Voltage Ripple on the 15 V Output of DRV8350R at an average 50mA load current

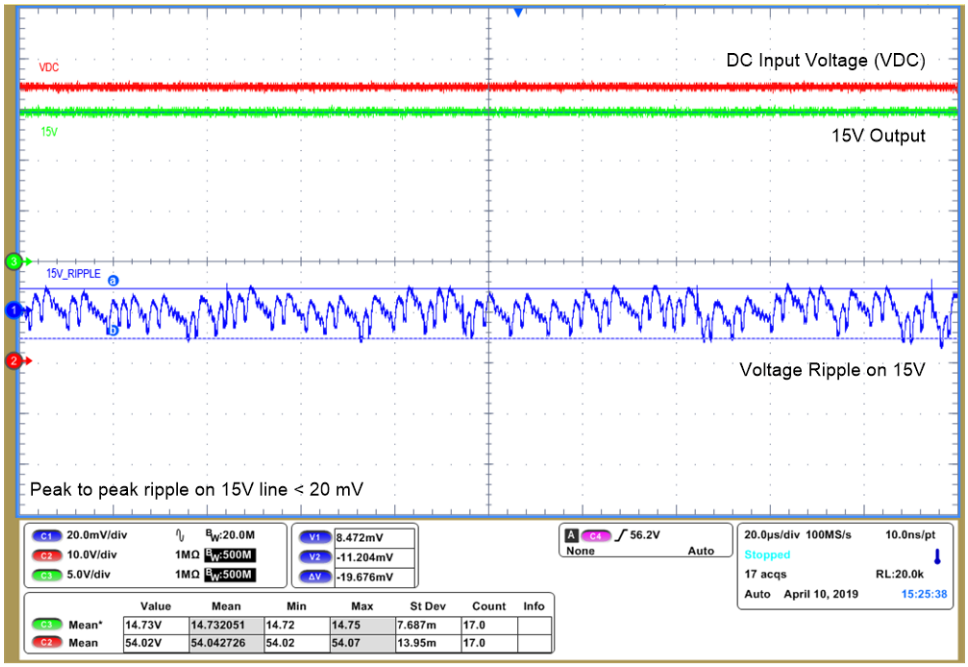
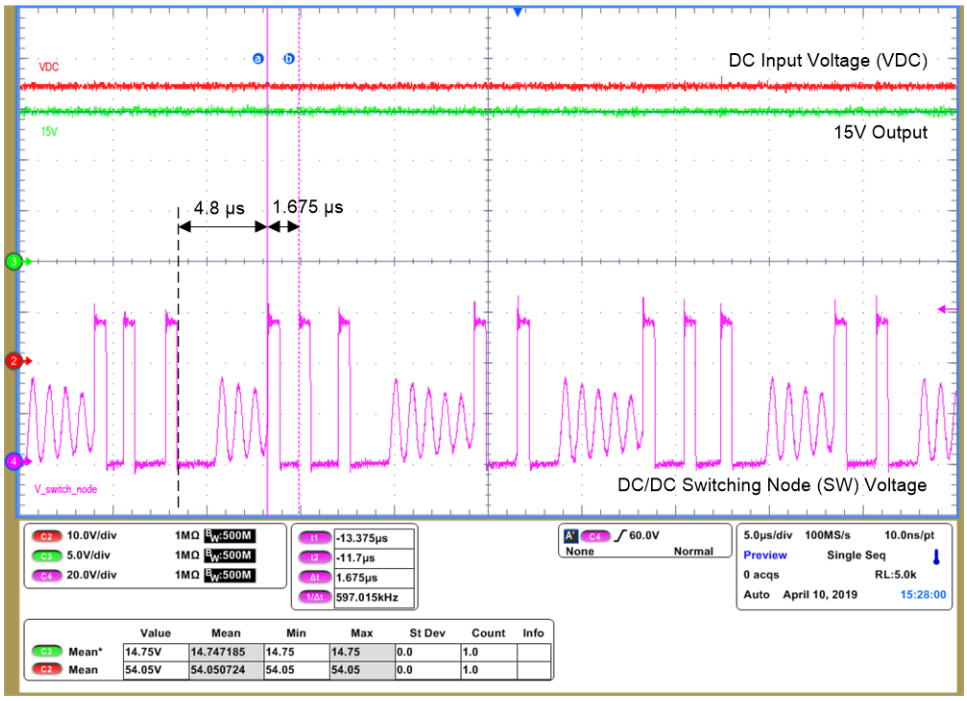


図 14 shows the voltage at the switching node of the DC/DC buck converter (SW pin of DRV8350R)

図 14. Switching Node Voltage of the DC/DC Converter of DRV8350R



The DC/DC regulator operates in discontinuous conduction mode (DCM) at light load currents, and continuous conduction mode (CCM) at heavy load current. 図 14 shows that the DC/DC operate between DCM and CCM, due to the load variation at DRV8350R VM pin. The maximum switching frequency observed during the CCM is approximately 600 kHz and the minimum switching frequency observed during DCM is approximately 200 kHz.

3.2.2.2 TPS70933 Linear Regulator Performance

The TPS70933 takes 15 V input voltage and generates 3.3 V and is designed to deliver an average current of 30mA. The EN pin of TPS70933 can be controlled from an external signal to reduce the power consumption. 図 15 shows the voltage ripple on the 3.3 V line at a load current of 20mA. The ripple is less than 10mV, and is assumed to be enough for the MCU ADC pin voltage reference for back EMF sensing and current sensing.

図 15. Voltage Ripple on the 3.3 V Output of TPS70933 at an Average 20mA Load Current

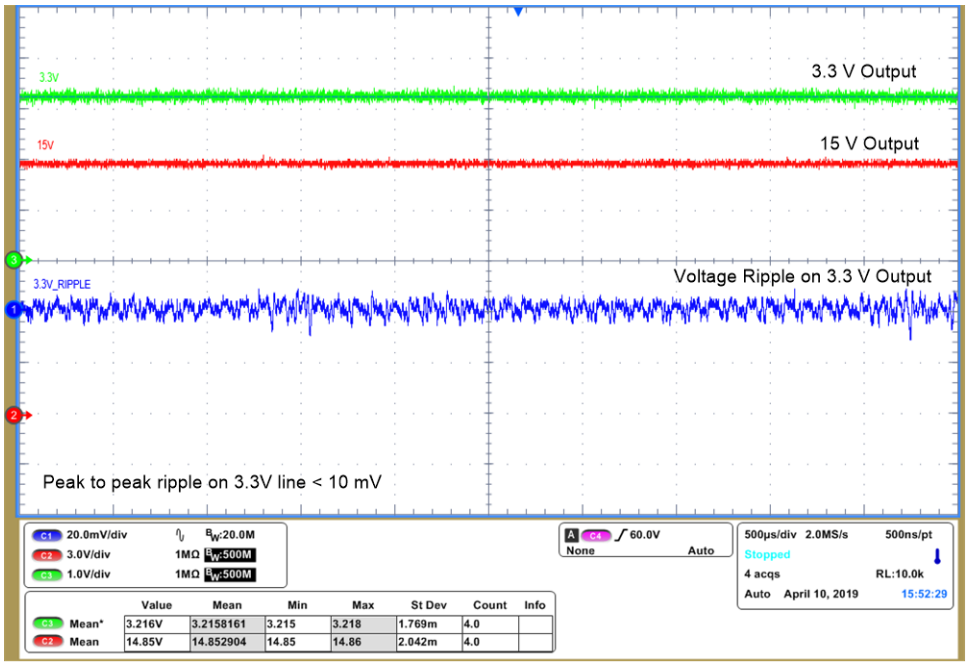


図 16 and 図 17 shows the start up and shut off of the 3.3 V output, when the TPS70933 regulator EN pin is controlled through external signal "POWER_ON."

図 16. 3.3 V Output Start Up When EN Pin Goes Low to High

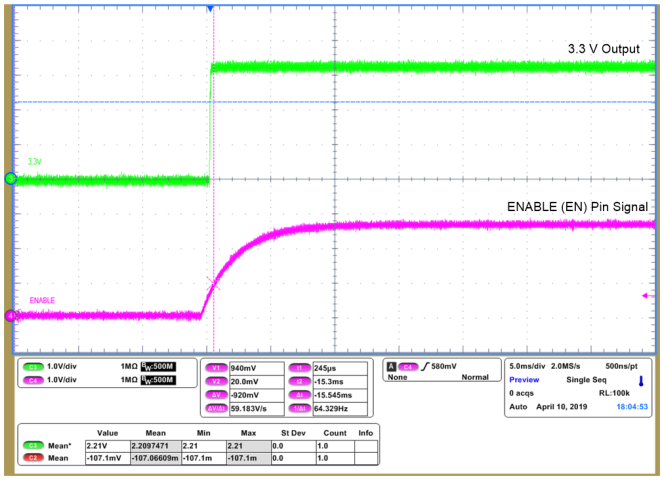
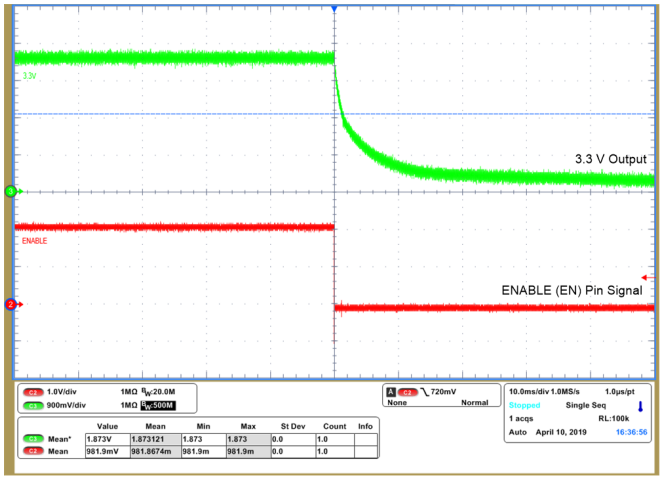


図 17. 3.3V Output Start Up When EN Pin Goes Low to High



3.2.2.3 Board Power Up and Power Down Sequence

図 18 shows the power up sequence of the system. The DRV8350R starts generating the 15V regulator output when VIN goes above approximately 6V. As the 15V output reaches approximately 6V, the 3.3 rail starts developing. 図 19 shows the power down sequence. The DRV8350R DC/DC starts powering down at around 6V VIN supply, followed by 3.3 V power down.

図 18. Power Up Sequence of the Board

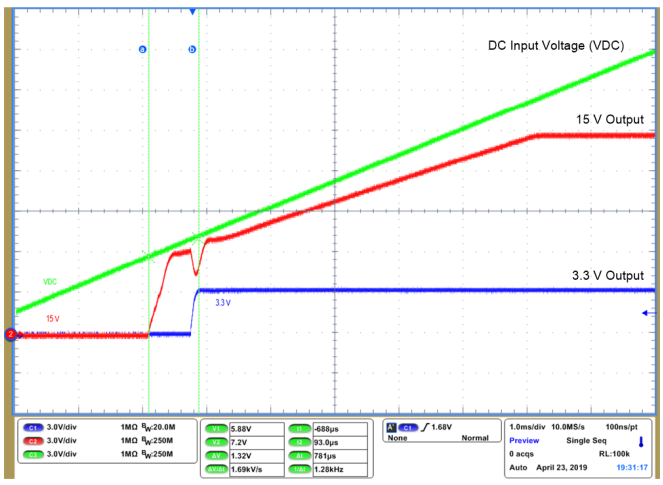
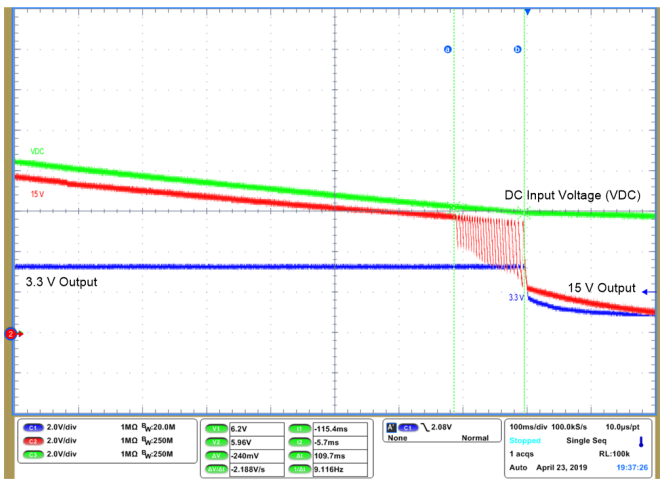


図 19. Power Down Sequence of the Board



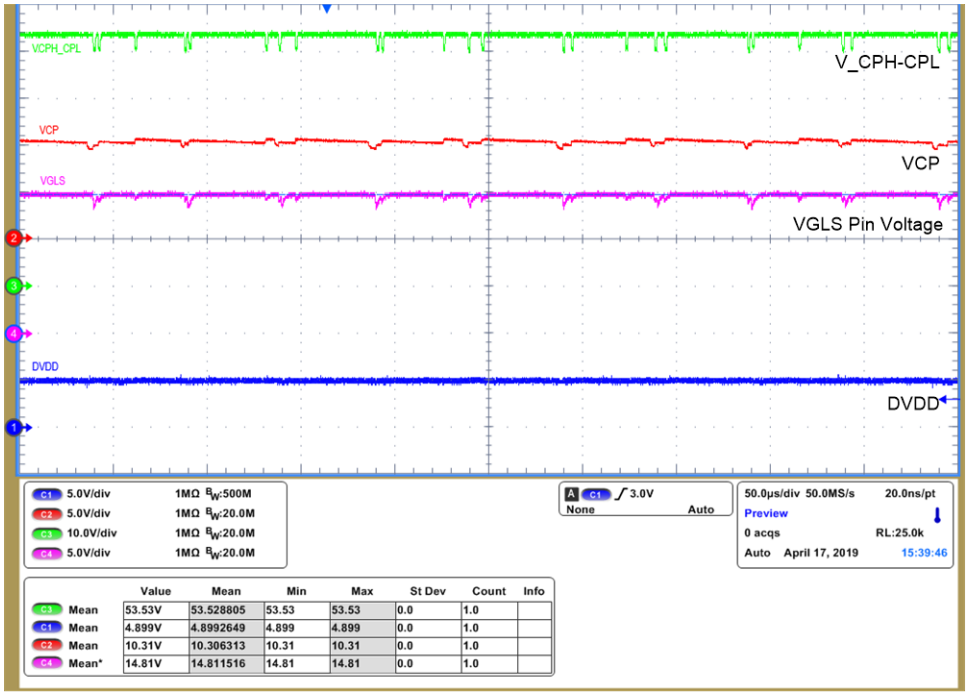
3.2.2.4 Functional Evaluation of DRV8350R Gate Driver

The high-side gate drive supply voltage is generated using a double charge-pump architecture that regulates the VCP output to VVDRAIN + 10.5-V. The low side gate drive supply voltage is generated using a linear regulator from the VM power supply that regulates the VGLS output to 14.5-V. The VGLS supply is further regulated to 11-V on the GLx low-side gate driver outputs. DRV8350 provides a linear regulator output of 5V at DVDD pin with a source capability of 10 mA to external loads. 図 20 shows the internal power supply voltages generated by DRV8350R. The average voltage values are tabulated in 表 4.

表 4. Internal Regulator Voltages of DRV8350R

INTERNAL REGULATOR NAME	AVERAGE VOLTAGE (V)
VGLS (Internal low side gate driver regulator output)	14.81
VCP (Charge pump output)	10.31
DVDD (5-V internal regulator output)	4.9

図 20. Internal Regulator Voltages of DRV8350R



The functional evaluation of the gate driver is done with gate driver DRV8350R power supply VM is powered from the 15V DC/DC regulator output. 図 21 and 図 22 shows the low side and high side gate drive output voltage at 54V DC input and 15V DC input at 20 kHz switching frequency. The gate drive voltage is approximately 10 V at 54V DC input, which means effective gate driving of standard MOSFETs. The gate drive voltage of the DRV8350R at a DC bus voltage of 15 V (Assuming 1 V/cell in a 15s Li-ion battery configuration during load transients), at a VM pin voltage of 12.76 V (Output of the DC/DC regulator) is approximately 10 V.

図 21. Low- and High-Side Gate Drive Voltage at 54-V DC

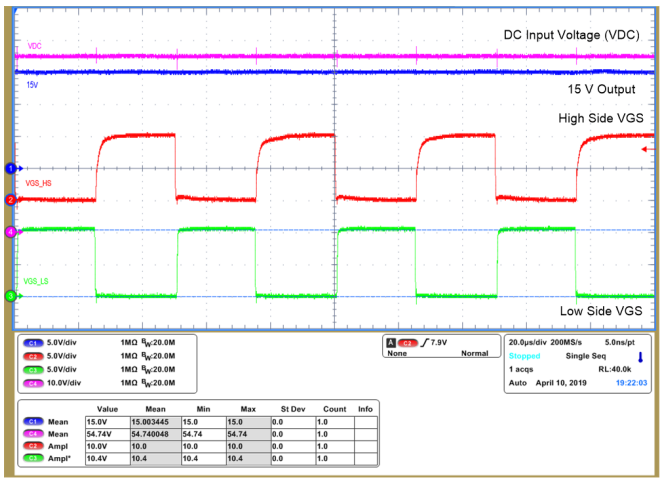
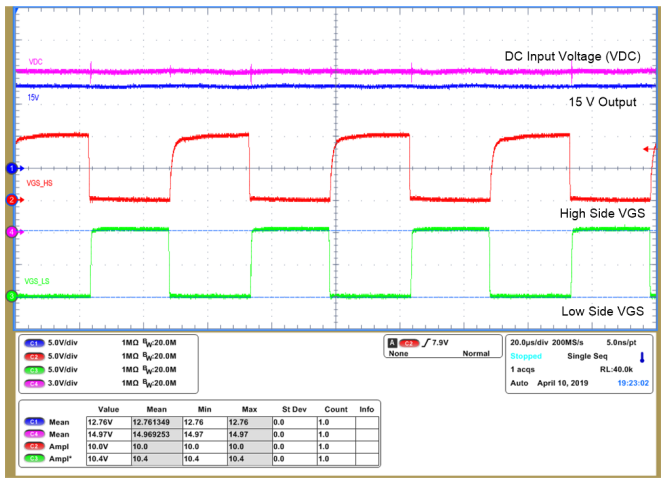


図 22. Low- and High-Side Gate Drive Voltage at 15-V DC



3.2.2.5 Dead Time Insertion by DRV8350R

図 23 and 図 24 shows the high-side and low-side gate source voltage from the DRV8350RH, which shows the dead time inserted by the DRV8350RH at the both the edges of the PWM. The dead time is 100ns, fixed value in hardware version of DRV8350. The DRV8350 inserts the dead time after the VGS handshake, ensuring that no shoot through happens and also benefits in inserting minimum dead time to achieve very minimum diode loss during dead time.

図 23. Dead Time at Rising Edge of Low-Side VGS

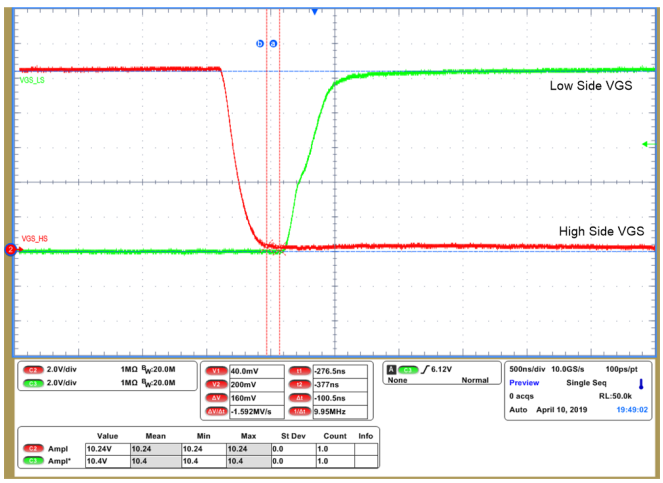
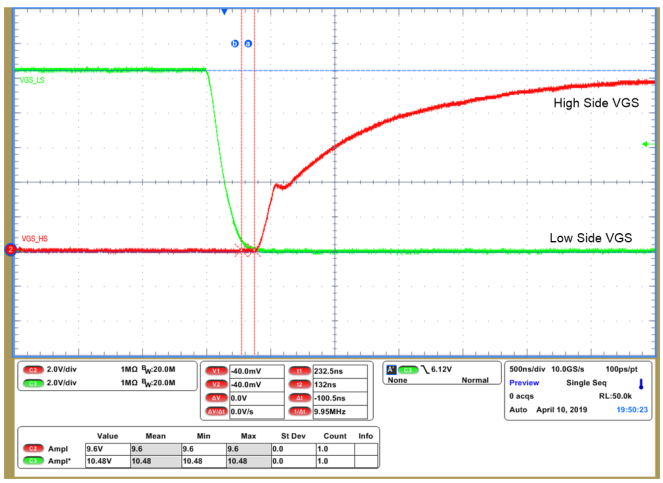


図 24. Dead Time at Trailing Edge of Low-Side VGS



3.2.2.6 MOSFET Switching Waveforms

図 25 shows the PWM scheme used in the reference design testing for trapezoidal control of the BLDC motor. The controls is a six-step block commutation where PWM is applied to top switch and bottom switch is operated in active freewheeling during the positive phase winding current for 120° electrical period. The bottom MOSFET switch is kept continuously ON during the negative phase winding current for 120° electrical period. The MOSFET switching waveforms are evaluated by using the PWM scheme shown in 図 25.

図 25. Low- and High-Side FET PWM Generated by MCU for Unipolar Trapezoidal Control

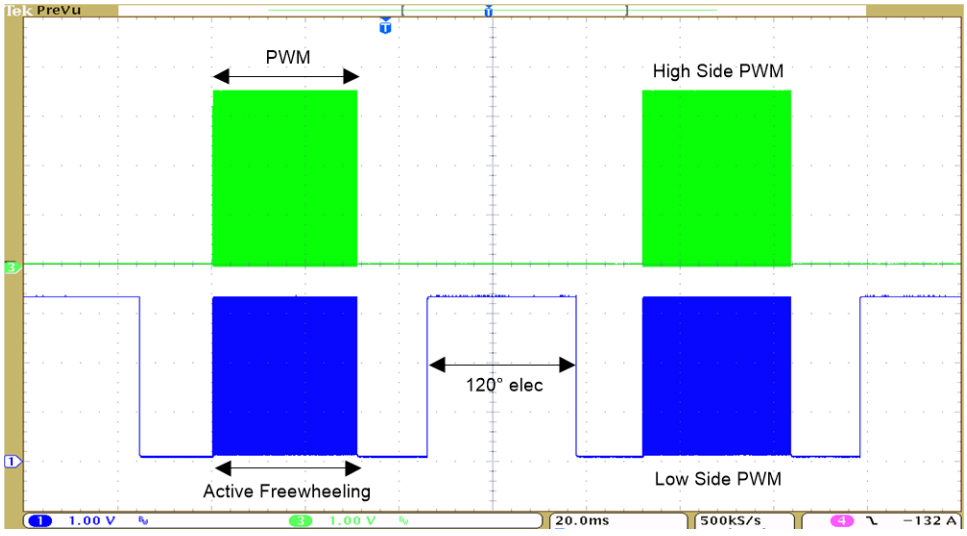


図 26, 図 27, 図 28, and 図 29 show the VDS and VGS waveforms of the low-side and high-side MOSFETs with the gate current of DRV8350RH (IDRIVE) set at a 100-mA source and a 200-mA sink current. The switching slew rate control of the gate driver with adjustable gate current and strong pull down to eliminate dv/dt pick up at the gate of a MOSFET during the complimentary MOSFET turn on, helps to optimize the switching waveforms. The reference design uses RC snubbers ©$_{snub}$ = 3.9 nF, R_{snub} = 1.5 Ω) across low side FETs to optimizes voltage ringing caused due to FET diode reverse recovery. Loss in one snubber resistor at 63VDC, 20kHz PWM trapezoidal control = (1/3) x CV^2 x fsw ≈ 0.1W. The reference design uses a snubber resistor rated for 0.25 W. It is recommended to use a pulse-power rated resistor for snubber. Switching waveforms are clean without much over-voltage ringing.

図 26. Turnon: Low-Side VGS and VDS at 25-ARMSWinding Current

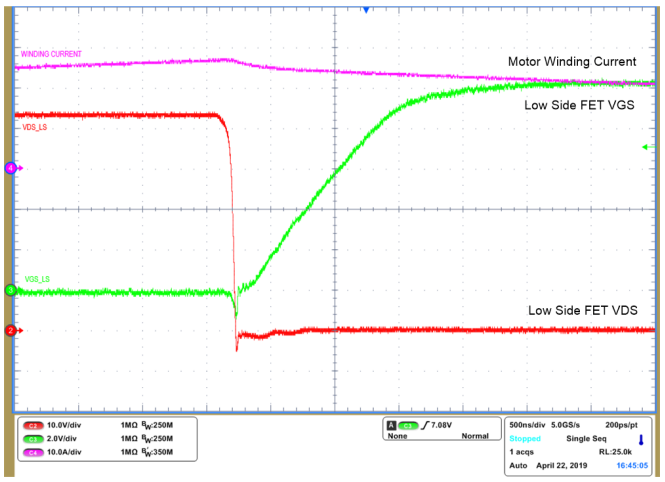


図 27. Turnoff: Low-Side VGS and VDS at 30-ARMS Winding Current

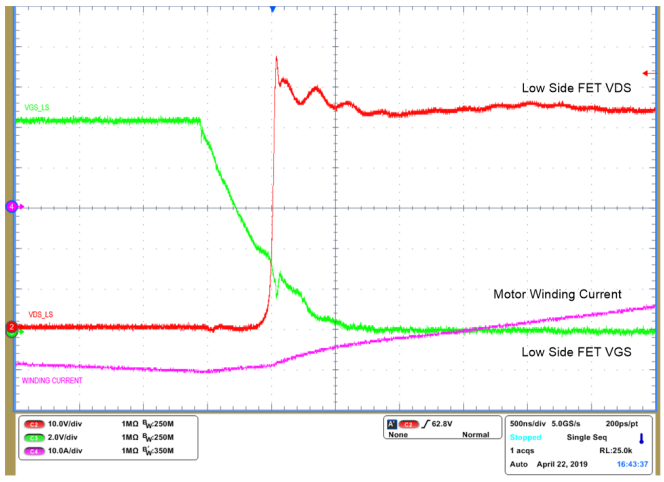


図 28. Turnon: High-Side VGS and VDS at 25-ARMS Winding Current

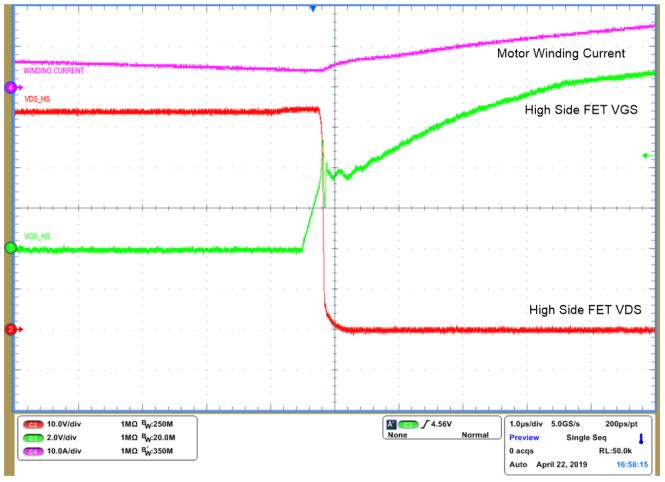
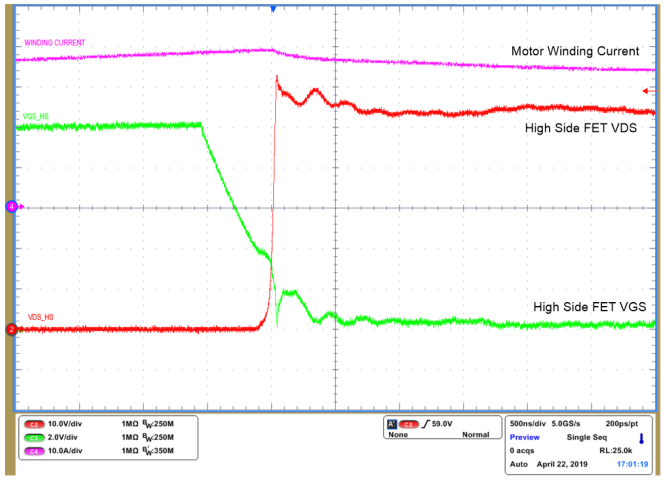


図 29. Turnoff: High-Side VGS and VDS at 30-ARMS Winding Current



3.2.2.7 Load Test

The design board is tested with an external BLDC motor and load using the test setup in 図 12. The testing is done without heat sink and without forced airflow at different duty cycles. The key results are summarized in 表 5.

図 30 shows the motor winding current and winding voltage waveforms at a 54-V DC input and a 22.9-ARMS winding current. The testing is done at 100% duty cycle.

表 5. Load Test Results at Different Duty Cycle Without Heat Sink and Without Forced Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	INVERTER DUTY CYCLE (%)	MAXIMUM FET TEMPERATURE (°C)
54	25.95	22.9	1401	95	95
54	30.05	26.6	1623	100	91

図 30. Load Test Results at 54-V DC Input, 23-ARMS Winding Current, 95% Duty Cycle

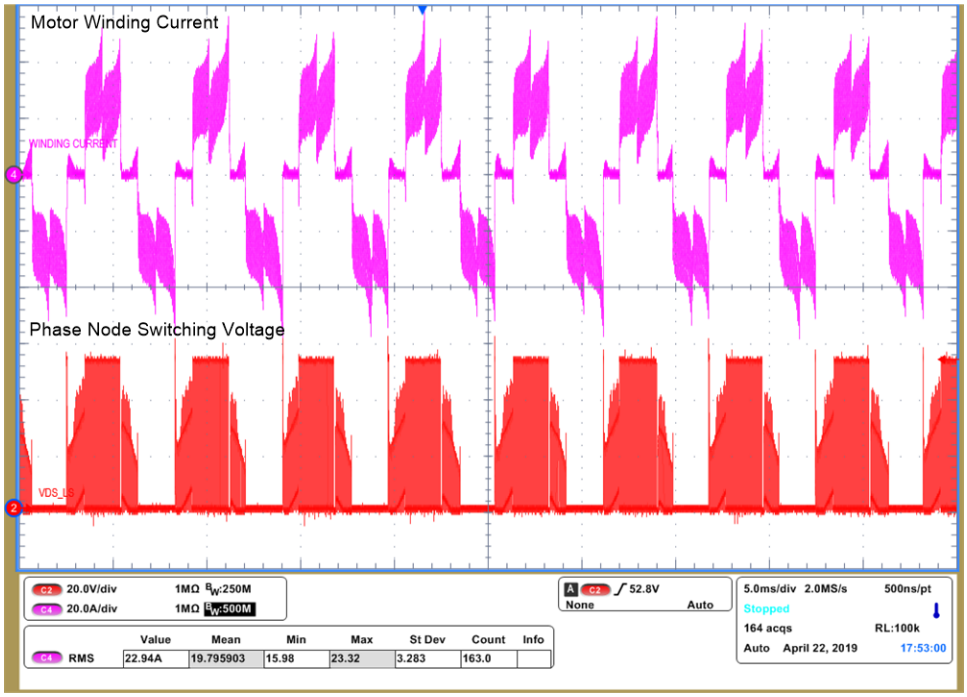


図 31 shows the steady state thermal image of the board when delivering 26-ARMS at 54V DC input and 100% duty cycle, captured after 10 minutes of continuous running. The maximum FET temperature observed is 89.7°C. 図 31 shows the steady state thermal image of the board when delivering 22.8-ARMS at 54V DC input and 95% duty cycle , captured after 10 minutes of continuous running. The maximum FET temperature observed is 93.7°C.

図 31. Thermal Image at 54-V DC Input, 26-ARMS Winding Current, 100% Duty Cycle

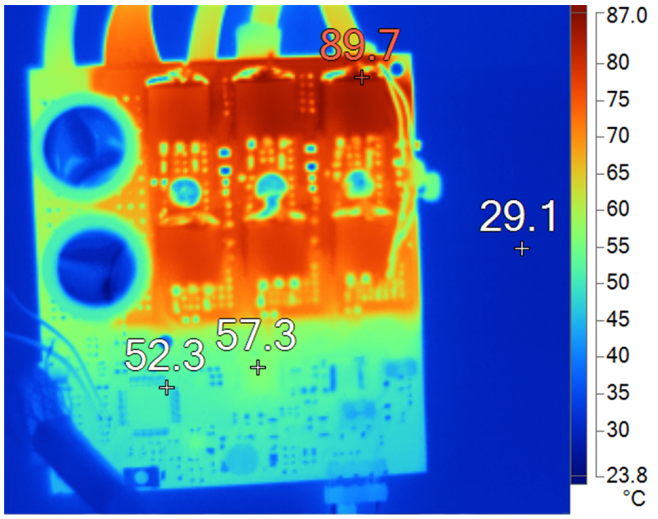


図 32. Thermal Image at 54-V DC Input, 22.8-ARMS Winding Current, 95% Duty Cycle

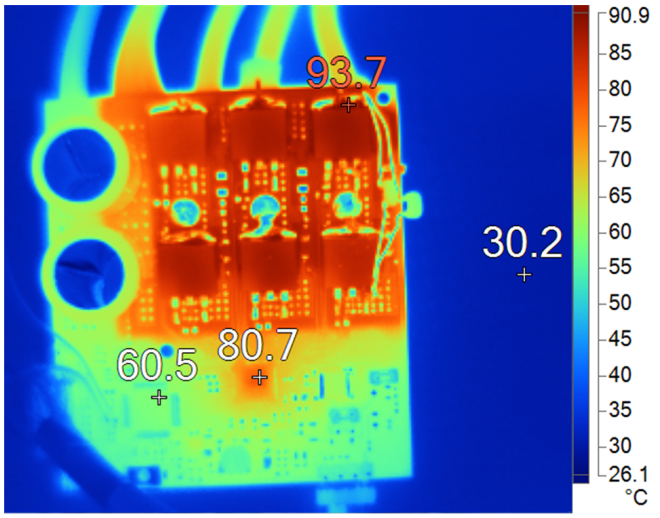


図 33 shows the maximum steady state temperature observed on the MOSFET at different winding current and duty cycle when tested without any heat sink and without forced airflow.

図 33. Maximum Steady State Temperature on MOSFET Across Winding Current

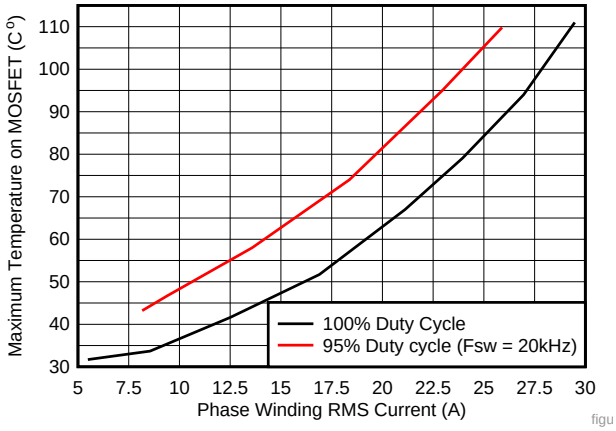
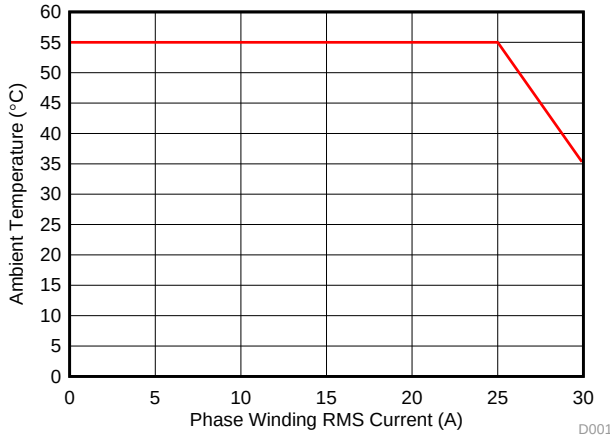


図 34 shows the safe operating area of the board TIDA-010056 with no heat sink and with natural convection.

図 34. TIDA-010056 Safe Operating Area With Natural Convection



3.2.2.8 Power Stage Efficiency Test

The inverter efficiency is experimentally tested with a load setup as shown in 図 12. The efficiency test is done without a heat sink and without forced airflow. The efficiency test results at 100% duty cycle are listed in 表 6 and the test results at 95% duty cycle are listed in 表 7. The efficiency across RMS output current of the inverter is plotted in 図 35. The power loss of the power stage across RMS winding current is shown in 図 36.

The design could achieve the high efficiency due to the following key factors:

- Low R_{DS_ON} of the MOSFET reducing the conduction losses
- The smart gate driver DRV8350 enable clean FET switching reducing the switching losses and diode losses
- The VGS handshake feature of the gate driver allows minimum dead time, reducing the diode loss
- Optimum PCB design helping in much reduced PCB parasitic and hence low PCB losses
- High gain current sense amplifier using INA180A3 with very low gain error and offset voltage error helps to reduce the shunt resistor value

表 6. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)	INVERTER LOSS (W)
54.05	8.64	7.34	467.06	464.50	99.45	2.566
53.93	13.38	11.37	721.33	717.91	99.53	3.423
53.98	18.27	15.48	986.06	981.15	99.50	4.912
53.95	24.02	20.47	1295.68	1288.87	99.47	6.806
54.14	29.85	25.51	1616.03	1606.61	99.42	9.421
53.63	32.37	27.72	1736.35	1725.62	99.38	10.725

表 7. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)	INVERTER LOSS (W)
53.85	9.21	8.13	495.98	492.38	99.27	3.604
54.13	13.09	11.56	708.60	704.13	99.37	4.475

表 7. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow (continued)

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)	INVERTER LOSS (W)
53.95	17.92	15.87	966.55	959.20	99.24	7.348
54.05	24.24	21.43	1310.41	1299.54	99.17	10.872
54.04	29.08	25.72	1571.58	1557.11	99.08	14.475
53.99	31.08	27.57	1677.93	1661.19	99.00	16.740

図 35. Inverter Efficiency versus Output Power

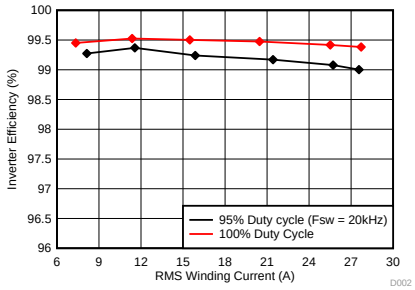
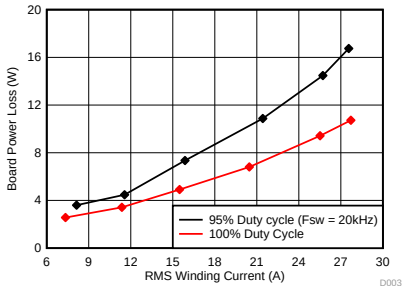


図 36. Board Losses Vs Output RMS Current at 54 V Input



3.2.2.9 *Overcurrent and Short-Circuit Protection Test*

Over current and short circuit protection of the power stage is implemented using the VDS monitor feature of the gate driver DRV8350RH. The gate drivers implement adjustable VDS voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the VDS trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device VDS fault mode.

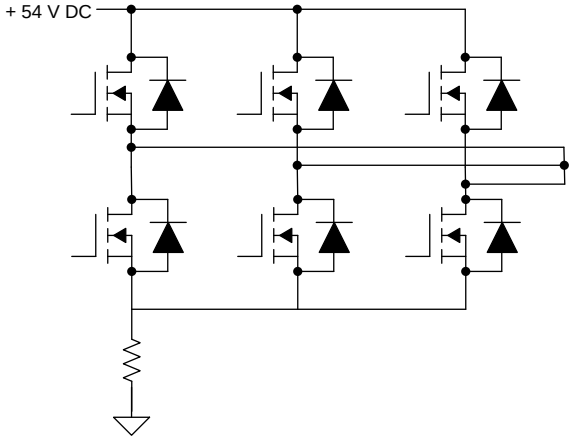
The test conditions as per 表 8 are used for all the test results in this section and Section 3.2.6.3.

表 8. Test Conditions for Short-Circuit Protection by VDS Monitoring

PARAMETER	VALUE
Test temperature (ambient)	25ºC
MOSFET R_{DS_ON} at 25ºC junction temperature	2 mΩ
Deglitch time	4 µs
Supply Voltage	54 VDC

図 37 shows the test setup to simulate a short circuit at the inverter output.

図 37. Test Setup to Simulate Inverter Short Circuit



Using a VDS threshold of 0.06 V, current limit threshold = VDS threshold / R_{DS_ON} = 30 A

This means once the MOSFETcurrent reaches 30A, the VDS comparator in the gate driver trips and wait for a delay deglitch period of 4 µs, before turning off the MOSFET, to ensure that the overcurrent trip is caused by actual overcurrent event and not by any noise signal. But the circuit current increases from 30-A to a higher value within the deglitch time. The increase in current is determined by deglitch time, short circuit resistance, inductance, and applied DC bus voltage.

For example, assuming:

- Short circuit inductance, L_{SC} = 3 µH
- Driving voltage during short circuit = 54 V (DC)
- Short circuit resistance, R_{SC} = 0 Ω (for simplicity of analysis)

The increase in current in OCP_DEG can be calculated as in 式 16.

$$\Delta I = \frac{V_{SC}}{L_{SC}} \times \Delta t \tag{16}$$

Substituting the values, ΔI = 36 A

The inverter is shorted with a copper wire at the output of the three-phase inverter of this design. The expected peak current setting ≈ 30+ 36 = 66 A

図 38 shows the overcurrent protection acted at around 65 A. Once the current hits 65 A, the PWM shuts off immediately and the response time is less than 1 µs. 図 39 shows the automatic retry time of 8 ms with a persistent short circuit at the inverter output, tested with a 100% duty cycle.

図 38. Overcurrent Protection With Inverter Output Shorted

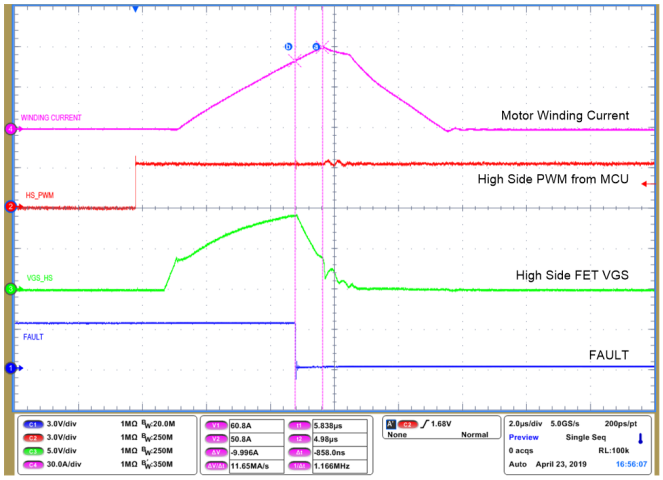


図 39. Automatic Retry on Every 8 ms on Persistent Short Circuit

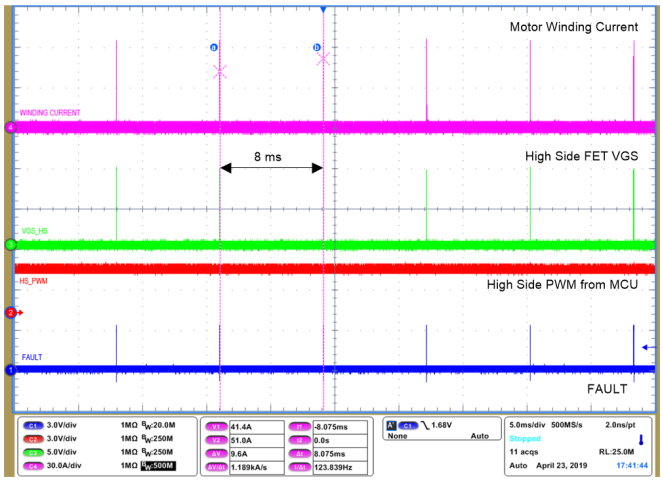


図 40 shows the test setup to simulate a stall current when the motor is rotating. A fault is created by closing the switch SW, that induce a short circuit between the inverter phase A and B output. Before SW is closed, the motor was rotating at a steady speed. 図 41 shows the waveforms obtained when the switch SW is closed. When SW is closed, SW carries the short-circuit current. During this condition the motor stops, which causes the Hall state to continue at the current commutation state or jerk to the next commutation state; therefore, the controller continues to generate the PWM corresponding to the commutation state. The overcurrent protection acted at around 70 A and the PWM shuts off immediately with response time less than 1 µs. 図 41 shows the test results with motor stall condition.

図 40. Test Setup to Simulate Stall Current When Motor is Running

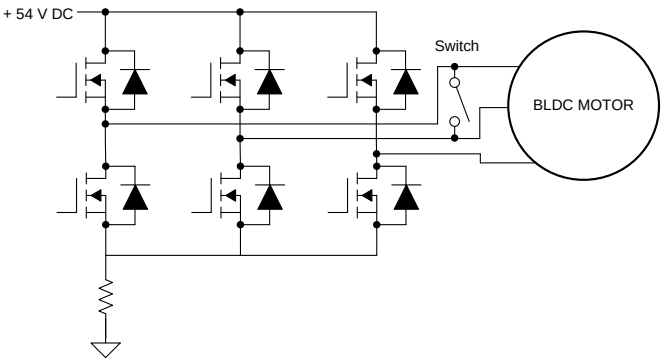
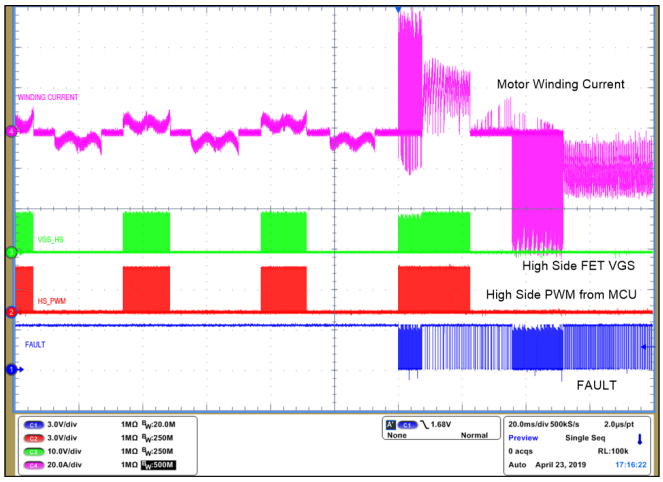


図 41. Overcurrent Protection With Motor Stall



3.2.2.10 MOSFET Gate Fault Protection

The Gate driver DRV8350 monitors the GHx and GLx pins such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

図 42 shows test results when an open circuit is created between the GHx pin of DRV8350RH and the gate pin of the external high side MOSFET. The DRV8350RH (hardware version of DRV8350) has a fixed t_{DRIVE} period of 4 µs. 図 42 shows that high side PWM (HS_PWM) is set at around 50% duty cycle. However the gate driver detects the gate open condition and issue a fault after t_{DRIVE} time and turns off all the MOSFETs. The testing is done with an IDRIVE setting 300 mA source current and 600 mA sink current

図 42. Gate Fault Protection - Open Circuit Between Gate Driver and MOSFET Gate

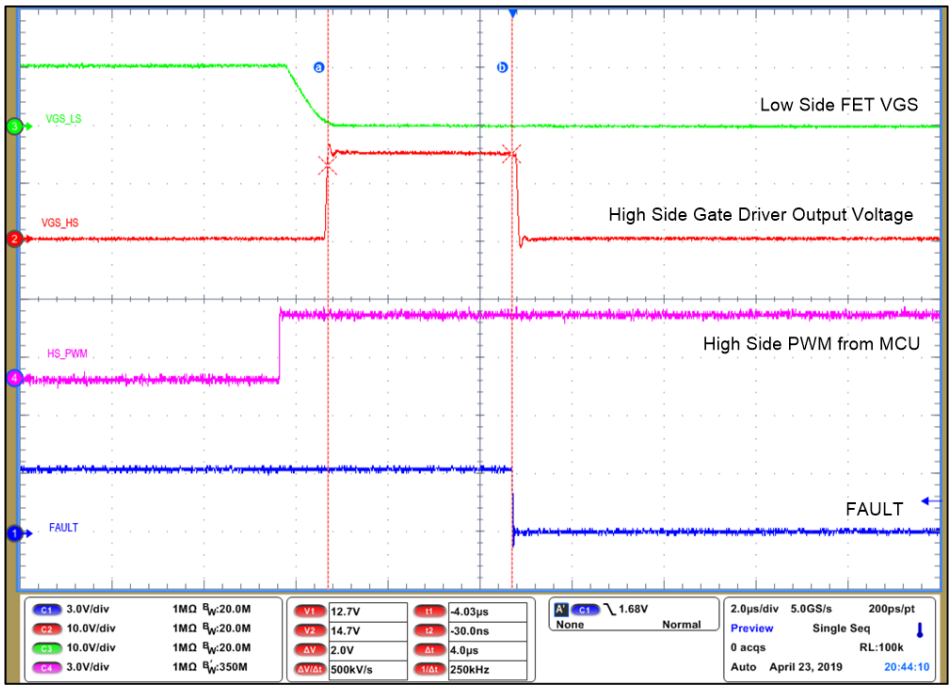
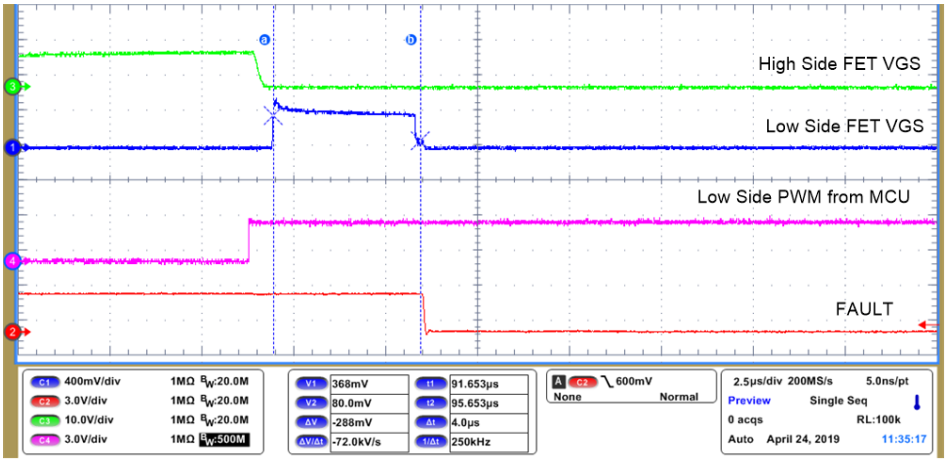


図 43 shows test results when a short circuit is created between the gate and source of external low side MOSFET. 図 43 shows that low side PWM (LS_PWM) is set at around 50% duty cycle. However the gate driver detects the gate to source short circuit condition as the gate voltage did not reach the commanded gate drive voltage after t_{DRIVE} time and issue a fault after t_{DRIVE} time and turns off all the MOSFETs. The testing is done with an IDRIVE setting 300 mA source current and 600 mA sink current

図 43. Gate Fault Protection - External MOSFET Gate to Source Short Circuit



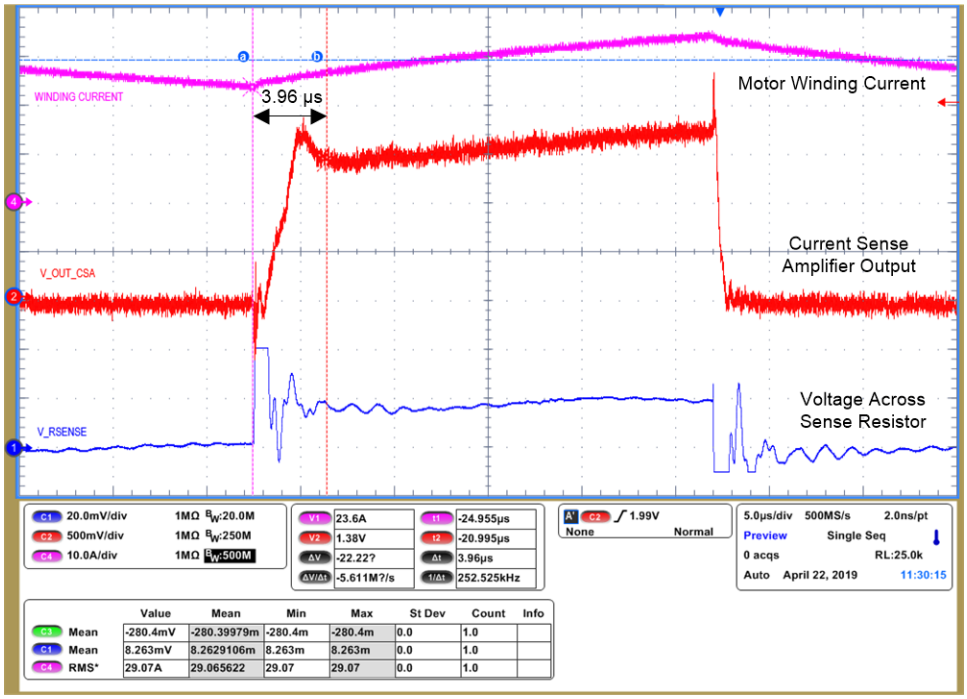
3.2.2.11 Current Sense Amplifier Testing

The step response of the current sense amplifier is evaluated under the test conditions:

- Two 1-mΩ resistors are connected in parallel to get an effective shunt resistance of 0.5 mΩ
- Amplifier gain of 100V/V by INA180A3 with a bandwidth of 150 kHz
- Winding current of approximately 25A RMS. The winding current rises from 24A to 34A in the PWM on period

図 44 shows the step response of the amplifier circuit. The settling time at the rated winding current is less than 4 µs. The testing is done with input filter component values of R22 = R27 = 10 Ω and C21 = 3300 pF, to suppress the voltage oscillations across the shunt resistor during switching and to attenuate high frequency noise pick up due to MOSFET switching. Current sense amplifier output filter values used are R23 = 100 Ω, and C23 = 1000 pF.

図 44. Transient Response of Current Sense Amplifier



3.2.2.12 *Power stage Sleep Current Consumption*

表 9 list the sleep current consumption of the power stage at different test conditions. All testing done at an input voltage of 54V.

表 9. Power Stage Sleep Current Consumption

TEST CONDITION (INVERTER OPEN CIRCUITED)	POWER STAGE CURRENT CONSUMPTION
DRV8350R: Fsw =20kHz, VDC = 54V, VM = 15V, DC/DC input = 54 V, VDRAIN = 54V	29.45 mA
DRV8350R: VDC = 54V, VM pin open, DC/DC input = 54 V, VDRAIN = 54V	< 20 mA
DRV8350R: VDC = 54V, VM pin open, DC/DC input = 0V, VDRAIN = 54V	< 60 µA

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010056.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010056.

4.3 PCB Layout Recommendations

Use the following layout recommendations when designing the PCB

- Connect all the decoupling capacitor and charge pump capacitors of DRV8350R close to DRV8350R pins to minimize loop impedance for the bypass capacitor.
- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8350R GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8350R GL_X to the power MOSFET and returns through GND.
- In this design guide, the PCB is a four-layer layout with a 2-oz (70-micron) copper thickness in every layer. The power tracks are made wide to carry a high current. The tracks are repeated in different layers and are connected by arrays of stitching vias.
- A GND star point is defined in the PCB from where the GND path for the DRV8350R and other signal circuits in the board is tapped.
- For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will spread heat better to the bottom surface copper area.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010056.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010056.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010056.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010056.

5 Software Files

To download the software files, see the design files at TIDA-010056.

6 Related Documentation

1. *Understanding Smart Gate Drivers,* Application Report
2. *36-V/1-kW, 99% Efficient, 18-cm^2 Power Stage Reference Design for Three- Phase BLDC Motors* Design Guide

3. *25.2-V, 30-A High-speed sensorless (> 100 krpm) brushless DC motor drive reference design* Design Guide

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7 Terminology

PWM Pulse width modulation

BLDC Brushless Direct Current

MCU Microcontroller unit

FETs, MOSFETs Metal-oxide-semiconductor field-effect transistor

RPM Rotation per minute

RMS Root mean square

8 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has experience in system-level product design of permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology, Calicut, India.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年6月発行のものから更新 **Page**

- タイトルを「*3 相 BLDC 駆動用 54V、1.5kW、効率 99% 未満、70×69mm² 電力段のリファレンス・デザイン*」から「*3 相 BLDC 駆動用 54V、1.5kW、効率 99% 超、70×69mm² 電力段のリファレンス・デザイン*」に 変更 1

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