参考資料

デザイン・ガイド: TIDA-010132
レーダーおよび電子戦アプリケーション向けのマルチチャネル RF トランシーバのリファレンス・デザイン

概要

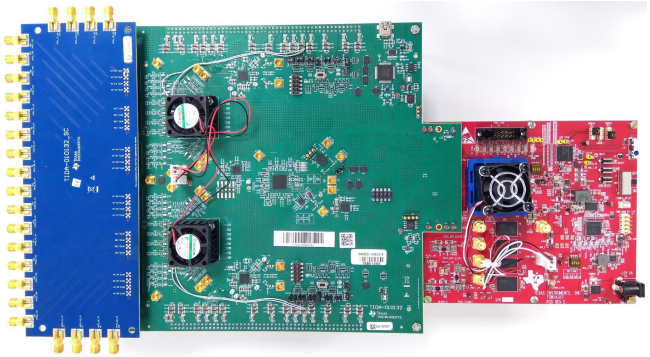
レーダーおよび電子戦 (EW) アプリケーションによく使用されるアクティブ電子スキャン・アレイ (AESA) アンテナ・システムは、ダイナミック・レンジが広い複数のトランシーバ (TRX) を搭載しており、アレイ全体の全要素を同期させるために高精度の低ノイズ・クロックを必要とします。動作周波数が高くなるとアンテナのサイズが小さくなり、TRX 回路、データ・インターフェイス、電源に使用可能な部分はわずかになります。このリファレンス・デザインでは、2 つの AFE7444 4 チャネル RF トランシーバと、16 以上のチャネルを持つ設計にも拡張できる LMK04828-LMX2594 ベースのクロック生成サブシステムとを使用した 8 チャネル・アナログ・フロント・エンド (AFE) の例を示します。各 AFE チャネルは、14 ビット 9GSPS の DAC と、2.6GHz で 75dB を超えるダイナミック・レンジを備え 10ps 未満のスキューで同期する 3GSPS の ADC で構成されています。

リソース

TIDA-010132	デザイン・フォルダ
AFE7444	プロダクト・フォルダ
LMX2594	プロダクト・フォルダ
LMK04828	プロダクト・フォルダ
LMK04832	プロダクト・フォルダ
LMK61E2	プロダクト・フォルダ
TSW14J57EVM	ツール・フォルダ

TI E2E™ Community

E2E™エキスパートに質問

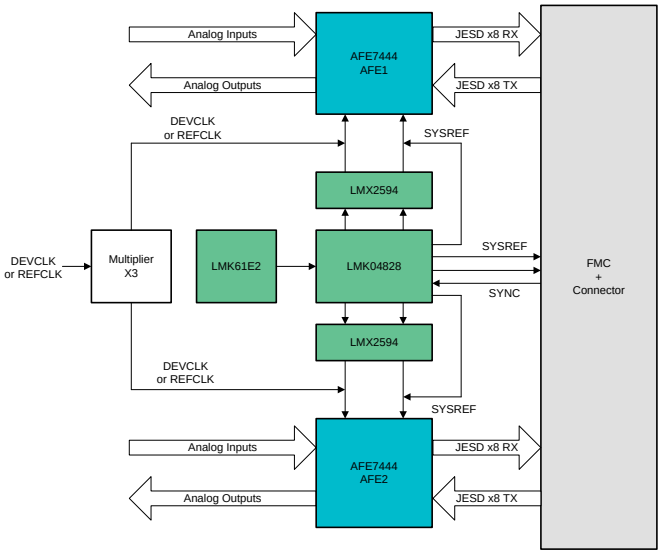


特長

- 共通の FCM インターフェイスを搭載した高密度でスケーラブルな 8 チャネル RF サンプリング・アナログ・フロント・エンド
- システム・クロックのスキューはデバイス間で 5psec 未満
- クロック位相は 0.5psec のステップ分解能で調整可能
- 低ノイズのクロック生成により 14 ビットのアナログ・フロント・エンド性能を実現
- デジタル機能 (NCO、DDC など) は複数のトランシーバ間で同期
- 高速データ・キャプチャ/ジェネレータ TSW14J57EVM をサポートしているため、独自の大規模設計をすぐに開始可能

アプリケーション

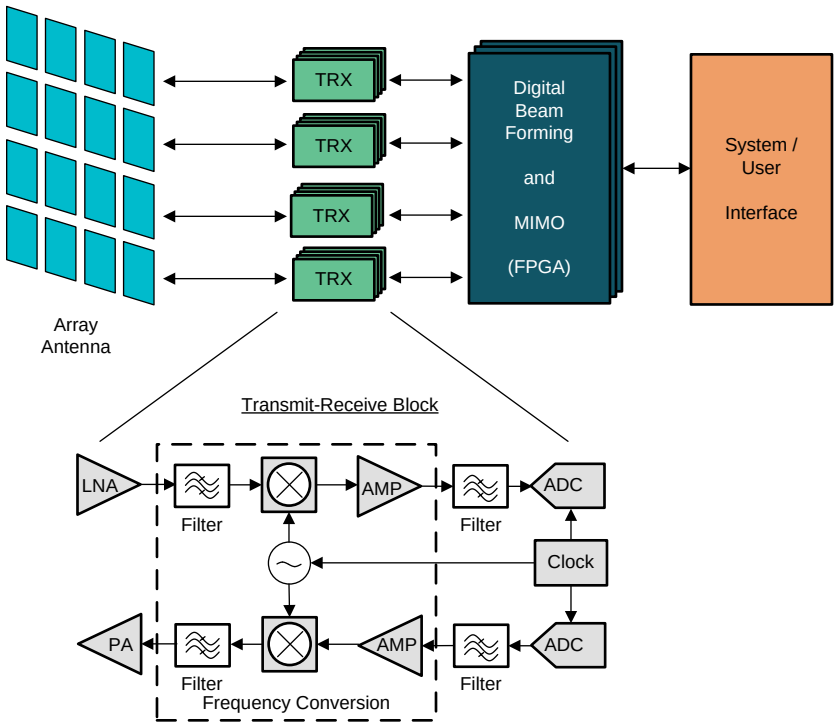
- レーダー
- 電子戦



1 System Description

Active electronically scanning array (AESA) antenna systems often used in radar and electronic warfare (EW) applications are used to focus electromagnetic energy to improve signal fidelity. Such a technique, known as beam forming, can effectively improve the application range, making it easier to identify threats and avoid targets at great distances. The AESA antenna system comprises of multiple dedicated high performance RF transceivers. Each transceiver (TRX) typically consists of power amplifiers (PA), low noise amplifiers (LNA), up/down converters, and data converters that must be precisely synchronized and clocked with minimal skew to effectively steer the electronic beam. Furthermore, as operating frequencies increase, antenna spacing decreases, leaving little area for TRX circuitry, including data interface and power. Following the TRX subsystem, the data is sent to a digital processor, often a FPGA, where further calibration and signal processing is performed as illustrated in 図 1.

図 1. Radar Block Diagram



This reference design demonstrates an 8-Transmit, 8-Receive (8T8R) analog front end subsystem including the multichannel clock generation. This reference design describes the design details in implementing an 8T8R analog front end with AFE7444 that meets phased-array radar and electronic warfare application requirements.

1.1 Key System Specifications

The 8T8R RF sampling transceiver focuses on the demonstrating the signal chain performance and precise clock synchronization (deterministic latency) with a low noise multichannel clock generator. The system performance is measured with TI's data capture and generator TSW14J57EVM hardware. 表 1 lists the key system-level specifications of the 8T8R transceiver. See Testing and Results (3.2) for more details.

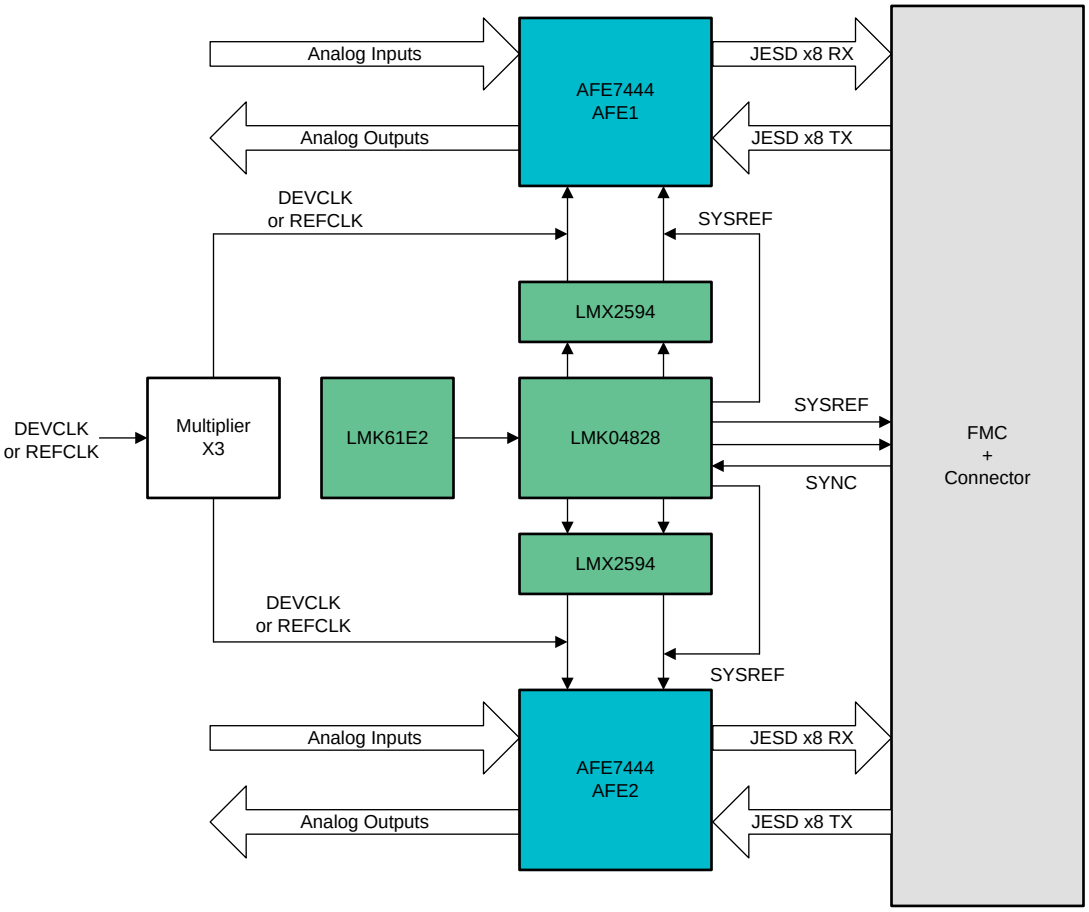
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Transmitter (mode4, interpolation 12), -1 dBFS baseband input		
SFDR (dBc) for 0 – FDAC/2BW	68	890-MHz DAC output signal
	55	1800-MHz DAC output signal
	56	2100-MHz DAC output signal
	62	2600-MHz DAC output signal
SFDR (dBc) for Fout ±250-MHz BW	79	890-MHz DAC output signal
	80	1800-MHz DAC output signal
	70	2100-MHz DAC output signal
	76	2600-MHz DAC output signal
IMD3 (dBc)	73	890-MHz DAC output signal
	72	1800-MHz DAC output signal
	70	2100-MHz DAC output signal
	72	2600-MHz DAC output signal
Receiver (mode9, decimation 16), -3 dBFSdifferential input		
SNR (dBFS)	61.6	1900-MHz ADC input signal
	60	2600-MHz ADC input signal
Skew between RX/TX channels	Variation is less than 10 ps for multiple power cycles	

2 System Overview

2.1 Block Diagram

図 2. TIDA-010132 Block Diagram



2.2 Design Considerations

2.2.1 Multichannel Transceiver Front-End Design

Radar and EW systems typically operate in X, C, S and L frequency bands. Radar and EW are typically based on a multiple wideband frequency conversion super-heterodyne architecture followed by a data converter. The multiple wideband frequency conversion stages use large, complex switched microwave filter banks. The number of wideband frequency conversion stages and the filter banks in the super-heterodyne architecture could be reduced in size and complexity with a wideband high sample rate data converter.

Today, RF sampling analog front-end devices like AFE7444 allow direct sampling of S and L frequency bands. X and C bands could be realized with simpler COTS wideband frequency conversion stages with relaxed filter specifications preceding the AFE7444 using appropriate frequency planning.

Radar signal chain has several unique challenges:

- Radar signal bandwidth is large, typically up to several hundred MHz. The large signal bandwidth requires very fast A/D converters and interface to handle the sampled data.
- Radar signals have high dynamic ranges, typically greater than 70dB. Gain control at the receiver and side-lobe control are critical so that weak signals are not masked by stronger signals.
- Interference level in Radar is high, almost at same level of the required signal. The echo signal must be detected in the presence of noise and jamming signals.

2.2.1.1 Frequency Bands and Applications

S band radars operate on a wavelength of 8-15 cm and a frequency of 2-4 GHz which is less attenuated in propagation compared to other higher frequency bands. Lesser attenuation makes them useful for near and far range radars. The drawback to this band of radar is that it requires a large antenna and antenna array will be challenging.

C and X band radars operate on a wavelength of 4-8 cm - frequency of 4-8 GHz which is more easily attenuated in propagation. Lesser attenuation makes them useful for near-range radars. The antenna size for C and X bands are small that helps to realize antenna arrays. The smaller dimensions also allow applications like turbulence and weather radar in aerospace segment. Higher frequency bands like C and X allow higher bandwidth radar signals resulting in finer range resolution.

The key radar system parameters and their impact on system performance require a basic understating of the radar signal and associated signal processing. The following sections briefly cover the radar signal and processing that is applicable to this reference design.

2.2.2 Radar Signal and Processing

Radar (radio detection and ranging) has three basic functions: detection, tracking, and imaging. 図 3 shows the radar signal transmitted by the antenna striking the target and then reflecting back (echo) to the same antenna.

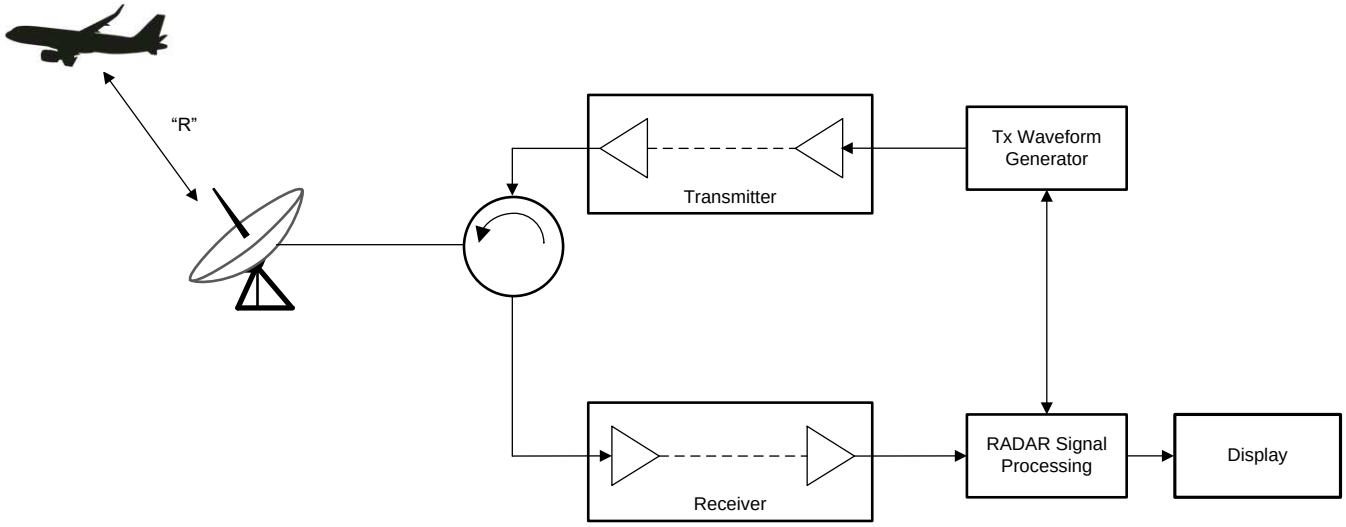
Detection involves determining whether or not there is an object located in some range space. The decision is based on processing the return signal in the presence of receiver noise, clutter echoes, and possible jamming, and determining whether or not the processed signal exceeds a pre-determined threshold.

Tracking is more sophisticated than detection because in addition to detecting the existence of an object, tracking systems attempt to calculate distance to and/or radial velocity of the target.

Imaging radar systems develop image maps of a region and are used to monitor climate, weather conditions, oil spills, land use, and many other things. The advantage of imaging radar systems is the ability to see through clouds, fog, rain, and darkness.

Radar systems can be classified into continuous wave (CW) Radar or a Pulsed Radar based on the transmit signal modulation. CW Radars typically use a circulator to connect the transmitter and receiver to the antenna. Pulsed Radars use a duplexer to connect the transmitter and receiver to the antenna.

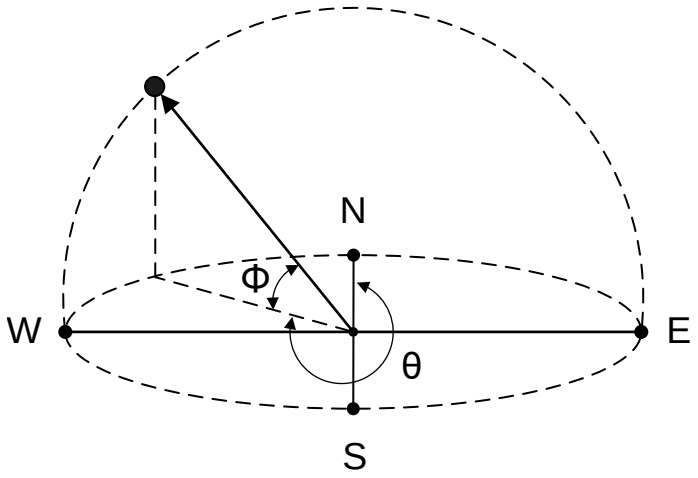
図 3. Radar Signal Flow



2.2.2.1 Performance Metrics

Radar measures the reflectivity in a three dimensional coordinate system (R, θ, ϕ) as shown in 図 4.

図 4. Radar Coordinate System



Where,

R = range to the object in the line of sight direction

θ = azimuth angle

ϕ = elevation angle

The azimuth and elevation angles determine the position of an object in space relative to the observation point. Radar applications such as tracking or searching for multiple objects in space require changing the direction of the antenna beam to effectively map the area surrounding the observer. Electronic beam steering of phased array antennas (composite antennas) allows for an almost-instantaneous change in beam direction (microseconds) and significantly increases the multi-mode capability of the radar system. Some of the common metrics used to measure performance of a radar system are:

- Signal-to-noise ratio (SNR)
- Range resolution
- Doppler resolution
- Range ambiguity
- Doppler ambiguity

2.2.2.2 Signal to Noise Ratio (SNR)

The SNR is the ratio of signal power to noise power and can be calculated at any node of the radar signal chain. SNR is an indication of the signal quality and is proportional to the transmitter power and pulse duration, τ_d, of the signal.

SNR of a pulse radar system, based on simple form of the radar equation, is:

$$SNR = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 k T_o B F L R^4} \quad (1)$$

Where,

SNR = Signal-to-noise ratio at receiver output (before signal processing)

P_t = Peak transmitted power (W)

k = Boltzmann's constant (1.38×10^{-23} J/K)

G = Directional antenna gain

T_o= Antenna effective temperature (290K)

λ = Wavelength = c/f_T (m)

f_T = Transmit frequency

B = Radar operating bandwidth =$1/\tau_d$ (Hz)

σ = RCS (radar cross section) of target (m^2)

F = Receiver noise figure

τ_d = Transmitted pulse duration (sec)

L = Total radar losses

R = Range to target (m)

2.2.2.3 LFM Chirp Signal

Radars use a pulse burst signal that is a linear frequency modulation (LFM), usually referred to as an LFM chirp signal, that can be represented as 式 2.

$$x(t) = a(t)\sin(2\pi f_T t + \pi\beta / \tau_d t^2) \quad (2)$$

Where,

x(t) = Radar chirp signal

a(t) = Amplitude of the chirp

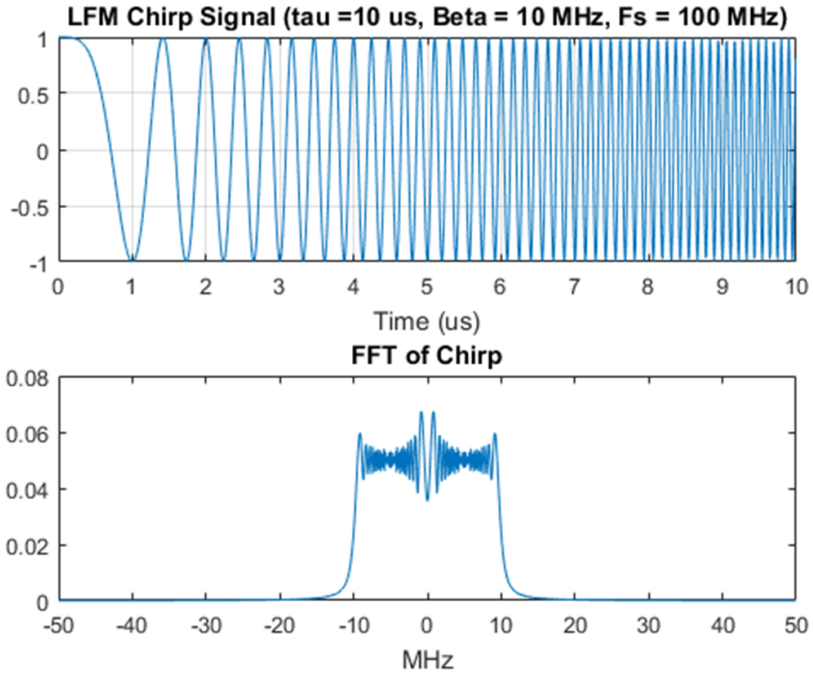
f_T = Transmit frequency

β = Frequency sweep range

τ_d = Pulse burst duration

The time and frequency domain plot of the chirp signal is shown in 図 5. Key parameters for the chirp signal are pulse duration, frequency sweep range, sampling frequency, and the time bandwidth product. The time bandwidth product is the product of the pulse width or burst time, τ_d, and the pulse bandwidth or equivalently the frequency sweep range, β.

図 5. Radar Linear Chirp and Frequency Spectrum

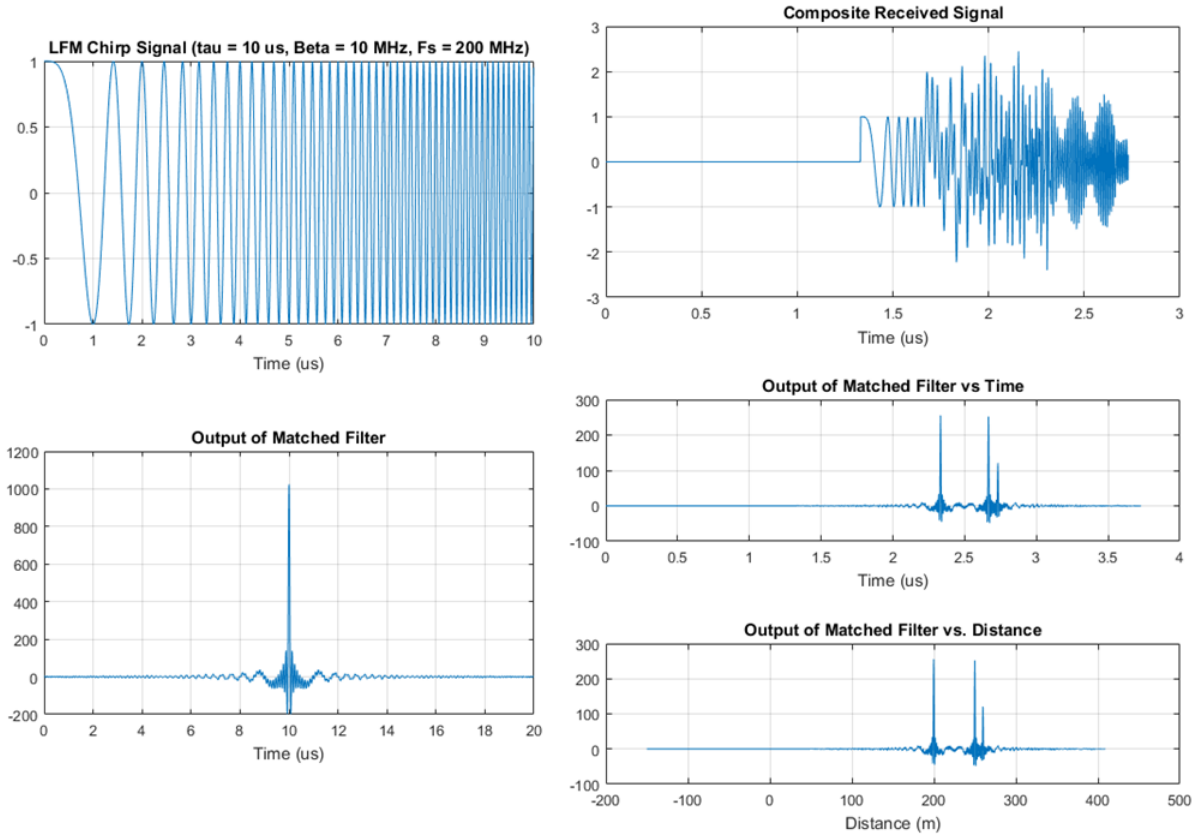


The Nyquist sampling rate for an LFM chirp signal would be 2 β, but in practice, the signal should be significantly oversampled to relax filtering requirements.

2.2.2.4 Pulse Compression and Matched Filter

As shown in 図 6, an LFM chirp signal, when processed through a filter matched to the chirp signal, produces a much narrower, better-defined peak in the output response. The narrow pulse output as a result of a matched filter is called *pulse compression* of the LFM chirp signal. The narrow, well-defined peak indicates that an echo is received from the chirp signal that was transmitted by this design's transmitter. The time offset of the peak with reference to the transmitted chirp signal gives the distance information of the target and the amplitude of the pulse indicates the size of the target.

図 6. Matched Filter Output for Linear Chirp With and Without Noise



2.2.2.5 *Radar Range and System Dynamic Range*

Matched filtering of the LFM chirp signal (echo) improves the system SNR (process gain) proportional to the time bandwidth product of the radar pulsed signal:

$$SNR_{out} / SNR_{in} = 2\beta\tau_d \quad (3)$$

Where,

SNR_{OUT} = Output peak instantaneous SNR

SNR_{IN} = Signal-to-noise ratio into matched filter

β = Pulse bandwidth (frequency sweep for LFM chirp)

τ_d = Pulse duration (sec)

For radar systems using LFM chirp signals, the time bandwidth product ranges from 5 to several 1000. Longer pulse duration and wider-bandwidth LFM chirp signals will improve system SNR and dynamic range.

2.2.2.6 Radar Range Resolution

The radar range resolution is the minimum between the two objects a radar system can resolve. One benefit of matched filtering of the LFM chirp signal (echo) is that it decouples the dependency of the pulse duration on the range resolution. The range resolution, in meters, using an LFM chirp signal with a frequency sweep range of β (Hz), is given by 式 4.

$$\Delta R = c / 2\beta \tag{4}$$

Where,

ΔR = Range resolution for chirp pulse (m)

c = $3x10^8$ (m/s)

β = Frequency sweep range (Hz)

2.2.2.7 Doppler Processing and Radial Velocity

Radar signal processing must handle Doppler frequency shifts due to moving targets. The frequency of the echo increases if the target is moving towards the radar and vice-versa. The moving target velocity can be computed from the Doppler shift using 式 5.

$$v = (cf_D) / (2f_T) \tag{5}$$

Where,

v = Target radial velocity (m/s)

c = 3 x 108 (m/s)

f_D= Doppler shift (Hz)

f_T= Transmit frequency (Hz)

A moving target changes the expected matched filter output to an LFM pulse; the peak time will shift, the peak output level will decrease, and the main peak will widen. The shift in peak time results in an error in range estimation proportional to the Doppler shift, f_D, is as follows:

$$R_{error} = -(c\tau_d f_D) / (2\beta) \tag{6}$$

2.2.3 Multichannel Clock Generation, Synchronization and Calibration

Radar and EW signal chain will have multiple wideband RF transceivers. Each transceiver needs a low-noise clock at the precision phase to achieve a low channel-to-channel skew. The clock generation should have low jitter to meet system SNR and SFDR requirements. The clock generation should also have a provision to adjust the clock phase in fine steps to minimize the channel-to-channel skew. The clock phase adjustment is typically done as part of system calibration and across operating temperature range.

2.2.3.1 Clock Jitter and System SNR

The ADC SNR degrades due to external clock jitter and internal ADC aperture jitter. SNR of the ADC, limited by the total jitter, can be calculated as:

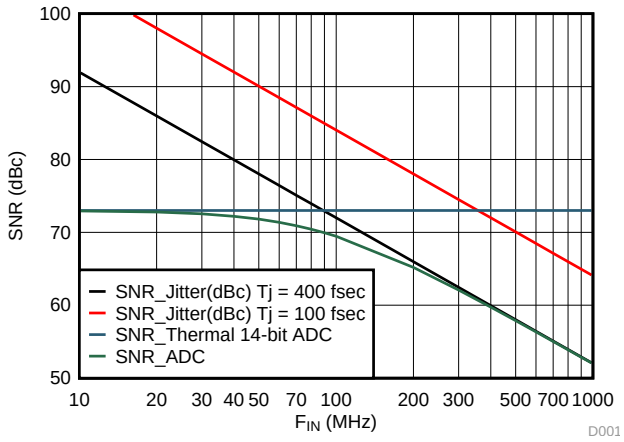
$$(SNR)_{jitter} = -20log(2\pi f_{in} T_{jitter}) [in \quad dBc] \tag{7}$$

SNR of the ADC is also affected by ADC's quantization noise, thermal noise, and jitter. The effective SNR of ADC that includes all of these artifacts can be represented as:

$$(SNR)_{ADC} = -20log\sqrt{([10^{-\frac{SNR_{quantization\ \ noise}}{20}}]^2 + [10^{-\frac{SNR_{thermal\ \ noise}}{20}}]^2 + [10^{-\frac{SNR_{jitter}}{20}}]^2)} \quad [in \quad dBc] \tag{8}$$

図 7 shows the effective SNR of a 14-bit ADC from Texas Instruments. The external clock jitter depends on the clock generator section and should be designed in such a way that it is not limiting the ADC SNR performance.

図 7. Jitter and Thermal Noise Impact on ADC SNR



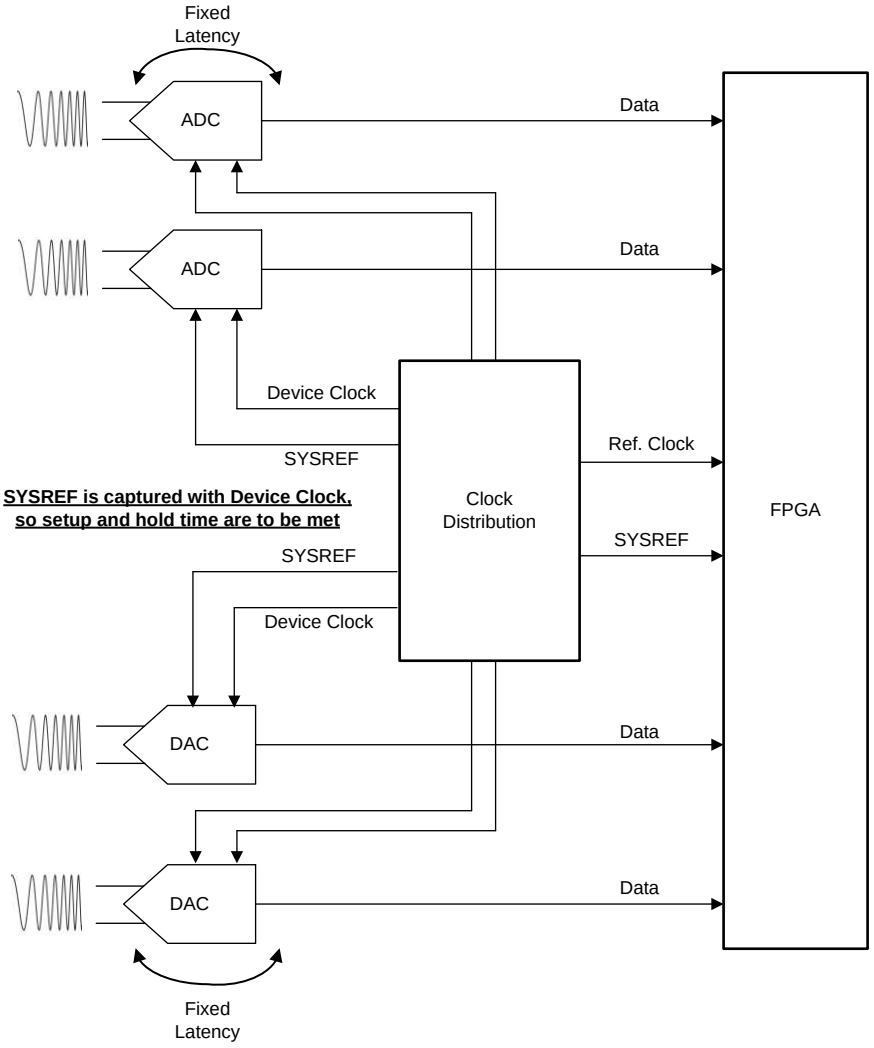
2.2.3.2 Device Clock and SYSREF Requirement for Multiple Data Converters

A signal chain that uses multiple data converters must have clocks that are synchronized to make sure all of the sampling instances of the data converters are aligned. However, in the case of a JESD204B-based data converter, the following requirements for device synchronization are critical for performance.

- Phase align device clocks at each converter
- Generate and capture SYSREF signal with appropriate timing margin
- Achieve deterministic latency with appropriate elastic buffer release point

図 8 represents critical requirements to achieve device synchronization and deterministic latency. The serializer-deserializer (SerDes) data lanes connecting the FPGA and data converters need not be length matched, as the JESD204B deterministic absorbs delay variations.

図 8. Device Clock and SYSREF Requirement



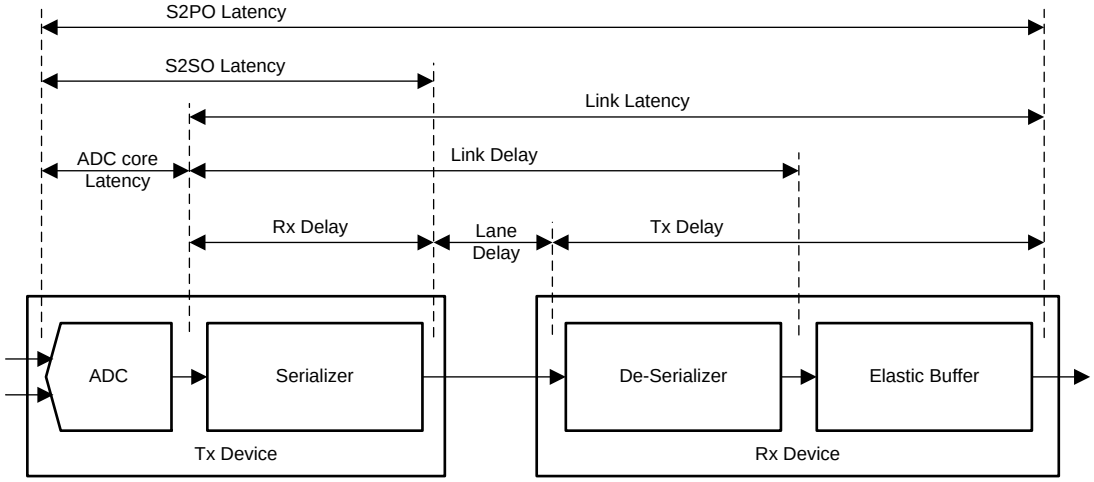
To achieve multi-device synchronization, SYSREF must meet setup and hold times relative to the device clock. The frequency of SYSREF must meet LMFC and clock divider requirements. The implementation requirements of SYSREF will depend on whether the interface is AC coupled or DC coupled. Errors in the capture of SYSREF will result in some number of device clock cycle variations between devices, and JESD204B devices must have some features that can help meet some of these needs.

2.2.4 Deterministic Latency

JESD204B-based serial data interface between data converters and FPGA/ASIC helps to improve PCB area, size, power, and timing complexity. When serial data interface is used, the link latency, as indicated in 図 9, should be deterministic to have consistent performance for every power cycle. Deterministic latency is the repeatability of the link latency over power cycles and re-sync event. As an example, inconsistent latency in a time interleaved multiple data converter system, typically used to achieve high sample rate, will result in random ordering of samples over different power cycles. Knowing the exact link latency is usually not as important compared to constant link latency.

JESD204B protocol has defined 3 subclasses out of which 2 subclasses support deterministic latency of the link. Subclass 0, which is backwards compatible with JESD204 and JESD204A, does not support deterministic latency. Subclass 1 supports deterministic latency by use of a system reference signal called SYSREF. Subclass 2 supports deterministic latency by a dual purpose use of the ~SYNC signal. Subclass 2 is typically used only for data converters with less than 500-MSPS data converters due to the complex timing requirement for ~SYNC signal.

図 9. Link Latency in Data Transfer Path



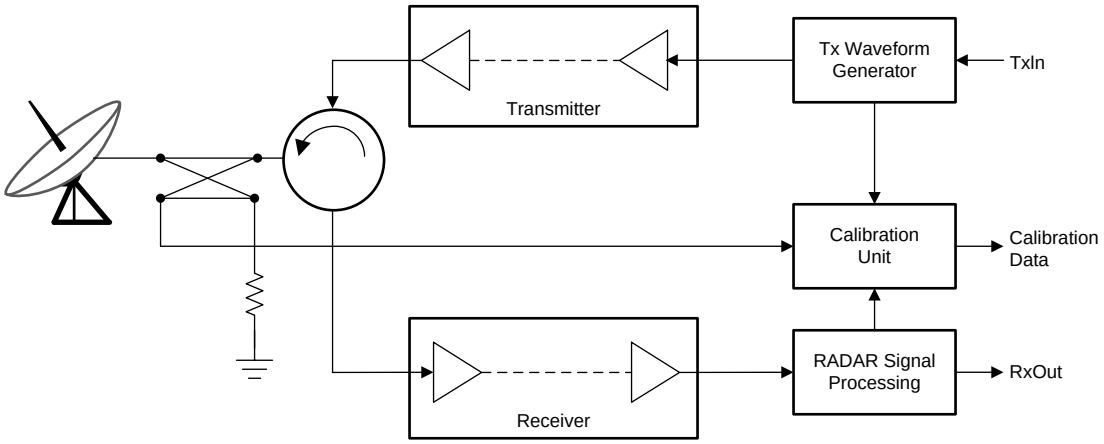
S2PO – Serial to Parallel Output
S2SO – Serial to Serial Output

2.2.5 System Calibration

The multichannel signal chain, comprising of multiple Transmit-Receive Modules (TRM) must be calibrated for phase and amplitude errors. The phase and amplitude errors must be minimized across the TRMs to meet the system accuracy requirement. The complexity of radar TRM and the real-time correction requirement pose additional challenges for the calibration, offer new opportunities for the calibration such as on-board error correction and digital calibration.

It is preferable to have the real time calibration to avoid interruption to the radar operation and performance during the real time calibration process. A typical calibration process on the signal chain involves injecting a calibration chirp tone outside of the receiver band and calibrating the receive chain. Once the receiver chain is calibrated, the transmit chain can also be calibrated by doing a loopback from transmit to receive path.

図 10. Typical Front-End Calibration Scheme



The calibration algorithm will also consider other physical quantities like temperature, humidity, and time to arrive at an appropriate error correction or compensation scheme. The error correction or compensation can be done at different node in the signal path, such as:

- Fine adjustment of data converter clock timing to minimize channel-to-channel skew
- Fine adjustment of the weights of the adaptive matched filter in the receive path

The objective of the above process is to minimize the channel-to-channel phase and gain variations in the signal chain thereby improving the overall system accuracy.

2.2.6 Data Transfer - FMC Interface Considerations

Radar systems often need to support multifunction mode which dynamically change the function system functions and operating parameter adapting to the environmental changes. The adapting requirement is similar to the specifications of cognitive and software defined radios. Modern radars have most of the radar signal processing in digital domain, and the digital boundary is moving closer to the antenna. The dynamic configuration of the radar functions and the digital boundary moving closer to the antenna makes the data transfer interface between the analog front end and the digital domain a critical requirement in terms of speed, latency, and capacity. A FMC-based interface is typically preferred for the data transfer interface.

FPGA Mezzanine Card (FMC) is an ANSI/VITA 57.1 standard based interface that defines IO mezzanine modules connecting to an FPGA or similar device with re-configurable IO capability. FMC specifies a low-profile connector and compact board size for compatibility with several industry standard slot card, blade, low profile motherboard, and mezzanine form factors. Some of the benefits of FMC are:

- Widely adopted by large number of vendors who develop FPGA card
- More flexible I/O than PMC/XMC
  - Differential data pair, differential clock pairs, high speed SerDes and clock
  - I^2C control
  - JTAG
  - Power
- Support for wide parallel interfaces
  - Low latency

- Support for higher speed I/O
- Configurable voltage support

The FMC connector pinouts are standardized. Designs based on the FMC should try to use the SerDes lanes and the differential data optimally to maximize the data converter count and minimize latency.

2.2.7 Power Supply Design Considerations

Low noise power supply is critical to the performance of the analog front end. 図 11 shows the noise coupling paths from power supply to the analog front end. 図 11 also shows the impact of the power supply noise on the output spectrum of the data converter. As mentioned, the data converter spectrum has two components due to power supply noise:

- Direct coupled frequency component
- Modulated frequency component

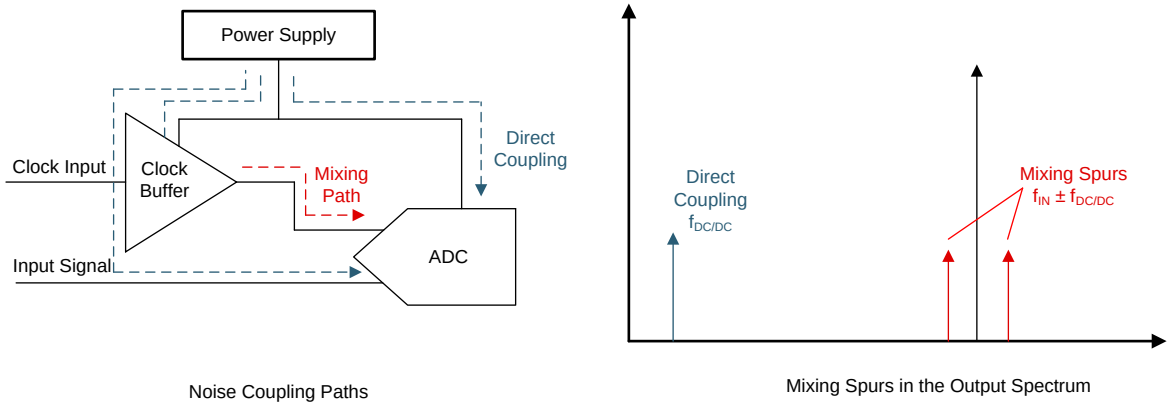
System design should consider the following for a robust design:

- Reduce the noise at the source
- Eliminate or minimize the coupling path
- Desensitize the victim to noise

In the analog front end, the clock power rails and the analog power rails of data converters need low noise power supply. Necessary precautions must be taken in terms of using a post regulator for DC/DC converter or appropriate filtering of DC/DC converter output.

DC/DC converter followed by an LDO has tradeoffs in terms of size and thermal performance. Multiple DC/DC converters must be frequency synchronized to reduce beat frequencies and EMI.

図 11. Power Supply Noise Coupling Paths and Impact in Signal Chain



Noise Coupling Paths

Mixing Spurs in the Output Spectrum

In case of multiple power rails, care should be taken for proper sequencing of the power rails according to the load (data converters, MCU or FPGA) requirements.

2.3 Highlighted Products

2.3.1 AFE7444

The AFE7444 is a quad-channel wideband, RF-sampling transceiver based on 14-bit, 9-GSPS DACs and 14-bit, 3-GSPS ADCs. The AFE7444 offers very high integration (RF ADC, RF DAC, clock generation, digital up- and down conversion, RF gain control, power detectors, and so on) to meet the needs of high-density applications, such as phased array radar and electronic warfare. AFE7444 can handle wide input bandwidth and allows direct RF sampling up to 6 GHz. The AFE7444 as a wideband RF sampling transceiver. Implementation with AFE744 is flexible as it can process very wide instantaneous bandwidths up to 800 MHz to 1200 MHz or smaller single and dual band frequency spectrums as low as 200 MHz. The DAC signal path supports interpolation and digital up conversion option that supports up to 800 MHz of signal bandwidth. The differential output path includes a digital step attenuator (DSA), which provides tuning of output power.

2.3.2 LMX2594

The LMX2594 is a high-performance, wideband RF PLL with integrated VCO that supports a frequency range from 10 MHz to 15 GHz without using an internal doubler. The high performance PLL with a figure of merit of –236 dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter. The device's integrated noise of 45 fs for a 7.5-GHz output makes the device an ideal low-noise clock source. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-noise clock and SYSREF generator for high-speed data converters. Fine delay adjustment (9-ps resolution) is provided in this configuration to account for delay differences of board traces. This device uses a single 3.3-V supply and has integrated LDOs that eliminate the need for onboard low-noise LDOs.

2.3.3 LMK04828, LMK04832

The LMK04828 is a dual-PLL jitter cleaner and clock generator for JESD204B systems. LMK04828 has 14 clock outputs from PLL2 that can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. LMK04828 supports a range of two VCOs that are 2370 to 2630 MHz and 2920 to 3080 MHz. The LMK04828 also supports a distribution mode, which accepts the high-frequency reference signal and distributes it to all 14 clock outputs without adding a PLL noise.

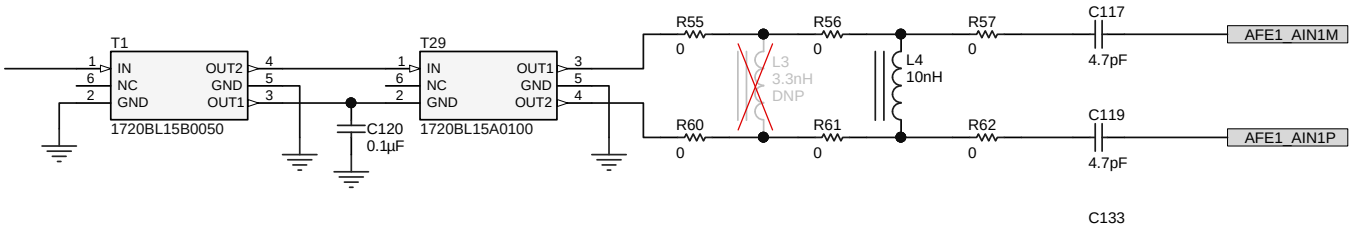
2.4 System Design Theory

2.4.1 Analog Front End

The analog front end section is implemented using two AFE7444, to realize the 8T8R transceiver that is suitable for radar and electronic warfare applications. The RF ADCs have differential input, and a balun is used to convert a singled input drive to differential drive. A 1:2 balun transformer is required to convert the 50-Ω single-ended signal to 100-Ω differential for input to the ADC. The balun outputs can be either ac-coupled, or directly connected to the ADC differential inputs, which are terminated internally. The balun and associated matching circuit should provide a good match to 50 ohms at the frequency of interest. 図 12 shows the input matching used for the ADC input. The first balun at the input of the ADC

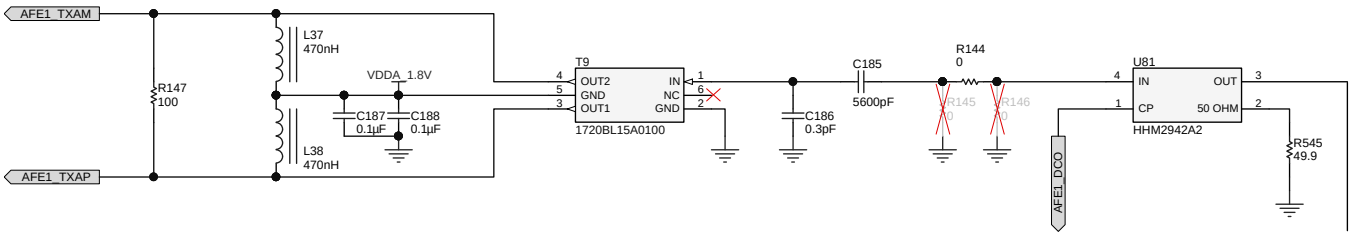
1720BL15A0100 is the 1:2 balun and the preceding balun, 1720BL15B0050, is a 1:1 50 ohms balun. Configuration like this provides good phase balance and return loss better than 15 dB in a 800- to 2800-MHz input frequency range. The matching components should be as close as possible to the AFE7444 input pins to minimize the parasitic effects. A LTCC balun is chosen because it results in a compact front-end matching circuit for 8 receive channels of a single AFE7444.

図 12. ADC Input Matching Circuit



RF DAC outputs are differential and converted to single-ended using 1:2 LTCC balun 1720BL15A0100. The DAC output needs DC feed bias, which can be provided through L37 and L38 as shown in 図 13. There is an option to feed the DC bias through the LTCC balun. There are 4 transmit paths per the AFE7444 and one of the transmit paths (channel A) has a directional coupler (18 dB at 2500 MHz) to provide a feedback to the other AFE7444. The feedback option can be used to calibrate the clock timing during the system calibration process.

図 13. DAC Output Matching Circuit



2.4.2 Clock Tree and Options

The AFE7444 has few clocking options. In one of the clock options, the DAC can be fed to AFE7444 and the ADC clock and other clocks for the device is derived by the AFE7444 itself. The ADC clock is generated within the device by a programmable clock divider from the DAC clock. For multi-device ADC clock synchronization, the clock divider (Fdac/Fadc) resets through SYSREF. For synchronizing the NCOs in multiple devices, NCO frequency should be an integer multiple of SYSREF frequency and also reset through SYSREF. The AFE7444 requires a DC-coupled SYSREF with 0.5-V, common-mode voltage to operate properly in a system. For more details, see the DAC3xJ8x Device Initialization and SYSREF Configuration application report on DAC3xJ8x device initialization and SYSREF configuration, which has a similar SYSREF requirement as the AFE7444.

図 14 shows the clocking scheme using the LMX2594 generating the device clock for the AFE7444s and the LMK04828 generating the SYSREF. The LMK04828 SYSREF level is made compatible to the SYSREF requirement of the AFE7444.

図 14. AFE7444 Clocking Scheme With LMX2594 and LMK04828

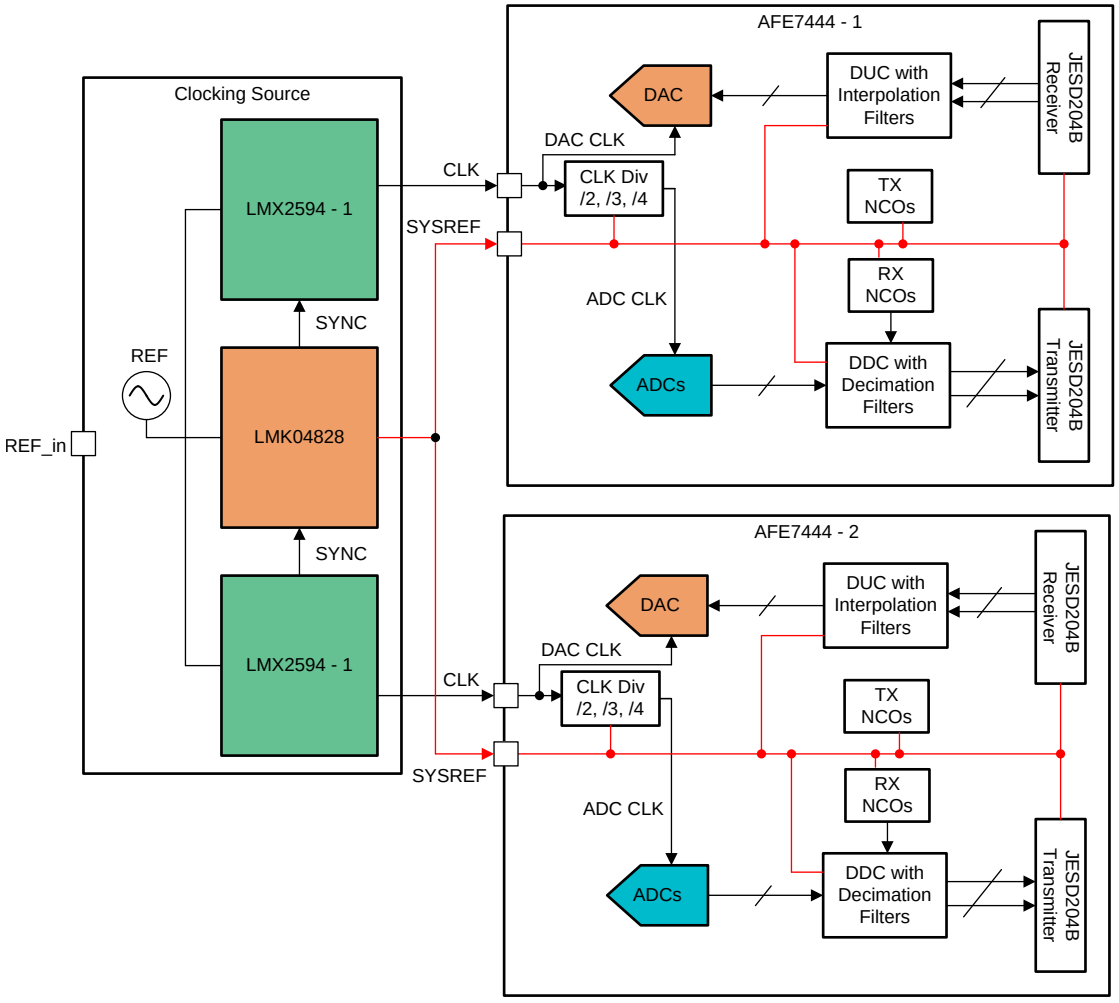


図 15 shows all of the clocking options on the TIDA-010132 board. The default option is configured for the LMX2594 device clock generation and the LMK04828 generates the SYSREF. As shown in 図 15, a reference clock is generated by the LMK61E2 and is provided to the LMK04828 at the OSCin input. The LMK04828 generates SYSREF for the two AFE7444 devices, which is marked as *option 2*. The LMK04828 also provides FPGA reference clock and SYSREF to the TSW14J57 capture card through the FMC+ interface. The LMK04828 is configured in PLL mode to phase synchronize OSCin with all the clocks generated by the LMK04828.

Phase-synchronized device clocks to the AFE7444s are generated by the using a common reference clock to the REF_in of the two LMX2594 synthesizers using the LMK00304 marked as *option 1* and the SYNC signals for the LMX2594 are from the LMK04828, marked as *option 4*. As shown in 図 14, SYSREF and the device clock to the AFE7444s are provided through the LMK04828 and LMX2594, respectively. SYSREF to the AFE7444s are provided through two different outputs of the LMK04828, which allow independent SYSREF timing adjustments to meet the setup and hold time for the AFE7444s.

This design uses a device clock of 5898.24 MHz and a SYSREF setup, and the hold times of the AFE7444 are 50 ps each. With this, the valid window for meeting the setup and hold time is approximately 69 ps, which is less than the step size (150 ps) of SYSREF from the LMK04828. Hence, phase delay must be provided in device clocks, which is done by the MASH_SEED value in the LMX2594. Each LMX2594 device may require tuning for the MASH_SEED delays to achieve in-phase generated clocks and meet the setup and hold time of the SYSREFs. Use following frequency settings to configure the AFE7444 RX in Mode9 and TX in Mode 4:

- DAC_CLK = 5898.24 MHz
- ADC_CLK = 2949.12 MHz
- PLL_reference_CLK = 61.44 MHz
- ADC decimation = 12
- DAC interpolation = 12
- SYSREF = 15.36 MHz
- FPGA_CORECLK = 245.76 MHz
- ADC SERDES lane rate = 9.8304GSPS
- DAC SERDES lane rate = 9.8304GSPS

図 15. TIDA-010132 Clock Options

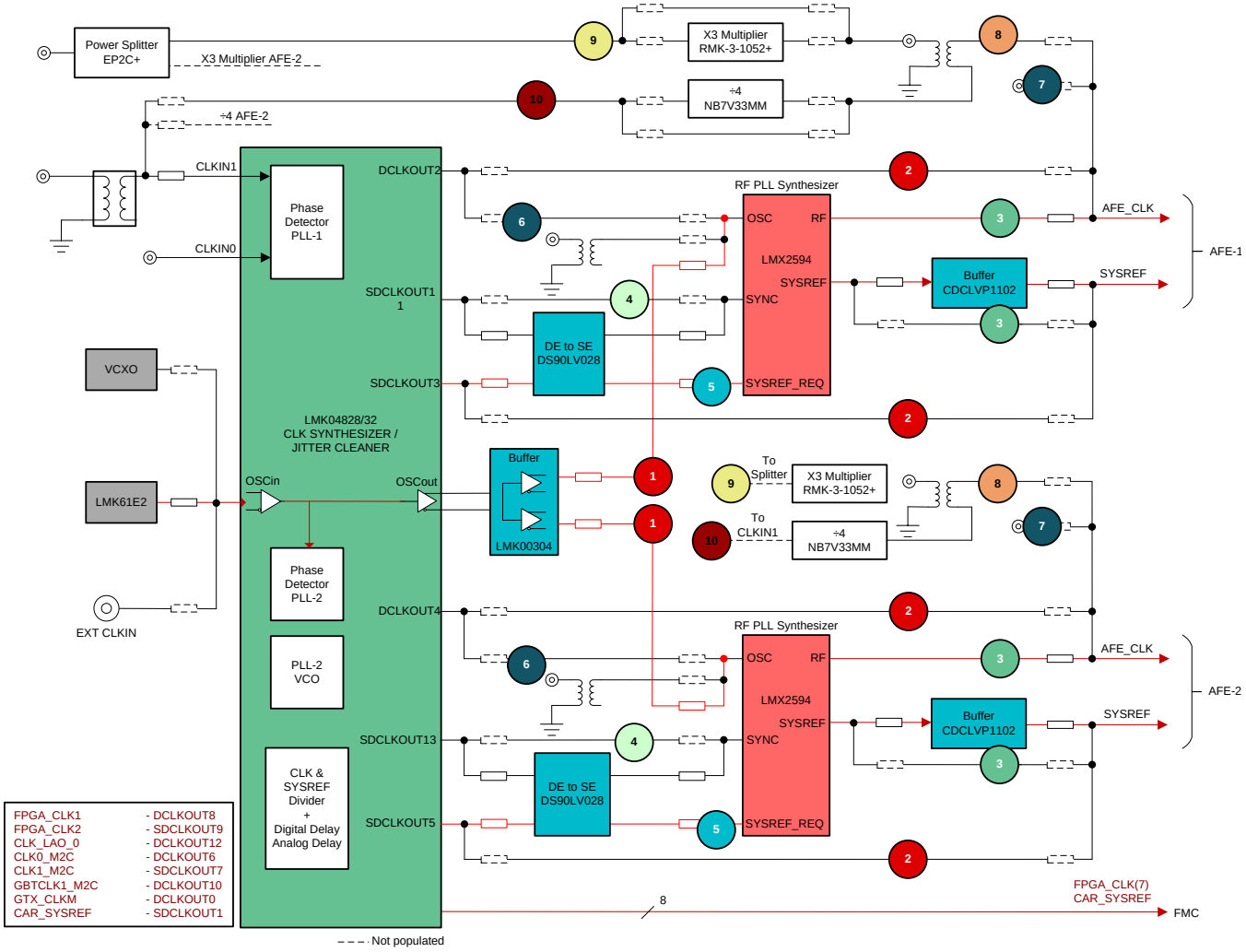


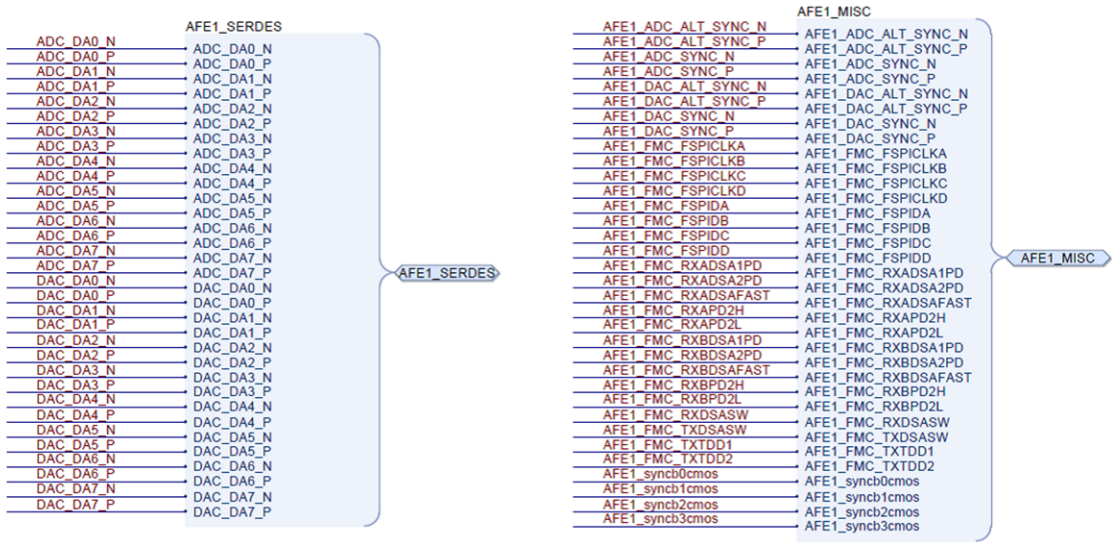
表 2. TIDA-010132 Clock Options

Option 1	PLL reference clock of LMX2594 devices from LMK00304 buffer
Option 2	AFE7444 DEV_CLK and SYSREF from LMK04828
Option 3	AFE7444 DEV_CLK and SYSREF from LMX2594
Option 4	SYNC to LMK2594 from LMK04828
Option 5	LMX2594 SYSREF_REQ from LMK04828
Option 6	LMX2594 PLL reference from LMK04828
Option 7	External differential clock for AFE7444
Option 9, Option 8	External device clock with multiplier input to AFE7444 device clk
Option 10, Option 8	AFE7444 device clock with divider input to LMK04828 (distribution mode)

2.4.3 Data Transfer and FMC

A single AFE7444 has 8 SerDes lanes for TX and 8 SerDes lanes for RX. This design, with two AFE7444s, has 16 TX SerDes lanes and 16 RX SerDes lanes that are connected to the FMC+ connector. Apart from the SerDes lanes, the SPI lines, JTAG lines are also connected to the AFE7444 and the clock devices as shown in 図 16. SYNC and ALT_SYNC signal are connected to the AFE7444's ADC and DAC. Connecting two AFE7444s to a single FMC+ eases the data capture and generation because the timing synchronization is much simpler within an FPGA. The FPGA firmware also supports timing synchronization across multiple FMC.

図 16. FMC Signals for a Single AFE7444



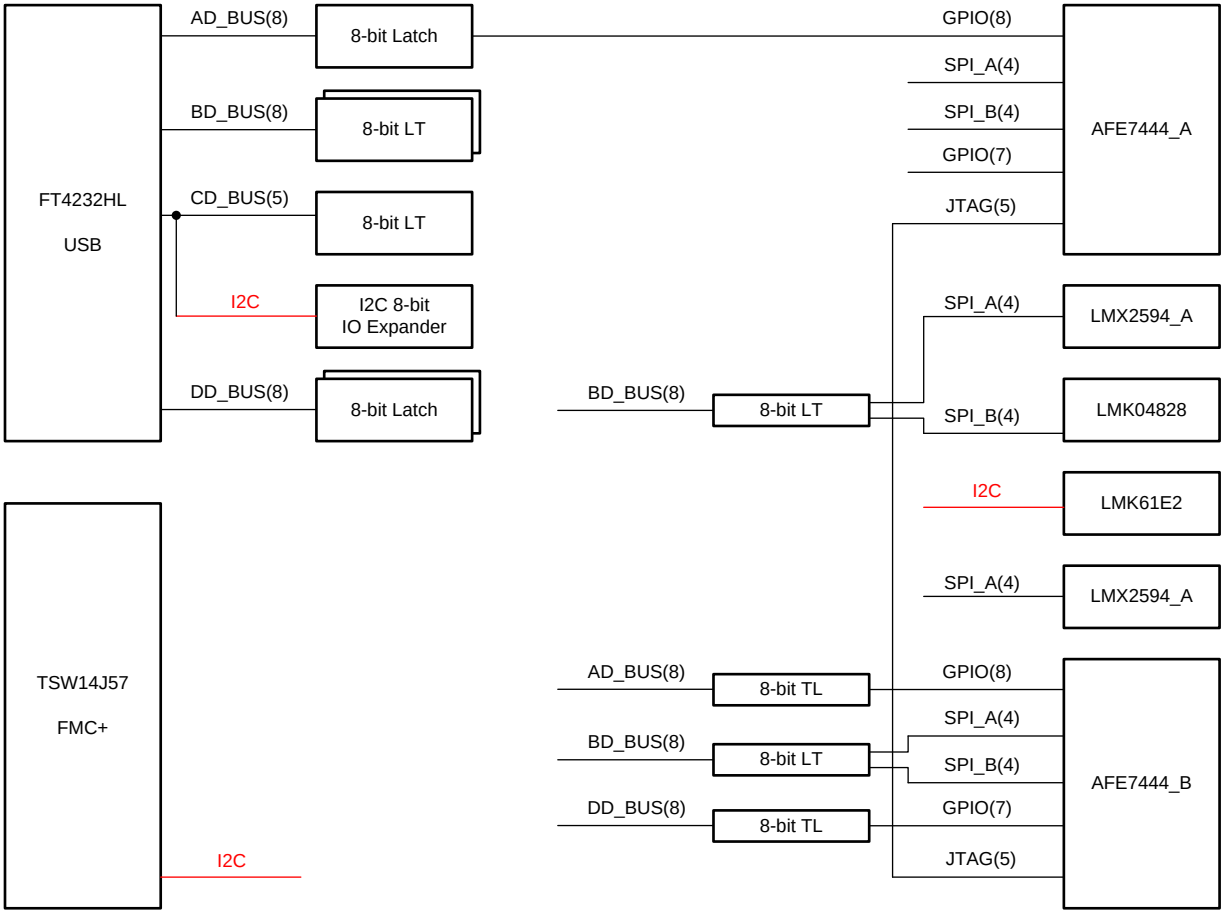
2.4.4 Programming Interfaces

The TIDA-010132 has the following programming options, also shown in the 図 17.

- USB programming
- FMC+ programming
- Direct interface to each device

By default, the USB programming option is configured. Each AFE7444 has two SPI ports which are connected to the FT4232 Quad High Speed USB to Multipurpose UART/MPSSE device. The FT4232 is also configured to emulate an I^2C interface and SPI that connects to the LMX2594, LMK04828, and LMX61E2 devices. The I^2C interface is connected to an IO expander that is used to do various CS signal for the SPI interface device.

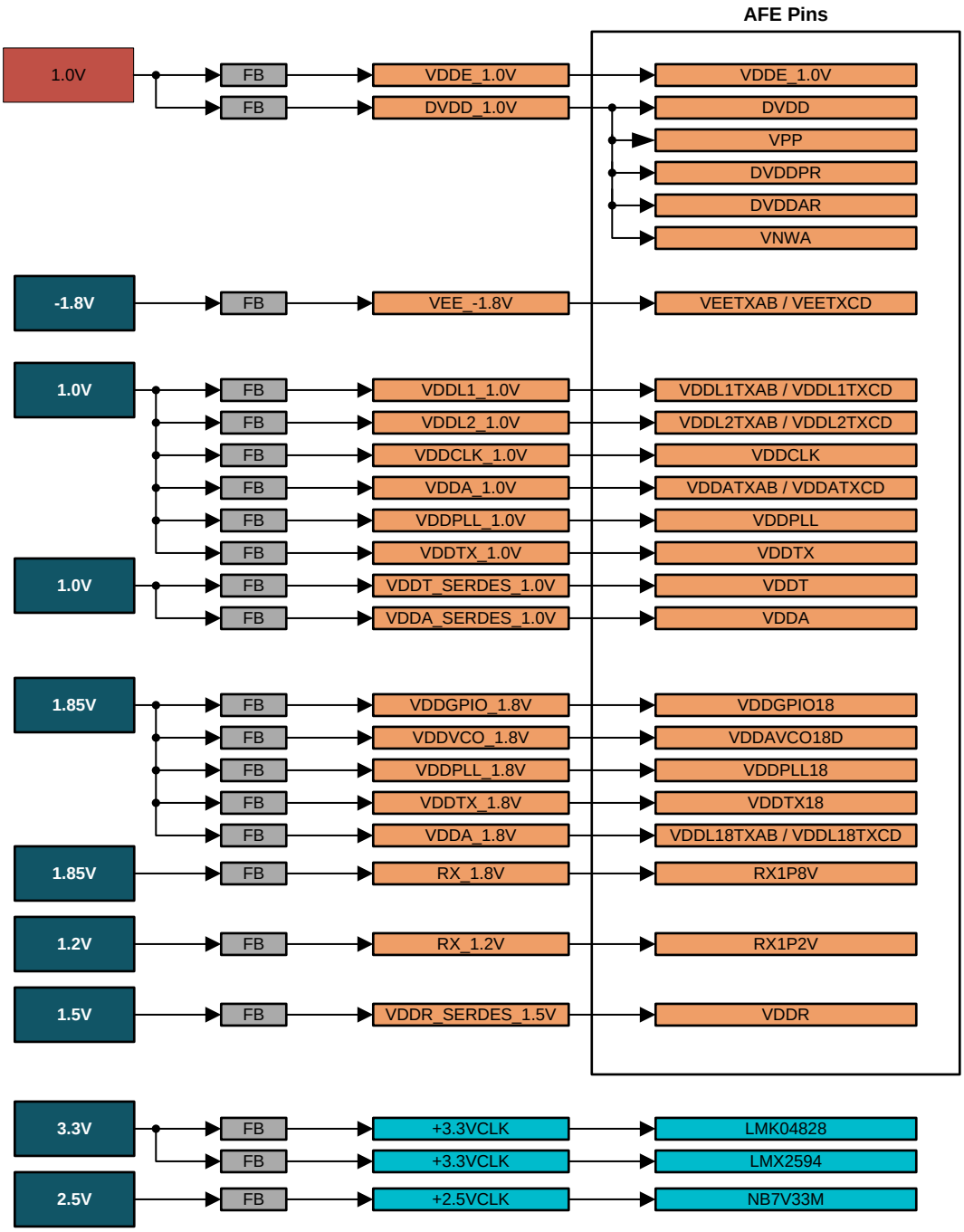
図 17. Programming Interfaces in TIDA-010132



2.4.5 Power Tree

The various power supply rail requirements for the TIDA-010132 are shown in 図 18. The TIDA-010132 design uses an external power supply, which is a standalone reference design, to demonstrate and evaluate various power supply configurations and options for the TIDA-010132.

図 18. TIDA-010132 Power Rails



The power consumption of the two AFE7444s is calculated as shown in 表 3. These are typical values. The power supply board should have a margin of around 25% to take care of variations in different modes of operation and environmental conditions.

表 3. AFE7444 Power Consumption

PIN NAME	VOLTAGE	CURRENT (mA)	CURRENT x2	POWER	GROUPING
DVDD_1.0V	1	6018	12036	12036	1
VEE_1.8	-1.8	314	628	1130.4	2
AVDD_1.0V	1	1985	3965	3965	3&7
AVDD_1.8V	1.8	986	1972	3549.6	4
RX_1.2V	1.2	849	1698	2037.6	5
RX_1.8V	1.85	1010	2020	3737	6
Total Power				26.5	Watts

2.4.6 PCB Layout Considerations

2.4.6.1 PCB Stackup

The TIDA-010132 is a layer PCB with the layer stackup as shown in 表 4. The ground and power layers, with a 2-ounce copper thickness, are required to have low voltage drop when high currents are drawn by the AFE7444. The DVDD_1.0V rails of the AFE7444 draw a current of more than 12 A. Care should be taken to route the power plane connecting these pins with wide plane widths and minimum vias cutting the connecting planes.

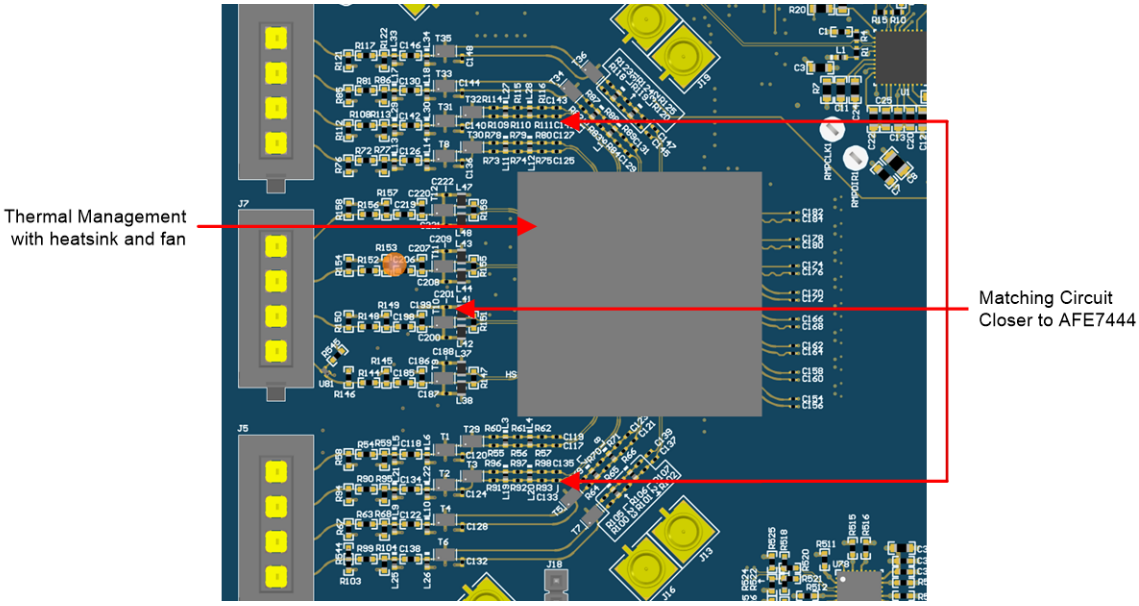
表 4. TIDA-010132 PCB Layer Stackup

LAYER NUMBER	LAYER	LAYER TYPE	Cu THICKNESS
1	L1_Top Layer	Signal	0.5 oz
2	L2_GNDP1 Layer	PWR/GND	2 oz
3	L3_PWRP1 Layer	PWR/GND	2 oz
4	L4_SIG1 Layer	Signal	0.5 oz
5	L5_GND Layer	Signal	0.5 oz
6	L6_SIG2 Layer	Signal	0.5 oz
7	L7_GND Layer	Signal	0.5 oz
8	L8_SIG3 Layer	Signal	0.5 oz
9	L9_GND Layer	Signal	0.5 oz
10	L10_SIG4 Layer	Signal	0.5 oz
11	L11_PWR Layer	PWR/SIG	0.5 oz
12	L12_PWRP2 Layer	PWR/GND	2 oz
13	L13_GNDP2 Layer	PWR/GND	2 oz
14	L12_Bottom Layer	Signal	0.5 oz

2.4.6.2 Front-End Placement

The analog matching circuitry for the ADC inputs and DAC output should be placed closer to the AFE7444 to ensure good return loss with the input and output ports. As shown in 図 19, the matching circuit uses LTCC-type baluns, which are small in footprint and can be placed closer to the AFE7444. There are 8 paths for the ADC input and 4 paths with matching circuit for each AFE7444. Apart from keeping the matching circuit closer to the AFE7444, the spacing between the matching circuits of adjacent channels must be sufficient enough to get less than 70 dB of isolation to minimize channel-to-channel crosstalk.

図 19. Front-End Placement

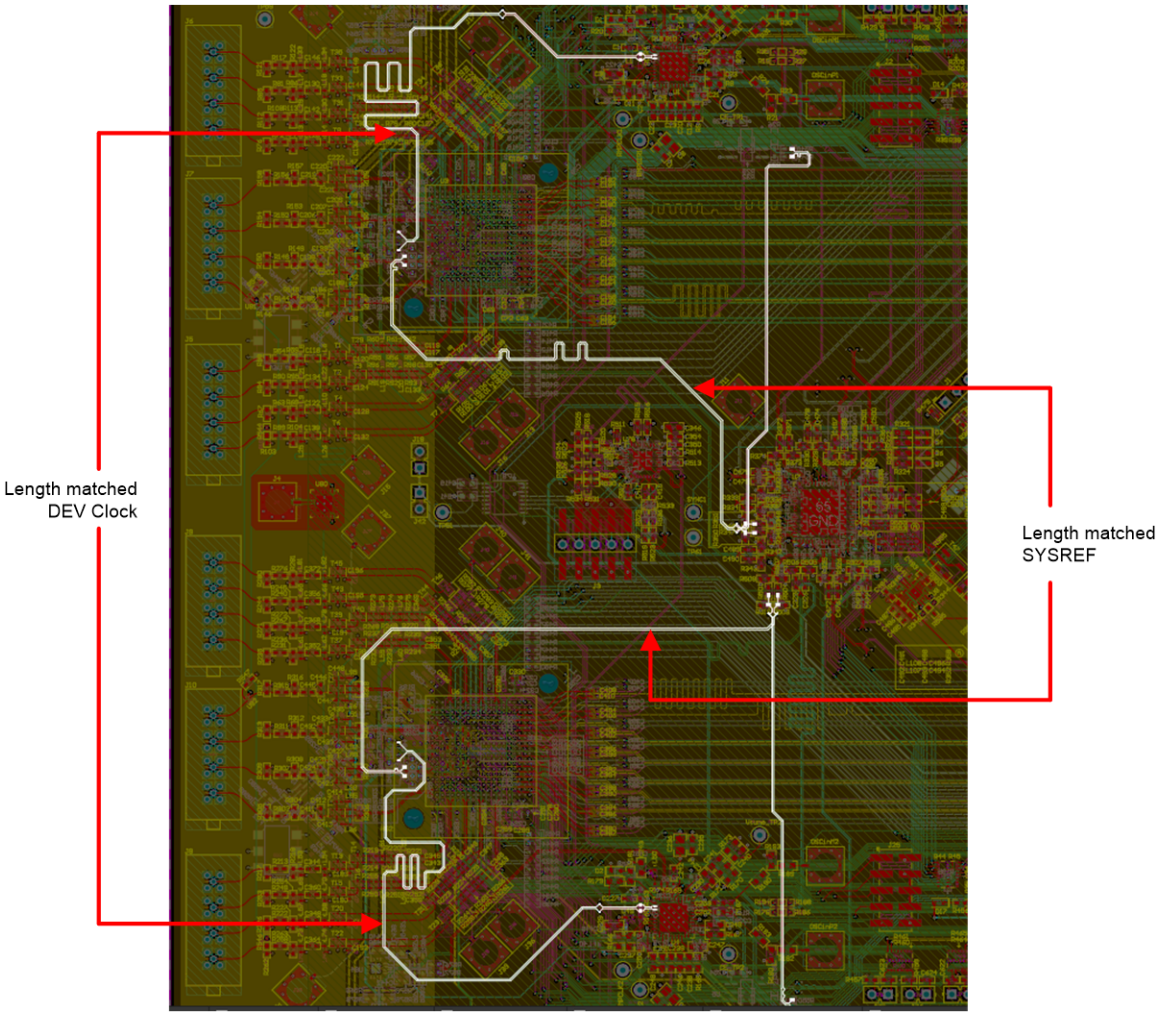


Each AFE7444 consumes around 12 W of power. Adequate provisions for heat removal from the AFE7444 should be provided to have good margin in the device junction temperatures. The 2-ounce copper ground and power plane provide a path to heat flow. However, the copper planes are not sufficient to remove the heat, and hence, a heatsink with fan mounted on the top of the AFE7444 is provided.

2.4.6.3 Clock Routing and Precautions

The device clocks to the AFE7444 should be maintained at minimum skew to achieve low channel-to-channel skew. Minimizing the clock skew due to PCB routing is critical to get good timing margins for the SYSREF gating. The device clocks to the AFE7444 must be length matched from the LMX2594 as highlighted in 図 20. The SYSREFs from the LMK04828 to the AFE7444 should also be length matched. Apart from the length matching, the reference clocks to the LMX2594 should also be length matched to get the reference clock skew to a minimum.

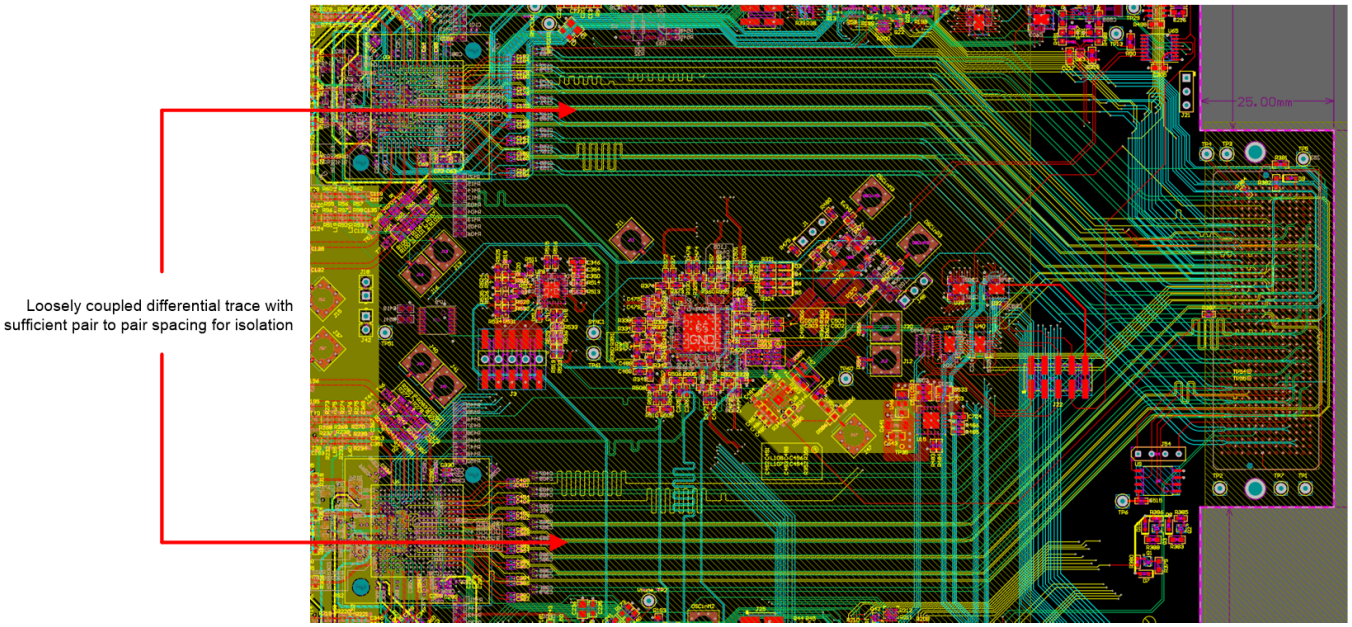
図 20. Device Clock and SYSREF Routing



2.4.6.4 FMC Serdes Routing

There are 16 SerDes lanes for each AFE7444. The SerDes lanes are routed as loosely coupled differential traces to get good return loss and better margin in the eye pattern. The lane-to-lane spacing is also critical to get the crosstalk to a minimum. The constraints force the use of multiple routing layers to achieve the required crosstalk isolation and return loss. As shown in 図 21, the SerDes lanes run crisscross near the FMC connector, which require additional precautions to manage return loss and crosstalk.

図 21. FMC Serdes Signals Routing



3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This reference design uses the following hardware and software:

- TIDA-010132 (RF sampling analog front end)
- TSW14J57EVM (JESD204B high-speed data capture and pattern generator card)
- HSDC TIDA GUI (used to program TIDA-010132 board)
- High-speed data converter pro (TSW14J57EVM GUI)

3.1.1 Hardware

図 22 and 図 23 show various portions of the TIDA-010132 hardware.

図 22. Hardware Setup, Top View

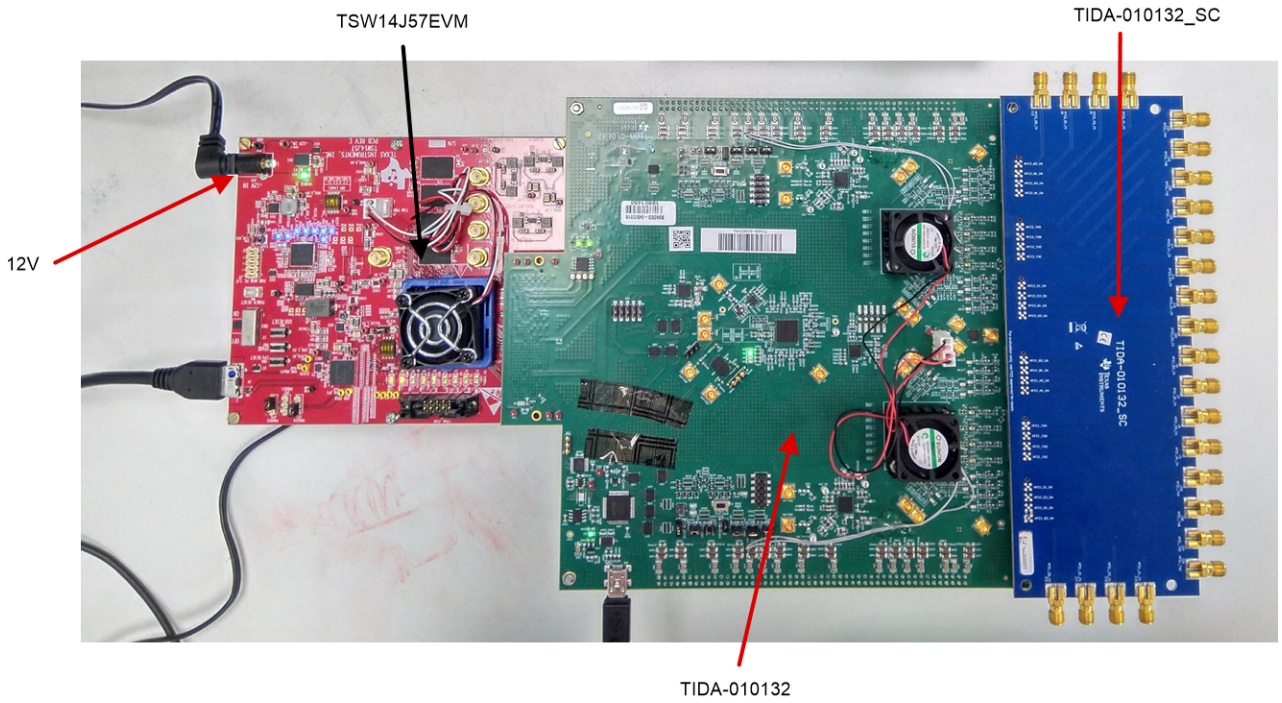
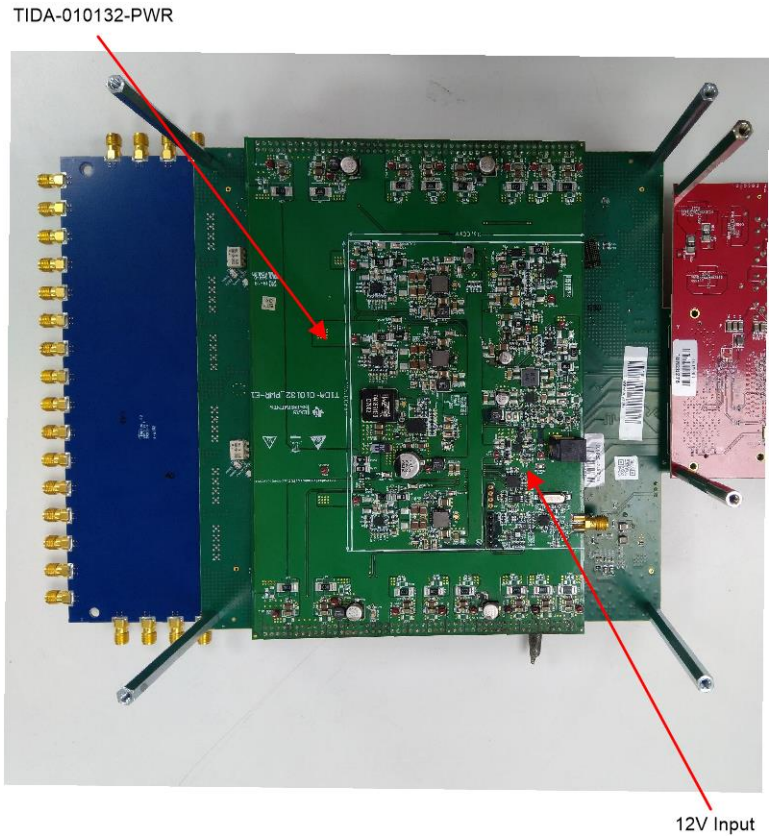


図 23. Hardware Setup, Bottom View



Use following steps to set up the hardware:

1. Install TIDA-010132-PWR-CONN or TIDA-010132-PWR board. TIDA-010132-PWR-CONN is used to connect to external lab power supplies. TIDA-010132-PWR board is a 12-V input power supply board that generates all power rails required for the TIDA-010132 hardware.
2. Install TIDA-010132-SC board.
3. Connect the FMC+ connectors of the TSW14J56 EVM and TIDA-010132 hardware. Ensure that the TIDA-010132 and TSW14J57 are not powered and are not connected to the USB port of the PC.
4. Connect the lab power supplies (1.0 V / 20 A, 1.2 V / 3 A, 1.8 V / 3 A, -1.8 V / 1 A, 3.3 V / 3 A, 5 V / 1 A) to the TIDA-010132-PWR-CONN board or use the TIDA-010132-PWR board. The TIDA-010132-PWR board requires a 12-V / 5-A adapter.
5. Connect the 12-V / 3-A power supply to the TSW14J57 EVM.
6. Connect the TIDA-010132 and TSW14J57EVM to the USB port of the PC.
7. Ensure that the RXTDD1/2 jumpers (J60 and J70) and the TXTDD1/2 jumpers (J67 and J77) are installed for RX and TX operations respectively.
8. Follow the programming steps mentioned in 3.1.2.4 to configure the hardware.

注: Ensure that the AFE7444 fan is running before programming the hardware.

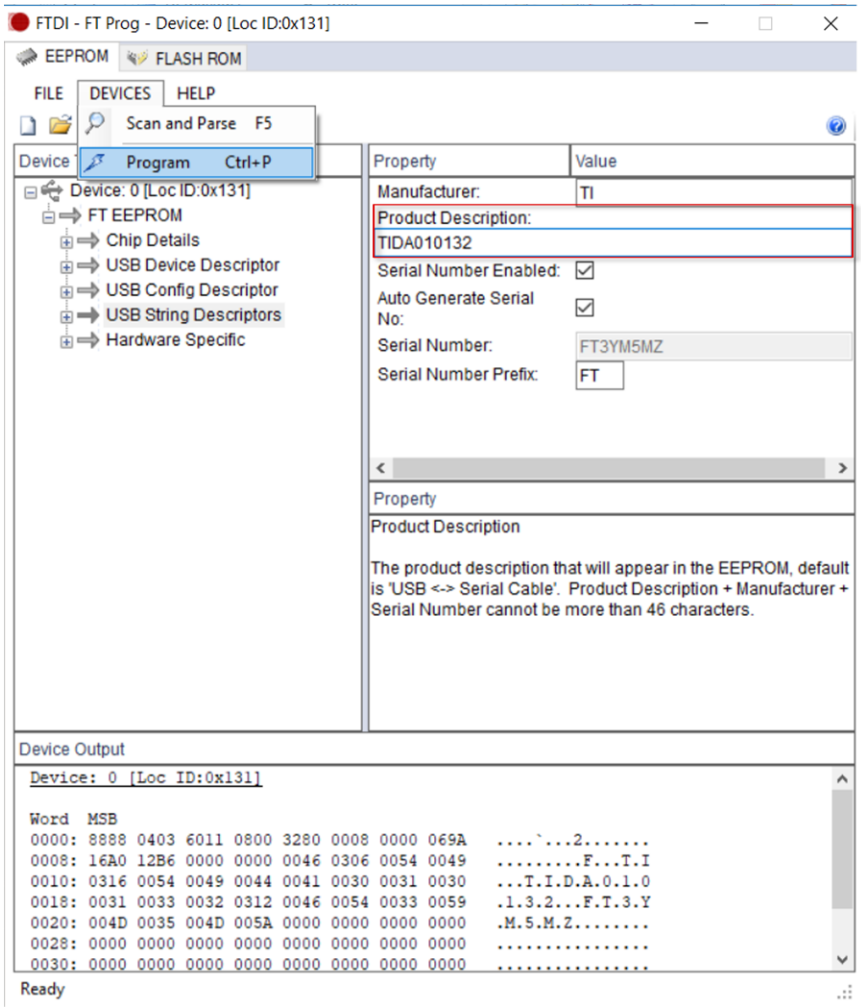
3.1.2 Software

This section describes installation of the HSDC TIDA GUI and high-speed data converter pro software and how to use them to program the hardware.

3.1.2.1 Configuring FTDI

Every new hardware's FTDI chip needs to program once to support the HSDC TIDA GUI. An FTDI utility FT-prog is installed from the web. Product description is set to the TIDA-010132 as shown in 図 24.

図 24. FTDI Setup



3.1.2.2 HSDC TIDA GUI

The HSDC TIDA GUI software interfaces with the TIDA-010132 hardware to configure the AFE7444, LMX2594, LMK04828, and LMK61E2 devices. Install this software from the *Software* section of the TIDA-010132 reference design folder.

3.1.2.3 High Speed Data Converter Pro

The high-speed data converter pro software interfaces with the TSW14J57EVM to support data transfer to the AFE7444EVM through a JESD204B link. Install the software from DATACONVERTERPRO-SW.

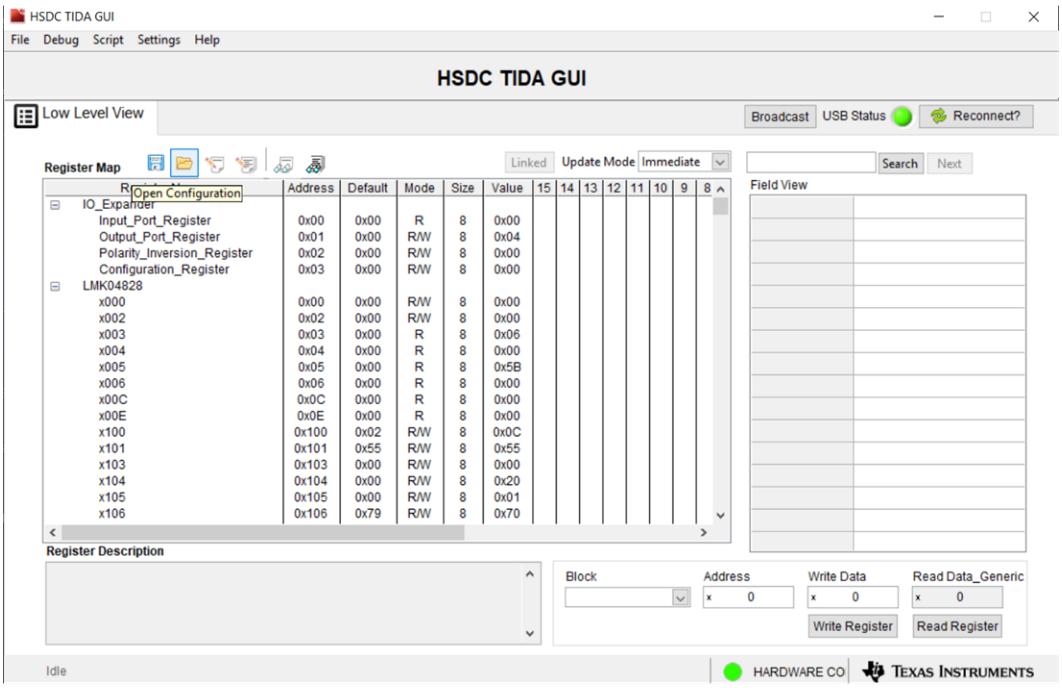
For more information, see the AFE74xxEVM user guide and the High Speed Data Converter ProGUI User's Guide.

3.1.2.4 Programming Steps

This section describes the steps for configuring the TIDA-010132 hardware in 8T8R. The AFE7444 RX and TX are configured in mode 9 and mode 4 respectively. All configuration files are loaded using HSDC TIDA GUI. If the AFE7444 is required to configure in other modes, the TIDA-010132 hardware can be programmed in a similar way with different configuration files. These files are generated using TICS pro and AFE7444 EVM GUI. See the TICS pro and EVM user guide for more details.

1. Load the *TIDA-010132_ LMK61E2_61.44MREF.cfg* and *TIDA-010132_LMK61E2_EEPROM_Write.cfg* files to program EEPROM of the LMK61E2 programmable oscillator at 61.44-MHz reference frequency. 図 25 shows how to load the configuration file to the TIDA-010132 hardware.

図 25. Loading the .cfg File Using HSDC TIDA GUI

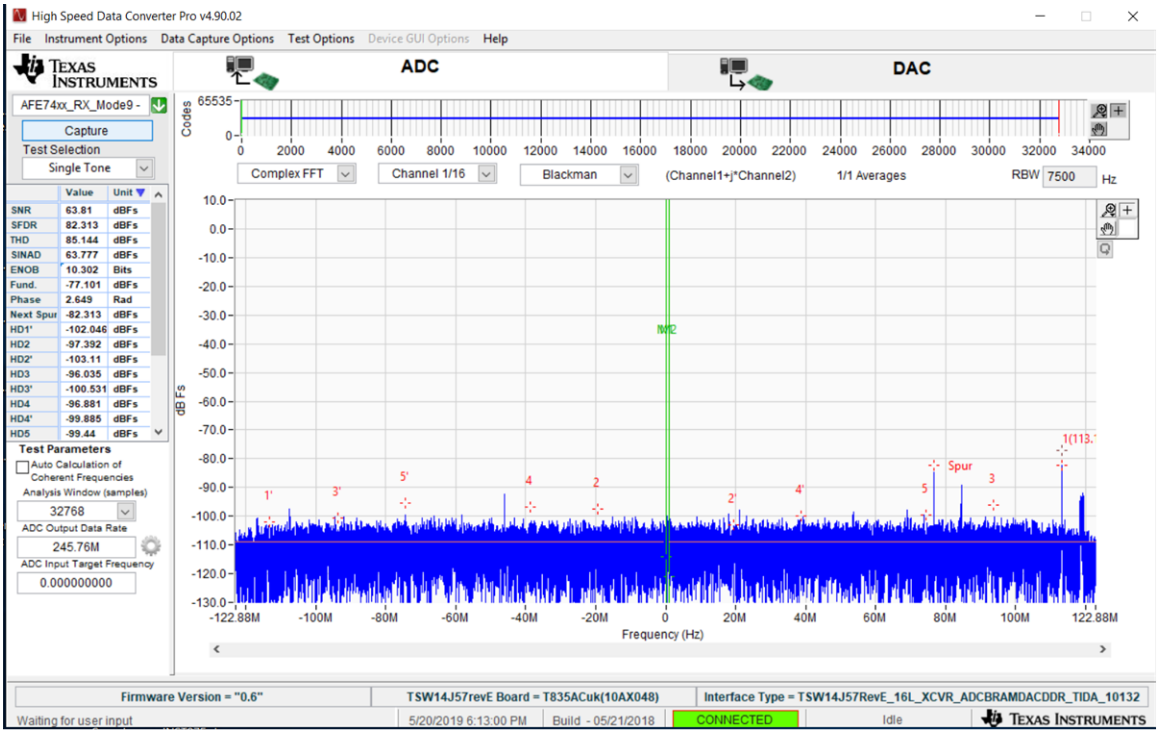


2. Load the *TIDA-010132_LMK04828_61.44MREF_245.76MFCLK_15.36MSYSREF.cfg* file to program onboard LMK04828 to generate SYSREF and FPGA clocks.
3. Load the *TIDA-010132_LMX2594_A_B_5898.24MCLK_61.44MREF_SYNC.cfg* file to generate synchronized device clocks at 5898.24 MHz from LMX2594.
4. Once the clocks are programmed, data to the AFE7444 from that FPGA is sent. 図 26 shows the high-speed data converter pro GUI. If only the receiver needs to be programmed, skip this step.
   a. Open the high-speed data converter GUI and connect to the TSW14757 card.
   b. Switch to the DAC window and select *TIDA010132_AFE74xx_ TX_Mode4 _A_B* to interface with the AFE7444EVM for Mode4 as described in 図 26.
   c. Set the data rate for Mode4 and interpolation 12, for example, 491.52 Msps.
   d. Set I/Q frequency based on the desired output frequency. TX output frequency is (I/Q + NCO).
   e. Click *Send* to start data transmission.

図 26. High Speed Data Converter Pro DAC Settings

5. Load the *TIDA-010132_AFE7444_RX_Mode9_TX_Mode4_A_B.cfg* file to configure the AFE7444 devices. Once the AFE7444 devices are programmed, D2 LED in the TSW14J57 card will begin blinking. If only the transmitter needs to be configured, skip step 6.
6. After the AFE7444 configuration, switch to a high-speed data converter ADC window and complete the following steps:
   a. Select *TIDA010132_AFE74xx_ RX_Mode9 _A_B* to interface with the AFE7444EVM for Mode9 as described in 図 27.
   b. Set the ADC sampling frequency, decimation, ADC input target frequency, and NCO frequency to get the ADC output data rate.
   c. Click *Capture*. This configures the FPGA RX JESD lanes. At this point, the RX LED (D4) on the TSW14J57EVM will begin blinking. If only the receiver needs to enabled, ignore subsequent steps and move on to step 7.
   d. The AFE7444 JESD must reset to enable the AFE TX output. Switch back to the DAC window and use the *TIDA010132_AFE74xx_ RX_Mode4 _A_B_xcvr.ini"* file to send data again. Use the HSDC TIDA GUI to load the *AFE7444_JESD_Reset.cfg* file. Another TX LED (D2) will begin blinking on the TSW14J57 card.
   e. Use *TIDA010132_AFE74xx_ RX_Mode9 _A_B_xcvr.ini* and *TIDA010132_AFE74xx_RX_Mode9_TX_Mode4_A_B_xcvr.ini* for all subsequent captures/sends to avoid accidentally disturbing the RX or TX FPGA links.

図 27. High-Speed Data Converter Pro ADC Settings



7. At this point, all RX and TX channels are working. However, RX and TX NCO are not synchronized. Therefore, load the *TIDA-010132_NCO_SYNC_A_B.cfg* file using the HSDC TIDA GUI. This file turns off the Sysref to the AFE7444 devices and synchronizes both RX and TX NCO. If required, Sysref to the AFE7444 devices can be enabled again by loading the *TIDA-010132_Enable_SYSREF_to_AFE7444.cfg* file.

If both RX and TX must be configured in Mode9, replace the *TIDA-010132_AFE7444_RX_Mode9_TX_Mode4_A_B.cfg* file with the *TIDA-010132_AFE7444_RX_Mode9_TX_Mode9_A_B.cfg* file in the previously-mentioned steps.

3.2 Testing and Results

3.2.1 Test Setup

図 28 and 図 29 show the test setup for transmitter and receiver performance measurement. During receiver tests, transmitters are set in standby mode (TXTDD1/2 = 0) and vice-versa for transmitter tests. 表 5 describes the TIDA-010132 hardware operating mode.

表 5. AFE7444 Test Settings

PARAMETERS \ TEST	SYNCHRONIZATION TEST (SKEW MEASUREMENT)	TX PERFORMANCE	RX PERFORMANCE
Transmitter Mode	Mode 4	Mode 4	-
LMFS	44210	44210	-
Interpolation	12	12	-
DAC Sampling Frequency (MHz)	5898.24	5898.24	-
Interpolated DAC clock rate (MHz)	491.52	491.52	-
Lane rate (Mbps)	9830.4	9830.4	-
Receiver Mode	Mode 9	-	Mode 9
LMFS	24410	-	24410
Decimation	12	-	16
DSA	0 dB	-	0 dB
ADC Sampling Frequency (MHz)	2949.12	-	2949.12
Decimated output rate (MHz)	245.76	-	184.32
Lane rate (Mbps)	9830.4	-	7372.8
SYSREF Frequency (MHz)	15.36	15.36	11.52
FPGA Clock (MHz)	245.76	245.76	184.32
Configuration file	TIDA-010132_AFE7444_RX_Mode9_TX_Mode4_A_B.cfg	TIDA-010132_AFE7444_RX_Mode9_TX_Mode4_A_B.cfg	TIDA-010132_AFE7444_RX_Mode9_TX_Mode9_A_B.cfg

図 28. Test Setup for SNR Measurement of the Receiver

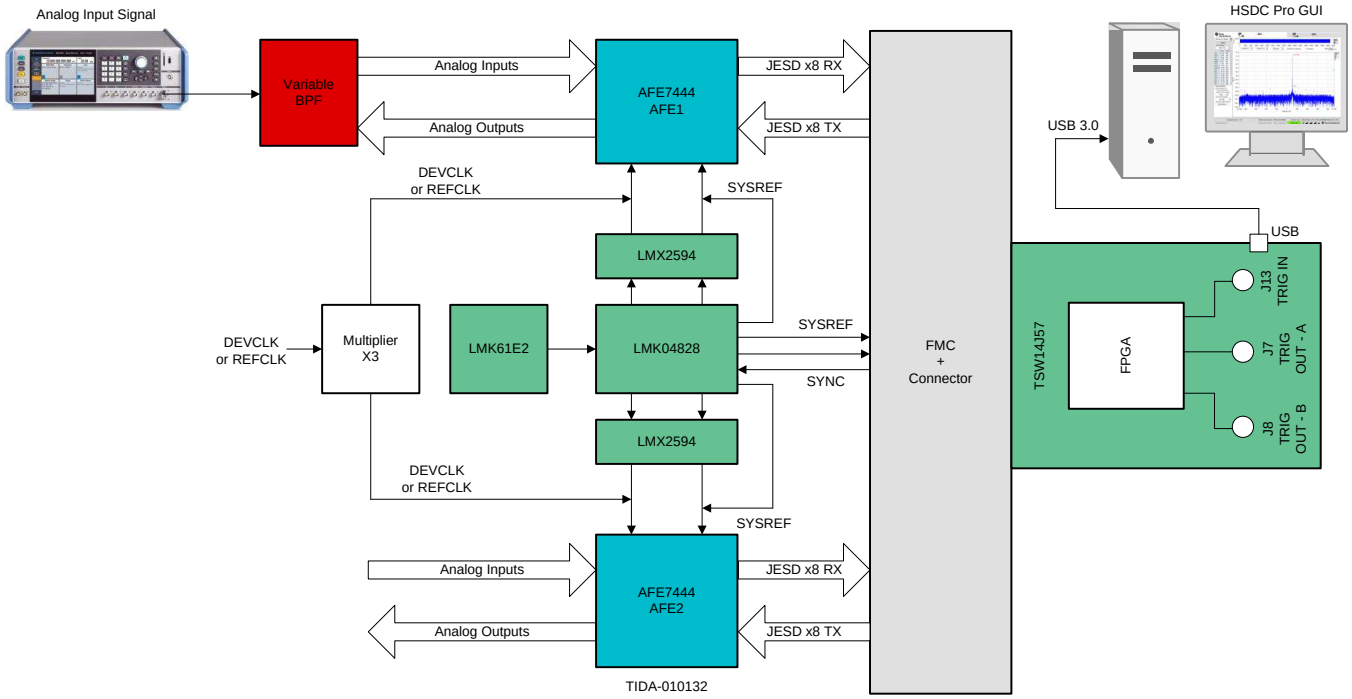
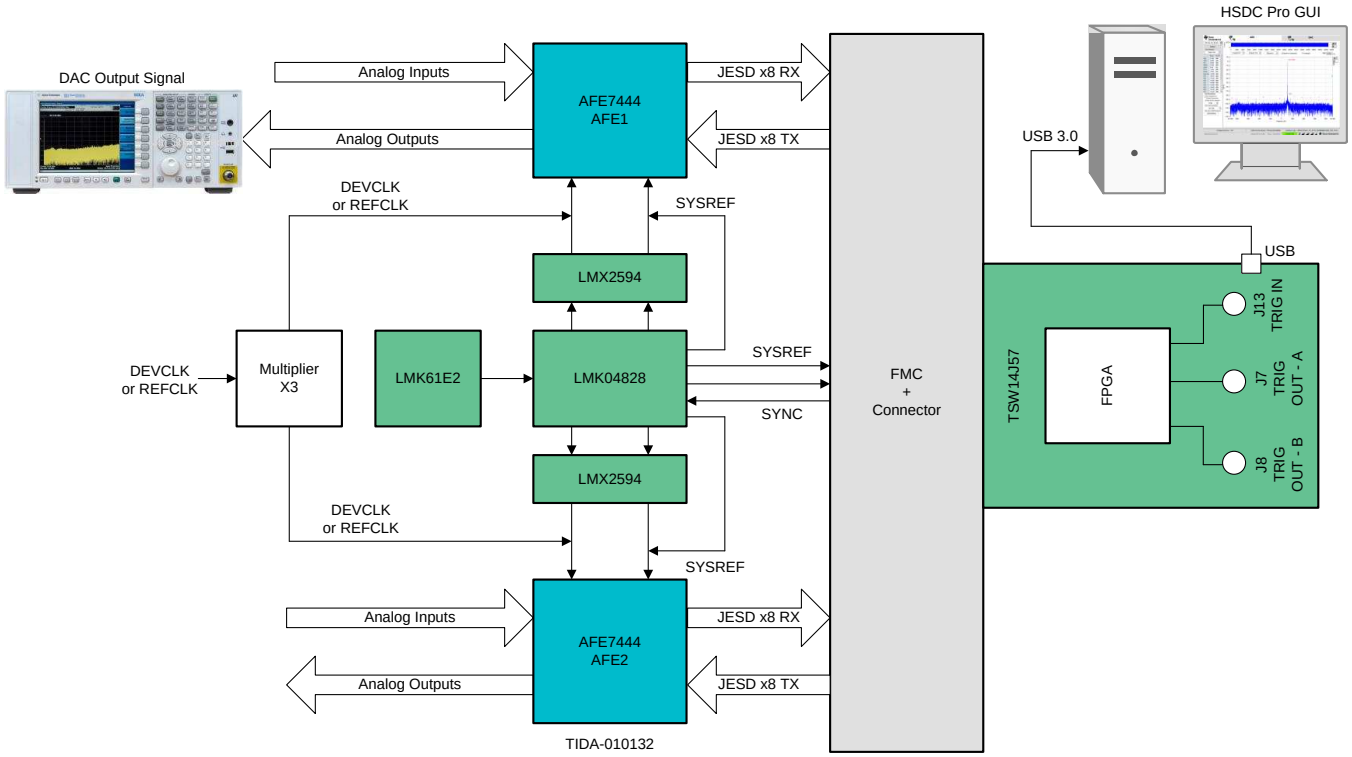


図 29. Test Setup for SFDR and IMD3 Measurement of the Transmitter



3.2.2 Test Results

In this section, the TIDA-010132 hardware performance is analyzed and compared with data sheet specifications.

注: The results in this section are measured with lab power supplies.

3.2.2.1 Clock Phase Noise

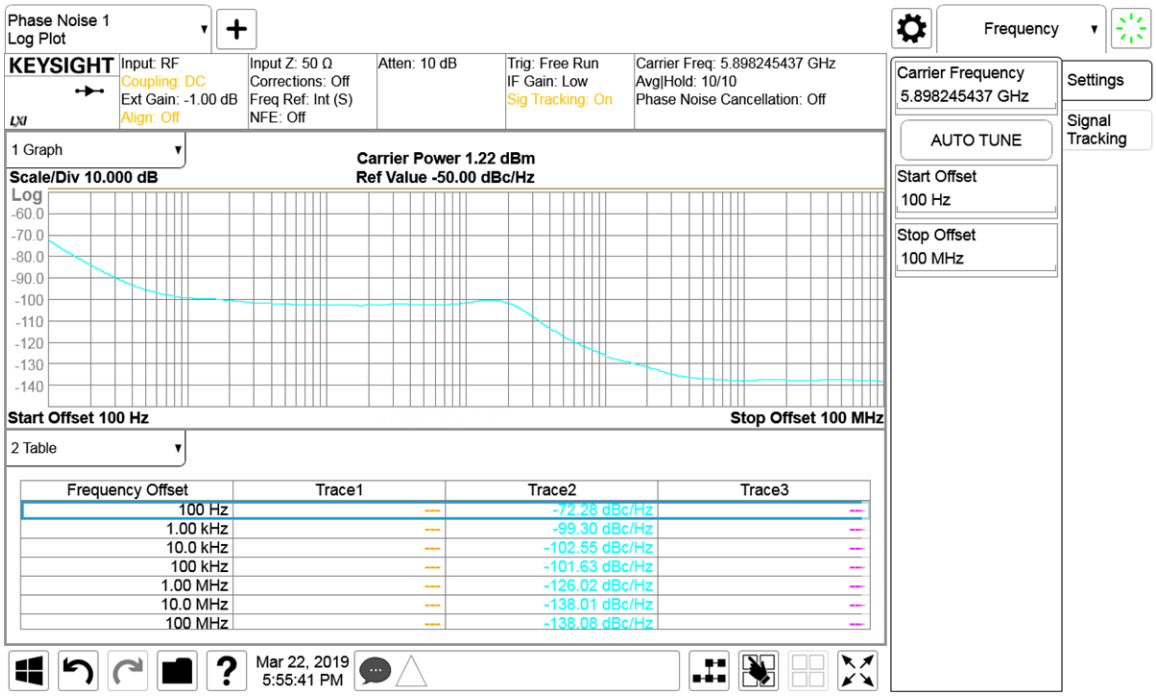
図 30 shows phase noise of the TIDA-010132 board at 6 GHz. The PLL reference frequency is 61.44 MHz. Total approximate clock jitter is calculated using an online jitter calculator tool. Clock jitter is equal to 130 fs for 10 KHz to 20-MHz bandwidth. Total ADC output jitter is calculated using 式 9. SNR degradation due to jitter is calculated using 式 7. It is found that using the TIDA-010132 clocks with 130 fs jitter instead of an external low noise signal generator of 40 fs jitter provides SNR degradation of 2 dB. The 2-dB difference can be seen in the following section where SNR of the TIDA-010132 hardware is compared with data sheet specifications.

$$ADC\ \ output\ \ jitter = \sqrt{t_{clock\_jitter}^{2} + t_{aperature\_jitter}^{2}} \tag{9}$$

Aperture jitter of the AFE7444 is 140 fs.

$$SNR_{degradation\ due\ to\ clock} = 20 * log\left(\frac{\sqrt{\left((130)^2 + (140)^2\right)}}{\sqrt{\left((40)^2 + (140)^2\right)}}\right) dB \approx 2dB \tag{10}$$

図 30. Clock Phase Noise Plot



3.2.2.2 RX Performance

表 6 shows the SNR of the receiver of the TIDA-010132 hardware for Mode 9 and decimation 16. SNR of the receiver of the TIDA-010132 hardware is better than the AFE7444 EVM tested with internal PLL clocks and is close to the data sheet specifications. The 2-dB difference between the data sheet specifications and the measured results is explained in 3.2.2.1. 図 31 and 図 32 show spectrum results of the ADC at 1900-MHz and 2600-MHz input frequencies respectively.

表 6. SNR of the Receiver at Different Frequencies

INPUT FREQUENCY	CONDITIONS	UNIT	AFE7444 (DATA SHEET SPECIFICATION)	AFE7444EVM (INTERNAL PLL)	TIDA-010132 MEASURED
1900 MHz	DSA - 0dB, -3dBFS input signal, 16384 point FFT, x16 decimation	dBFs	63.3	60.5	61.6
2600 MHz		dBFs	61.2	58.8	60

図 31. ADC Spectrum at 1900-MHz Input Signal

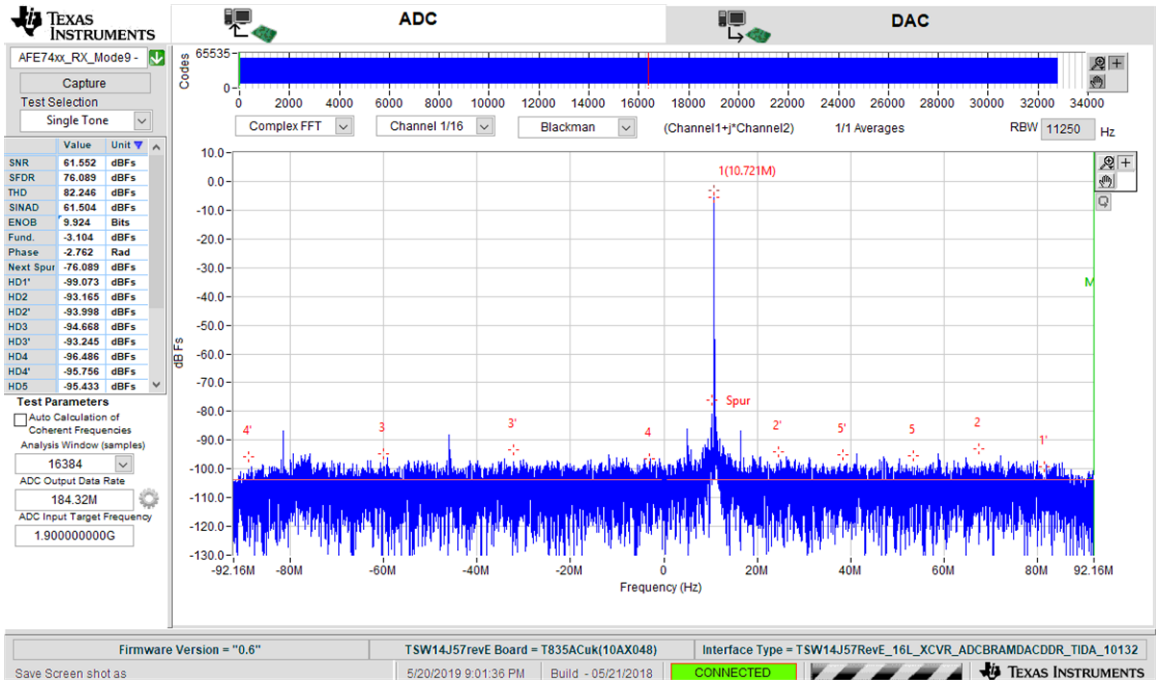
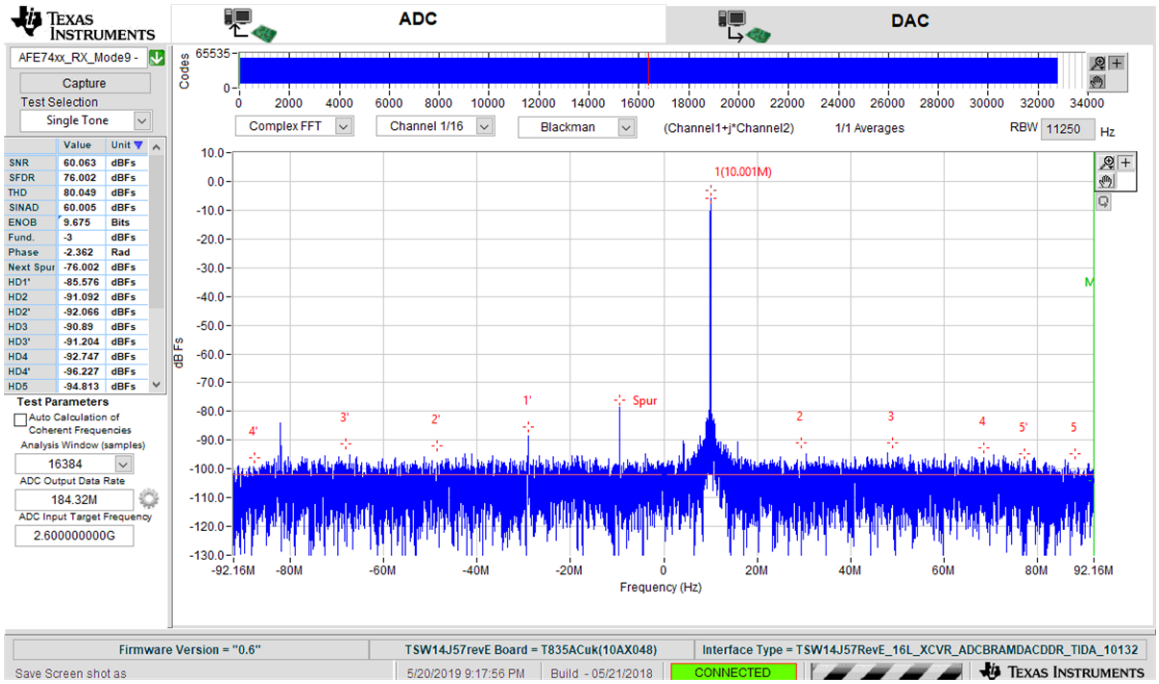


図 32. ADC Spectrum at 2600-MHz Input Signal



3.2.2.3 TX Performance

表 7 shows the measured transmitter performance results in terms of SFDR and IMD3 for mode 4 and x12 interpolation. Measured SFDR and IMD3 of the transmit channels is comparable with the internal PLL as a clock source. It is observed that there is a dip in the SFDR (0 - FDAC/2) performance near 1800 MHz. SFDR is limited by HD2 due to non-linearity of balun. It can be improved by adding compensations to minimize balun phase imbalance or selecting different baluns.

表 7. SFDR and IMD3 of the Transmitter at Different Frequencies

PARAMETERS	CONDITIONS	UNIT	AFE7444 (DATA SHEET SPECIFICATION)	AFE7444EVM MEASURED (INT PLL)	TIDA-010132 MEASURED
SFDR	SFDR for 0-FDAC/2 BW, DSA - 0dB, -1dBFS				
890 MHz		dBc	60	63	68
1800 MHz		dBc	55	58	55
2100 MHz		dBc	56	59	56
2600 MHz		dBc	58	67	62
SFDR	SFDR for Fout +/- 250MHz BW, DSA - 0dB, -1dBFS				
890 MHz		dBc	84	83	79
1800 MHz		dBc	74	83	80
2100 MHz		dBc	75	74	70
2600 MHz		dBc	74	74	76
IMD3	IMD3 for ±10MHz tone offset, DSA - 0dB, -1dBFS each tone				
890 MHz		dBc	69	77	73
1800 MHz		dBc	69	75	72
2100 MHz		dBc	68	69	70
2600 MHz		dBc	68	70	72

図 33. DAC Spectrum at 2100-MHz Output (0 to $F_{s/2}$)

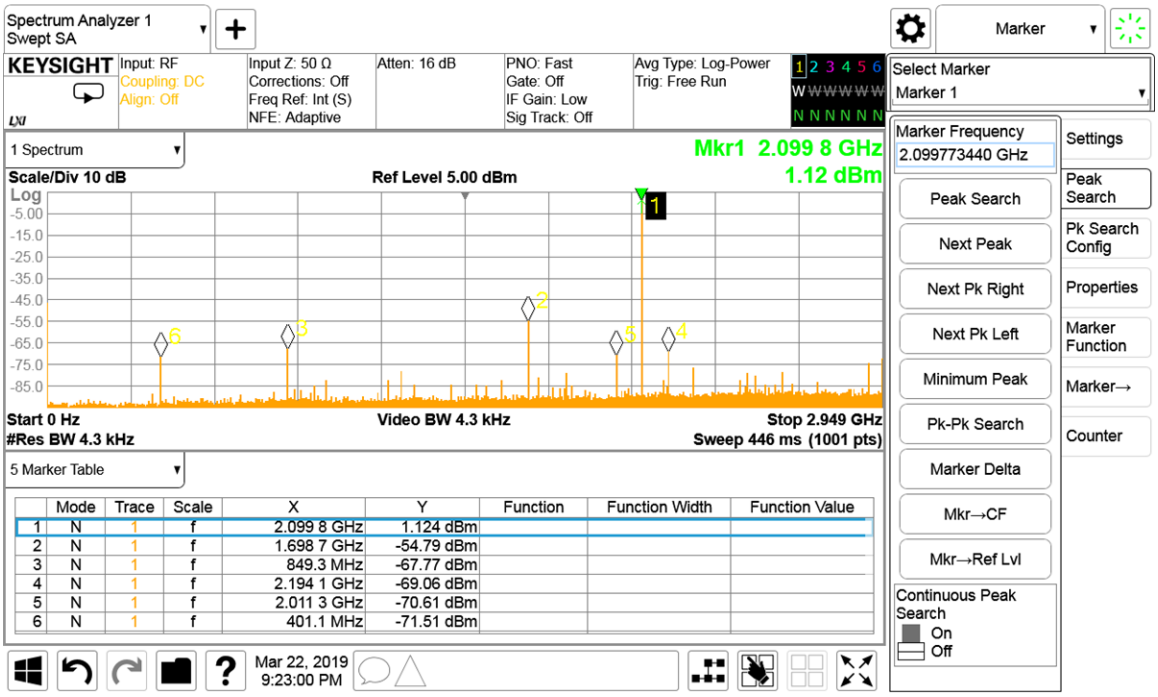
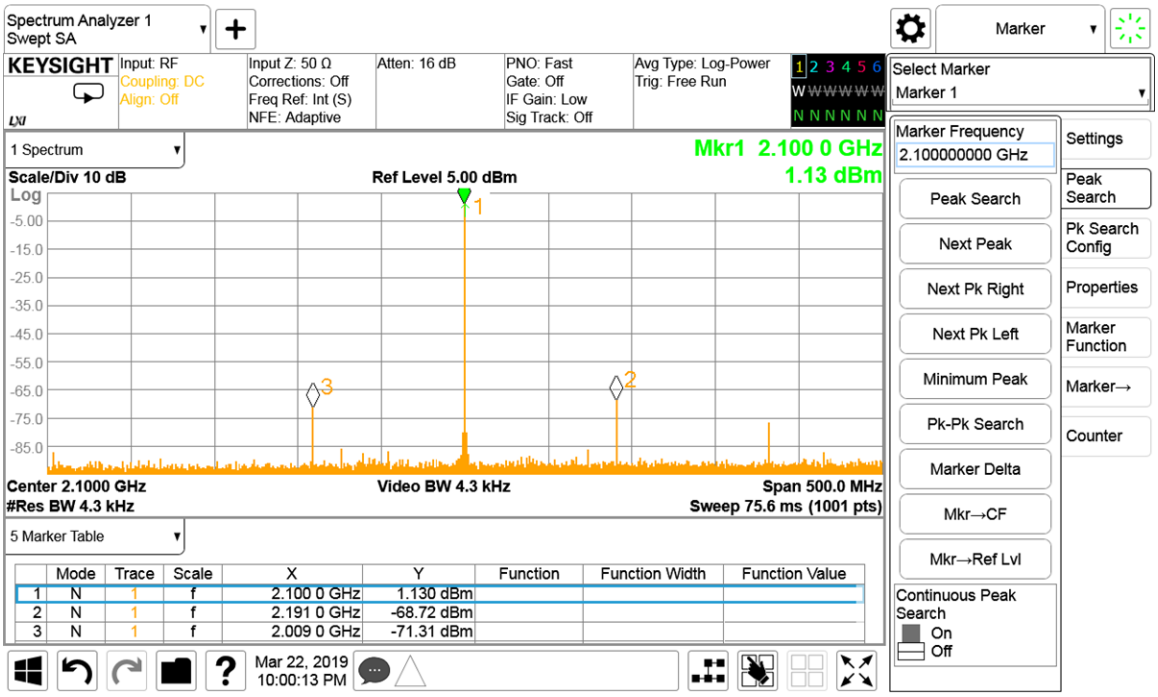


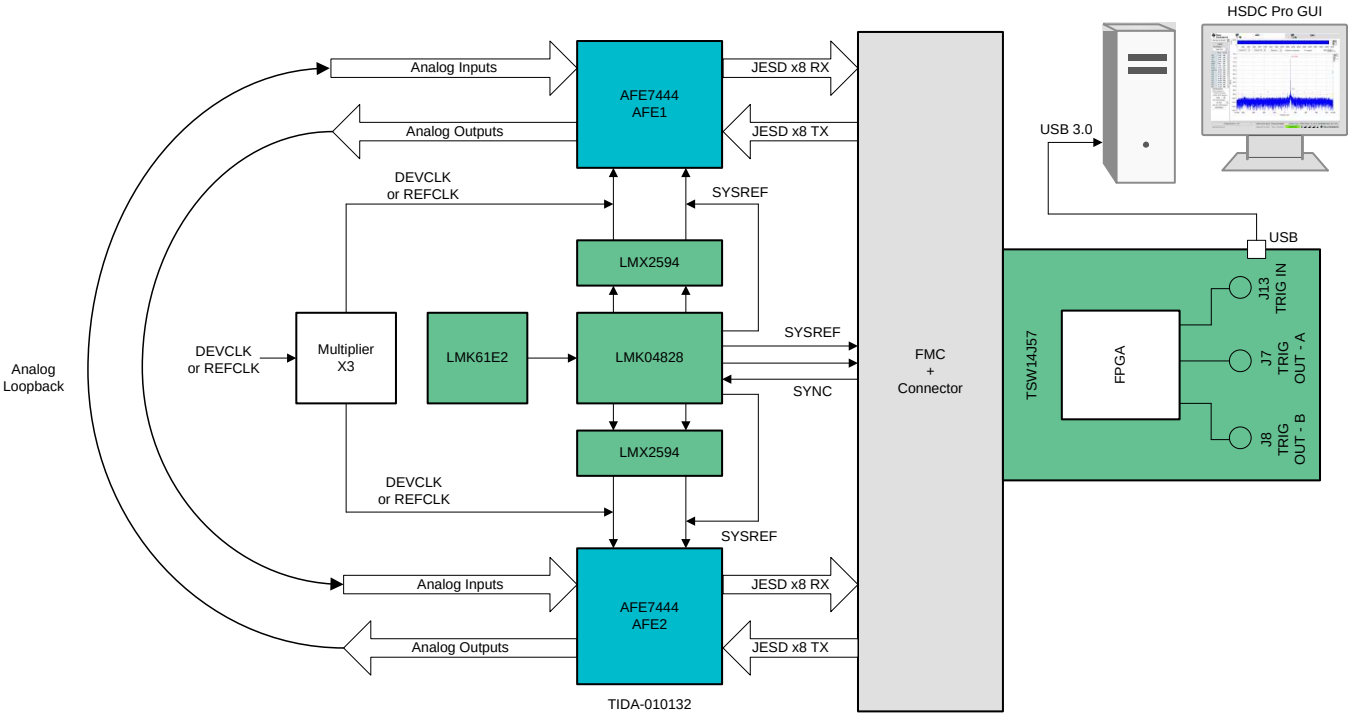
図 34. DAC Spectrum at 2100-MHz Output (± 250 MHz)



3.2.2.4 *Skew Measurement, Analog Loopback*

図 35 shows the hardware setup for analog loopback. Skew between two receive channels is calculated using FFT by taking phase difference of the fundamental frequency. It is found that variation of measured skew is less than 10 ps for multiple power cycles. This explains why the RX / TX JESD and DSP (NCO and Mixer) blocks are synchronized within 10 ps.

図 35. Analog Loopback Setup



3.2.3 Summary

The reference design achieves RX and TX performance close to the AFE7444 data sheet specifications with on-board clocks using the LMX2594 and LMK04828 devices. It also attains skew variation of less than 10 ps between multiple receive and transmit channels of the AFE7444 devices for multiple power cycles. This is crucial for radar and EW applications that require multi-device synchronization and high signal chain performance.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010132.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010132.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010132.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010132.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010132.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010132.

5 Software

To download the software, see the software section at TIDA-010132.

6 Related Documentation

1. M. C. Budge, Jr (2011), The University of Alabama Huntsville, RADAR range equation
2. University of Cincinnati, INTRODUCTION TO RADAR PROCESSING
3. Texas Instruments, Concept and Performance of Internal Instrument Calibration for Multi-Channel SAR
4. Texas Instruments, Multichannel RF transceiver clocking reference design for RADARs and wireless 5G testers
5. Texas Instruments, Multichannel JESD204B 15-GHz Clocking Reference Design for DSO, Radar, and 5G Wireless Testers

6.1 商標

6.2 デベロッパー・ネットワークの製品に関する免責事項

7 About the Author

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