参考資料

デザイン・ガイド: TIDA-050028
ソリッド・ステート・ドライブ（SSD）モジュール向け、eFuse 搭載、VBus 保護機能のリファレンス・デザイン

概要

このリファレンス・デザインは、ソリッド・ステート・ドライブ (SSD) モジュールのフロントエンド保護を提供し、標準の 3.3V、1.8V、1.5V レール用の完全な機能を持つ電力ツリーを示しています。このデザインはサイズが最適化されており、適切な IC 保護デバイス、負荷スイッチ、DC/DC コンバータを選択するために役立ちます。

リソース

TIDA-050028	デザイン・フォルダ
TPS2595	プロダクト・フォルダ
TPS22975	プロダクト・フォルダ
TPS22976	プロダクト・フォルダ
TPS62821	プロダクト・フォルダ
TPS62822	プロダクト・フォルダ
TPS61372	プロダクト・フォルダ
TLV743P	プロダクト・フォルダ

TI E2E™ Community

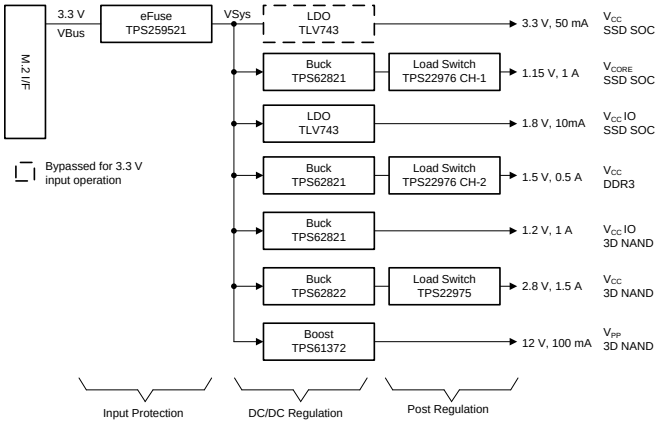
E2E™エキスパートに質問

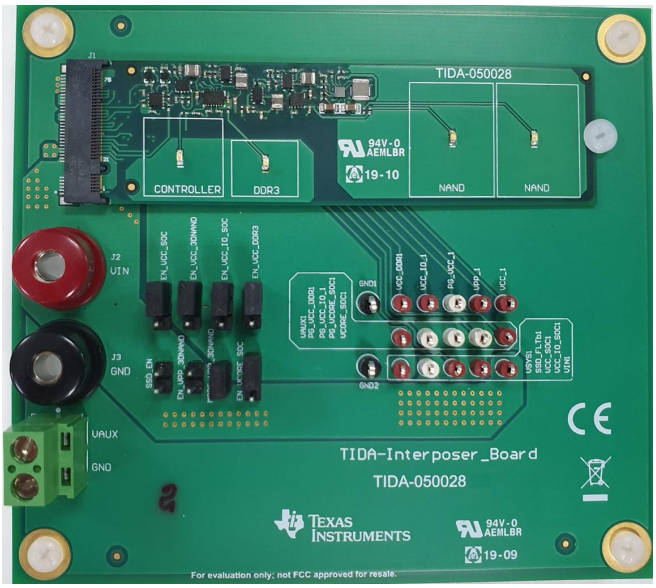
特長

- システム保護
  - 応答時間 5µs (標準値) の高速な過電圧保護クランプ
  - 突入電流に対する保護および過負荷電流制限 (±7.5%) 機能により堅牢な VBus を実現
- スイッチングされるすべての電力レールについてスルーレート制御を行い、突入電流を制限
- 迅速な出力放電 (QOD) により、入力電力が消失した場合でも、すべてのレールを安全に放電
- サイズが最適化された電力ソリューション

アプリケーション

- ソリッド・ステート・ドライブ (SSD)
- ソリッド・ステート・ドライブ (SSD) - エンタープライズ





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1 System Description

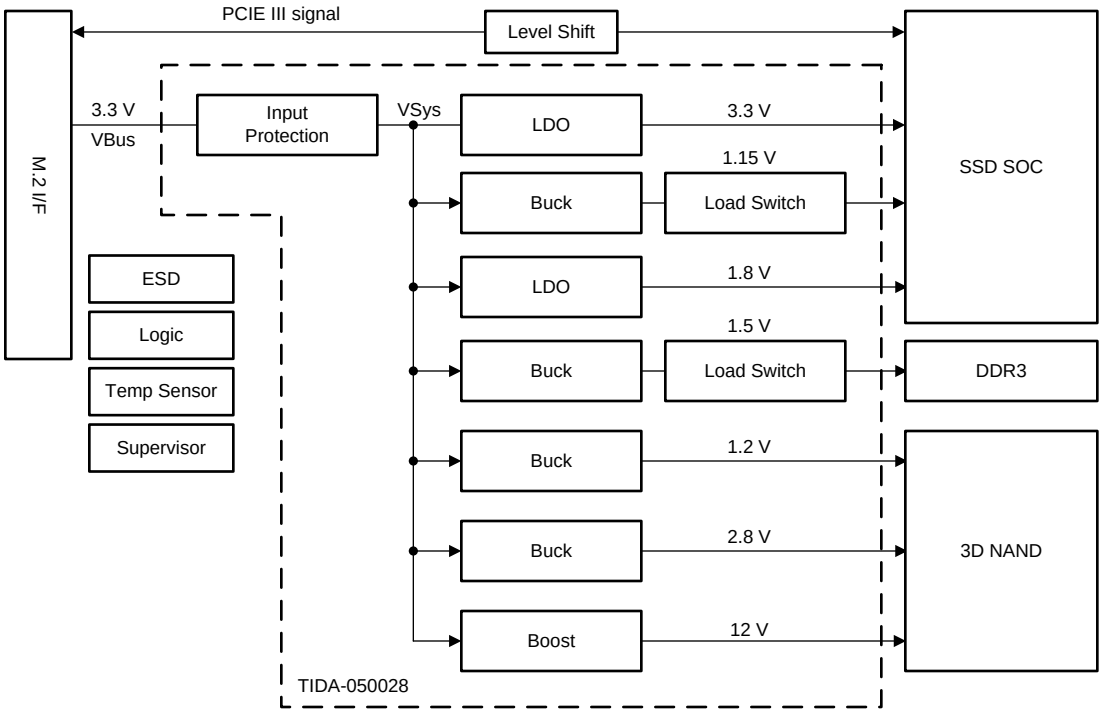
Solid-state drive (SSD) is a solid-state storage device that uses integrated circuit assemblies as memory to store data persistently. 図 1 shows a typical block diagram of SSD, which consists of memory, controller, temperature supervisor, voltage supervisor, and logic buffer circuits. Most of the SSD manufacturers use non-volatile NAND flash memory because of the lower cost, higher capacity integration, and data persistence without a power supply. SSDs are available in various form factors such as mSATA, M.2, U.2 of which M.2 (also known as the Next Generation Form Factor (NGFF)) is popular in general and space constrained applications such as ultra-books or tablet computers.

Solid state drive designs require the following:

- Input power protection on VBus from overvoltage, overload, and inrush-currents.
- Compact and efficient power solutions to achieve large storage capacity per area.
- Controllability and inrush current limit on the power rails.

This reference design TIDA-050028 focuses on the previous requirements. This reference design includes an eFuse, synchronous step-down DC/DC converters, synchronous boost converter, and load switches.

図 1. Typical Block Diagram of SSD (Reference Design Highlighted)



1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
System Input, VBus	VIN Input voltage range		2.5		3.5	V
	Input current	VIN = 3.3 V		3	3.7	A
System Bus, VSys	Output clamp voltage	VIN > 4.1 V	3.4	3.6	3.8	V
TLV743 (3.3 V Output)	Output current	VIN = 3.3 V			50	mA

表 **1. Key System Specifications (continued)**

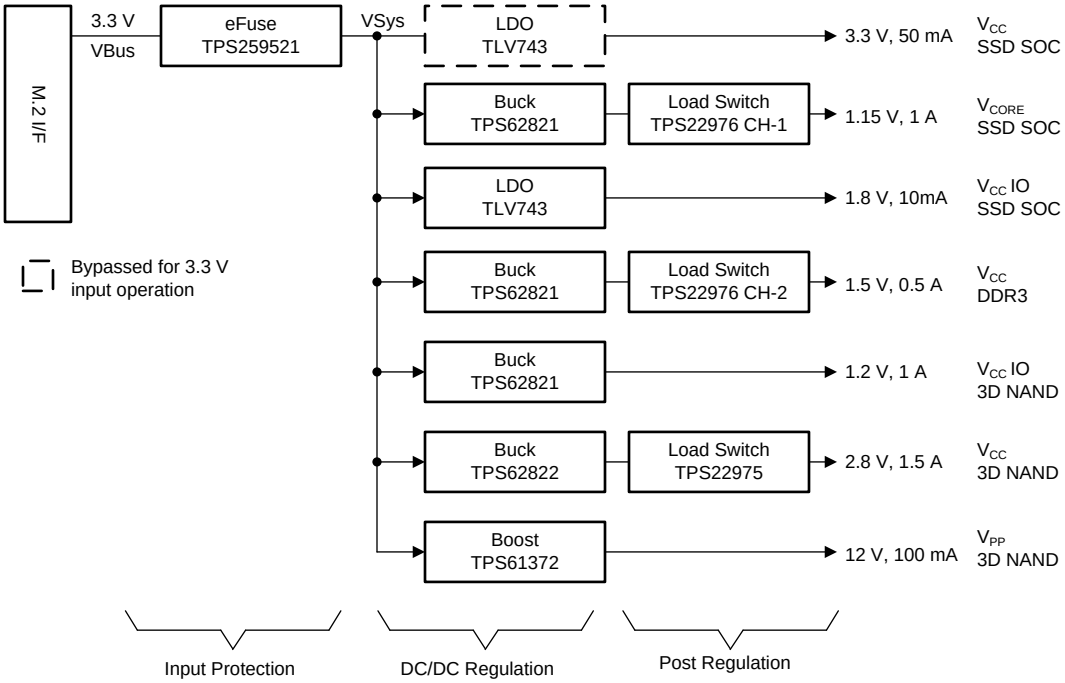
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
TPS62821 (1.15 V Output)	Output current	VIN = 3.3 V		0.8	1	A
TLV743 (1.8 V Output)	Output current	VIN = 3.3 V			10	mA
TPS62822 (2.8 V Output)	Output current	VIN = 3.3 V		1.2	1.5	A
TPS62821 (1.5 V Output)	Output current	VIN = 3.3 V		0.4	0.5	A
TPS62821 (1.2 V Output)	Output current	VIN = 3.3 V		0.8	1	A
TPS61372 (12 V Output)	Output current	VIN = 3.3 V		80	100	mA
Operating Temperature			-40		85	°C
Form Factor			22 × 80			mm

2 System Overview

2.1 Block Diagram

TIDA-050028 implements the design of a typical power tree in a SSD. 図 2 illustrates the block diagram of TIDA-050028 along with the selected power components. TPS259521 provides input protection for SSD from overvoltage, overload, and inrush-currents. TPS22975 and theTPS22976 are used to switch supply rails NAND flash, SSD controller, and DDR sections respectively. TPS62821 is used to step down the system voltage VSys to 1.15 V and 1.5 V rails where as TPS62822 is used to step down VSys to 2.8 V to power NAND flash. Synchronous boost converter, TPS61372, is used to step up VSys to 12 V for Vpp rail.

図 2. TIDA-050028 Block Diagram



2.2 Design Considerations

TIDA-050028 design is composed of two boards: an interposer board and a daughter card. The daughter card mimics the physical appearance of an SSD with components placed accordingly in a M.2 module of 2280 size (22-mm wide and 80-mm long). The interposer board provides an interface to the daughter card and implements necessary jumpers to control individual sections on SSD, test points for probing various rail voltages and “power good” signals.

2.3 Highlighted Products

This section highlights the key features for selecting the devices for this reference design. Find the complete details of the highlighted devices in their respective product data sheets.

2.3.1 TPS259521

The TPS2595xx family of eFuses is a highly-integrated circuit protection and power management solution in a small package. The devices use few external components and provide multiple protection modes. They provide robust protection against over voltages, overloads, short circuits, and excessive inrush current. Current limit level can be set with a single external resistor. Overvoltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required.

This reference design uses the TPS259521 to provide input protection for the SSD module.

2.3.2 TPS22975

The TPS22975 device is a single-channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.7 V. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals. The device has a configurable slew rate for applications that require a specific rise-time. The TPS22975 is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch OFF. The switch turns ON again when the junction temperature stabilizes to a safe range. The TPS22975 also offers an optional integrated 230-Ω on-chip load resistor for QOD when the switch is turned OFF. The integrated control logic, driver, power supply, and output discharge FET eliminates the requirement for any external components, which reduces solution size and BOM count.

This reference design uses the TPS22975 to switch the supply of NAND section.

2.3.3 TPS22976

The TPS22976 device is functionally similar to TPS22975 but comes with dual load switch channels integrated in a 14-pin WSON package. Each channel supports a maximum continuous current of 6-A and can be independently controlled by an ON and OFF inputs (ON1 and ON2).

In this reference design, the two channels of TPS22976 are used to switch supply to SSD controller and DDR sections respectively.

2.3.4 TPS6282X

The TPS6282x is an all-purpose and easy to use synchronous step-down DC/DC converter with a very low quiescent current of only 4 µA. It supplies up to 3-A output current (TPS62823) from a 2.4 V to 5.5 V input voltage. Based on the DCSControl™ topology it provides a fast transient response. The internal reference allows to regulate the output voltage down to 0.6 V with a high-feedback voltage accuracy of one percent over the junction temperature range of -40°C to 125°C. The TPS6282x includes an automatically entered power save mode to maintain high efficiency down to very light loads. The device features a Power Good signal and an internal soft start circuit. For fault protection, it incorporates a HICCUP current limit as well as a thermal shutdown. The TPS6282x are packaged in a 2-mm×1.5-mm QFN-8 package.

In this reference design, TPS62821 serves to step down the input 3.3 V to 1.15 V and 1.5 V rails. TPS62822 serves to step down the input 3.3 V to 2.8 V. The TPS6282-series was selected to maintain output voltage accuracy also over the typical load transients observed in SSD applications.

2.3.5 TPS61372

The TPS61372 is a full-integrated synchronous boost converter with the load disconnect built-in feature. The device supports input voltage ranges from 2.5 V to 5.5 V and output voltage up to 16 V with a 3.8-A current limit. The TPS61372 uses the peak current mode with the adaptive off-time control topology and has Auto PFM mode to provide high efficiency at light load. In addition, the device implements output overvoltage and thermal shutdown protection. The TPS61372 is packed in a 1.57-mm×1.52-mm WCSP 16-pin package.

This reference design uses TPS61372 to boost input 3.3 V to 12 V at 100 mA load.

2.3.6 TLV743

The TLV74333 is a low-dropout regulator (LDO) which consumes low quiescent current and delivers excellent line and load transient performance. Combined with low noise, good PSRR, and low-dropout voltage, these characteristics make this device well-suited for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is -40°C to 125°C.

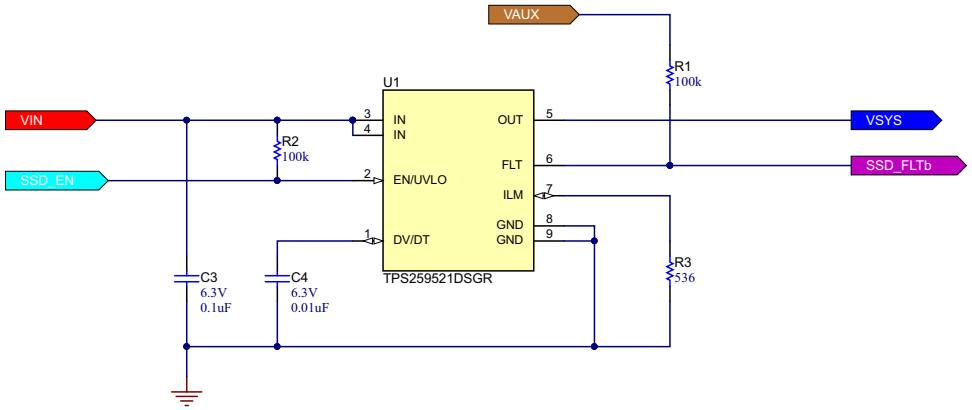
2.4 System Design Theory

This section discusses the considerations behind the design of each subsection in the system. This section also provides necessary calculations for external components for each device and device modes to meet the system requirements of this reference design.

2.4.1 Input Protection Design with TPS259521 eFuse

TPS259521 provides protection against overvoltages, overloads, and excessive inrush currents. Overvoltage events are limited by internal fixed clamping value, which is 3.8 V (max) for TPS259521 device. The current limit is set using external resistor R3 connected on pin-7 (ILM) of TPS259521 and 図 3.

図 3. TPS259521 eFuse Circuit Schematic



$$R_{ILM} = \frac{2000}{I_{ILIMIT} - 0.04} = \frac{2000}{3.77 - 0.04} = 536\text{-}\Omega \quad (1)$$

The inrush current is directly proportional to the load capacitance and the output voltage slew rate (dVdt). The 式 2 can be used to find the slew rate (SR_{ON}) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR_{ON}\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \quad (2)$$

For design example under discussion, target I_{INRUSH} is 300-mA for C_{OUT} of 66-µF; From 式 2, the required output voltage slew rate (dVdt) is 4.54 V/ms.

The required CdVdt capacitance, C4 on DV/DT pin to set 4.54 V/ms slew rate can be calculated using the 式 3.

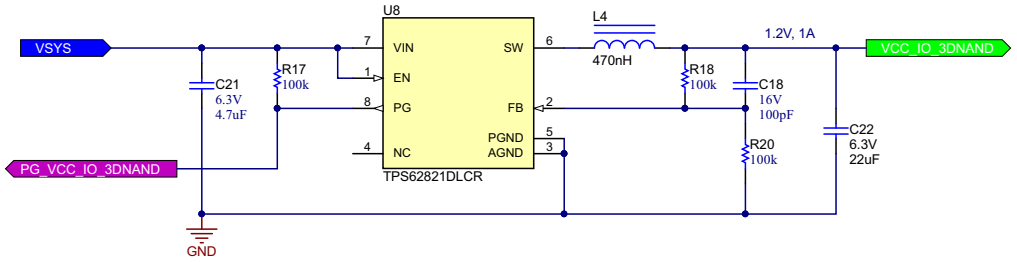
$$C_{dVdt}\,(pF) = \frac{42000}{SR_{ON}\left(\frac{V}{ms}\right)} = \frac{42000}{4.54} \approx 10\text{-}nF \quad (3)$$

2.4.2 Designing Buck Converter Circuit TPS6282x

The TPS6282x is a synchronous buck converter that can accept input voltage from 2.4 V to 5.5 V and generate a constant voltage between these values.

The calculations for input capacitor, output capacitor, and inductor are taken from the TPS6282x synchronous step-down DC-DC converter with DCS-Control™ topology data sheet.

図 4. TPS6282x Buck Converter Circuit Schematic



A resistive divider (from VOUT to FB to AGND) sets the actual output voltage of the TPS6282x. 式 4 and 式 5 calculates the values of the resistors. I_{FB} is recommended to be in the range of 5-µA.

$$R_{20} = \frac{0.6}{I_{FB}} \tag{4}$$

$$R_{18} = \frac{V_{OUT}}{I_{FB}} - R_{20} \tag{5}$$

For output voltage of 1.2 V, 100-kΩ is chosen for R_{18}, R_{20} resistors.

To improve regulation speed, TPS6282x preferably operates with a feed-forward capacitor, connected between VOUT and FB. The appropriate value is calculated using 式 6. 100-pF is chosen for C_{18}.

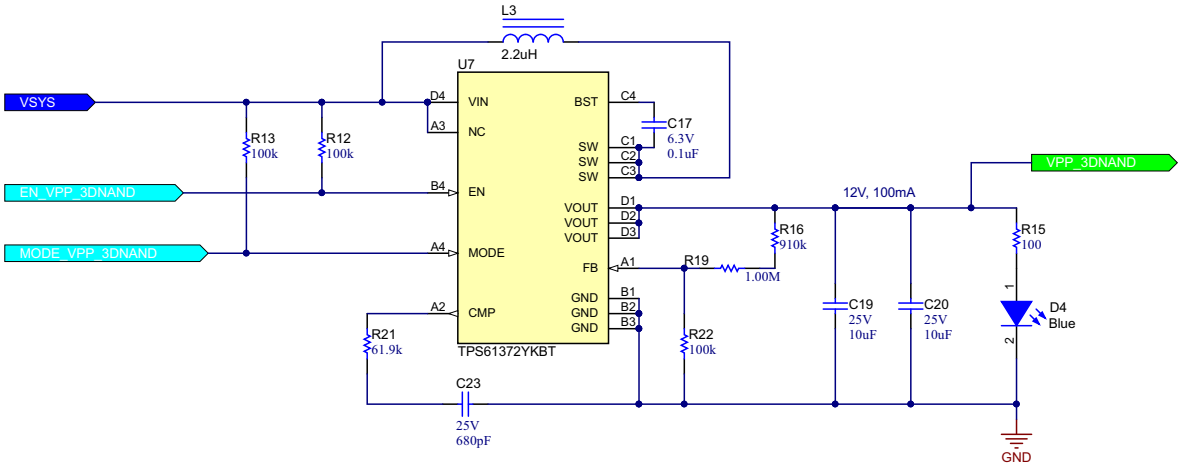
$$C_{18} = \frac{12\ \mu s}{R_{20}} \tag{6}$$

2.4.3 Designing Boost Converter Circuit TPS61372

The TPS61372 is a synchronous boost converter that can accept input voltage from 2.5 V to 5.5 V and supports output voltage up to 16 V.

The calculations for input capacitor, output capacitor, inductor, and loop compensation parameters are taken from the TPS61372 synchronous boost with load disconnect data sheet.

図 5. TPS61372 Boost Converter Circuit Schematic



The output voltage of the TPS61372 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by 式 7.

$$V_{OUT} = 0.594 \times \left(1 + \frac{(R16 + R19)}{R22}\right) \quad (7)$$

For this design, R22 is chosen as 100-kΩ which gives (R16+R19) as 1.91-MΩ to result in an output voltage of 12 V.

2.4.4 Output Voltage Rail Switching with TPS22975, TPS22976

When the load switch is enabled, the output capacitors (47-µF in this example) must be charged up from 0 V to the set value (2.8 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using 式 8.

$$\text{Inrush Current} = C_L \times \frac{dV_{out}}{dt} \quad (8)$$

The appropriate rise time to limit inrush current to 100 mA can be calculated using the 式 8 as shown in 式 9.TPS22975 and TPS22976 offers low ON-resistance which helps to reduce voltage drop on low voltage rails. These devices offer configurable slew rate for applications that require a specific rise-time and inrush current control. The capacitor on the CT pin sets the output voltage slew rate.

$$100\ \text{mA} = 47\ \mu\text{F} \times \frac{2.8\ \text{V}}{dt} \quad (9)$$

The value of rise time (dt) is given by 式 10.

$$dt = 1316\ \mu\text{s} \quad (10)$$

This gives slew rate, SR (in µs/V) of 470 µs/V at 2.8 V. To ensure an inrush current of less than 100 mA, choose a CT value that yields a rise time of more than 1316 µs.

An approximate formula for the relationship between CT and slew rate when VBIAS is set to 5 V is shown in 式 11.

$$SR = 0.43 \times CT + 26 \quad (11)$$

Using 式 11; CT value is chosen as 1000 pF to set slew rate of 470 µs/V.

2.4.5 SSD SoC Supply Rail

The low-dropout regulator TLV74333 is used to supply SSD Soc supply rail from VSys. A voltage drop, varying with the current multiplied by the ON-resistance, occurs on the eFuse. The LDO might stop regulating the SoC supply rail to Vcc = 3.3 V, missing the required headroom. To avoid this, the REG711-33 buck-boost converter can be used as an alternative to the LDO to operate as a voltage stabilizer. It can accept voltages higher than 3.3V if VBus overshoots and also stays in regulation if VSys drops due to the voltage drop on the eFuse and or if VBus is at the lower side of the tolerance window. The REG711-33 is a charge-pump based buck-boost converter, hence inductor-less with small solution size.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Hardware

This reference design uses following hardware to do the measurement:

- 6 V, 5 A output capability DC power supply
- Digital oscilloscope
- One E-Load

図 6 shows the general hardware connection test setup.

図 6. Hardware Connection Setup

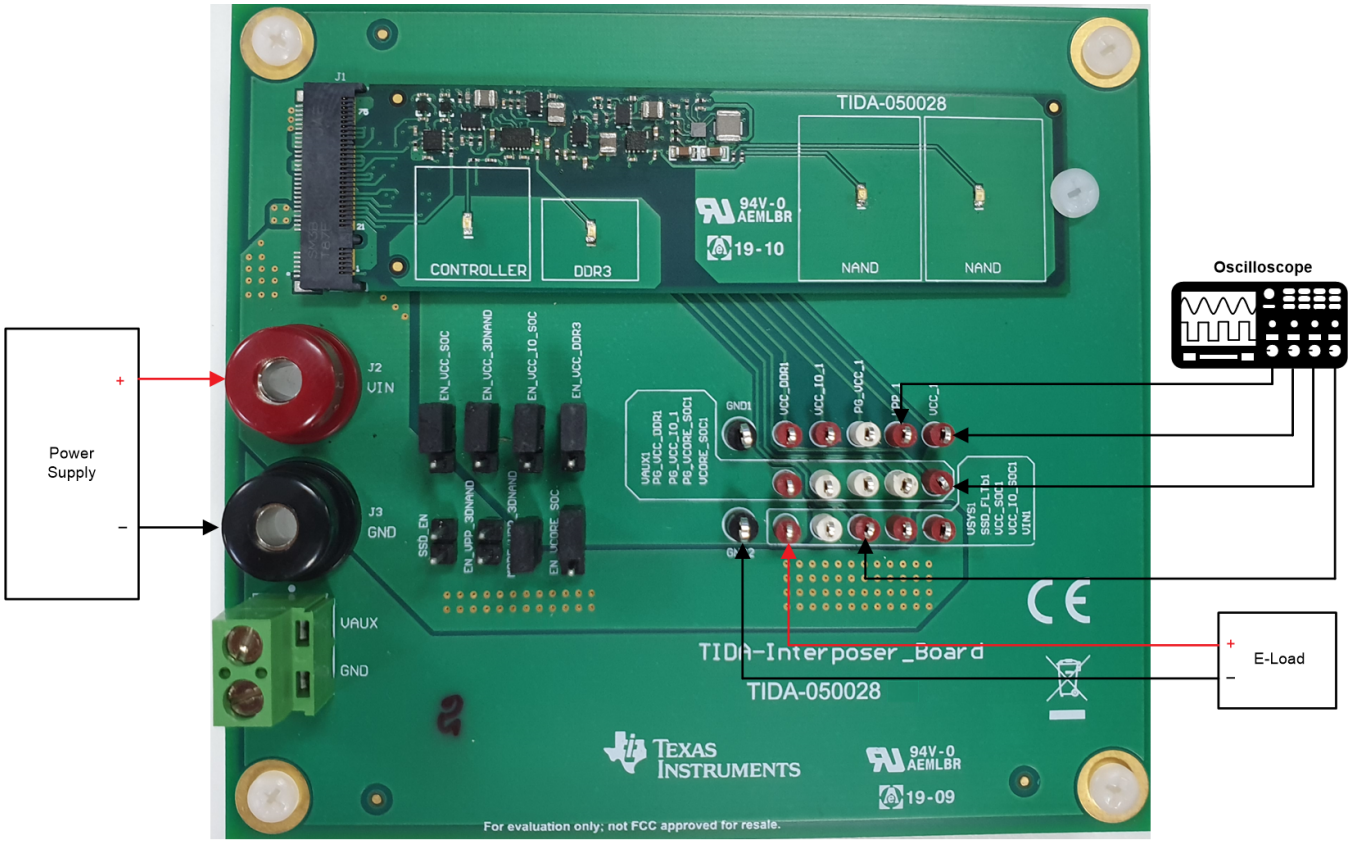
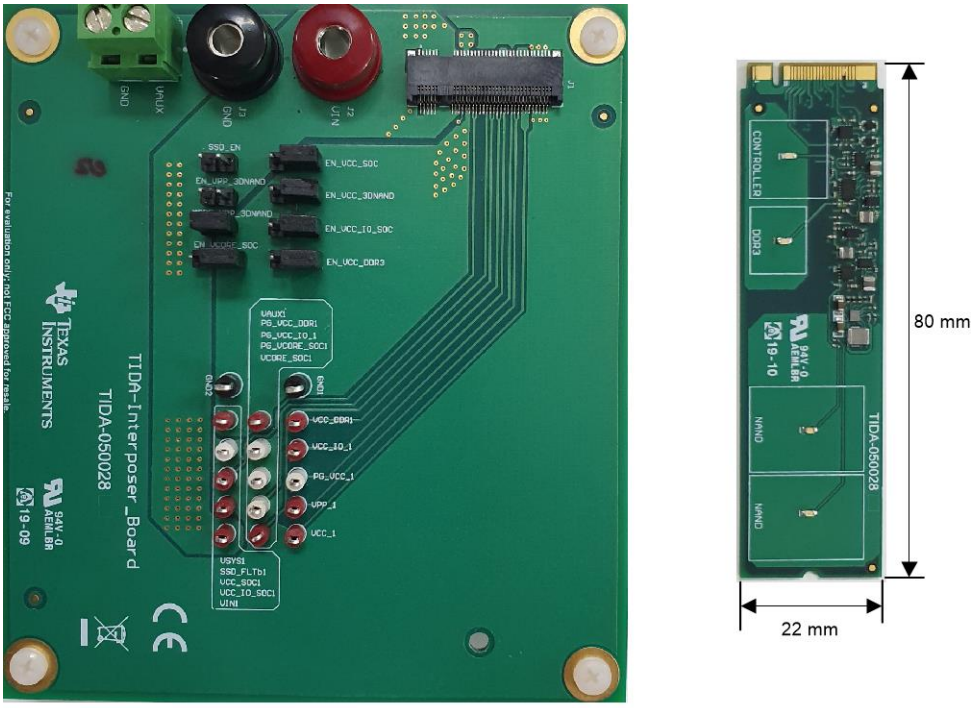


図 7. TIDA-050028 (a) Interposer Board (b) Daughter Card in M.2 2280 Form Factor



(a) (b)

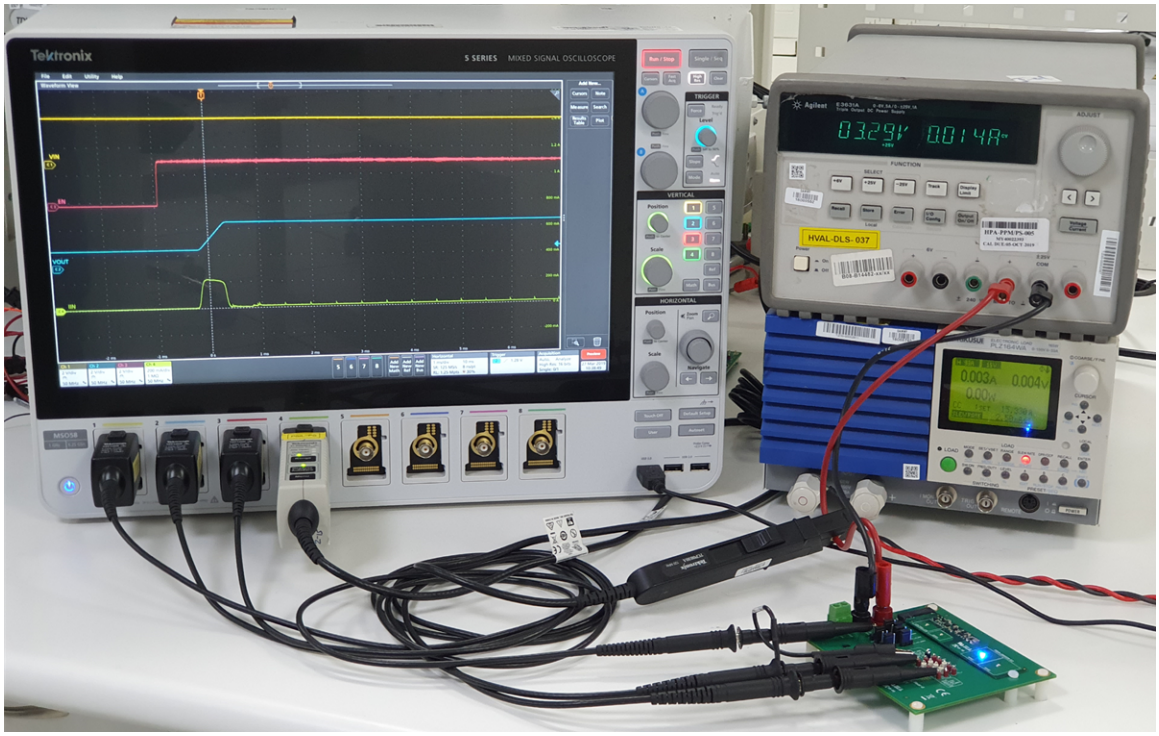
3.2 Testing and Results

3.2.1 Test Setup

The following section describes how we set up TIDA-050028 for testing.

- Connected DC power supply between J2 (VIN) and J3 (GND)
- Placed jumpers of eFuse and 3DNAND section in ENABLE position on the interposer board
- Set DC power supply to 3.3 V and 4 A and kept in OFF position
- Plugged SSD daughter card to the interposer board at the J1 connector
- Turned DC power supply ON
- Used jumpers on the interposer board to enable various sections of the daughter board

図 8. Test Setup



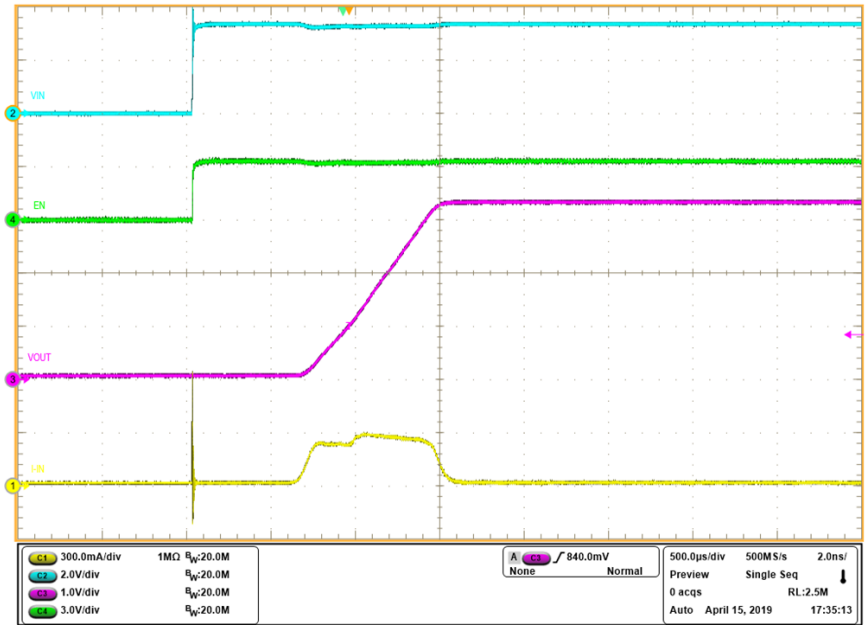
3.2.2 Test Results

The following shows the test results of this reference design.

3.2.2.1 VBus Protection: Hot-Plug Test

図 9 shows output voltage response of TPS259521 during hot-plug event. The device maintains in OFF state to keep the output voltage VOUT at 0 V.

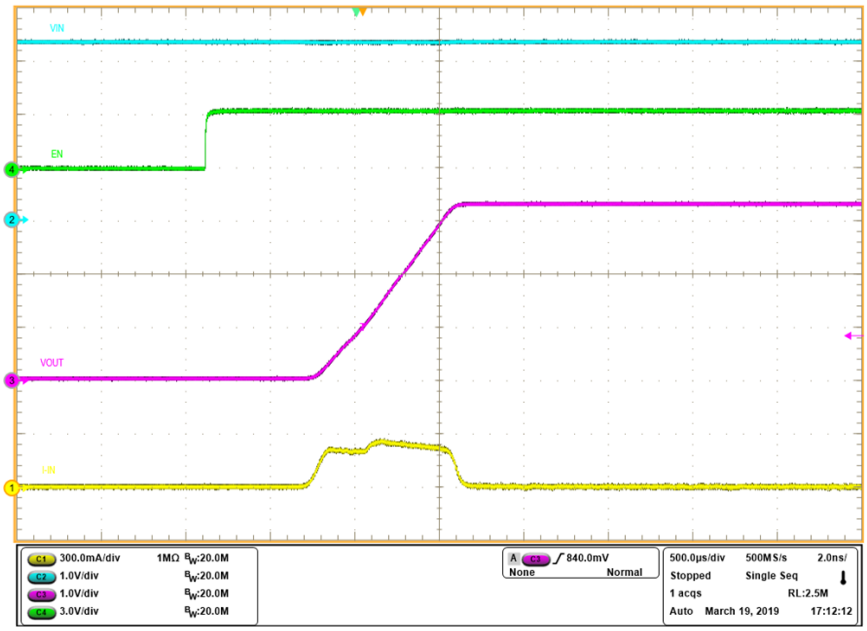
図 9. Hot-Plug Response of TPS259521 at V_{IN} = 3.3 V



3.2.2.2 VBus Protection: Inrush Current Limit

図 10 shows inrush current limit function of TPS259521 during startup. The eFuse limits the inrush current to 300-mA while starting a 66-µF capacitive load.

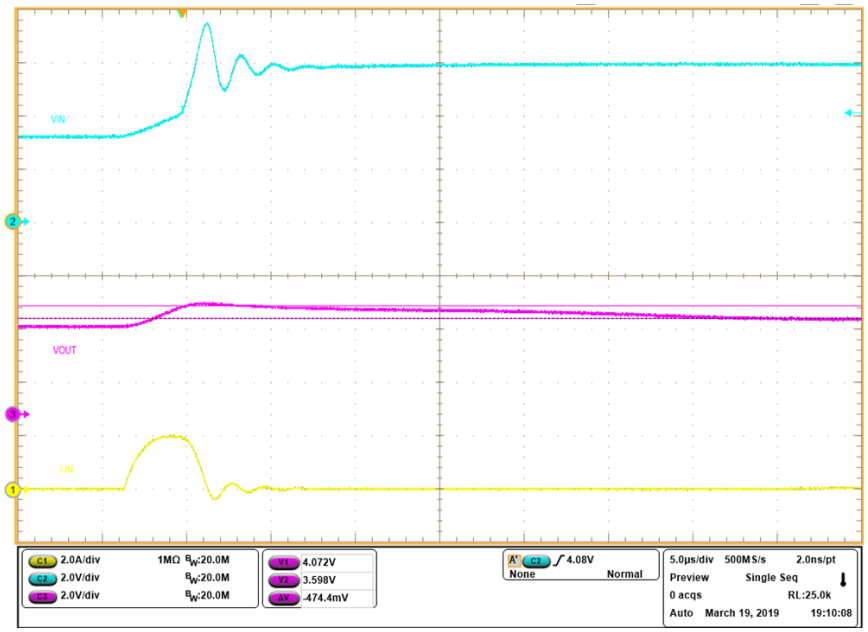
図 10. Inrush Current during SSD Startup; V_{IN} = 3.3 V, C_{OUT} = 66 µF, C_{dVdT} = 10 nF



3.2.2.3 VBus Protection: Overvoltage Test

The TPS259521 eFuse clamps the output voltage to a predefined value if the input voltage crosses overvoltage clamp threshold V_{OVC}.This ensures the load is not exposed to high voltages for any abnormal input voltage and lowers the dependency on external protection devices such as TVS or Zener diodes. 図 11 shows the output voltage clamp response when V_{IN} is stepped from 3 V to 6 V.

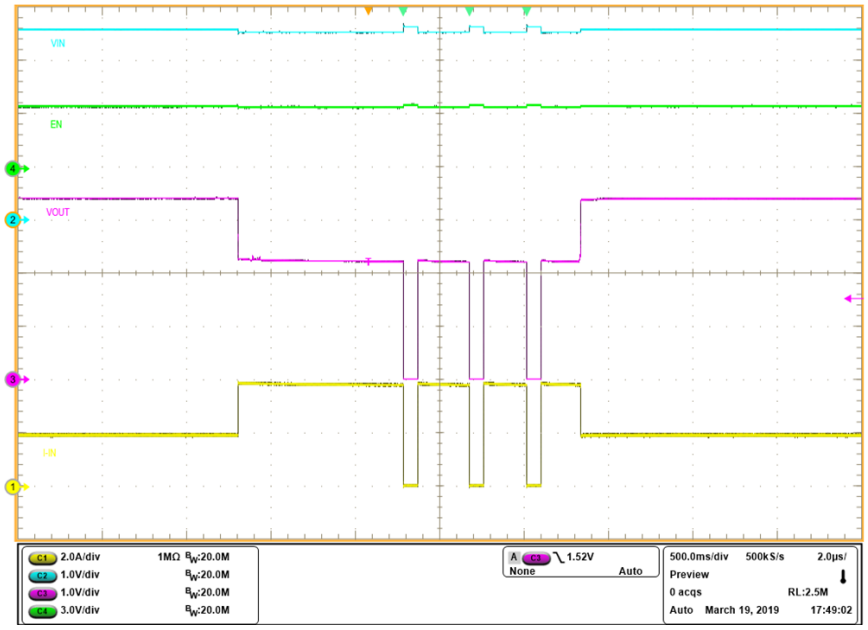
図 11. TPS259521 Overvoltage Clamp Response



3.2.2.4 VBus Protection: Overload Test

図 12 illustrates the overcurrent response of TPS259521 eFuse when the load R_{OUT} varied from 1.65-Ω to 0.73-Ω to 1.65-Ω.

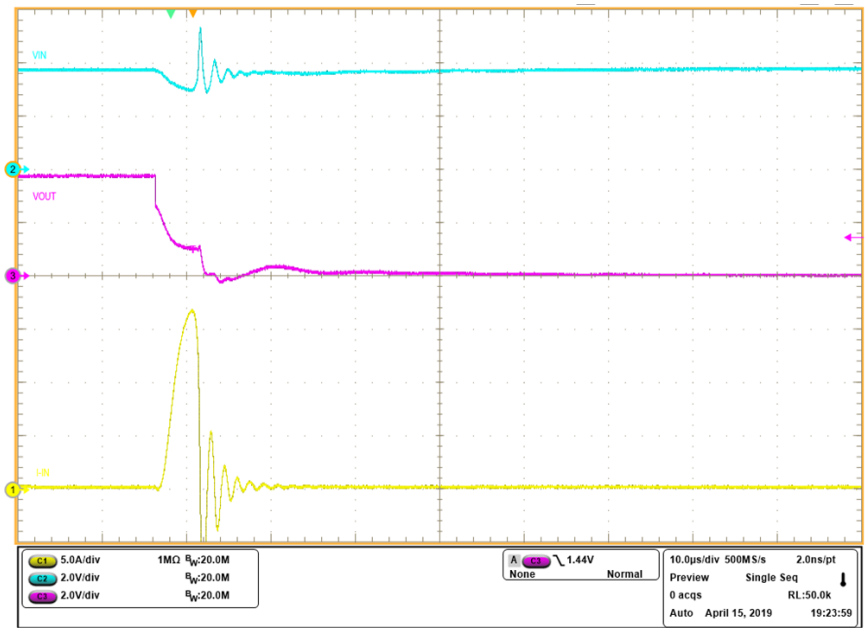
図 12. Overcurrent Response of TPS259521



3.2.2.5 VBus Protection: Short Circuit Test

図 13 shows hot-short behavior of TPS259521 device.

図 13. Output Hot Short to GND Response



3.2.2.6 Buck Converter Performance

The startup waveform of TPS62821 device is shown in 図 14. The TPS62821 device has internal soft-start circuitry to control the output voltage during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time of about 1-ms. 図 15 and 図 16 show steady state operating waveforms in PWM (pulse width modulation) and PSM (power save mode) modes. The output voltage transient regulation during load step from 100-mA to 400-mA and back to 100-mA is shown in 図 17.

図 14. Startup into 2.5-Ω Load; V_{OUT} = 1.2 V

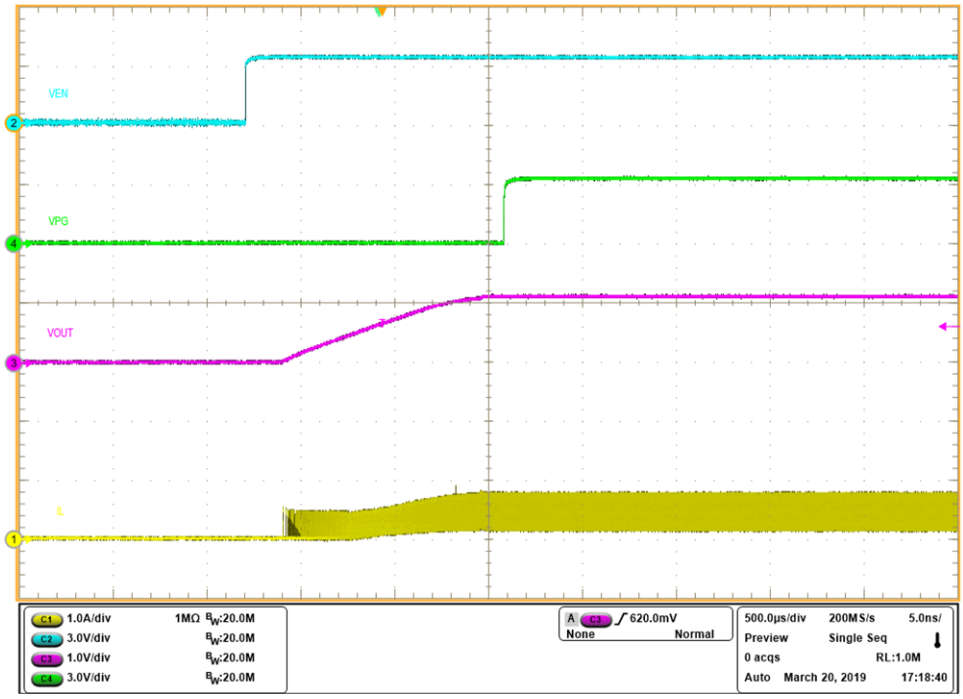


図 15. Typical PWM Operation

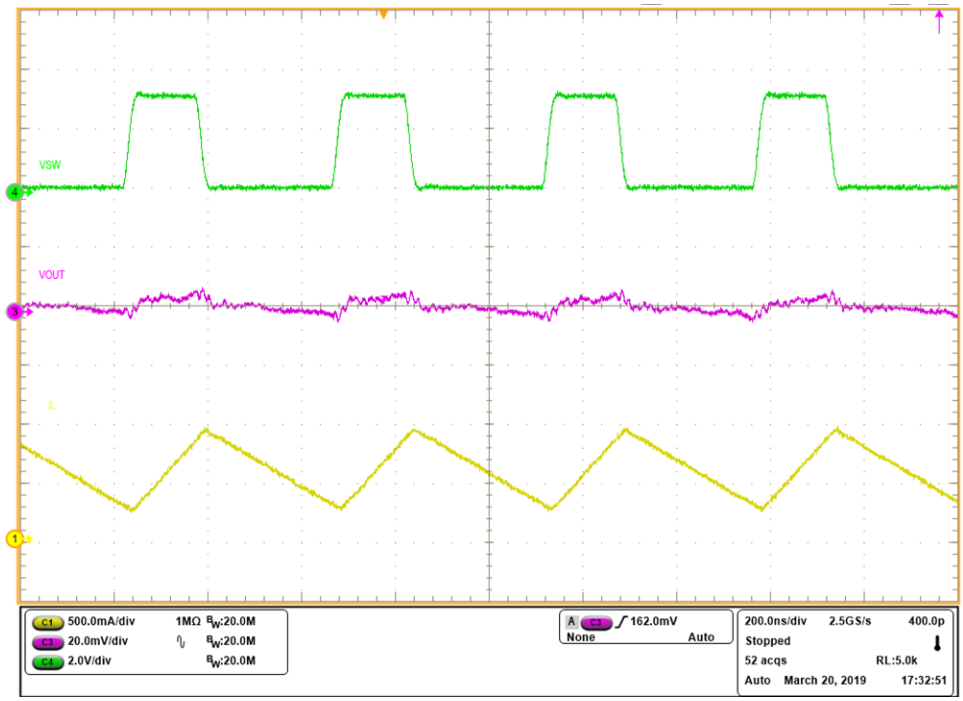


図 16. Typical PSM Operation

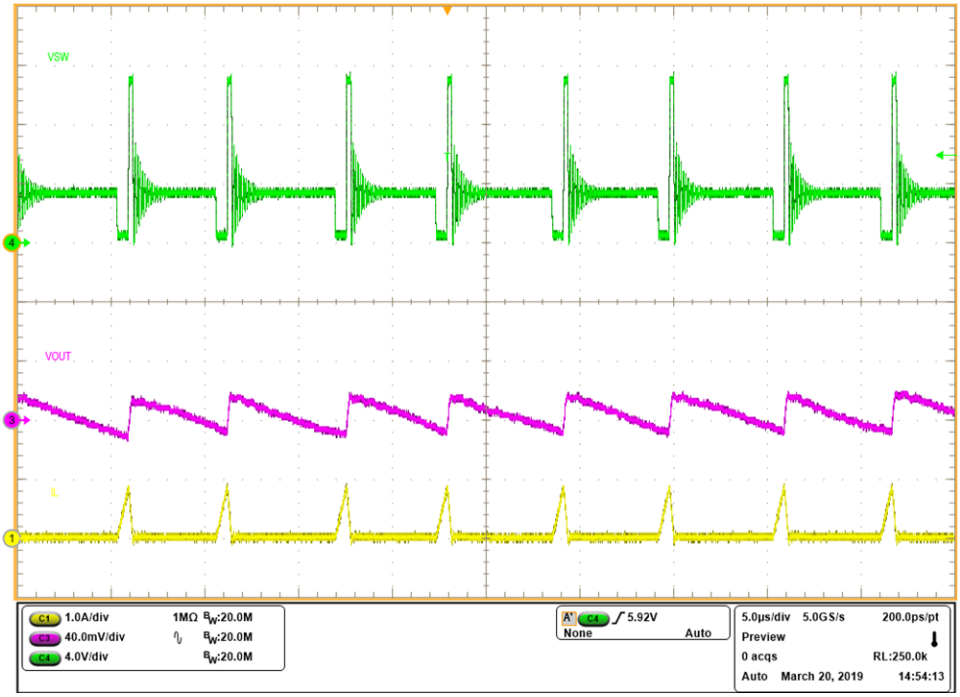


図 17. Load Transient Response of TPS62821

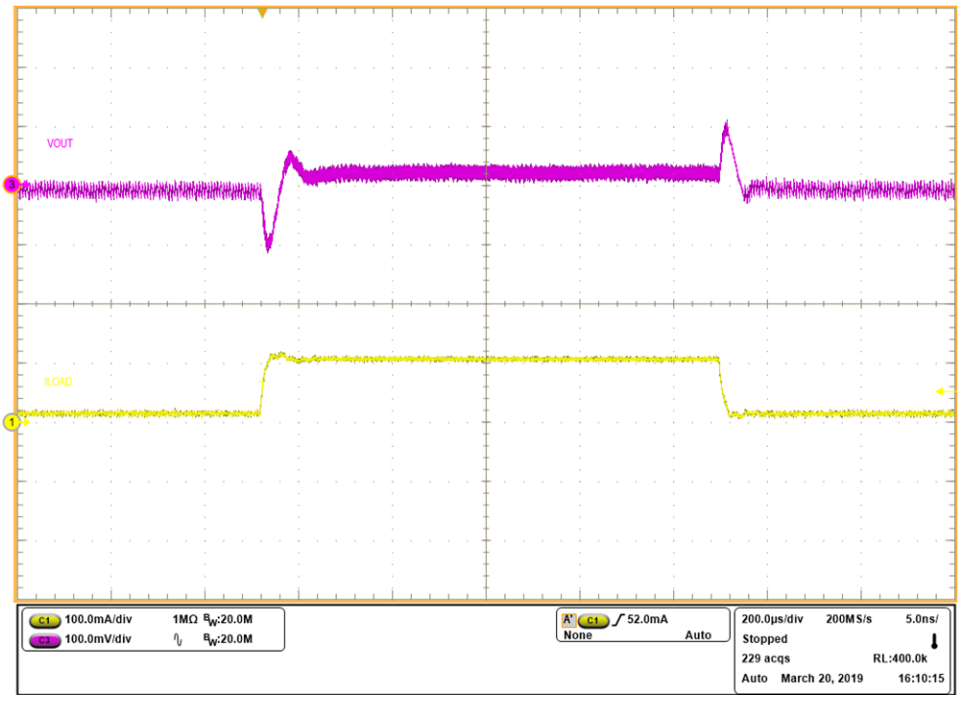


図 18. Efficiency of TPS62821 at V_{OUT} = 1.2 V

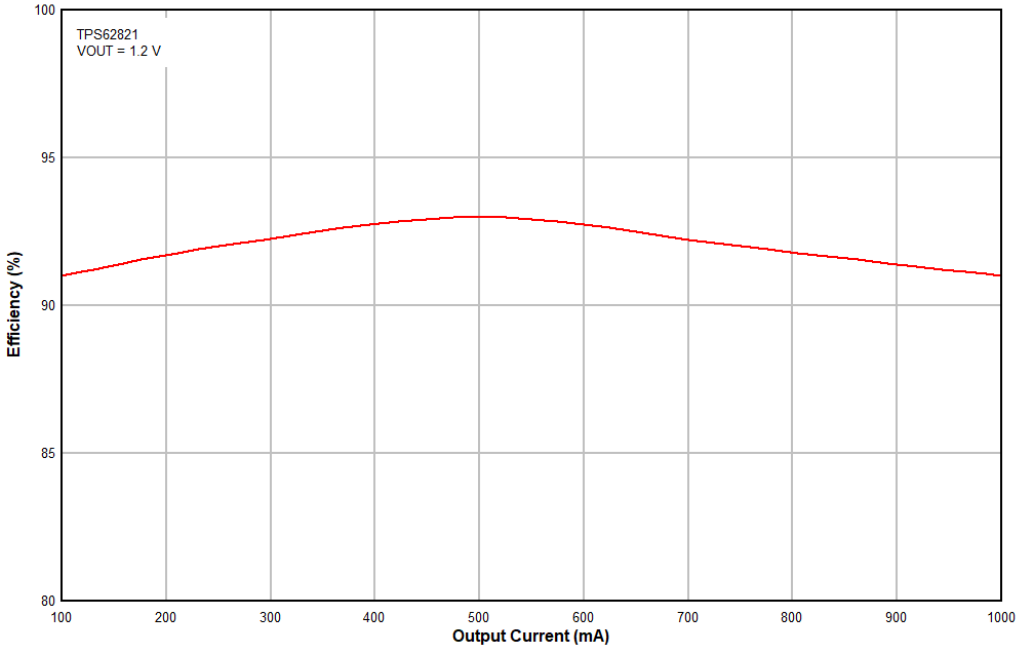
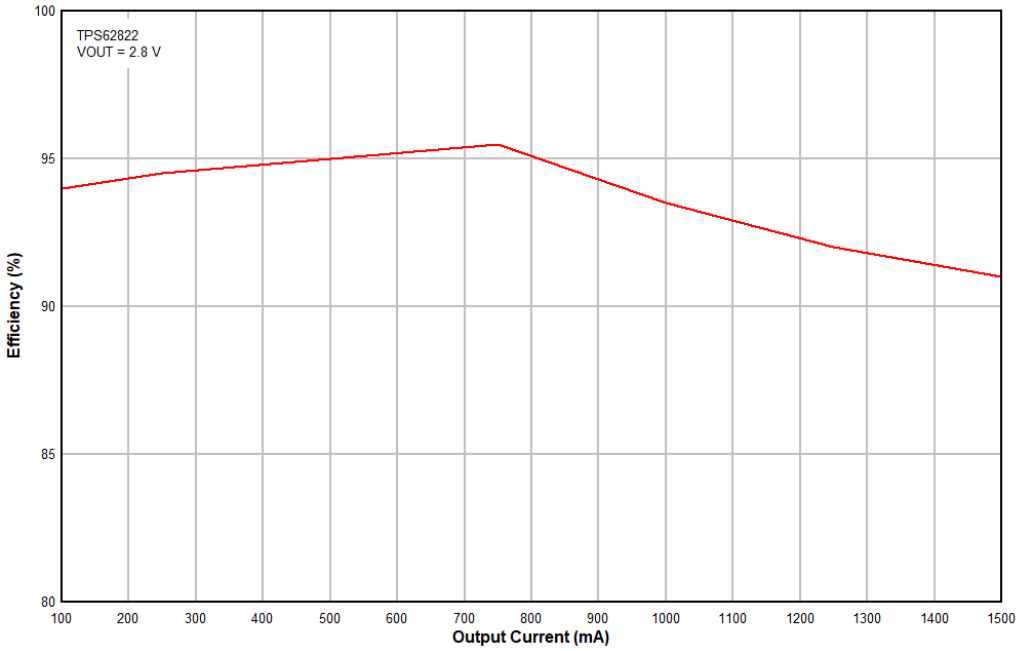


図 19. Efficiency of TPS62822 at V_{OUT} = 2.8 V



3.2.2.7 Boost Converter Performance

図 20 shows startup profile of TPS61372 during boosting 3.3 V input voltage to 12 V with 120-Ω load. 図 21 and 図 22 show the steady state operating waveforms. The TPS61372 device is configured in Auto PFM mode. So, at light loads, the device switches from pulse width modulation (PWM) to pulse frequency modulation (PFM) to optimize efficiency. 図 23 shows the load transient response for load step from 10 mA to 100 mA to 10 mA.

図 20. Startup into 120-Ω Load; V_{OUT} = 12 V

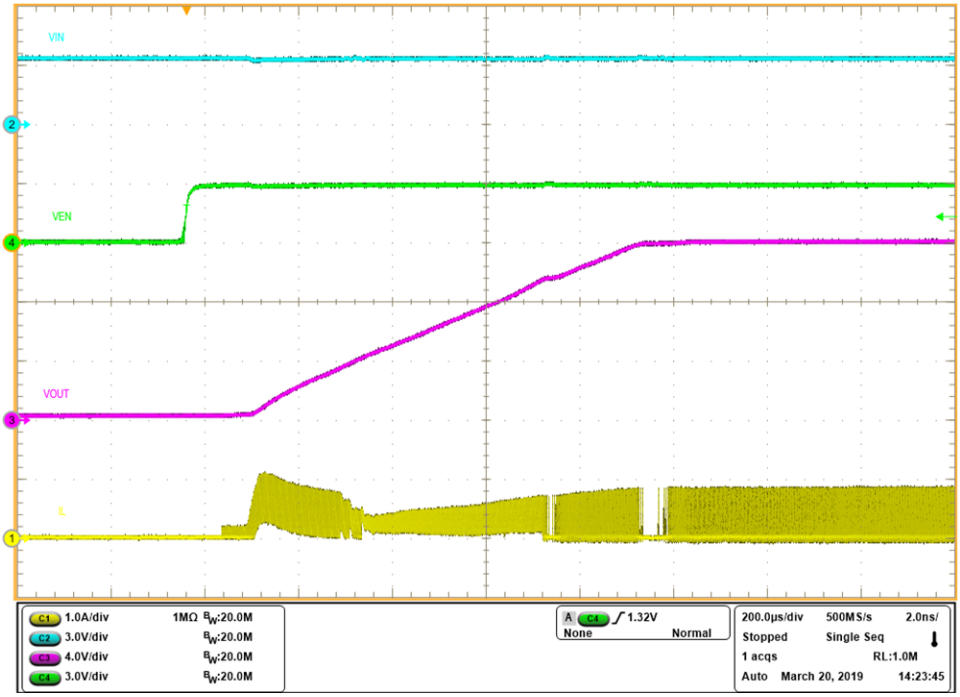


図 21. Steady State Operation at 100-mA Load

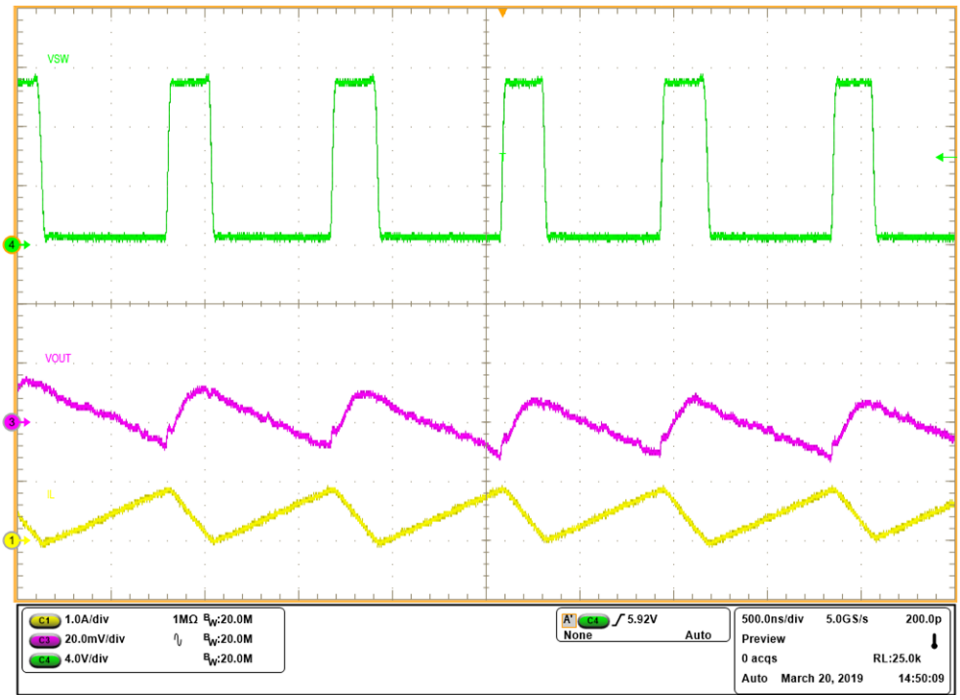


図 22. Steady State Operation at 10-mA Load

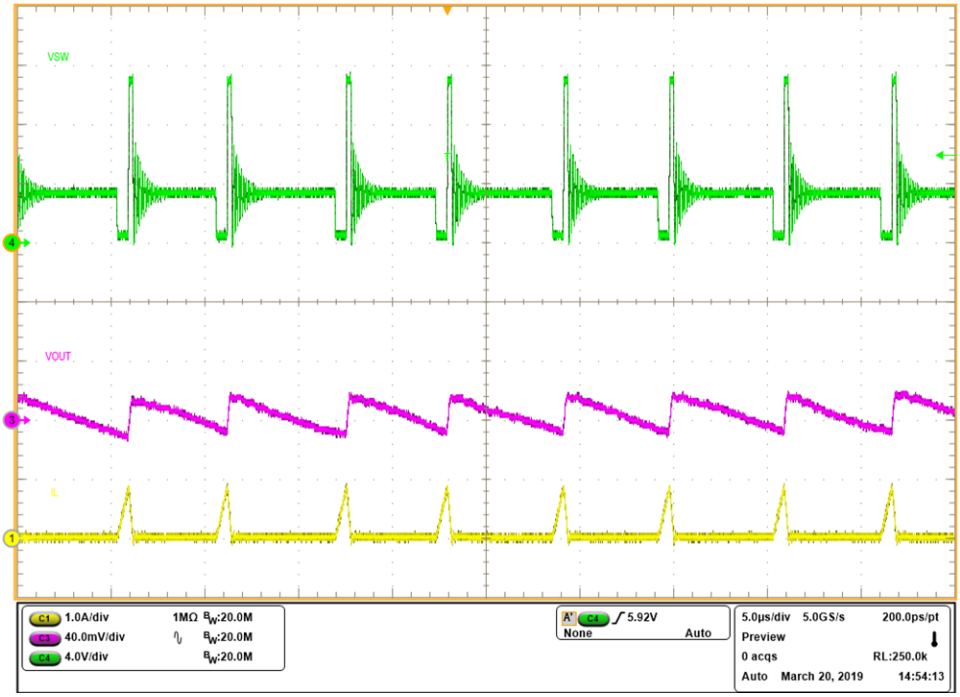
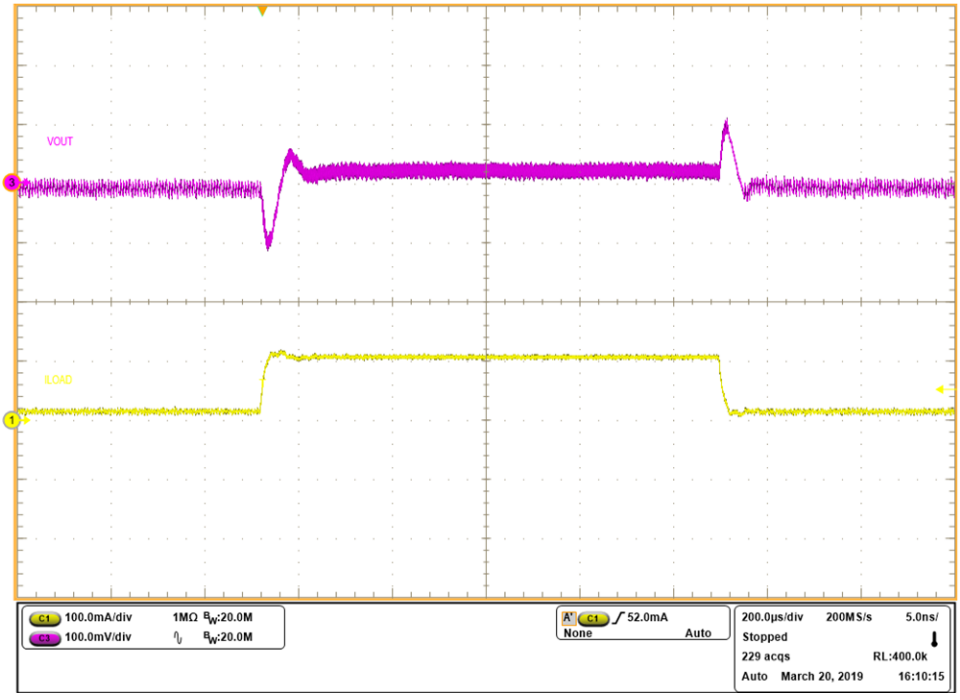


図 23. Load Transient Response of TPS61372



3.2.2.8 Inrush Current Control With Load Switch

図 24 and 図 25 demonstrates how the slew rate controlling capacitor CT of TPS22975 load switch helps in limiting the inrush current while turning-ON load capacitance of 47 µF on 2.8 V rail.

図 24. Inrush Current with CT = 0-pF

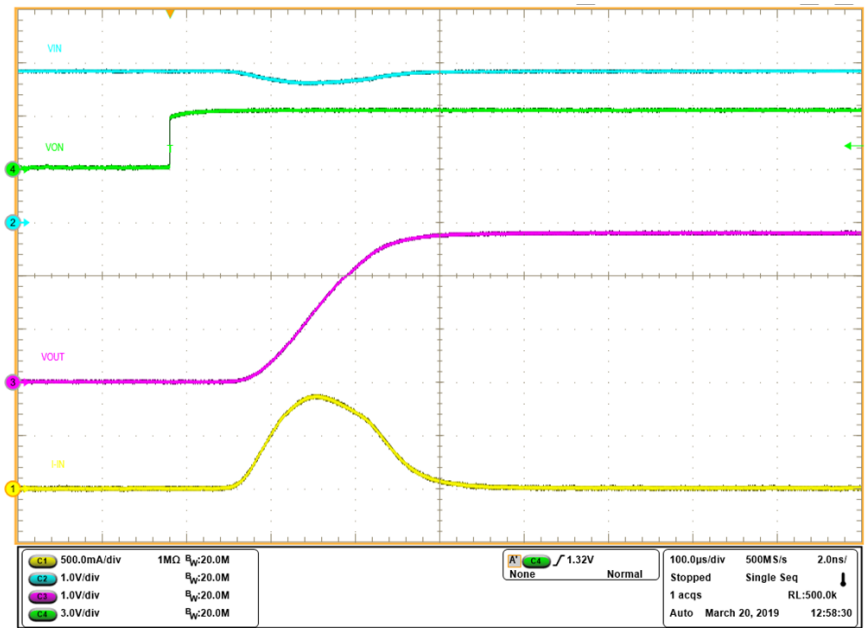
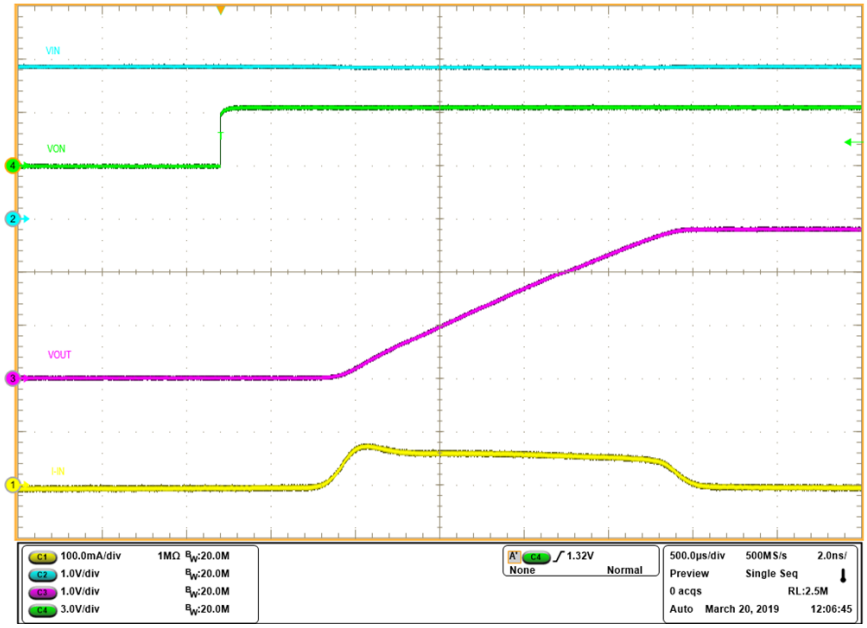


図 25. Inrush Current with CT = 1000-pF



3.2.2.9 Load Switch Startup and Shutdown Waveforms

図 26 and 図 27 show the turnon and turnoff timing waveforms for TPS22975 and TPS22976 load switches.

図 26. Turnon Response Time; TPS22975

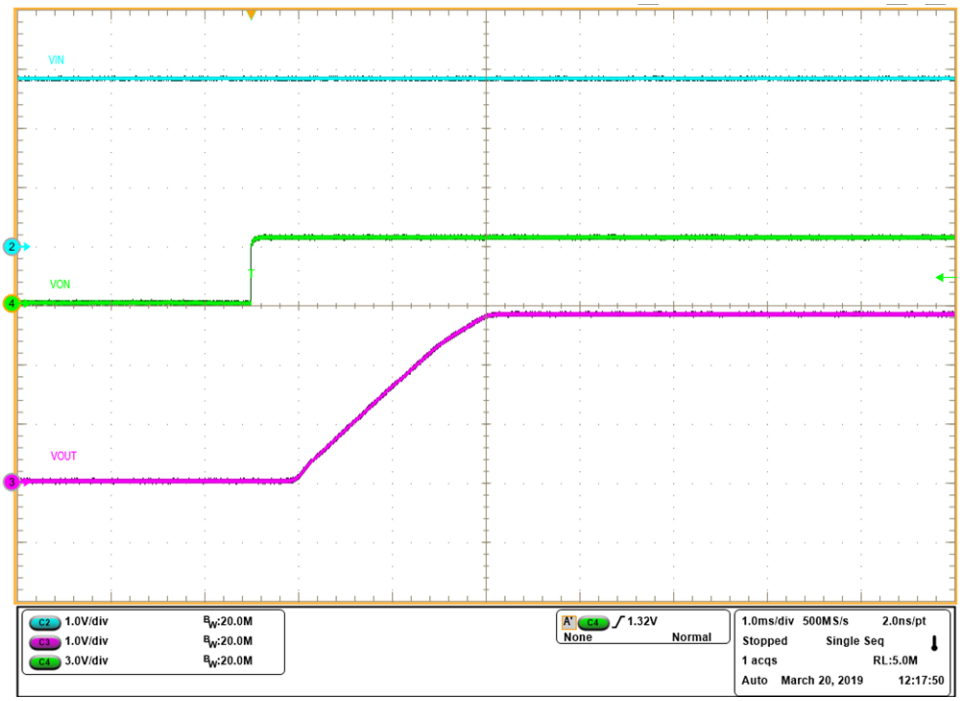


図 27. Turnoff Response Time; TPS22975

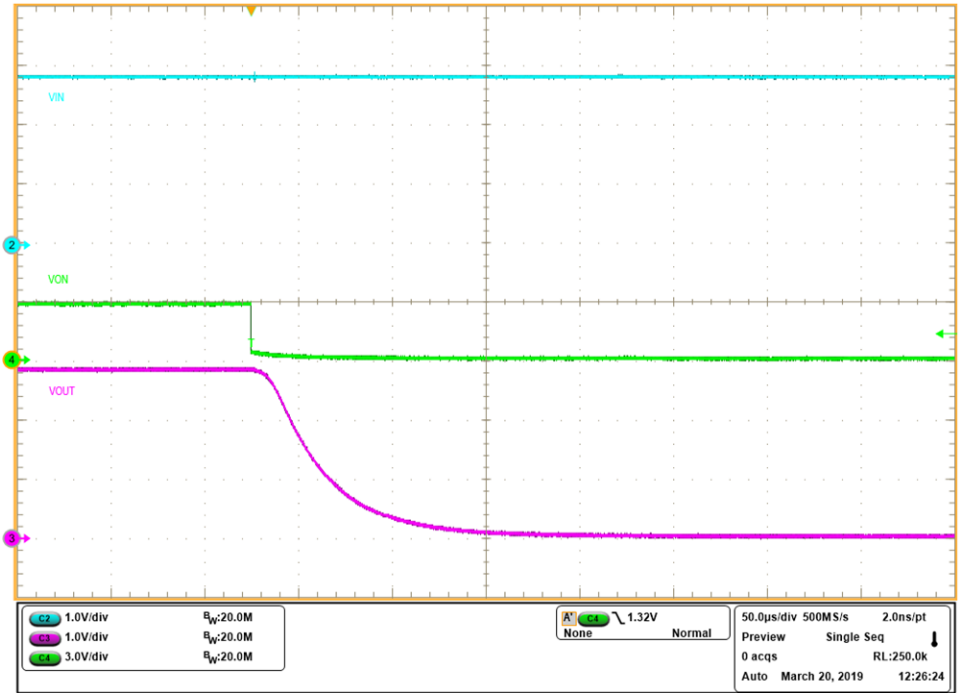


図 28. Turnon Response Time; TPS22976

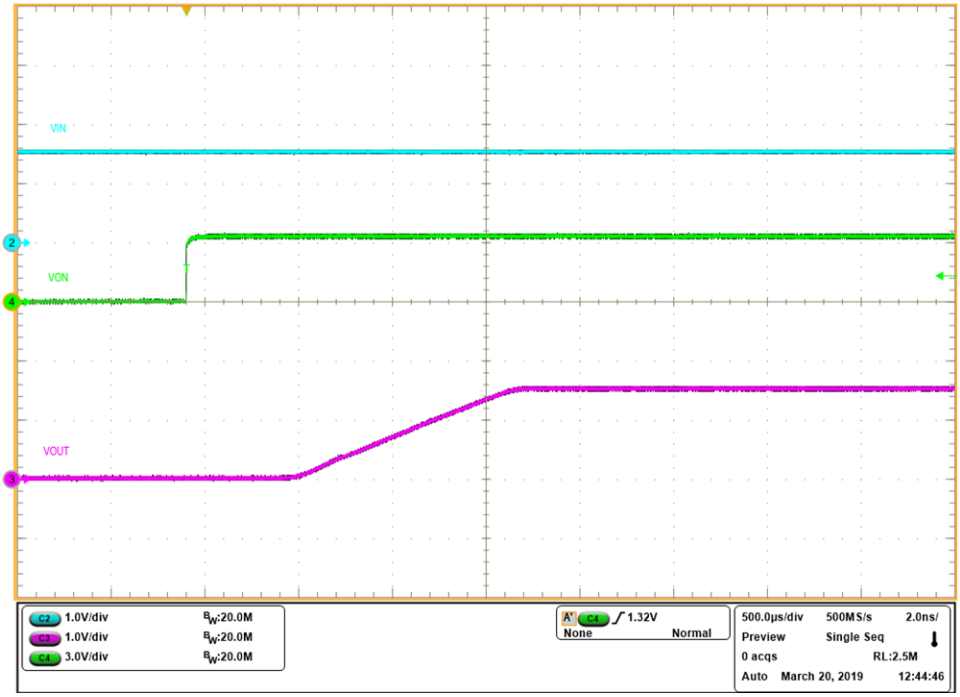
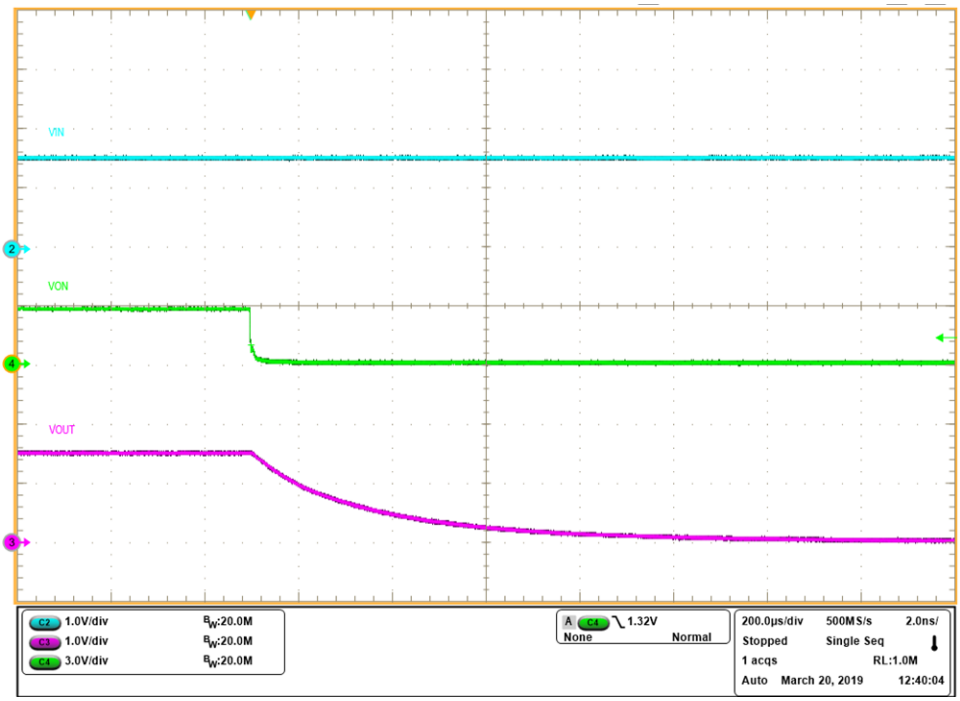


図 29. Turnoff Response Time; TPS22976



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050028.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050028.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050028.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050028.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050028.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050028.

5 Related Documentation

1. Texas Instruments, *TPS2595xx 2.7 V to 18 V, 4-A, 34-mΩ eFuse With Fast Overvoltage Protection* Data Sheet
2. Texas Instruments, *TPS22975 5.7 V, 6-A, 16-mΩ On-Resistance Load Switch* Data Sheet
3. Texas Instruments, *TPS22976 5.7 V, 6-A, 14-mΩ On-Resistance Dual-Channel Load Switch* Data Sheet
4. Texas Instruments, *TPS6282x 5.5 V, 1-, 2-, 3-A Step-Down Converter Family with 1% Accuracy* Data Sheet
5. Texas Instruments, *TPS61372 16 V, 3.8-A Synchronous Boost With Load Disconnect* Data Sheet
6. Texas Instruments, *TLV743P 300-mA, Low-Dropout Regulator* Data Sheet

5.1 商標

5.2 Third-Party Products Disclaimer

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