参考資料

デザイン・ガイド: TIDA-010048
チャネル相互間絶縁型アナログ入力モジュールのリファレンス・デザイン

概要

このリファレンス・デザインは、4つのチャネル相互間絶縁4～20mA 電流ループ・アナログ入力モジュールです。このデザインには、センサおよびモジュール・アプリケーションの状況監視のため、短絡、過電流、過電圧制限機能が含まれています。このアナログ入力モジュールの主な機能には、チャネル絶縁、TI の LM5180 デバイスを使用した単一のフライバック・コンバータにより給電されるマルチチャネルのアナログ入力モジュール、2 線式トランスミッタの電源、および短絡保護回路が含まれています。このデザインは、4チャネルのアナログ入力モジュールもサポートしています。

リソース

TIDA-010048	デザイン・フォルダ
LM5180	プロダクト・フォルダ
ADS122U04	プロダクト・フォルダ
TPS2662	プロダクト・フォルダ
ISO7721	プロダクト・フォルダ
TPS7A47	プロダクト・フォルダ
TVS3300	プロダクト・フォルダ
SN74LV4052A	プロダクト・フォルダ

TI E2E™ Community

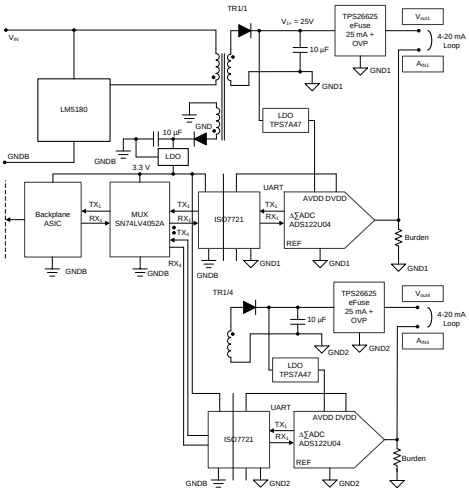
E2E™エキスパートに質問

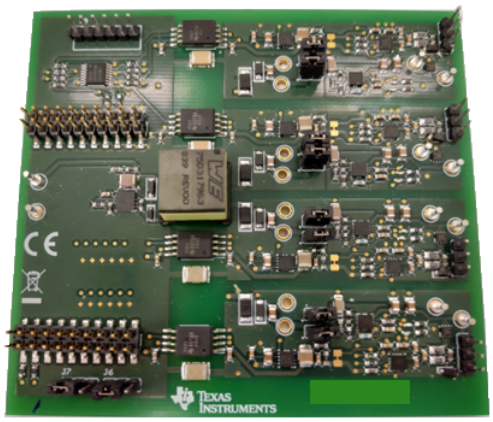
特長

- 1～4 チャネル間の絶縁アナログ入力モジュール
- 出力電力制限を備えたフィールド・トランスミッタ用電源 (短絡時に 25mA に制限)
- トランスミッタ電源: 25 ±1V、IOUT < 25mA (ピーク)
- 入力を誤配線から保護
- UART インターフェイス 24b ΔΣADC により BOM サイズとコストを削減

アプリケーション

- 混合モジュール (AI、AO、DI、DO)
- アナログ入力モジュール

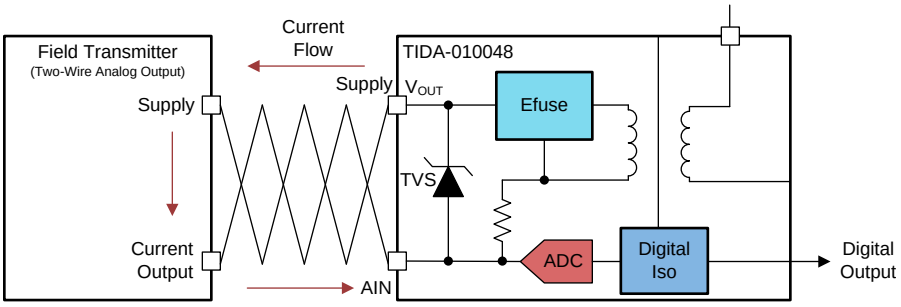




1 System Description

The TIDA-010048 universal analog input module is four channel-to-channel isolated with short-circuit protection, over-current limit, overvoltage limit and high-performance design. Analog input modules digitalize temperature, current (4–20 mA) and voltage (±10V). Analog input modules are challenged with increasing channel density, tolerating high common mode voltages, high throughput with low power, functional or intrinsic safety, high dynamic range, EMI and miswiring protection. This design implements a two-wire 4–20 mA current-loop analog input module system. The design supports remote sensor transmitters without an additional power supply which can eliminate the external ground pin on the casing so the field engineer can avoid miswiring problems. It also can support four-channel analog input module with a single flyback converter. This means the PLC side can reduce the cost and BOM size and achieve channel-to-channel isolated analog input module system. 図 1 shows the typical two-wire current-loop system. The supply of the field transmitter is provided by the analog input module side and current output of field transmitter transfer the analog signal back to analog input module side. There is another key characteristic of this design which uses the eFuse to prevent the overcurrent and overvoltage simultaneously to limit the power flow into the field side.

図 1. Typical Two-Wire Current-Loop System



1.1 Key System Specifications

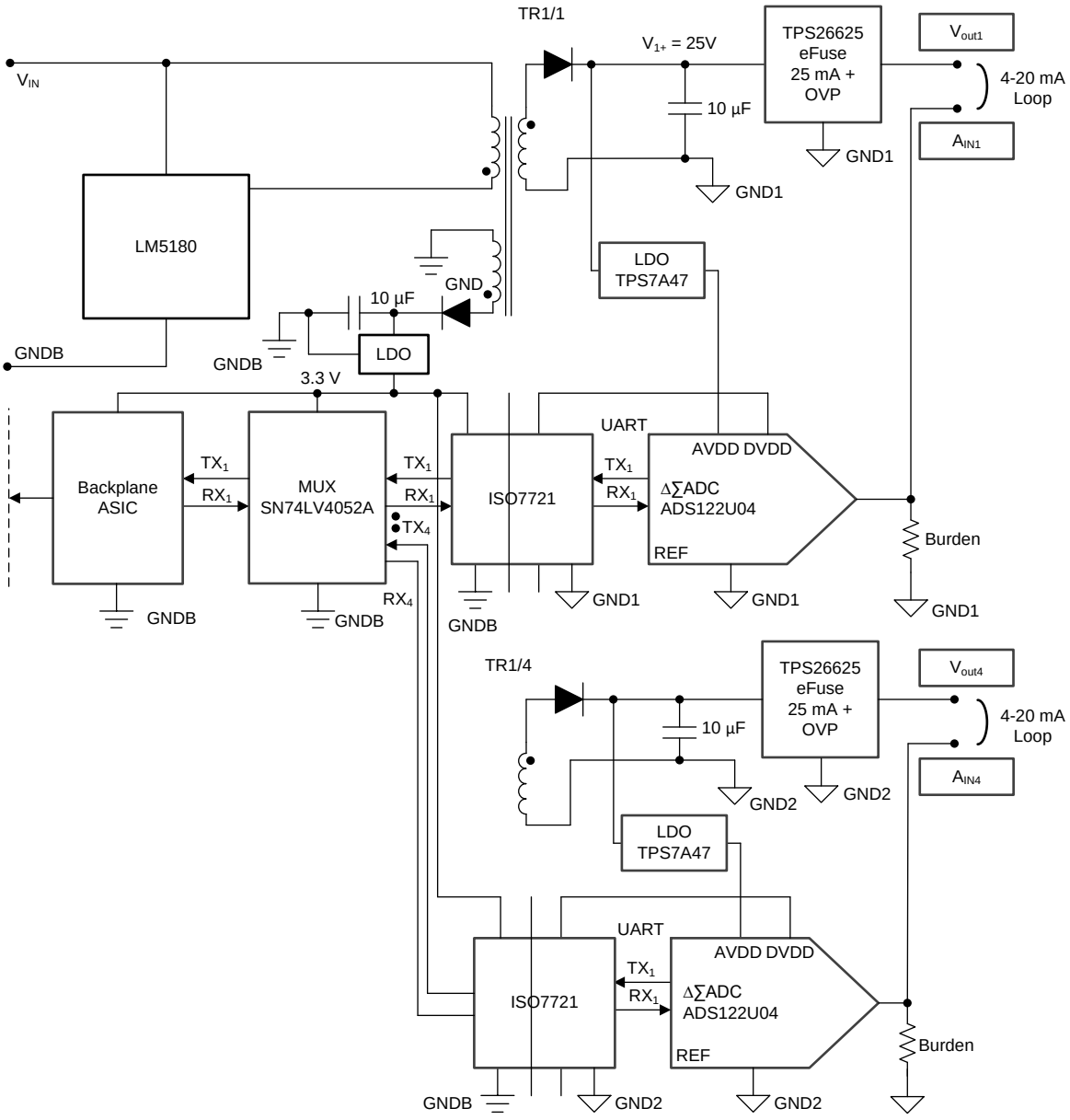
表 1. Key System Specifications

PARAMETER		SPECIFICATIONS
Number of analog input channels (2-wire transmitters)		Four Channels
Power supply part for 2-wire transmitter per channel	Supply voltage	25 VDC
	Overvoltage limit	33 VDC
	Overcurrent and short-circuit limit	25 mA
Isolation	Between backplane and analog input channels	1000 VAC, 1 minute
	Between analog input channels	1000VAC, 1 minute
Analog input module for current loop per channel	Range	4–20 mA
	Resolution	24-bit
	Internal PGA Gain	1, 2
	Sampling Cycle	20 SPS to 1000 SPS
Form factor	Each Channel	5.2 cm × 1.8 cm
	Entire board	9.5 cm × 8.4 cm
Operating temperature		–40°C to 85°C

2 System Overview

2.1 Block Diagram

図 2. System Block Diagram



2.2 Design Considerations

The block diagram in 図 2 is separated into three parts: isolated power, analog front end, and digital isolation signal readout circuit.

The isolated power is mainly implemented with TI's flyback converter (LM5180). The transformer uses Wurth Electronics to customize the transformer which can achieve one-four channel isolated power. The current limit on every channel is set into 25 mA at 25 V DC which is enough for field transmitter applications. The isolation level is decided by the transformer which is functional insulation. The rated voltage of this transformer can be up to 1000 VAC for one minute. If a higher level of isolation is required, the transformer design can be changed to meet the specification. V_{IN} and V_{OUT} voltage are equal to 25 V. The current limit and voltage threshold of every channel which is decided by the eFuse set up at 25 mA and 33 V. Every isolated maximum channel power can provide the field side to 1.25 W.

The analog front end circuit implements a 4–20 mA current loop by the ADS122U04 device which uses the UART interface and a 24-bit ΔΣADC. It could reduce the channel number of digital isolator and the BOM size and cost. The power of ADC is supplied by the wide V_{IN} LDO (TPS7A47). Using the wide V_{IN} LDO can reduce the additional buck converter for stepping down voltage and retains ADC performance. If there are other analog input requirements such as voltage ±10 V, 0–5 V, 0–10 V; Current ±25 mA, 0–20 mA; temperature input RTD, thermocouple and thermistor, see the following TI reference design.

The designers can choose a dual-channel digital isolator for signal isolation due to UART ADC. It can reduce the silicon package size and total BOM cost. A dual four-channel analog MUX in the PLC side helps the customer choose the necessary analog input module to measure the analog signal which can decrease the pins of UART interface on the microcontroller in the backplane side. This provides more flexibility in analog input module system design.

2.3 Highlighted Products

2.3.1 LM5180

The LM5180 device is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 65 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation.

2.3.2 ADS122U04

The ADS122U04 device is a high precision, 24-bit, analog-to-digital converter (ADC) that offers integrated PGA, reference, and internal fault monitors. The device features two differential or four single-ended inputs through a flexible input multiplexer (MUX). The device data rates can be up to 2000 samples-per-second (SPS) with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128. The ADS122U04 features a 2-wire, UART-compatible interface. With a UART interface, engineers only need a two-channel digital isolator. It could reduce the cost and BOM size.

2.3.3 TPS26625

The TPS2662X family have a wide supply input range of 4.5 V to 57 V. The device can withstand and protect the loads from positive and negative supply voltages to ±60 V. TPS26625 devices support both input as well as output reverse polarity protection features. Load, source, and device protection are provided with many adjustable features including overcurrent, output slew rate and overvoltage, undervoltage thresholds. Therefore, using a single eFuse circuit can achieve power limit functions for field transmitter in hazardous region.

2.3.4 TPS7A47

The TPS7A470x is a family of positive voltage (+36 V), ultra-low noise (4 μV_{RMS}) low-dropout linear regulators (LDO) capable of sourcing a 1-A load. The TPS7A47 device is designed with bipolar technology, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

2.3.5 TVS3300

The TVS3300 is a protection device with a very low leakage current component. It also can robustly shunt up to 35 A of IEC 61000-4-5 fault current to protect systems from high-power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to 1-kV IEC 61000-4-5 open circuit voltage coupled through a 42-Ω impedance.

2.3.6 ISO7721

The ISO772X devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW and DWV packages) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO7721 device has both channels in the opposite direction; therefore, it also could support UART interface.

2.3.7 SN74LV4052A

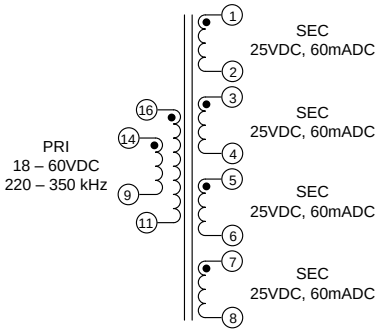
The SN74LV4052A device is a dual, 4-channel multiplexer and demultiplexer that is designed for 2-V to 5.5-V V_{CC} operation. The dual 4-channel MUX can help to choose the necessary analog input module to measure analog signal.

2.4 System Design Theory

2.4.1 Channel-to-Channel Isolated Power Supply for Field Transmitter

This reference design provides four channel-to-channel isolated power supplies for 4–20 mA current-loop circuit as 図 3 illustrates. The four-channel supply units are all powered up by the single flyback converter (LM5180). Every channel can support the current up to 30 mA and output voltage at 25 V. The isolated rated voltage is 1000 VAC in 1 minute.

図 3. Flyback Transformer Symbol for TIDA-010048

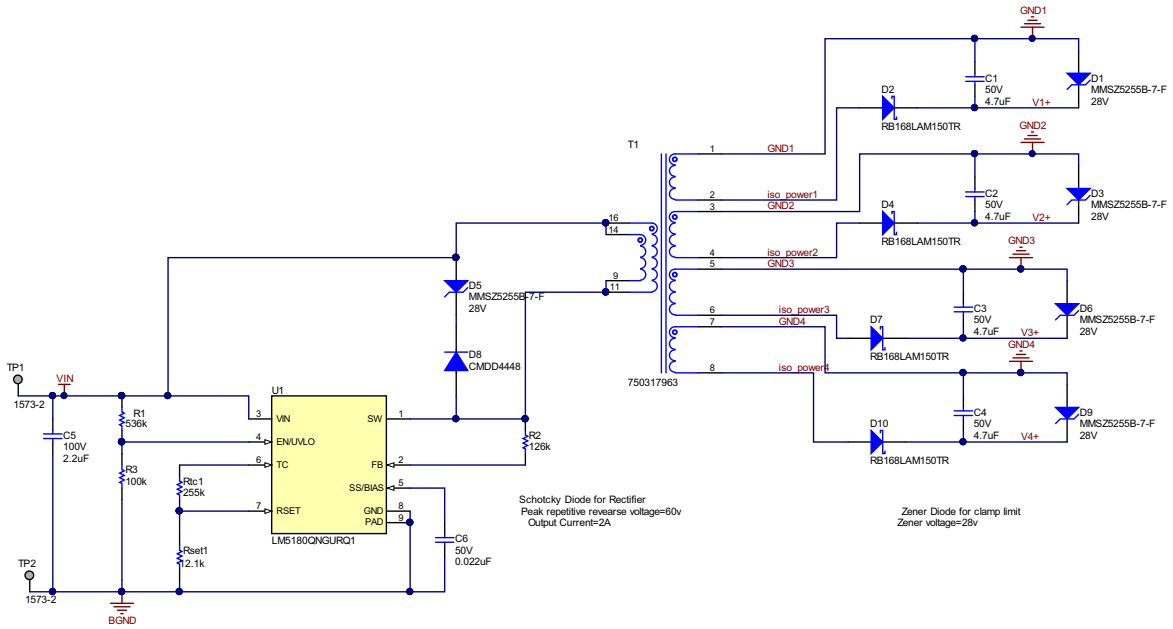


The detailed requirements of the transformer follow:

- Four 25-V isolated outputs: all of them with 30 mA
- Switching frequency range: 100 kHz–350 kHz
- Isolation voltage:
  - Primary to secondary, 1000-VAC for 1 minute
  - Secondary to secondary, 1000-VAC for 1 minute
- Functional insulation between windings

If the design architecture requires higher safety requirement more than functional isolation, the transformer can be redesigned.

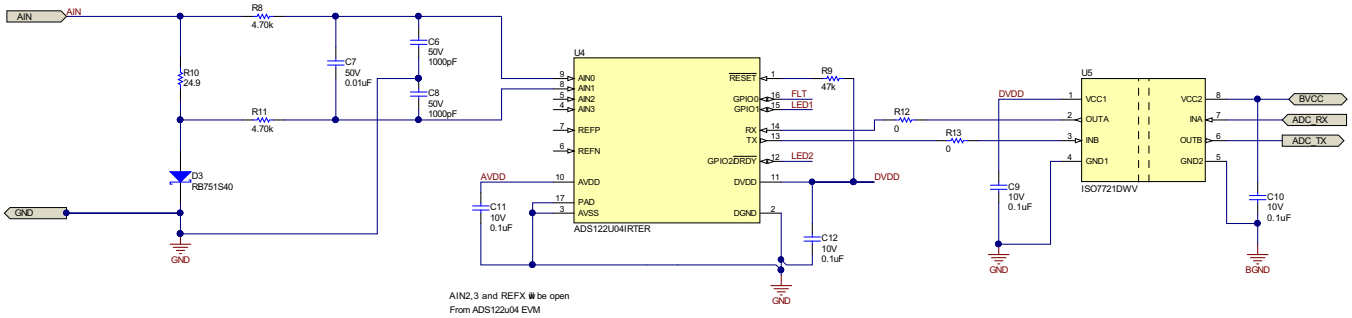
図 4. Channel-to-Channel Isolated Power Supply Using LM5180



2.4.2 Analog Front End

The module features a two-wire, four channel, 4–20 mA analog input module which can be used with sensor transmitters with 4–20 mA current loop. The main purpose of this circuit is to build a reliable delivery of 4–20 mA loop current analog input front end. 図 5 shows the detail of the analog front end circuit. R10 is the R_{shunt} to transfer the current signal into voltage. A first-order resistor-capacitor (RC) filter is used in the AFE. The filter corner frequency is set at 1.6 kHz. D3 is for shifting the input signal level. It can make the analog input signal remain in full-scale range of the ADC when the PGA is on. The ADC using a UART interface can reduce the number channels of digital isolator.

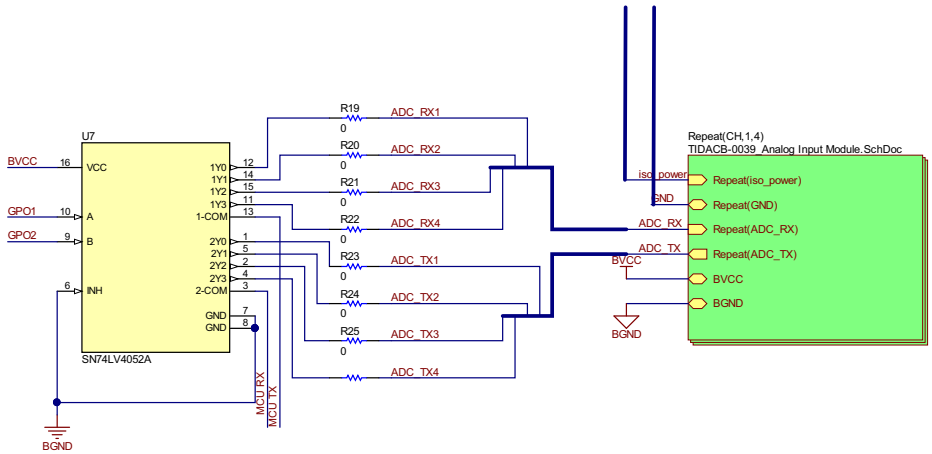
図 5. Analog Input Front End



2.4.3 Data Accquistion Systems Using UART Interface

In the *Reducing System Cost, Size and Power Consumption in Isolated Data Acquisition Systems Using ADS122U04 Tech Note*, the ADS122U04 replaces the standard SPI interface with a 2-wire UART interface. Engineers only need a twochannel digital isolator with no additional uC or processor in the ADC side which is depicted in 図 6. Using TI's ADS122U04 device, the industry's first sensor measurement ADC with UART interface, designers can reduce their digital isolator power consumption and cost by > 30% compared to conventional implementations while still taking advantage of the high resolution and integration of a 24-bit delta-sigma ADC. To build the data acquisition systems for four sets of analog input modules, the design uses the dual four-channel MUX to capture the required data from different analog input module as 図 6 shows.

図 6. Data Acquisition Systems Using UART Interface Block Diagram



2.4.4 Two-Wire 4–20 mA Current-Loop Analog Input Module

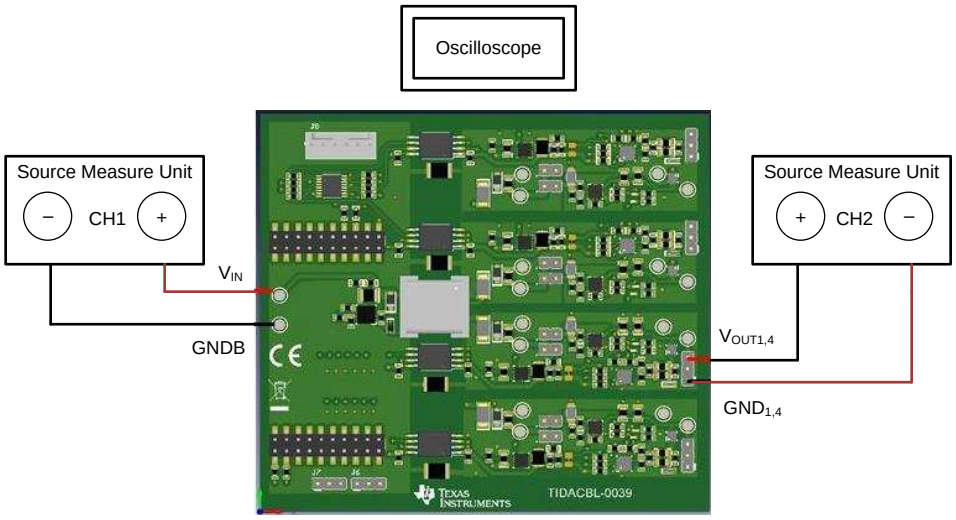
図 1 shows a typical two-wire, 4–20 mA current-loop analog input module which TIDA-010048 is based on. The key advantage of the two-wire system can provide 4–20 mA power for the field transmitter. Therefore, the whole field side system does not need an extra power supply to power-up the field transmitter. Another advantage is to avoid setting the grounding pin outside the casing of analog input module, so you can use TVS to connect the power supply and the analog input pin to protect the surge as the *Typical Application* section in the *TVS3300 33-V Flat-Clamp Surge Protection Device Data Sheet* details.

3 Test and Measurement Results

3.1 Power Tree Test Result

図 7 shows the power tree test setup. Use the source measure unit to get the flyback efficiency, cross regulation, start-up waveform, and the waveform of ripple when the load variation is in the other channel. Because the actual performance data may be affected by measurement techniques and environmental variables, these curves and waveforms are presented for reference and may differ from actual field measurements.

図 7. Power Tree Test Setup



3.1.1 Efficiency Performance

The efficiency measurements were taken channel by channel as 図 8 shows. The efficiency performance is as expected. 表 2 shows the whole system performance. It includes the power dissipation of other channels quiescent current loss and the power loss of the signal chain circuit. Although, it is a little lower than ideal, it is still enough for the power dissipation of the field transmitter.

図 8. Efficiency Performance of Flyback

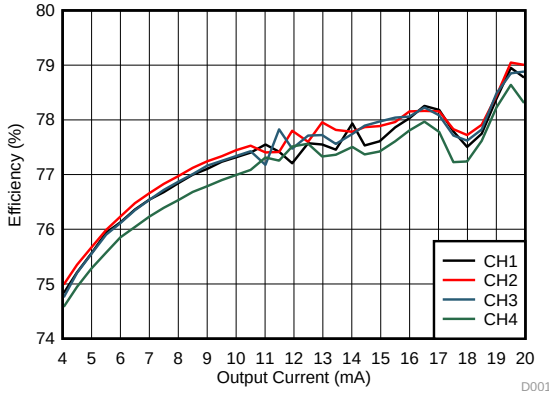


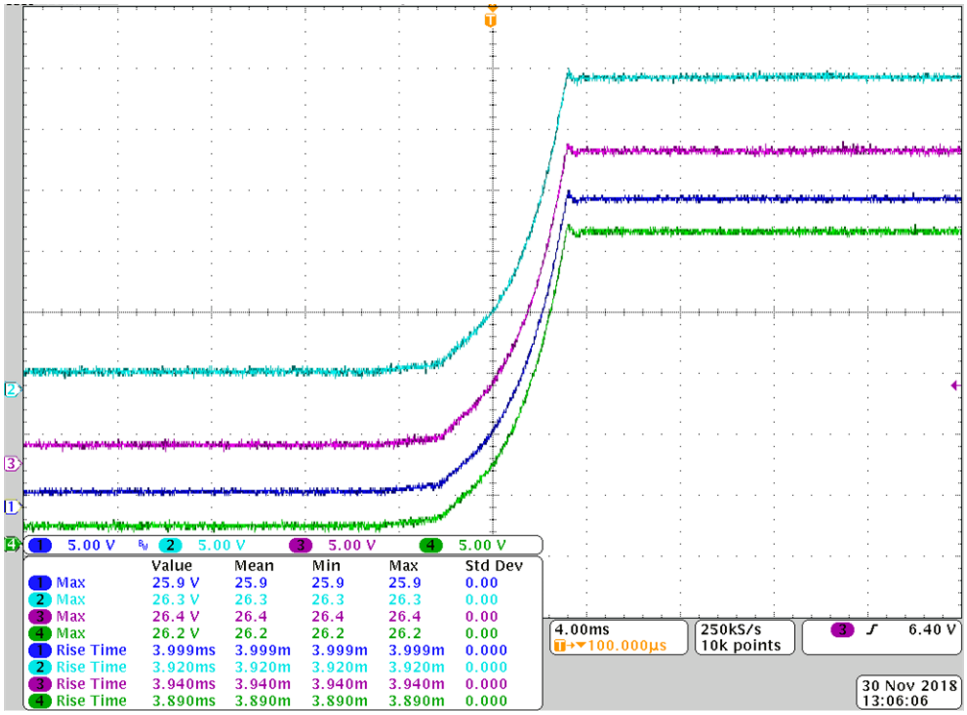
表 2. Total System Efficiency

	4 mA FOR EACH CHANNEL	12 mA FOR EACH CHANNEL	20 mA FOR EACH CHANNEL
Input power (W)	0.763	1.65	2.65
Output power (W)	0.413	1.27	2.12
Total efficiency (%)	54.1	77.3	79.9

3.1.2 Start-Up Waveform

図 9 shows the start-up waveform. The waveform is tested at full load at 25-V input. The four channel sets at the same output load and input situation. The default internal soft-start time of the LM5180 device is 6 ms and an externally-programmable soft start.

図 9. Start-Up Waveform



3.1.3 Load Regulation and Cross Regulation

図 10 shows the influence at the output of flyback with the other channel load varying from 4 mA to 20 mA. The green line and the blue line, respectively, represent the load state of the load variation channel and the constant 20-mA channel under load variation conditions. The normal channel of V_{OUT} variation is about 22.4 mV. The load variation channel of V_{OUT} variation is about 94 mV.

図 10. Load Regulation Waveform

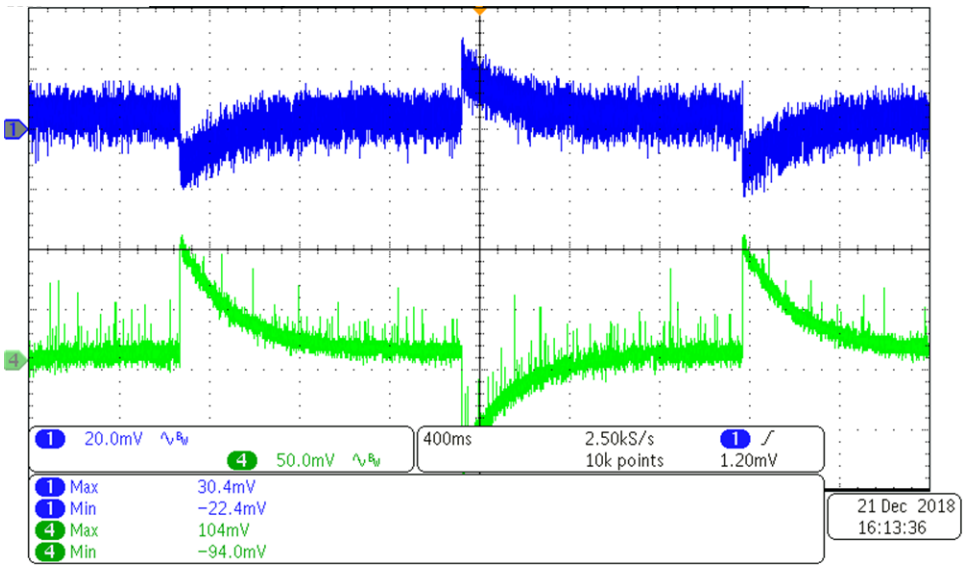
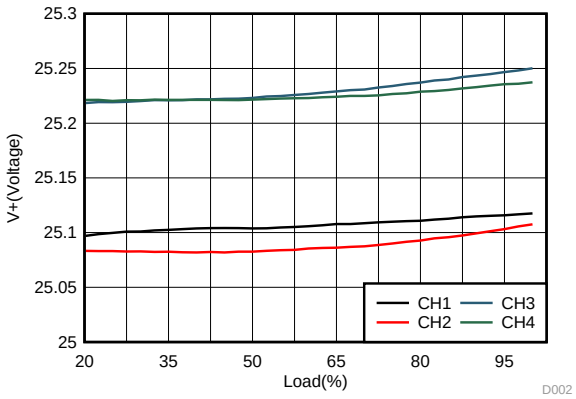


図 11 shows the cross regulation performance of the reference design. The flyback output voltage is influenced by the load current of the other channels. The variation of the output voltage level is fairly stable under all conditions in the 4–20 mA load current and the reasons of voltage gap between CH1,2 and CH3,4 is mostly related with transformer parameter differences.

図 11. Cross Regulation Performance



3.2 Test Result of Overcurrent and Short-Circuit Protection

The eFuse provides the short-circuit and overcurrent limit protection feature for two-wire current loop. 図 12 illustrates the behavior of the system during output short-circuit condition. The short-circuit behavior induces about 42-mV overvoltage in V_{OUT} in the normal channel. 図 12 also shows the auto-retry function and the retry time per cycle is 512 ms.

図 12. eFuse Short-Circuit Protection Waveform

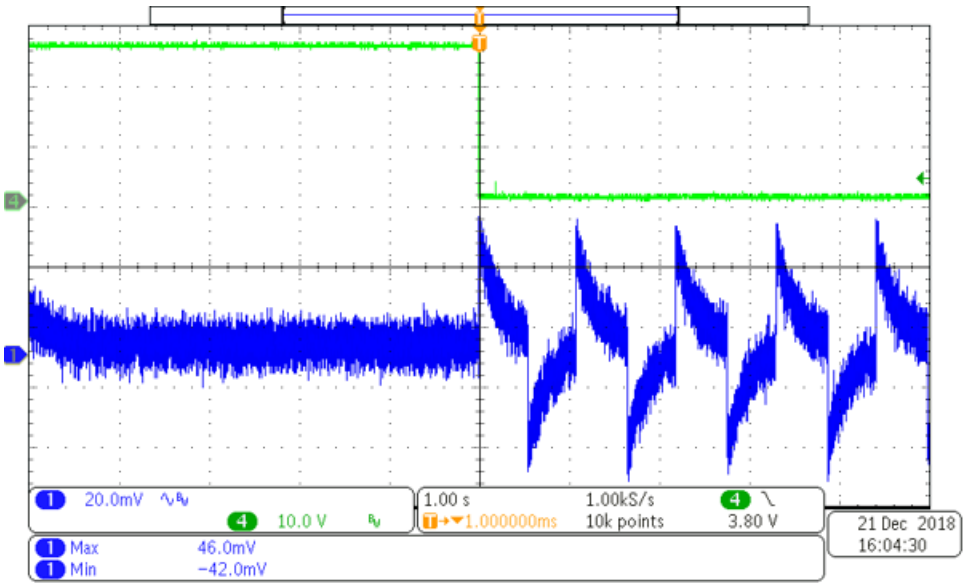


図 2 shows the VOUT pin of the normal and short channel and the FLT pin. The voltage of the Fault pin goes down after the short-circuit occurs. It could provide the alert signal to the controller side, if the short circuit happens.

This reference design has an eFuse in the power line which can provide the overvoltage and overcurrent protection simultaneously. If the field transmitter is located in a hazardous region, any sparks or blink create the high possibility of explosion. Due to that, the eFuse can provide the power limit for the field transmitter side, it is suitable for safety applications. 表 3 shows voltage, current, and power limit of every channel.

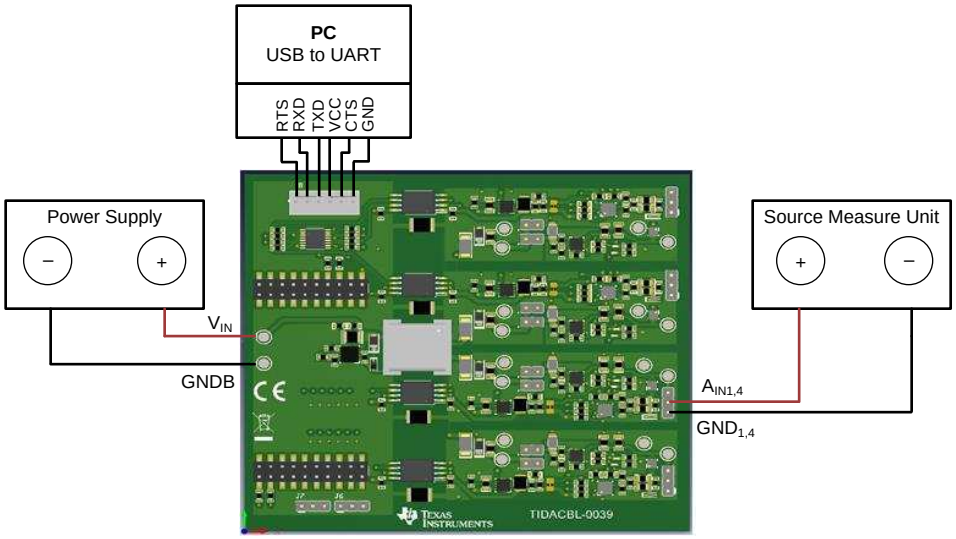
表 3. Power Limit by eFuse

	CH1	CH2	CH3	CH4
Overvoltage limit	33.3 V	33.3 V	33.3 V	33.2 V
Overcurrent limit	24.944 mA	25.174 mA	25.311 mA	25.574 mA
Over power limit	830 mW	839 mW	843 mW	849 mW

3.3 Test Result of Analog Input Module Performance

図 13 shows the signal chain test setup. Due to the UART interface signal chain design, testing the ADC performance is easier. Using the STDI, connect the PC and the board directly to reduce the number of isolation channels and the current consumption. The 4–20 mA analog input current source used is the high precision SMU (B2912A) which is accurate up to 0.02% in the 10-mA range. It ensures the real performance of the ADC is measured. To obtain the effective and noise-free bits, the standard deviation is calculated from 750 samples taken from an externally-applied 4-mA, 12-mA, and 20-mA constant current. The loop current is not measured by an external DMM since the absolute value is not of importance. 図 14 through 図 25 show the relatively current data histogram based on 図 13 at different conditions.

図 13. Signal Chain Test Setup



$$I_{4-20mA} = \left(\frac{2^{\frac{code}{N-1}} \times V_{INT,REF}}{R_{BURDEN}} \right) = \left(\frac{2^{\frac{code}{23}} \times 2.048}{24.9} \right) \quad (1)$$

The effective number of bits and noise-free bits are calculated using 式 2 and 式 3:

$$\text{Effective bits} = \log_2 \left(\frac{2^N}{\text{stddev}[\text{samples}]} \right)$$

where

- N = data width of converter (2)

$$\text{Noise} - \text{Free bits} = \log_2\left(\frac{2^N}{\text{stddev}[\text{samples}] \times 6.6}\right) = \text{Effective} - 2.72 \text{ bits} \quad (3)$$

図 14. Histogram – 4 mA, Gain = 1, SPS = 20, STD = 21.61 ENOB = 19.56

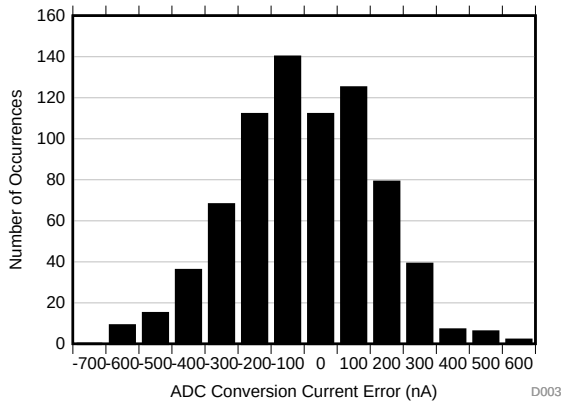


図 15. Histogram – 4 mA, Gain = 1, SPS = 1000, STD = 183.84 ENOB = 16.47

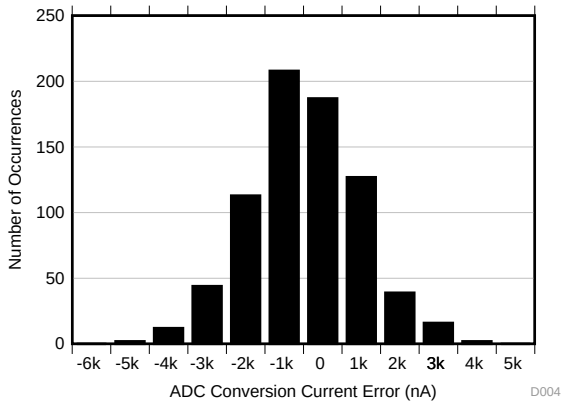


図 16. Histogram – 4 mA, Gain = 2, SPS = 20, STD = 21.8 ENOB = 19.55

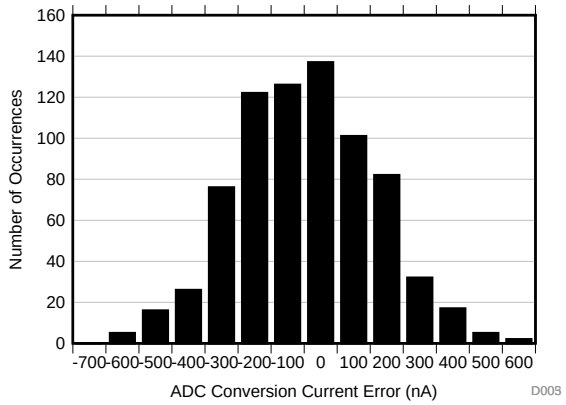


図 17. Histogram – 4 mA, Gain = 2, SPS = 1000, STD = 149.64 ENOB = 16.77

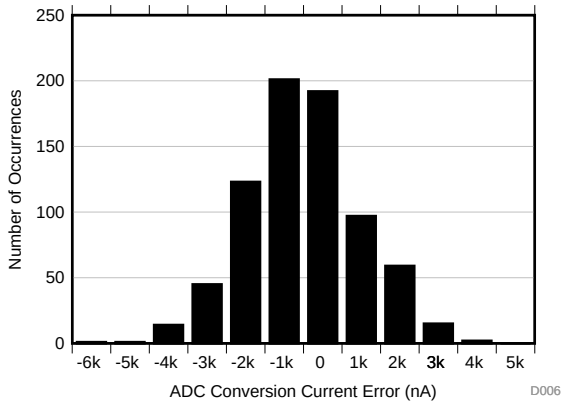


図 18. Histogram – 12 mA, Gain = 1, SPS = 20, STD = 24.4 ENOB = 19.39

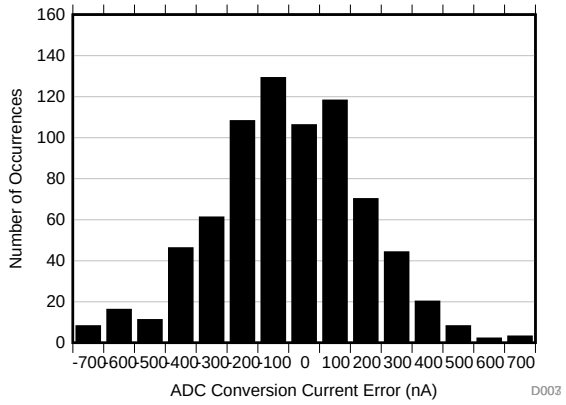


図 19. Histogram – 12 mA, Gain = 1, SPS = 1000, STD = 152.7 ENOB = 16.75

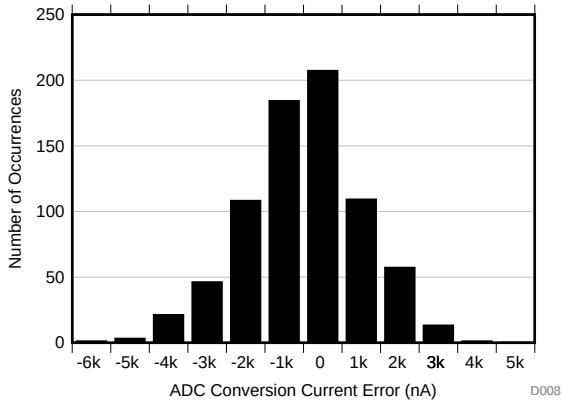


図 20. Histogram – 12 mA, Gain = 2, SPS = 20, STD = 31.25 ENOB = 19.03

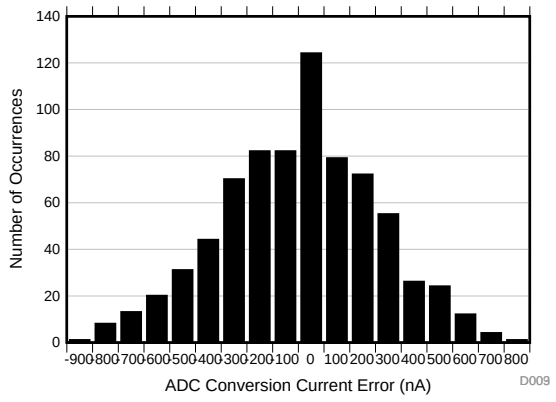


図 21. Histogram – 12 mA, Gain = 2, SPS = 1000, STD = 177.51 ENOB = 16.53

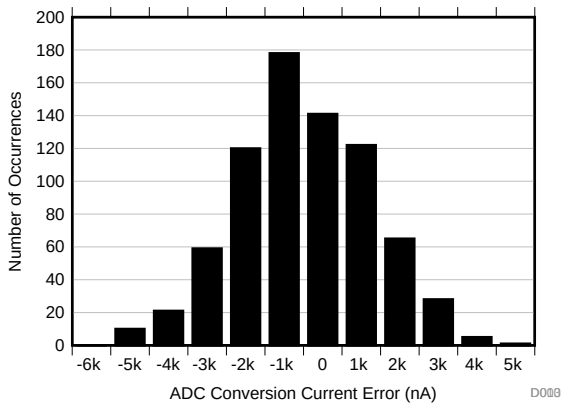


図 22. Histogram – 20 mA, Gain = 1, SPS = 20, STD = 25.43 ENOB = 19.33

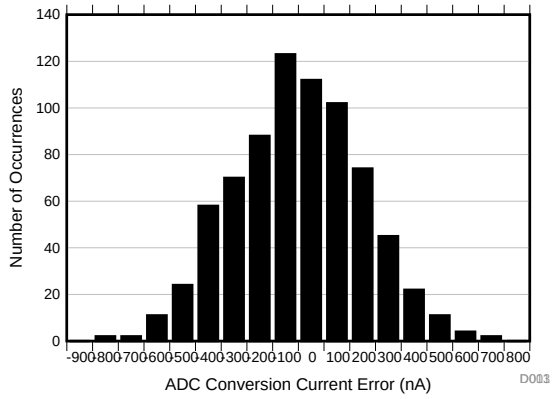


図 23. Histogram – 20 mA, Gain = 1, SPS = 1000, STD = 150.07 ENOB = 16.77

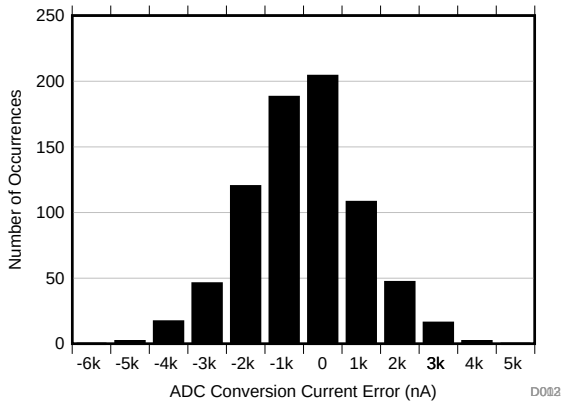


図 24. Histogram – 20 mA, Gain = 2, SPS = 20, STD = 35.07 ENOB = 18.87

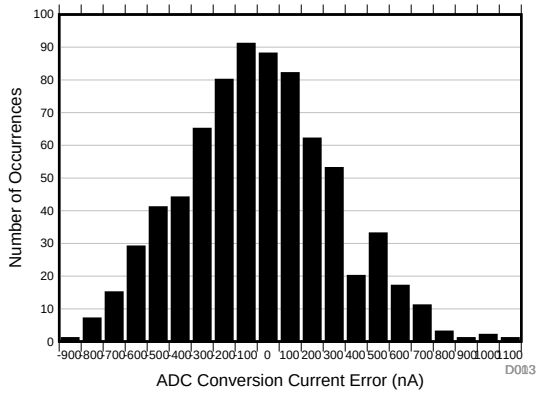
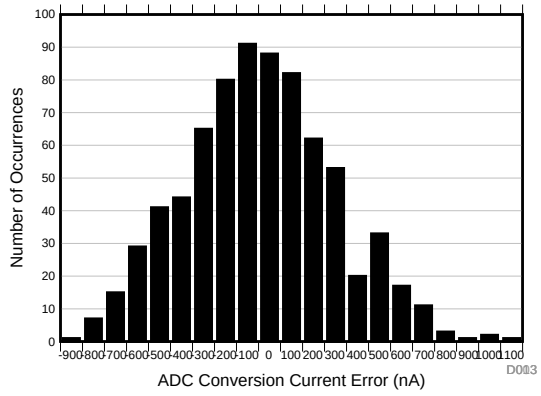


図 25. Histogram – 20 mA, Gain = 2, SPS = 1000, STD = 168.73 ENOB = 16.60



With the obtained effective bits and noise-free bits, the input referred noise can be calculated by taking the range of the input range (dependent on gain) into account (式 4 and 式 5). The full-scale range is –2.5 V to 2.5 V = 5 V.

$$\text{RMS noise } (\mu V_{RMS}) = \frac{\left(\frac{\text{Full} - \text{scale range}}{\text{Gain}}\right)}{2^{\text{effective bits}}} \quad (4)$$

$$\text{Peak noise}\left(\mu V_{PP}\right) = \frac{\left(\frac{\text{Full}-\text{scale range}}{\text{Gain}}\right)}{2^{\text{noise}-\text{free bits}}} \quad (5)$$

表 4 and 表 5 summarize the device noise performance on different current situation without any load variation. Data are representative of typical noise performance at T_A = 25°C using the internal 2.048-V reference. Because the actual performance data may be affected by measurement techniques and environmental variables, these measurement results are presented for reference and may differ from actual field measurements.

表 4. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V

	GAIN (PGA ENABLE)	
4-mA Data Rate (SPS)	1	2
20	19.56 (16.84)	19.55 (16.83)
1000	16.82 (14.10)	16.77 (14.05)
12-mA Data Rate (SPS)	1	2
20	19.39 (16.66)	19.03 (16.31)
1000	16.74 (14.02)	16.52 (13.80)
20-mA Data Rate (SPS)	1	2
20	19.33 (16.61)	18.86 (16.14)
1000	16.77 (14.04)	16.60 (13.87)

表 5. Noise in μV_{RMS} (μVPP) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V

	GAIN (PGA ENABLE)	
4-mA Data Rate (SPS)	1	2
20	5.28 (34.82)	2.66 (17.56)
1000	35 (230)	18.3 (121)
12-mA Data Rate (SPS)	1	2
20	5.96 (39.3)	3.81 (25.18)
1000	37.3 (246)	21.7 (143)
20-mA Data Rate (SPS)	1	2
20	6.21 (41)	4.28 (28.3)
1000	36.6 (242)	20.6 (136)

This reference design measures the noise performance in load transient (4 mA to 20 mA). 図 26 through 図 31 show the noise performance of ADC. 表 6 through 表 9 show the detailed results. As the tables show, the overvoltage does not significantly affect the overall ADC performance, due to wide V_{IN} LDO with high PSRR.

図 26. Histogram – 4 mA, Gain = 1, SPS = 20, STD = 20.96 ENOB = 19.61

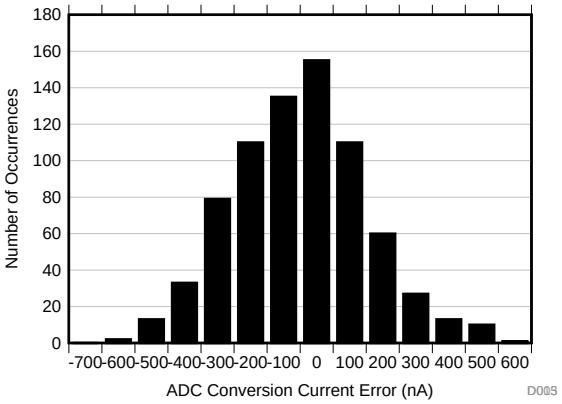


図 27. Histogram – 4 mA, Gain = 1, SPS = 1000, STD = 141.87 ENOB = 16.85

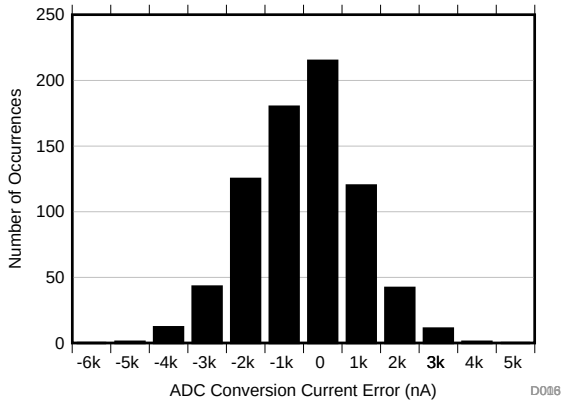


図 28. Histogram – 12 mA, Gain = 1, SPS = 20, STD = 25.24 ENOB = 19.34

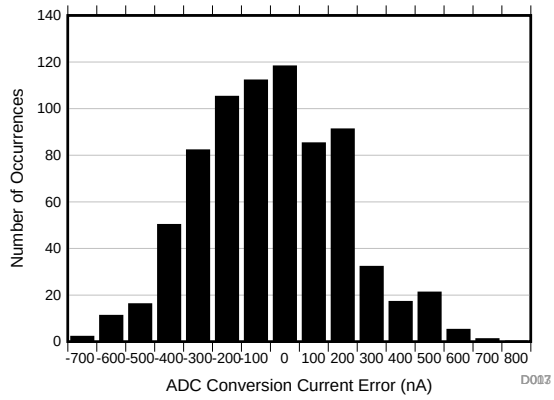


図 29. Histogram – 12 mA, Gain = 1, SPS = 1000, STD = 163 ENOB = 16.65

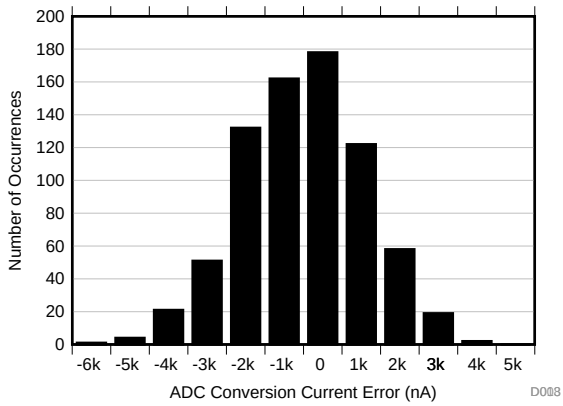


図 30. Histogram – 20 mA, Gain = 1, SPS = 20, STD = 24.02 ENOB = 19.41

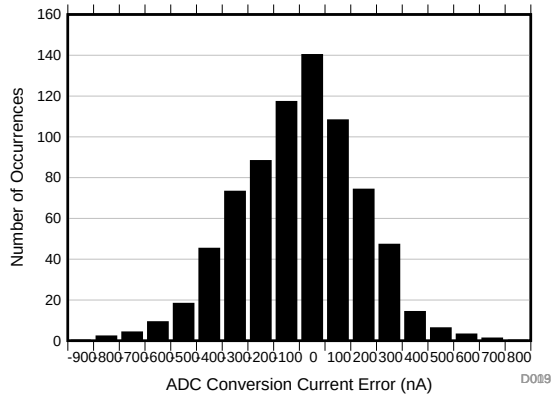


図 31. Histogram – 20 mA, Gain = 1, SPS = 20, STD = 161.22 ENOB = 16.67

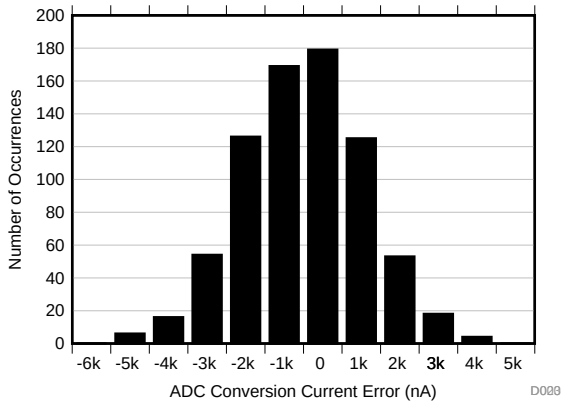


表 6. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V, Load Variation From 4–20 mA

	GAIN (PGA ENABLE)
4-mA Data Rate (SPS)	1
20	19.61 (16.89)
1000	16.85 (14.13)
12-mA Data Rate (SPS)	1
20	19.34 (16.62)
1000	16.65 (13.93)
20-mA Data Rate (SPS)	1
20	19.41 (16.69)
1000	16.67 (13.94)

表 7. Noise in μV_{RMS} (μVPP) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V, Load Variation From 4–20 mA

	GAIN (PGA ENABLE)
4-mA Data Rate (SPS)	1
20	5.12 (33.8)
1000	34.6 (229)
12-mA Data Rate (SPS)	1
20	6.16 (40.7)
1000	39.8 (263)
20-mA Data Rate (SPS)	1
20	5.87 (38.7)
1000	39.4 (260)

表 8. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V, Short Circuit

4-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	19.61 (16.89)
12-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	19.34 (16.62)
20-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	19.41 (16.69)

表 9. Noise in μV_{RMS} (μVPP) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, I_{IN} = 4 mA, 12 mA, 20 mA and Internal V_{REF} = 2.048 V, Short Circuit

4-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	5.39 (31.47)
12-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	5.91 (31.26)
20-mA Data Rate (SPS) = 20	Gain (PGA enable) = 1
	5.77 (31.32)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010048.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010048.

4.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010048.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010048.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010048.

5 Software Files

To download the software files, see the design files at TIDA-010048.

6 Related Documentation

1. Texas Instruments, Reducing System Cost, Size and Power Consumption in Isolated Data Acquisition Systems Using ADS122U04 Tech Note
2. Texas Instruments, *TVS3300 33-V Flat-Clamp Surge Protection Device Data Sheet*
3. Texas Instruments, LM5180 65-V_{IN} PSR Flyback DC/DC Converter With 100-V, 1.5-A Integrated Power MOSFET
4. Texas Instruments, ADS122U04 24-Bit, 4-Channel, 2-kSPS, Delta-Sigma ADC With UART Interface Data Sheet
5. Texas Instruments, TPS2662x 60-V, 800-mA Industrial eFuse With Integrated Input and Output Reverse Polarity Protection Data Sheet
6. Texas Instruments, ISO772x High-Speed, Robust EMC, Reinforced Dual-Channel Digital Isolators Data Sheet
7. Texas Instruments, TPS7A470x 36-V, 1-A, 4-µVRMS, RF LDO Voltage Regulator Data Sheet
8. Texas Instruments, TVS3300 33-V Flat-Clamp Surge Protection Device Data Sheet
9. Texas Instruments, SN74LV4052A Dual 4-Channel Analog Multiplexers and Demultiplexers Data Sheet

6.1 商標

E2E is a trademark of Texas Instruments.
Altium Designer is a registered trademark of Altium LLC or its affiliated companies.
すべての商標および登録商標はそれぞれの所有者に帰属します。

6.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

7 About the Author

BEN SU is a Field Application Engineer at Texas Instruments. Ben has mixed-signal IC design experience in TSMC fabrication and focused on wireless power IC and SAR ADC during his study career. Ben earned his masters degree in electrical engineering from National Chiao Tung University in Hsinchu, Taiwan.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。