参考資料

デザイン・ガイド: TIDA-010131
レーダーおよびワイヤレス 5G テスタ用のマルチチャネル RF トランシーバへのクロック供給のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

フェーズドアレイ・レーダー、ワイヤレス通信テスタ、電子兵器などの高速最終製品向けのアナログ・フロント・エンドには、同期されたマルチトランシーバ・シグナル・チェーンが必要です。各トランシーバ・シグナル・チェーンは高速な A/D コンバータ (ADC)、D/A コンバータ (DAC)、クロック・サブシステムを搭載しています。このクロック・サブシステムは高精度な遅延調整機能を使用して低ノイズのサンプリング・クロックを提供し、最小のチャネル間スキューを達成するとともに、信号対雑音比 (SNR)、スプリアス・フリー・ダイナミック・レンジ (SFDR)、IMD3、実効ビット数 (ENOB) などのシステム性能を最適化します。このリファレンス・デザインでは、AFE7444 EVM を使用して、マルチチャネル JESD204B クロックの生成とシステム性能を示します。最高 2.6GHz の無線周波数に対応する 6GSPS/3GSPS の DAC/ADC クロックにより、チャネル間スキューを 10ps 以内に抑えるとともに、AFE7444 のデータシート仕様に相当する SNR や SFDR などのシステム性能を実現します。

リソース

TIDA-010131	デザイン・フォルダ
AFE7444EVM、AFE7444	プロダクト・フォルダ
LMX2594、LMK04828、LMK61E2	プロダクト・フォルダ
TSW14J56EVM、TSW14J57EVM	プロダクト・フォルダ

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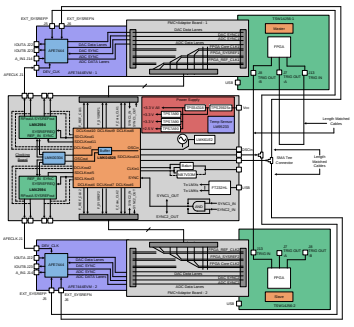
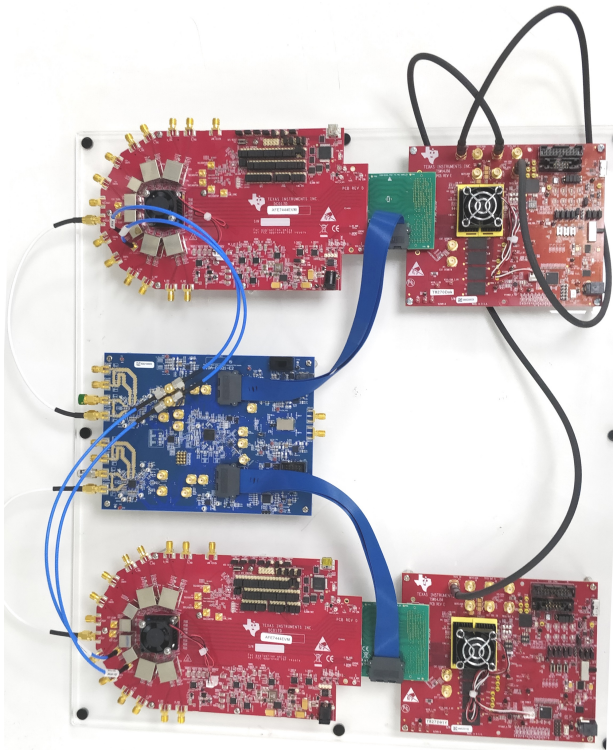


特長

- 8T8R（8 送信 / 8 受信）RF サンプリング・アナログ・フロント・エンド向け JESD204B 準拠クロック・ソリューション
- 複数の RF AFE トランシーバに対応するデジタル機能同期
- 14 ビット RF サンプリング AFE 向けの、位相ノイズが低いクロック生成
- 約 500fs 単位で位相遅延の微調整に対応し、複数のデバイス間で位相同期を実現
- TI の高速コンバータ・カードとキャプチャ・カード (AFE7444EVM、TSW14J56EVM、TSW14J57EVM) をサポート

アプリケーション

- フェーズドアレイ・レーダー
- ワイヤレス通信テスト機器
- 電子兵器

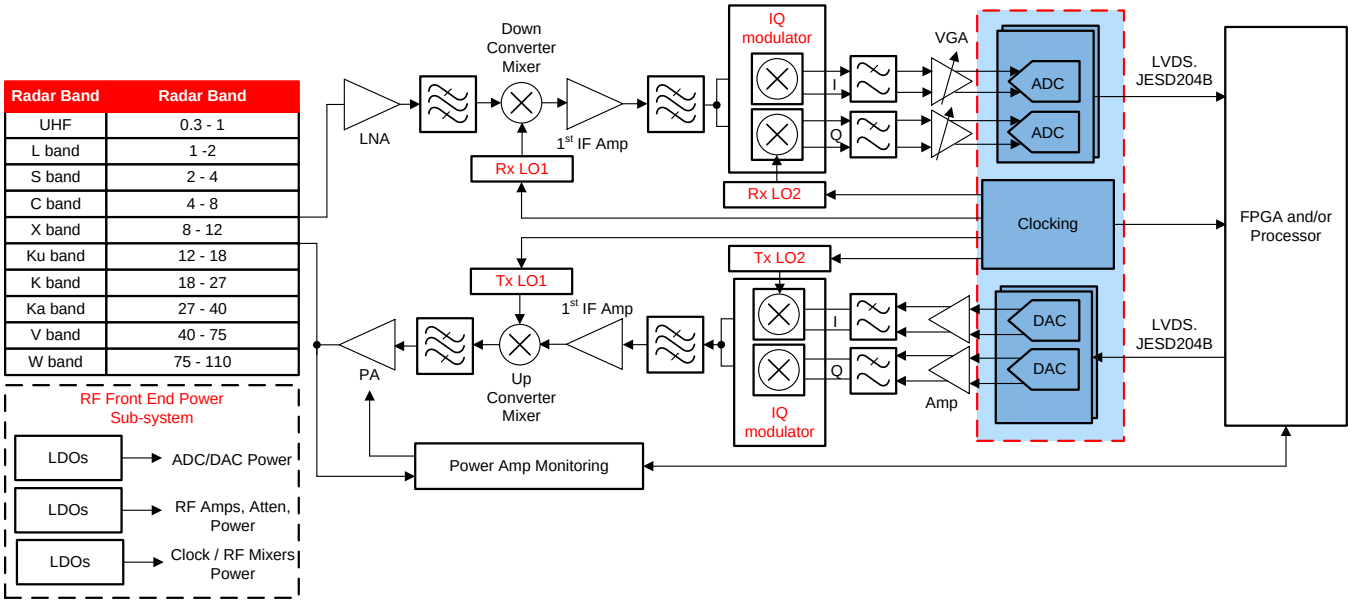


1 System Description

Multichannel, high-speed applications such as RADAR and wireless communication testers have a critical clocking requirement to achieve higher performance (high SNR, SFDR, IMD3, and so forth) of the analog front end and low analog channel-to-channel skew.

図 1 shows the subsystem block diagram of phase-array RADAR that consists of up and down converters, high-speed AFE, clocking, and calibration subsystems. The subsystem contains a high number of transceivers which need high dynamic range, wide transmitter and receiver bandwidth, low latency, and good synchronization between the transceiver channels. This design focuses on the high-speed data converters synchronization and clocking solution for this requirement. The signal chain solution based on the AFE7444 RF-sampling transceiver, LMX2594, and LMK04828 devices are able to achieve optimum performance for phased-array radar applications.

図 1. RADAR RF Front End Subsystem



Wireless tester equipment uses multichannel transceivers for testing cellular and multiple-input, multiple-outputs (MIMO) devices. Wireless testers require high dynamic range and wideband transceivers to test 3G, LTE and later wireless standards compliant equipment. The AFE7444 is well suited for the multichannel transceiver requirements of the wireless testers. The clocking solution described in this design supplements a high-performance signal chain solution based on multiple AFE7444 analog front ends to achieve a low time skew between channels providing both high dynamic range and wide bandwidth transmitters and receivers.

Electronic warfare equipments as electronic protection, security, and attack also require a multichannel transceiver system with wide dynamic range and higher instantaneous bandwidth for higher range and speed. The AFE7444 is a good fit for the multichannel transceiver requirements of the EW application, and this design shows the synchronization of multiple devices.

This reference design demonstrates the multichannel clock generation for two AFE7444s to synchronize them and make an 8-transmit and 8-receive (8T8R) system that meets phased-array RADAR, wireless communication tester, and electronic warfare application requirements.

1.1 Key System Specifications

The objective of the design is to demonstrate the high-speed clocking solution for a multichannel, RF-sampling transceiver signal chain. This design focuses on the clock solution performance impact on multichannel synchronization, SNR, SFDR, and IMD3 with two AFE7444EVMs. The data generation and capture is done by the TSW14J56/57EVM, which is interfaced with the AFE7444EVM using the FMC+ adapter card. 表 1 lists the key system-level specifications for the multichannel signal chains from the clocking solution perspective.

表 1. Key Specifications

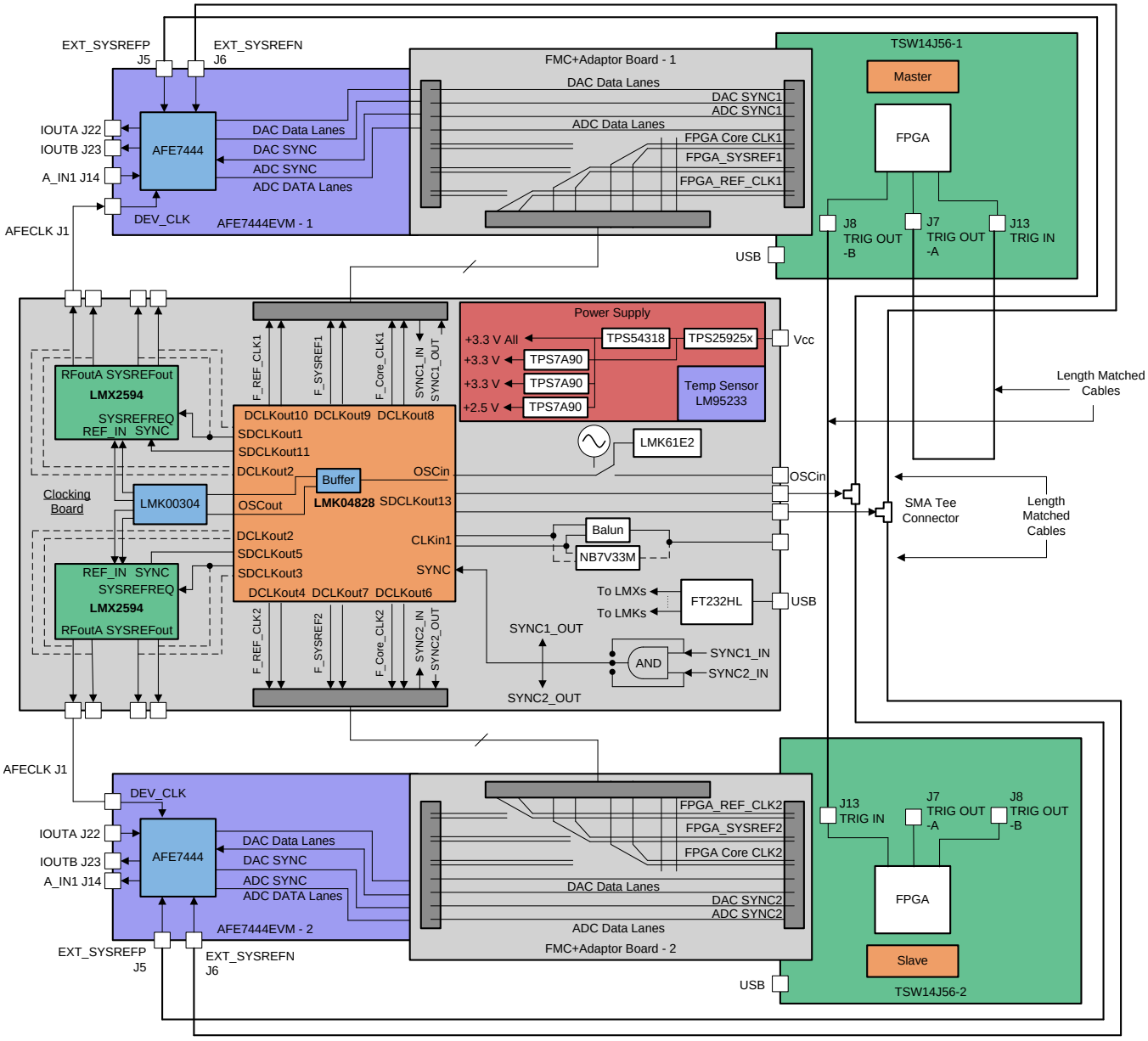
PARAMETER	SPECIFICATION	CONDITIONS
Transmitter (mode5, interpolation 8)		
SFDR (dBc) for 0 – FDAC/2 BW	60	890-MHz DAC output signal
	55	1800-MHz DAC output signal
	56	2100-MHz DAC output signal
	58	2600-MHz DAC output signal
SFDR (dBc) for Fout ±250-MHz BW	84	890-MHz DAC output signal
	74	1800-MHz DAC output signal
	75	2100-MHz DAC output signal
	74	2600-MHz DAC output signal
IMD3 (dBc)	69	890-MHz ± 10-MHz DAC output signal
	69	1800-MHz ± 10-MHz DAC output signal
	68	2100-MHz ± 10-MHz DAC output signal
	68	2600-MHz ± 10-MHz DAC output signal
Analog output channel-to-channel time skew	Less than 10 ps	All DAC output signal (mode4, interpolation 12)
Receiver (mode9, decimation 16)		
SNR (dBFS)	63.3	1900-MHz ADC input signal
	61.2	2600-MHz ADC input signal
Analog input channel-to-channel time skew	Less than 10 ps	All ADC input signal (mode9, decimation 12)

2 System Overview

2.1 Block Diagram

図 2 shows the block diagram of the proposed multichannel, phase-synchronized clock solution interface with multiple RF-sampling transceivers. The AFE7444EVM is interfaced with the TSW14J56EVM data capture board through the FMC+ adaptor card. Device clock and SYSREF to the AFE7444EVMs are provided by LMX2594 and LMK04828 respectively using the length-matched cables.

図 2. Block Diagram of TIDA-010131



In this solution, two LMX2594 devices receive an OSCin input signal from an LMK61E2 through an LMK04828 and an LMK00304 and generate the two in-phase device clocks at 5898.24 MHz for the AFE7444EVMs. Because the AFE7444 has a requirement of a DC-coupled SYSREF for JESD204B compliant clocks, the LMK04828 is used to generate the SYSREF for AFE7444 as the LMX2594 cannot generate DC-coupled SYSREF outputs. The LMK04828 also generates two pairs of in-phase FPGA reference clocks and SYSREF for the TSW14J56EVM capture cards and also provides the SYNC signal to the two LMX2594s to synchronize them to each other.

In this solution, SYSREF to the two AFE7444s is provided through a single port. Hence, to meet the SYSREF setup and hold time in both AFEs, the device clocks require phase adjustment to get a low channel-to-channel skew between two AFEs.

2.2 Design Considerations

The JESD204B-compliant, multichannel clock design for multiple RF transceivers is based on two design goals: low-phase noise device clock generation and a scalable, multichannel clock solution with provisions for phase-alignment trimming. This section describes the design considerations of various functional blocks that help to achieve these system design goals and synchronize multiple AFE7444EVMs.

2.2.1 Multiple JESD204B RF Transceiver Synchronization Challenges

In a JESD204B system environment, data transfer from the JESD204B RX block to the TX block happens in multiframes. These multiframes are aligned to the edges of the local multiframe clock (LMFC), which is internal to the JESD204B RX and TX block. The concept of the LMFC and the associated alignment requirements are critical in applications that require deterministic latency and multiple device synchronization. To achieve deterministic latency, multiple device synchronization, or both is to ensure that the LMFC of each JESD204B device in the JESD204B system environment are aligned. The LMFC of each JESD204B devices is aligned through the SYSREF signal, which is globally generated from the common source throughout the JESD204B system. Once the LMFCs of all devices in the system are aligned, the devices are synchronized and data transfer happens at the same rate and at the same instant.

High-speed applications like RADAR, electronic warfare, and WCTE, where multiple channels are needed to achieve higher data rates or multiple input and multiple outputs (MIMO), require a multichannel device to reduce system size, complexity, and cost. The AFE7444, a JESD204B-compliant device, supports 4-transmit and 4-receive signal chains and is a good fit for these multichannel systems with the provided clock solution. A large number of AFE7444 devices can be used in such systems requiring multiple device synchronization.

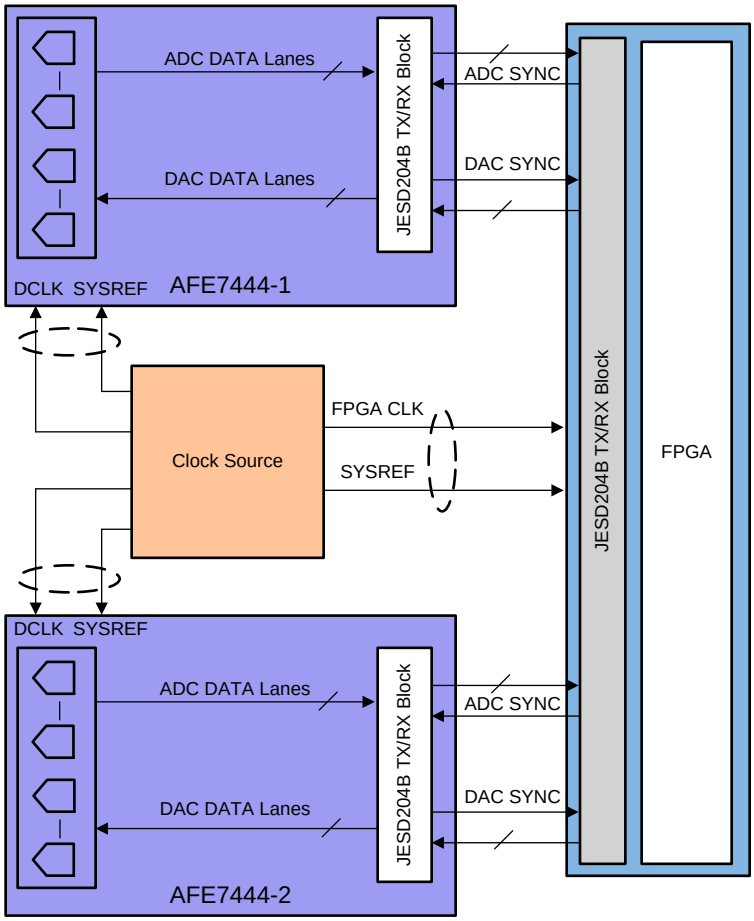
The key clocking challenges in multi-RF transceiver systems to minimize channel-to-channel skew include:

1. Synchronization of device clocks for RF transceivers
2. Synchronization of digital functions across RF transceivers

図 3 shows the typical setup for multiple JESD204B TX/RX device synchronization. For synchronization, the clock source requires:

1. Phase-align device clocks / sampling clocks (DCLK) at each AFE7444 device
2. In-phase SYSREF to each DCLK to meet SYSREF setup and hold time of the AFE7444
3. In-phase FPGA CLK and FPGA SYSREF, if using multiple FPGAs in a system

図 3. Typical Setup for Multi-Device JESD204B Clocks for AFE7444 Devices



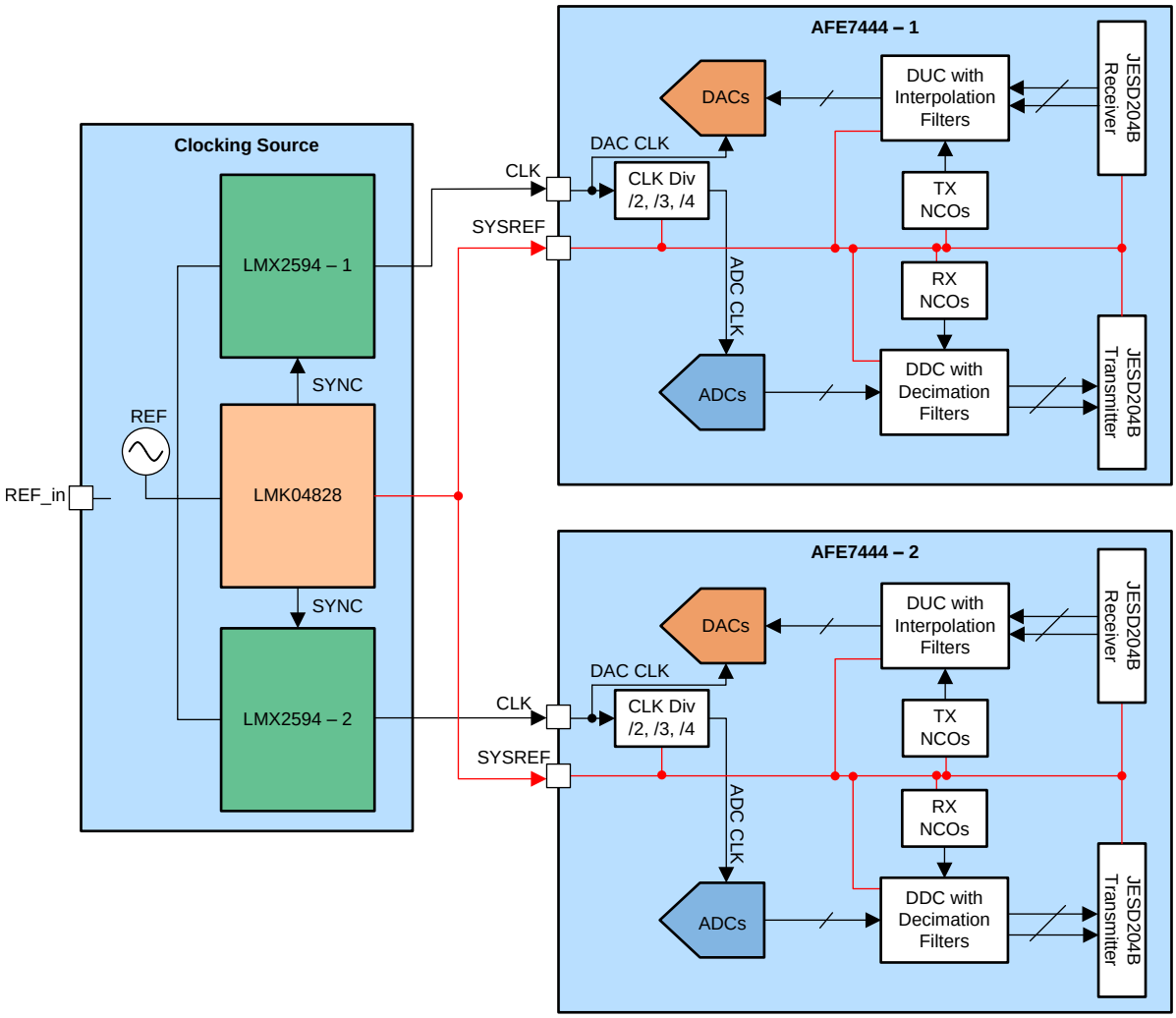
AFE clock, such as an ADC sampling clock, frame clock, or LMFC, are generated from the common DCLK. Hence the DCLK phase is critical to each data converter for multiple synchronized systems.

2.2.2 AFE7444 Digital Functions Synchronization

To synchronize the multiple AFE7444 devices, apart from the synchronized JESD204B-complaint clocks, AFE7444's digital functions must also be synchronized in the multichannel system. Digital functions of the AFE7444 include NCOs, DUC with interpolation filters, DDC with decimation filters, and JESD204B section. All of these digital functions have various options for synchronization using SPI, GPIOs and SYSREF. In multichannel systems, where all devices are programmed individually, SYSREF is the only feasible optionfor synchronization.

図 4 shows the interface diagram of the SYSREF signal in multiple devices to synchronize the digital functions of AFE7444.

図 4. Interface Diagram of the SYSREF Signal With Digital Functions of AFE7444



The AFE7444 requires a common clock for the DAC and the ADC of the device, which is the same as the DAC clock. The ADC clock is distributed within a device by the DAC clock using the clock divider. For multi-device ADC clock synchronization, the clock divider (Fdac/Fadc) resets through SYSREF.

For synchronizing the NCOs in multiple devices, NCO frequency should be integer multiple of SYSREF frequency and also reset through SYSREF. The AFE7444 requires a DC-coupled SYSREF with 0.5-V, commonmode voltage to operate properly in a system.

For more details, see the DAC3xJ8x Device Initialization and SYSREF Configuration application report on DAC3xJ8x device initialization and SYSREF configuration, which has a similar SYSREF requirement as the AFE7444.

2.2.3 Multichannel Phase Synchronized JESD204B Compliant Clocks

To synchronize the multiple RF transceivers, channel-to-channel skew becomes an important design consideration. Clock jitter and phase mismatch lead to deviation from the ideal sampling instant of a channel and thereby, results in channel-to-channel skew. The LMX2594 synthesizers used in this design have an excellent phase-noise performance at high frequencies. Additionally, because of the phase synchronization feature of the LMX2594, the device helps in improving the channel-to-channel skew.

図 5. Block Diagram of Multichannel Clocking Board

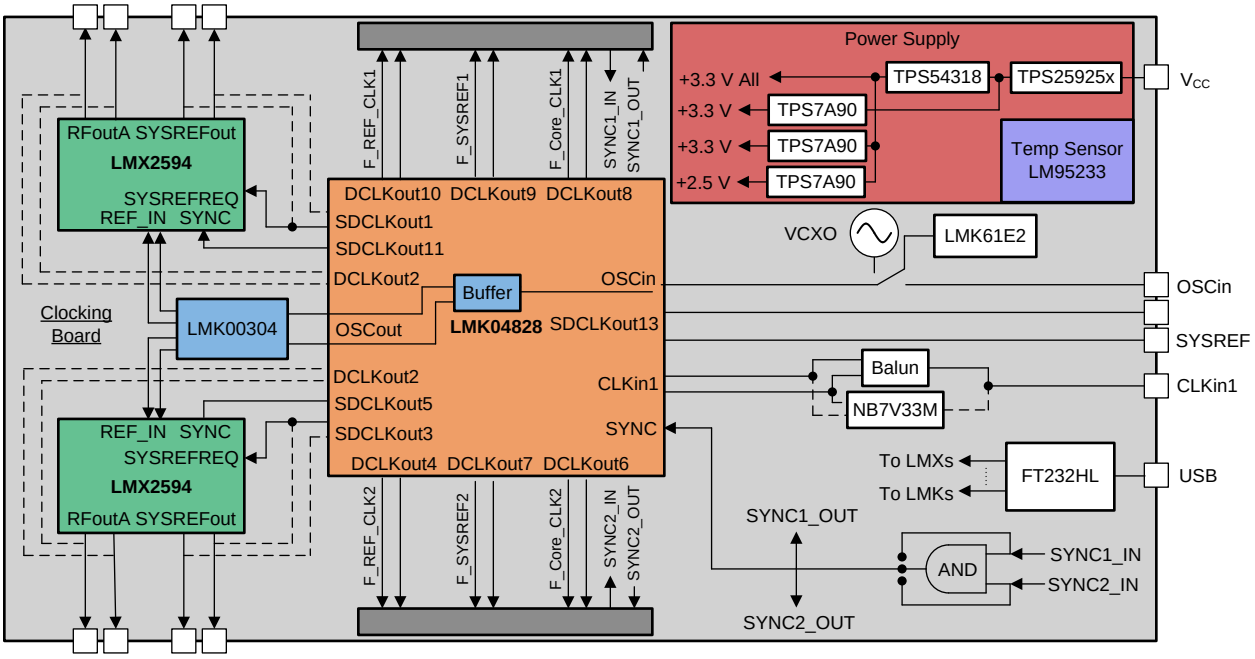
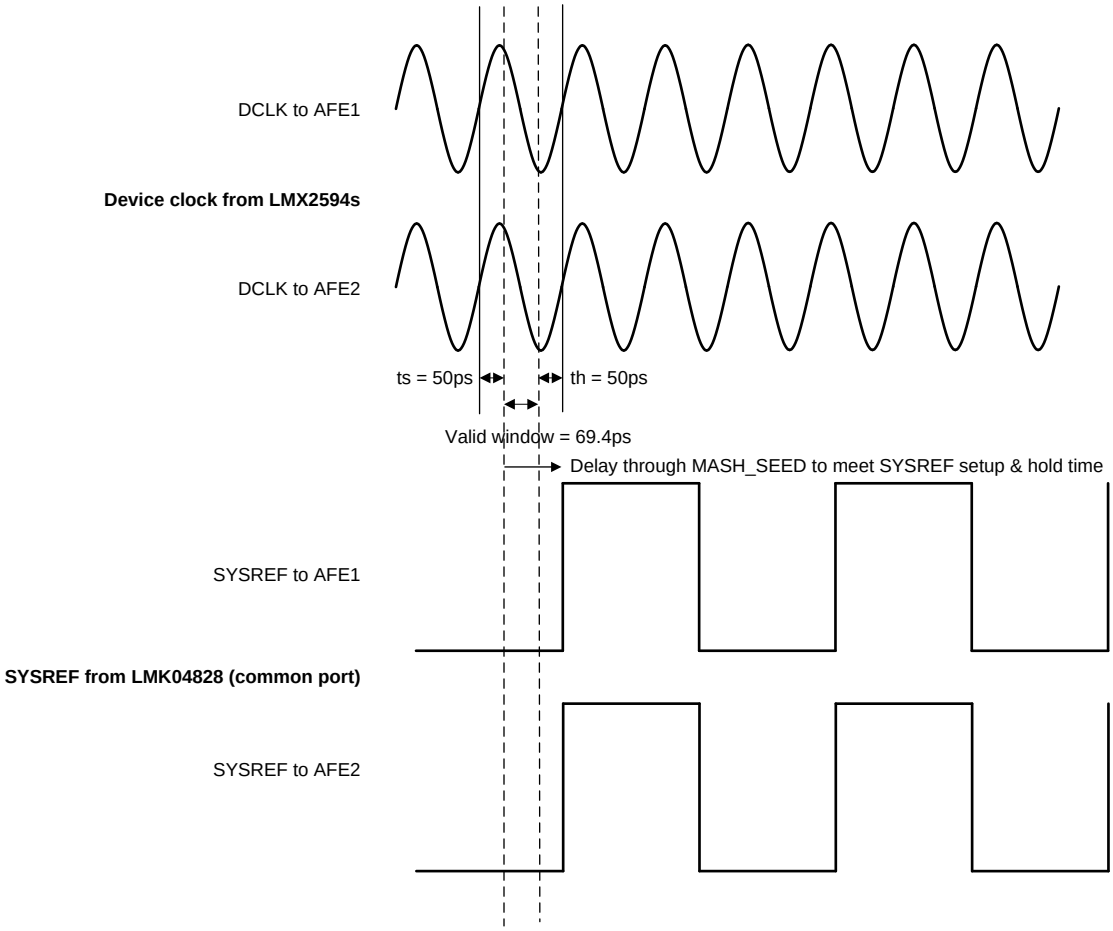


図 5 shows the block diagram of multichannel clocking board. A common reference frequency is generated by the LMK61E2 and is provided to the LMK04828 at the OSCin input. The LMK04828 on this design is used to provide an FPGA reference clock and SYSREF to the TSW14J56/57 capture card through the FMC+ adapter board and SYSREF to AFE7444EVMs. The LMK04828 is configured in PLL mode to phase synchronize OSCin and the remaining generated clocks.

To generate the phase-synchronized device clocks to AFE7444EVMs, a common reference frequency is input to the REF_in of the two LMX2594 synthesizers using LMK00304 and the SYNC signals from LMK04828. As shown in 図 2, SYSREF and the device clock to the AFE7444EVMs are provided through LMK04828 and LMX2594, respectively. SYSREF to the AFEs are provided through a common port of the LMK04828 using the T splitter. For multi-device JESD204B synchronization, device clocks should be phase aligned and meet the SYSREF setup and hold time of the AFE7444 device.

図 6 shows the waveform of the device clocks and SYSREF to both AFE7444EVMs. As the device clock and SYSREF are generating from different devices, they are not phase aligned. In this design, the device clock of the AFE7444 is 5898.24 MHz and SYSREF setup and hold time of the AFE7444 are 50 ps each. With this, the valid window for meeting the setup and hold time is approximately 69 ps, which is less than the step size (150 ps) of SYSREF from the LMK04828. Hence, phase delay must be provided in device clocks, which is done by the MASH_SEED value in the LMX2594. Each LMX2594 device may require tuning for the MASH_SEED delays to achieve in-phase generated clocks and meet the setup and hold time of the SYSREFs.

図 6. Device Clocks and SYSREFs Alignment



Reference frequency to the clocking board can be any standard frequency such as 10 MHz, 100 MHz, and so forth as per the operating clock frequency. In this design, the AFE7444 performance and synchronization test performed at 5898.24 MHz on the device clock is done to show the comparison with the internal PLL clock mode. To generate the synchronized device clock, the LMX2594 operates in integer PLL mode along with SYNC enable. During this mode, the N-divider value is limited at 28 for higher MASH_Order. Hence, the optimized input reference frequency is 61.44 MHz. The input reference frequency of 61.44 MHz is provided to the LMX2594 devices by the LMK61E2 using LMK04828. The phase-detector frequency also changes to 61.44 MHz, and the new loop filter configuration is shown in 表 2.

表 2. LMX2594 Loop Filter Component

COMPONENTS	VALUES
C62 and C95	2.7 nF
C60 and C93	82 nF
C59 and C92	Open
C58 and C91	1.8 nF
R96 and R129	82 ohm
R95 and R128	0 ohm
R94 and R127	82 ohm

2.3 Highlighted Products

2.3.1 AFE7444

The AFE7444 is a quad-channel wideband, RF-sampling transceiver based on 14-bit, 9-GSPS DACs and 14-bit, 3-GSPS ADCs. The AFE7444 operates up to 5.2-GHz radio frequencies. The AFE7444 has 8 JESD204B-compatible SerDes transceivers running up to 15 Gbps. The devices have up to two DUCs per TX channel and two DDCs per RX channel, with multiple interpolation and decimation rates and digital quadrature modulators and demodulators with independent, frequency-flexible NCOs. Each ADC input path includes a DSA and RF and digital power detectors. Flexible decimation options provide optimization of data bandwidth. The DAC signal paths support interpolation and digital up conversion options that deliver up to 800 MHz of signal bandwidth. The differential output path includes a digital step attenuator (DSA), which provides tuning of output power.

2.3.2 LMX2594

The LMX2594 is a high-performance, wideband RF PLL with integrated VCO that supports a frequency range from 10 MHz to 15 GHz without using an internal doubler. The device supports both fractional-N and integer-N modes, with a 32-bit fractional divider allowing fine frequency selection. The high-performance PLL with a figure of merit of –236 dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter. The device's integrated noise of 45 fs for a 7.5-GHz output makes the device an ideal low-noise source. The device accepts input reference frequency up to 1.4 GHz, which combined with frequency dividers and a programmable low-noise multiplier allows flexible frequency planning. The high-speed N-divider does not have a predivider, thus significantly reducing the amplitude and number of spurs. The additional programmable low-noise multiplier mitigates the impact of integer boundary spurs. In fractional-N mode, the device can adjust the output phase by a 32-bit resolution. For applications that need fast frequency changes, the device supports a fast calibration option, which takes less than 20 μs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-noise clock source for high-speed data converters. Fine delay adjustment (9-ps resolution) is provided in this configuration to account for delay differences of board traces. This device uses a single 3.3-V supply and has integrated LDOs that eliminate the need for onboard low-noise LDOs.

2.3.3 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator for JESD204B systems. LMK04828 has 14 clock outputs from PLL2 that can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. LMK04828 supports a range of two VCOs that are 2370 to 2630 MHz and 2920 to 3080 MHz. The LMK04828 also supports a distribution mode, which accepts the high-frequency reference signal and distributes it to all 14 clock outputs without adding a PLL noise.

3 Hardware, Software, Testing Requirements, and Test Results

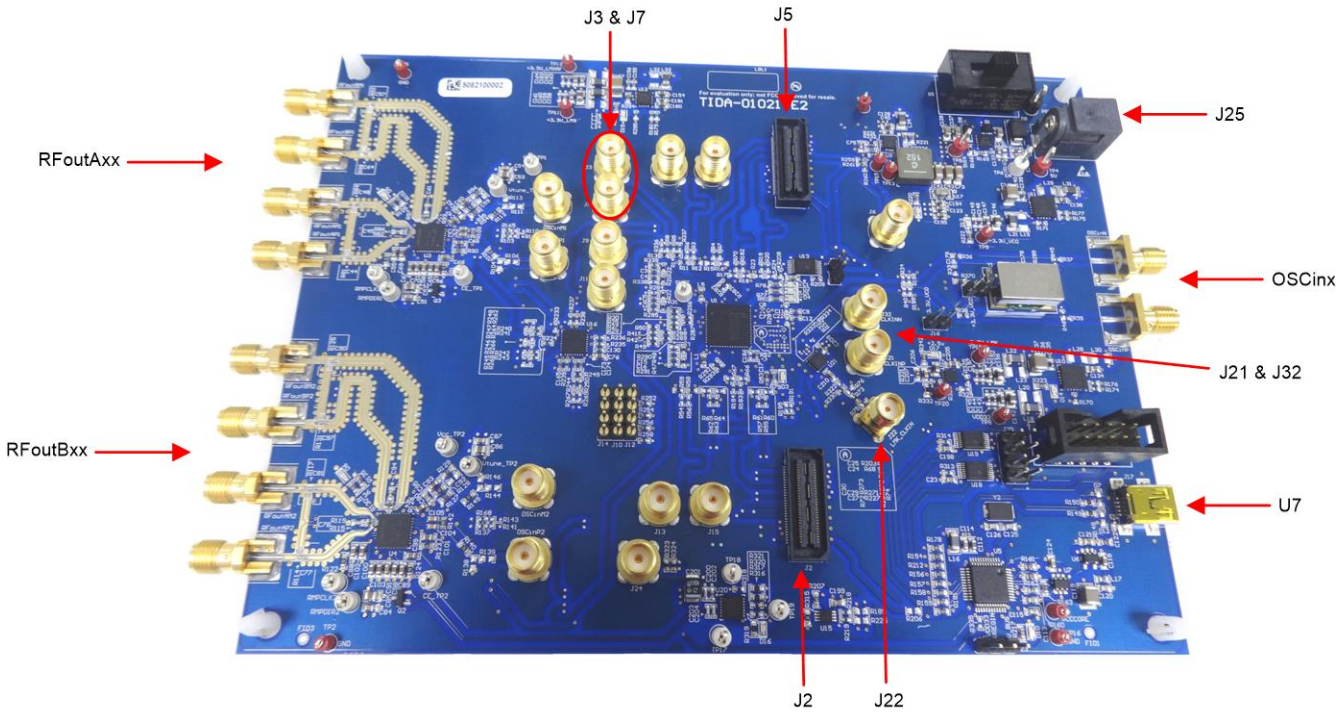
3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Clocking Board Setup

図 7 shows the multichannel clocking board.

図 7. Multichannel Clocking Board Hardware



- Power:
  - Power supply connector J25: This connector is used to connect the power supply. Set the power supply to 5 V with a 2-A current limit.
- Input reference signals:
  - Option 1: The onboard VCXO Y1 is powered on using the jumper J8 and outputs a 100-MHz signal to the LMK04828 OSCin* pin input. While using Y1, disconnect the clock inputs from LMK61E2 (U2) and external reference by removing R36 and R38. At the same time, isolate the power supply to U2 by removing the jumper J16.
  - Option 2: The onboard reference LMK61E2 (U2) is powered on using the jumper J16 and factory programmed to generate a 156-MHz LVDS output. U2 can be programmed to generate different clock frequencies using the I^2C interface. While using U2, disconnect the clock inputs from Y1 and external reference by removing C179, R37, and R39, then place R36 and R38. Isolate the power supply to Y1 by removing the J8.
  - Option 3: Connect the external reference to external OSCinP and OSCinN connectors. While

connecting external reference, disconnect the Y1 and U2 connection by removing C179, R45, and R46, and place R36 and R38. Disconnect the power supply of Y1 and U2 by removing jumpers J8 and J16.

  - Option 4: Use one of the previous options, when LMK04828 works in PLL mode. When LMK04828 is operating in distribution mode, connect the external reference to external connector J22. While operating in distribution mode, power down the Y1 and Y2 by removing jumpers J8 and J16.

- Input sync signal:
  - Connect the external sync signal at external J21 and J32 connectors to reset the LMK04828 dividers.
- Output signals:
  - RFoutAP1, RFoutAM1, RFoutAP2, and RFoutAM2 connectors generate the DCLK and are connected to AFE7444EVMs as an external sampling clock. Replace R82, R86, R115, and R119 with a 1-nH inductor to improve the LMX2594 output power at DCLK.
  - RFoutBP1, RFoutBM1, RFoutBP2, RFoutBM2, J3 and J7 connectors generate the low-frequency SYSREF signals.
  - Connectors J2 and J5 generate the FPGA CLKs and SYSREFs for two TSW14J5x capture cards.
- Programming interface:
  - Connect the USB mini cable to the onboard USB connector U7 and test the PC to program the clocking board devices using the High Speed Data Converter (HSDC) Pro Software GUI.

3.1.1.2 FMC+ to FMC Adapter Board Setup

The FMC+ to FMC adapter board provides the FPGA clocks to the TSW14J5x capture card from the clocking board or AFE7444EVM along with the data lanes directly connected from the AFE7444EVM to the capture card. Follow the schematic to connect the FPGA clocks and SYSREFs from the clocking board.

3.1.1.3 AFE7444EVM Setup

See the AFE74xxEVM User's Guide for the AFE7444EVM hardware setup procedure.

The AFE7444EVM has both internal PLL as well as external options for clocking the AFE. In external clock mode, feed the external clock signal at the AFECLK (J1) connector and SYSREF at the J5 and J6 connector from the clocking board. To enable external SYSREF from the clocking board, remove R12 and R13 and place R11 and R14. Also remove the jumpers from J12 to remove the spurs generated from the FTDI chip at fast SPI lines. Remove L1 and L2 and replace R322 and R323 with 0-ohm resistors to reduce the AFE7444 EVM click amplitude requirement.

3.1.1.4 TSW14J56EVM Setup

This design requires two TSW14J56EVMs to establish a JESD204B link with two AFE7444EVMs and to synchronize both JESD204B links. Both TSW14J56EVMs are set up in master and slave mode to ensure the alignment of the JESD204B link and input and output data alignment individually.

For more information, see the TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide and the High Speed Data Converter Pro GUI User's Guide.

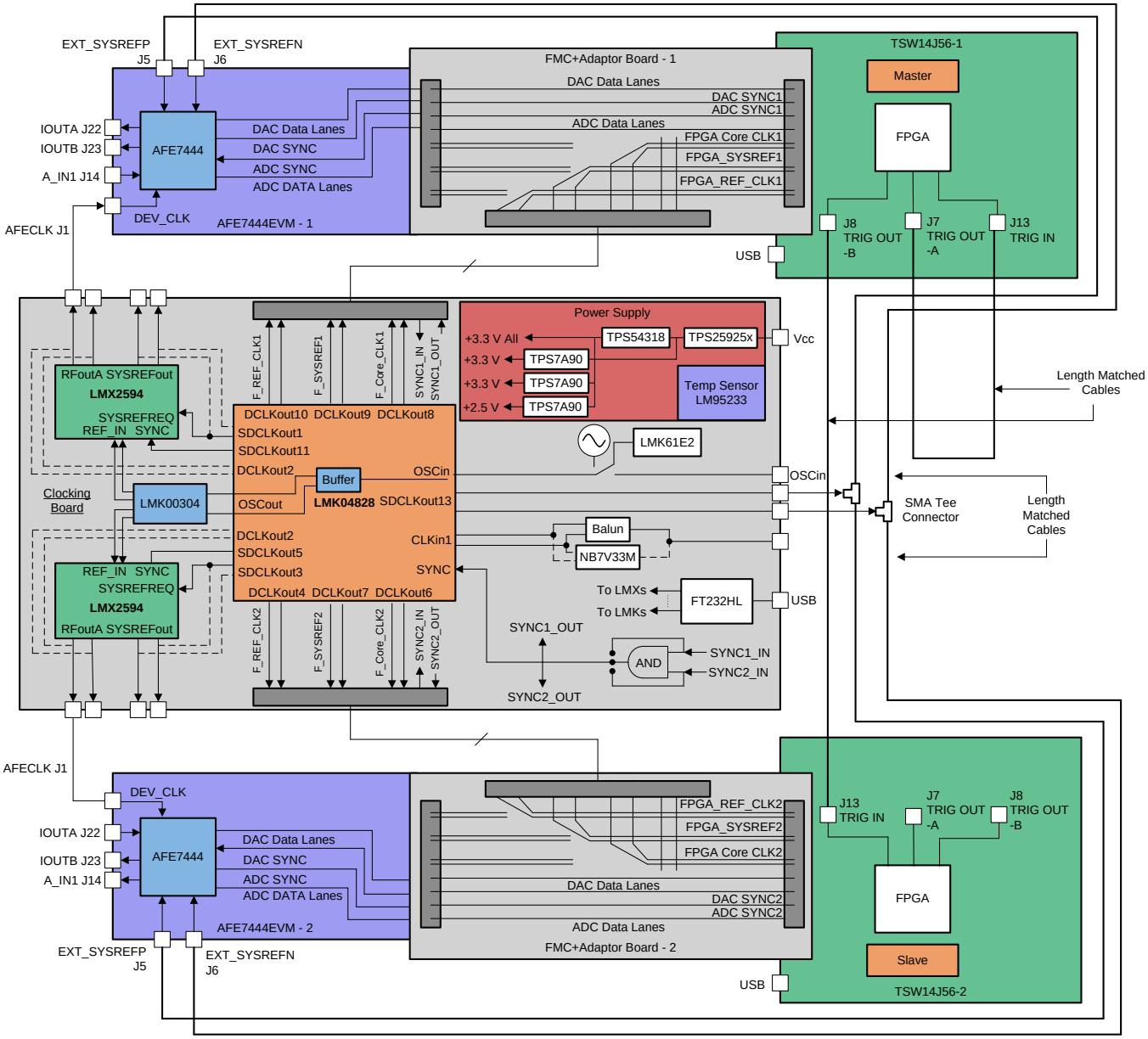
3.1.1.5 TSW14J57EVM Setup

See the TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide for the TSW14J57EVM hardware setup procedure.

3.1.1.6 Hardware Setup of Multiple Transceiver Synchronization

The proposed clocking solution is interfaced with the two AFE7444EVM and two TSW14J56EVM capture cards to show the synchronization between multiple AFE7444 devices. 図 8 shows the overall block diagram of the multiple transceiver synchronized system.

図 8. Block Diagram of the Multiple Transceiver Synchronized System



SYSREF signals to the AFE7444EVMs are provided through the LMK04828, and high-frequency AFECLK signals are provided through the LMX2594s. Ideally, the LMX2594 can operate up to 15 GHz with around 7-dBm output power. The AFE7444EVM has a requirement of +20 dBm at the 9-GHz sampling clock, which the LMX2594 is not capable of, but for 6-GHz sampling frequency, the power requirement is reduced. In this design, synchronization performance is tested at a 5898.24-MHz sampling clock, which is generating by the LMX2594.

表 3 shows the AFE7444 operating modes and frequency requirements for various tests in this design.

表 3. Frequency Requirement for Various Modes of AFE7444

PARAMETERS/TEST	SYNCHRONIZATION TEST	TX PERFORMANCE	RX PERFORMANCE
Transmitter mode	AFE74xx_TX_Mode4	AFE74xx_TX_Mode5	-
LMFS	44210	44210	-
Interpolation	12	8	-
DAC sampling frequency (MHz)	5898.24	5898.24	5898.24
Interpolated DAC clock rate (MHz)	491.52	737.28	-
Lane rate (Mbps)	9830.4	14745.6	-
Receiver mode	AFE74xx_RX_Mode9	-	AFE74xx_RX_Mode9
LMFS	24410	-	24410
Decimation	12	-	16
ADC sampling frequency (MHz)	2949.12	-	2949.12
Decimated output rate (MHz)	245.76	-	184.32
Lane rate (Mbps)	9830.4	-	7372.8
SYSREF frequency (MHz)	15.36	15.36	11.52
FPGA clock (MHz)	245.76	368.64	184.32

The AFE7444EVM has been tested with the proposed clocking solution for various test cases and modes to see the transmitter and receiver performance and compare with the datasheet performance along with a synchronization test for common frequency settings.

3.1.2 Software

Once the boards are modified and connected together, configure all devices in multiple boards.

3.1.2.1 Transmitter Performance SW Setup

This subsection provides the guidelines to program the AFE7444EVM along with the clocking board and the TSW14J57EVM to measure the TX SFDR and IMD3 performance for Mode5 with interpolation 8x.

3.1.2.1.1 Clocking Board Programming Sequence

Clocking board devices are programmed by HSDC TID GUI, as shown in 図 9. Download the HSDC TID GUI from TI.com to program the TIDA-010131 clocking board.

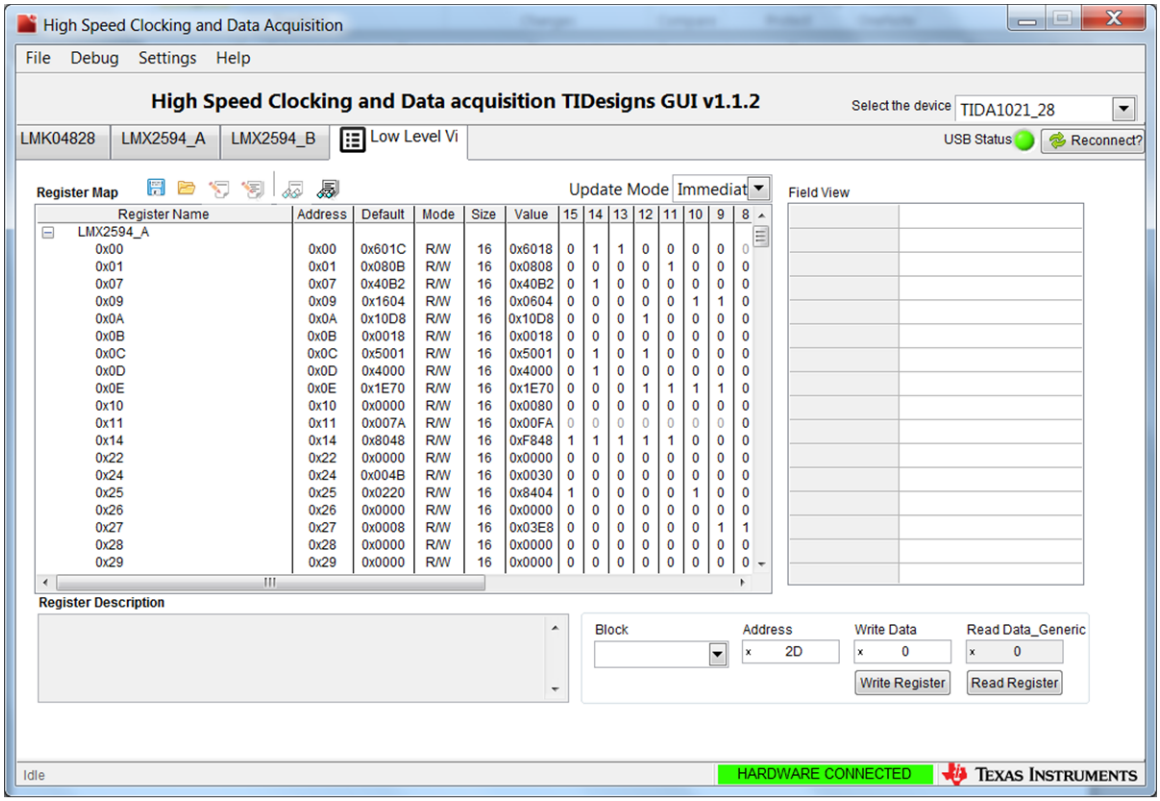
All devices are configured by loading the configuration files in the low-level view page.

1. Load the *AFE7444_LMK61E2_61.44MREF.cfg* file to program the LMK61E2 programmable oscillator at 61.44-MHz reference frequency.
2. Load the *AFE7444_LMK61E2_EEPROM_Write.cfg* file to write the frequency setting in EEPROM of the LMK61E2.
3. Load the *AFE7444_LMK04828_61.44MREF_368.64MFCLK_15.36MSYSREF.cfg* file to program

onboard LMK04828 to generate SYSREF and FPGA clocks.

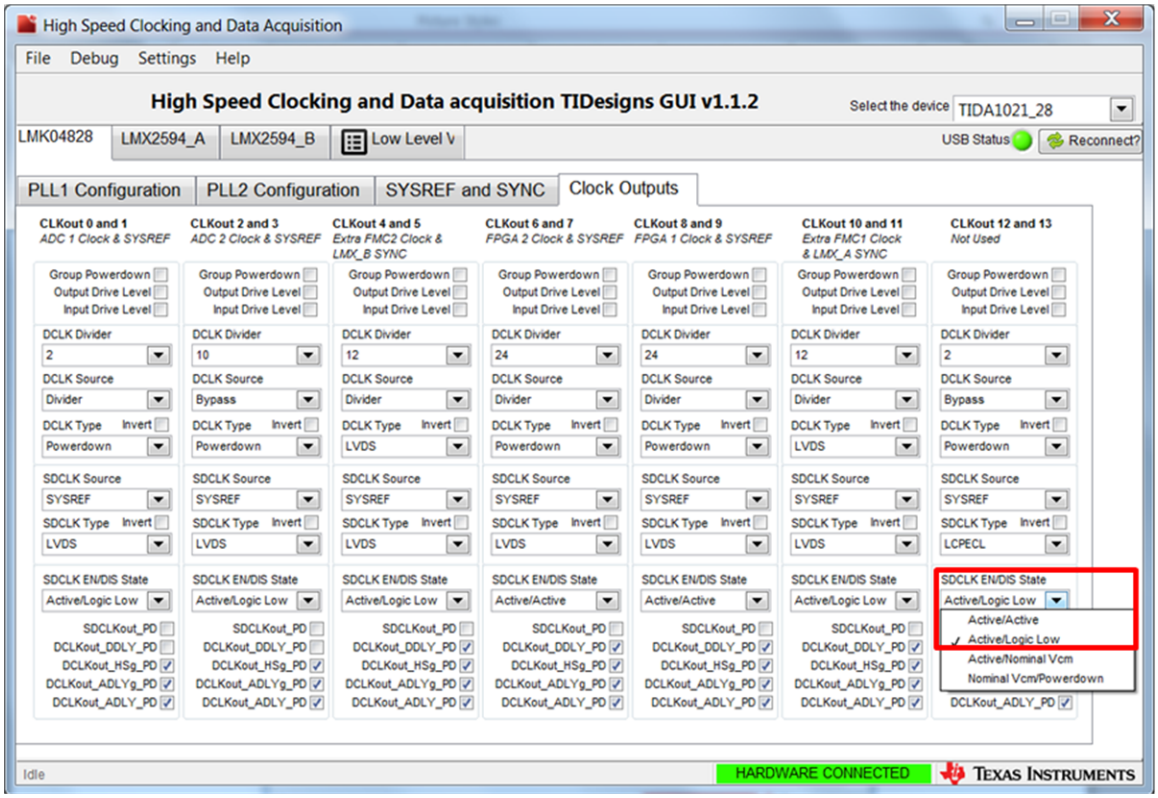
4. Load the *AFE7444_LMX2594_A_B_5898.24MCLK_61.44MREF_SYNC.cfg* file to generate synchronized device clocks at 5898.24 MHz from LMX2594s.

図 9. HSDC TID GUI



5. Once all boards are programmed, turn off the SYSREF to the AFE7444EVM by setting at *Active/Logic Low* from the clocking board as shown in 図 10.

図 10. SYSREF OFF in HSDC TID GUI



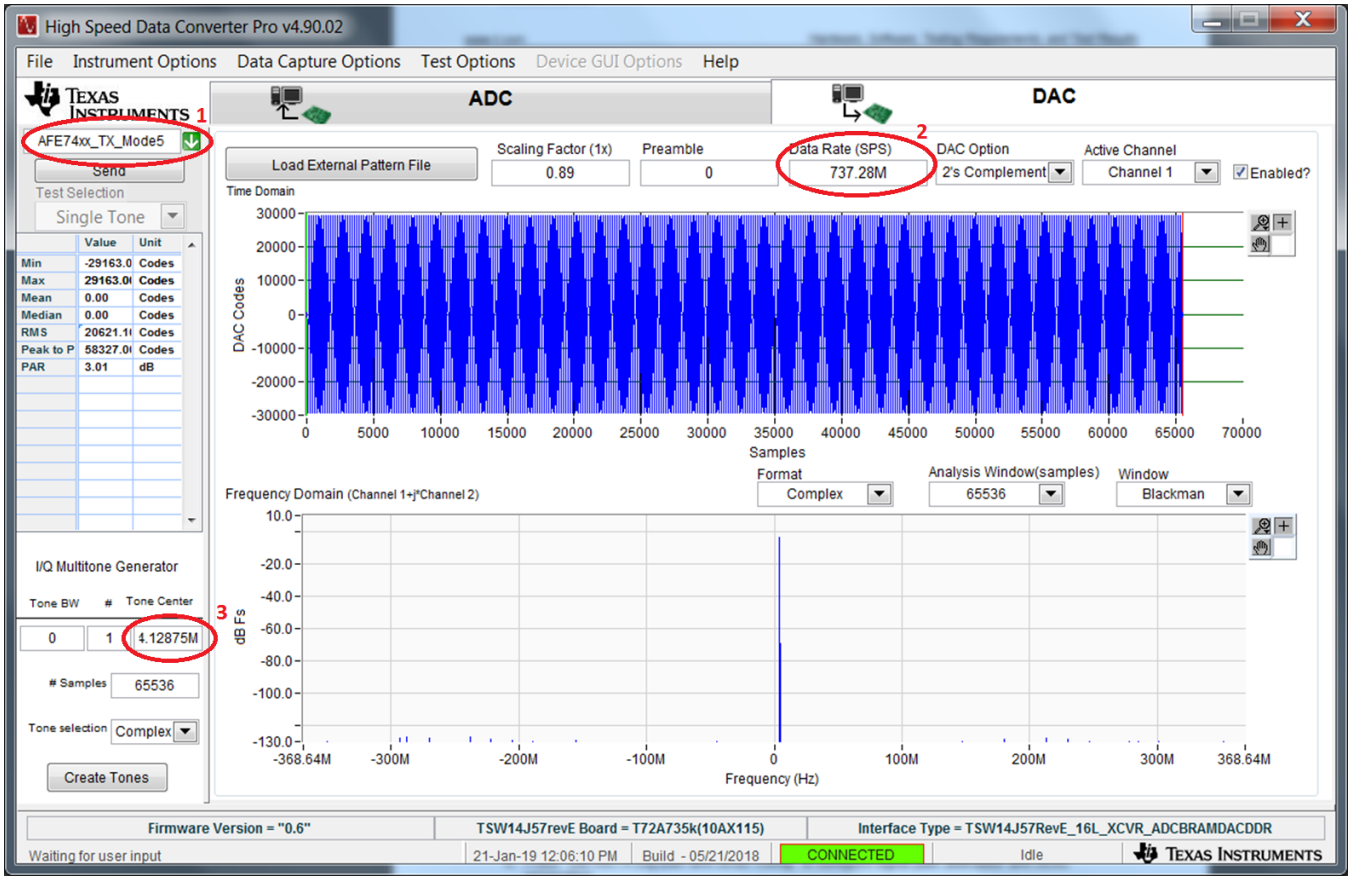
3.1.2.1.2 HSDC Pro Setup

The HSDC-PRO software interfaces with the TSW14J57EVM to support data transfer to the AFE7444EVM through a JESD204B link. For more information, see the TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide and the High Speed Data Converter Pro GUI User's Guide.

Use the following steps to program the TSW14J57EVM as shown in 図 11:

1. Select *AFE74xx_TX_Mode5* to interface with the AFE7444EVM for Mode5.
2. Set the data rate for Mode5 and interpolation 8, for example, 737.28 Msps.
3. Set the I/Q frequency based on the expected output frequency and NCO frequency.

図 11. HSDC Pro DAC Settings



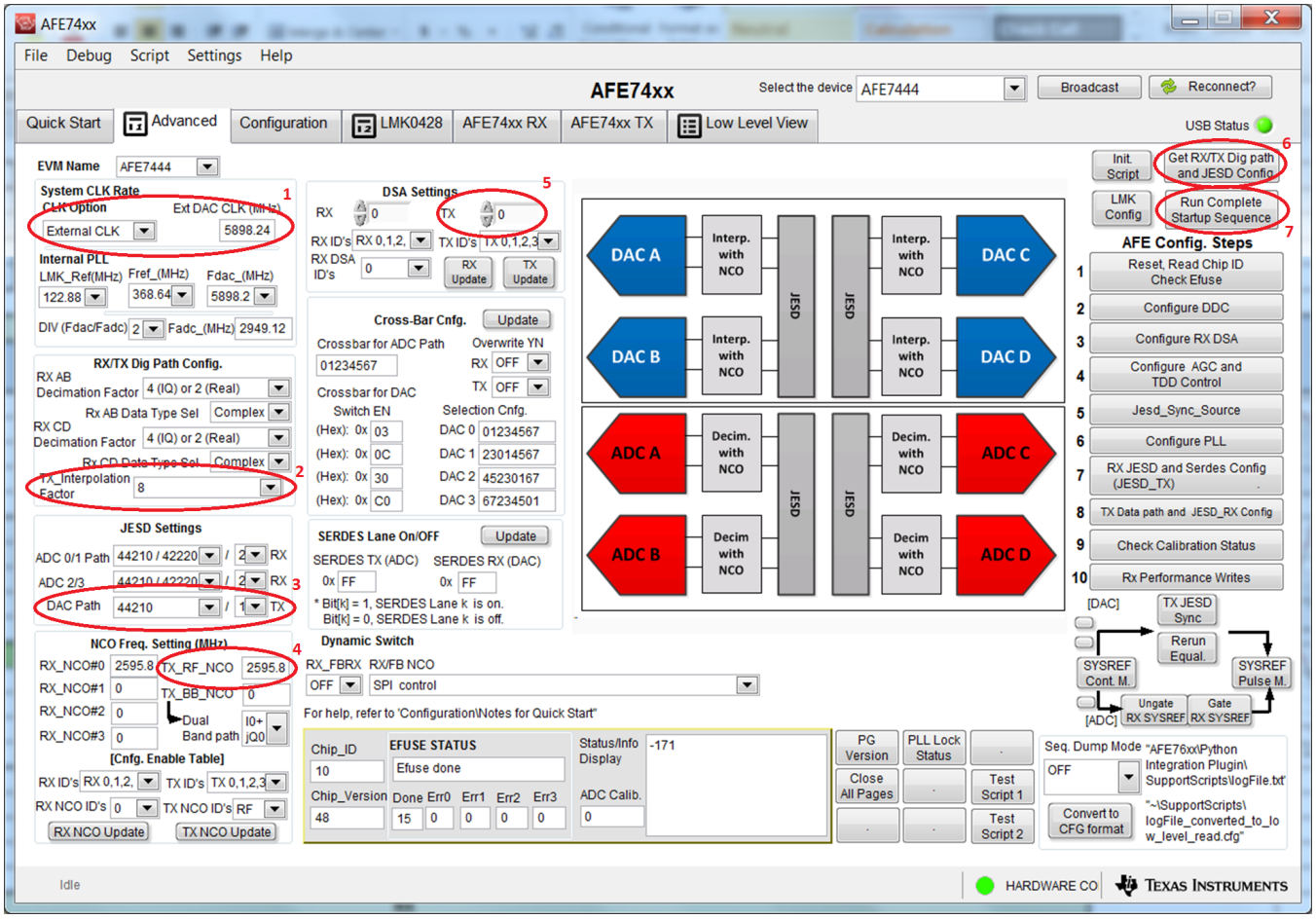
3.1.2.1.3 AFE7444 EVM Programming Sequence

Download the AFE74xx GUI from TI.com to program the AFE7444EVM. Configure the AFE7444 for transmitter and DAC performance tests in the AFE7444EVM for mode 5 with 8 interpolation factor as shown in 図 12.

Use the following steps to program the AFE7444EVM:

1. Set up the EVM in external clock source selection mode with a DAC sampling frequency of 5898.24 Msps.
2. Select TX interpolation factor 8.
3. Select Mode 5, for example, the 44210 JESD setting.
4. Set the TX_RF_NCO value based on the expected output frequency. The value should be a multiple of the SYSREF frequency.
   - For example,
     - DAC output frequency – 2600 MHz
     - I/Q frequency – 4.16 MHz
     - SYSREF – 15.36 MHz
     - TX_RF_NCO = N× SYSREF = 169 × 15.36 = 2595.84 MHz
5. Set the TX_DSA value to 0 withno attenuation at TX output.
6. Select*Get RX/TX Dig path and JESD Config* to configure the digital path attenuator and JESD parameters.
7. Select*Run Complete Startup Sequence* to program the AFE7444 to generate the expected output.

図 12. AFE7444EVM GUI DAC Programming Sequence



3.1.2.2 Receiver Performance SW Setup

This subsection provides the guidelines to program the AFE7444EVM along with the clocking board and the TSW14J57EVM to measure the RX SNR performance for mode9 with a decimation factor of 16.

3.1.2.2.1 Clocking Board Programming Sequence

Clocking board devices are programmed by HSDC TID GUI, as shown in 図 9.

All devices are configured by loading the configuration files in the low-level view page.

1. Load the *AFE7444_LMK61E2_61.44MREF.cfg* file to program the LMK61E2 programmable oscillator at 61.44-MHz reference frequency.
2. Load the *AFE7444_LMK61E2_EEPROM_Write.cfg* file to write the frequency setting in EEPROM of the LMK61E2.
3. Load the *AFE7444_LMK04828_61.44MREF_184.32MFCLK_11.52MSYSREF.cfg* file to program onboard LMK04828 to generate SYSREF and FPGA clocks.
4. Load the *AFE7444_LMX2594_A_B_5898.24MCLK_61.44MREF_SYNC.cfg* file to generate synchronized device clocks at 5898.24 MHz from LMX2594s.
5. Once all boards are programmed, turn off the SYSREF by setting it at *Active/Logic Low* from the clocking board shown in 図 10.

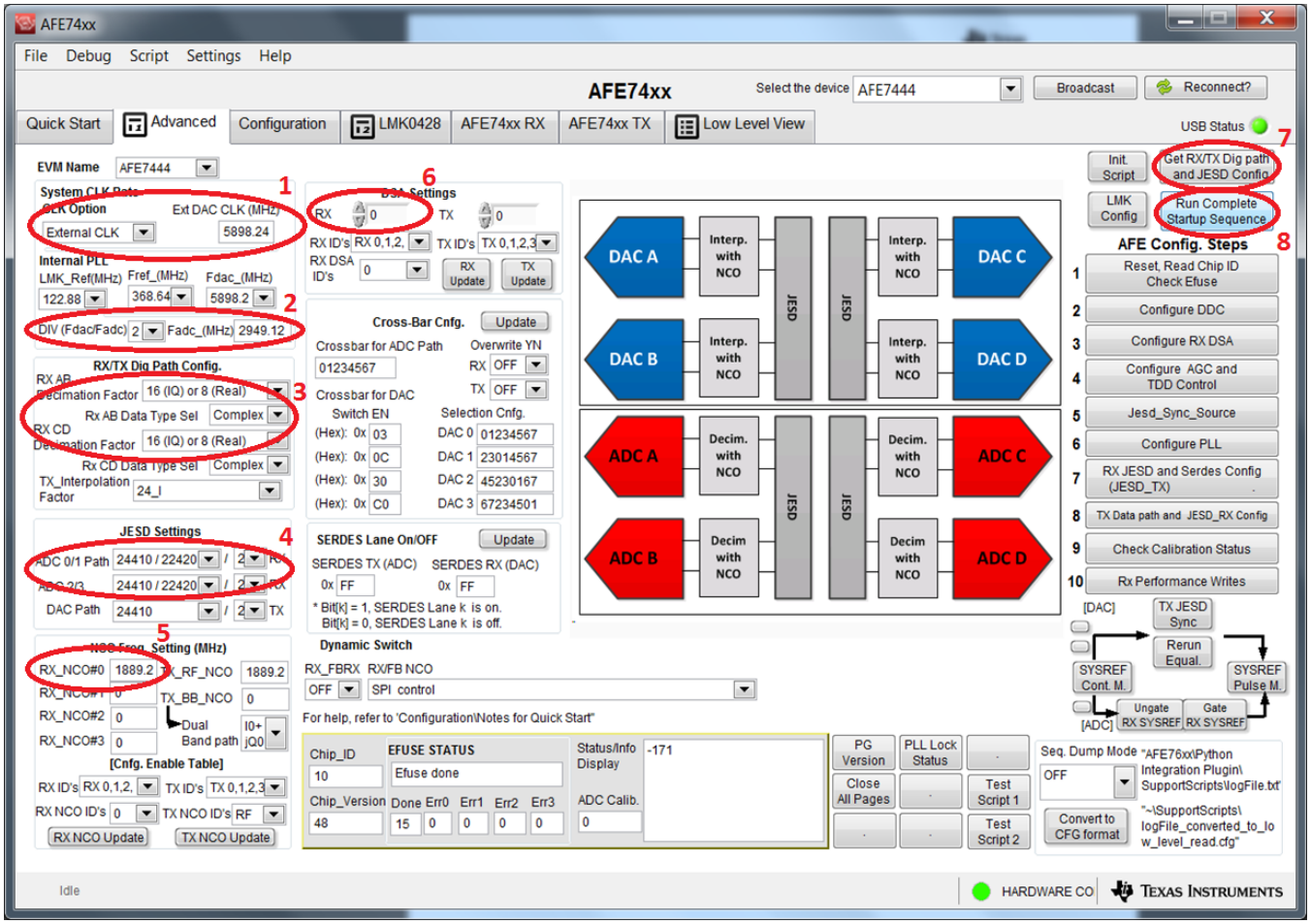
3.1.2.2.2 AFE7444 EVM Programming Sequence

Configure the AFE7444 for RX and ADC performance tests in the AFE7444EVM for mode 9 with a decimation of 16 along with the external clock source as shown in 図 13.

Use the following steps to program the AFE7444EVM:

1. Set up the EVM in external clock source selection mode with a DAC sampling frequency of 5898.24 MHz.
2. Set the Fdac/Fadc divider value to 2 to generate the ADC sampling clock to 2949.12MHz.
3. Select RX decimation factor 16.
4. Select Mode 9,for example, the 24410 JESD RX setting.
5. Set the RX_NCO value based on the expected input frequency.The value should be an integer multiple of the SYSREF frequency.
   - For example,
     - ADC input frequency – 1900MHz
     - SYSREF – 11.52MHz
     - I/Q frequency – 10.72MHz
     - RX_NCO = N× SYSREF = 164× 11.52 = 1889.28MHz
6. Set RX_DSA value to 0 withno attenuation at the RX input.
7. Select*Get RX/TX Dig path and JESD Config* to configure the digital path attenuator and JESD parameters.
8. Select*Run Complete Startup Sequence* to program the AFE7444 to convert the input signal to I/Q signal.

図 13. AFE7444EVM GUI ADC Programming Sequence



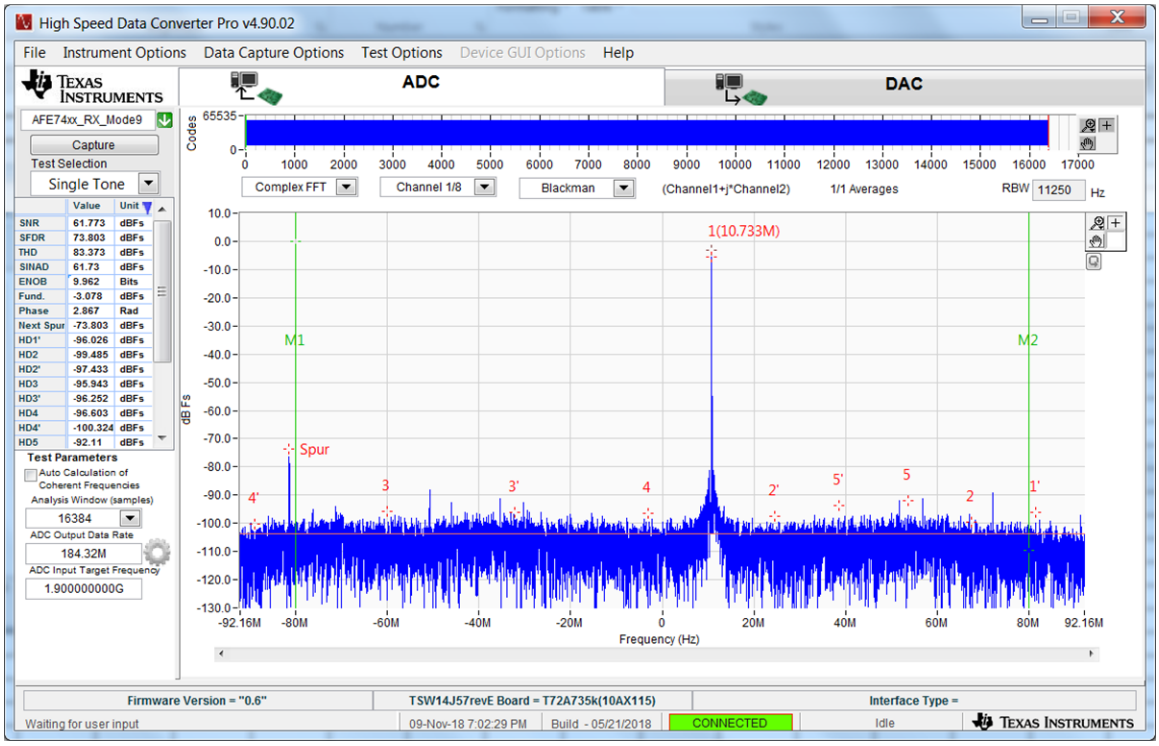
3.1.2.2.3 HSDC Pro Setup

The HSDC-PRO software interfaces with the TSW14J57EVM to capture and analyze the digital data from the AFE7444 in SNR measurement.

Use the following steps to program the TSW14J57EVM as shown in 図 14:

1. Select *AFE74xx_RX_Mode9* to interface with the AFE7444EVM for mode 9.
2. Set the ADC sampling frequency and NCO frequency to get an ADC output data rate.
3. Set the ADC input target frequency.

図 14. HSDC Pro ADC Settings



3.1.2.3 Multiple AFE7444 TX/RX Synchronization SW Setup

This subsection provides the guidelines to program the two AFE7444EVMs along with the clocking board and two TSW14J56EVMs to show the multiple AFE7444EVMs synchronization performance.

3.1.2.3.1 Clocking Board Programming Sequence

Clocking board devices are programmed by HSDC TID GUI, as shown in 図 9.

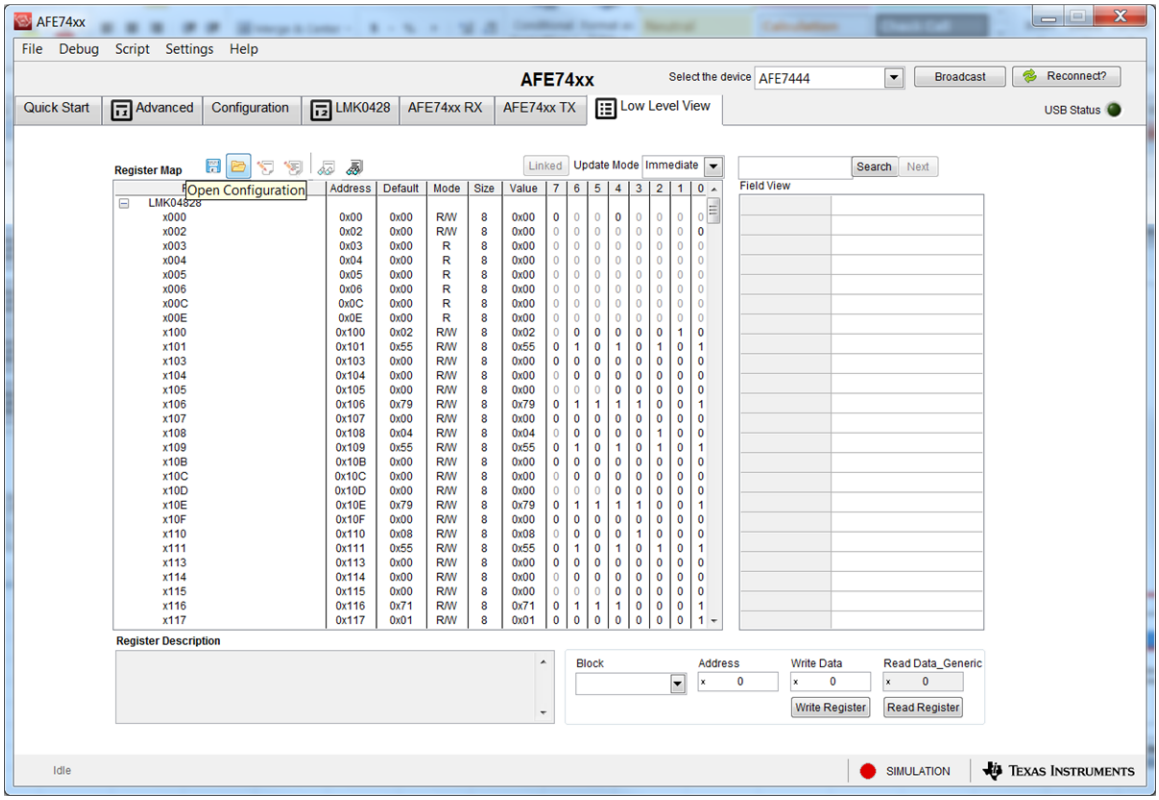
1. Load the *AFE7444_LMK61E2_61.44MREF.cfg* file to program the LMK61E2 programmable oscillator at 61.44-MHz reference frequency.
2. Load the *AFE7444_LMK61E2_EEPROM_Write.cfg* file to write the frequency setting in EEPROM of the LMK61E2.
3. Load the *AFE7444_LMK04828_61.44MREF_245.76MFCLK_15.36MSYSREF.cfg* file to program onboard LMK04828 to generate SYSREF and FPGA clocks.
4. Load the *AFE7444_LMX2594_A_B_5898.24MCLK_61.44MREF_SYNC.cfg* file to generate synchronized device clocks at 5898.24 MHz from LMX2594s.
5. Once all boards are programmed, turn off the SYSREF by setting it at *Active/Logic Low* from the clocking board as shown in 図 10.

3.1.2.3.2 AFE7444 EVM Programming Sequence

Configure the AFE7444s for TX and RX synchronization setup in both AFE7444EVMs with the external clock source mode. Use the following steps to program both AFE7444EVMs as shown in 図 15.

1. For quick programming, load *AFE7444_RX_Mode9_Dec12_900M_TX_Mode4_Int12_900M.cfg* file in the low-level view page as shown in 図 10 for the 900-MHz transmit and receive frequency.

図 15. AFE7444 GUI Programming Through Low-Level View Page



3.1.2.3.3 HSDC Pro Setup

In this setup, the HSDC-PRO software interfaces with the TSW14J56EVMs for TX as well as RX in master and slave mode.

Use the following steps to program the TSW14J56EVMs:

1. Before configuring the AFE7444, setup the DAC and TX of both capture cards for mode4 and an interpolation factor of 12, same as 3.1.2.1.2.
2. After configuring the AFE7444, setup the ADC and RX of both capture cards for mode9 and a decimation factor of 12, same as 3.1.2.2.3.

3.2 Testing and Results

3.2.1 Test Setup

図 16, 図 17 and 図 18 show the test setup for transmitter performance (SFDR, IMD3) measurement, receiver SNR measurement, and channel-to-channel skew measurement for multiple AFE7444s, respectively.

Use the following steps for each test setup:

1. Connect a 5-V/2-A power supply to the J25 connector of the clocking board.
2. Connect two separate 5-V/5-A power supplies to the J35 connector of both AFE7444EVMs.
3. Connect a 12-V/2-A power supply to the TSW14J57EVM and a 5-V/3-A power supply to the J11 connector of each TSW14J56EVM (capture card based on test setup).
4. Follow the programming sequence in 3.1.2 for each board based on the test setup.

図 16. Test Setup for AFE7444 Transmitter SFDR and IMD3 Measurement

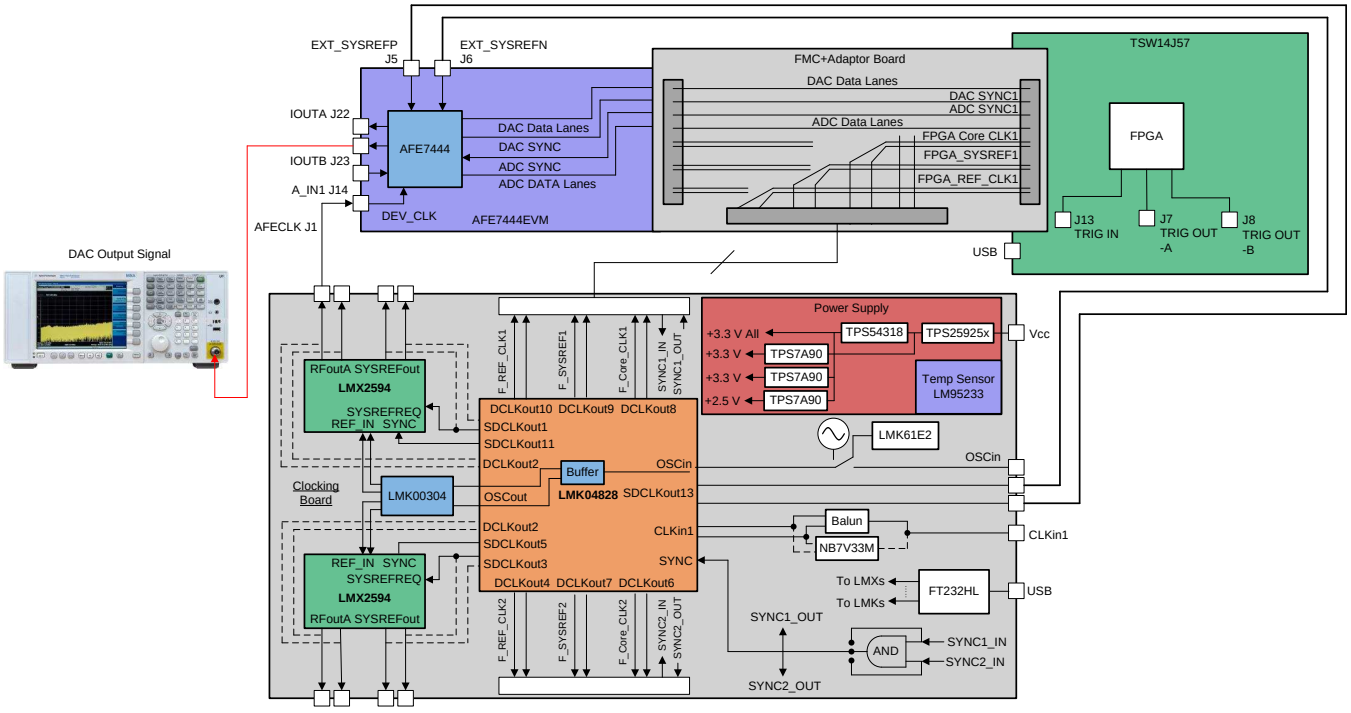


図 17. Test Setup for AFE7444 Receiver SNR Measurement

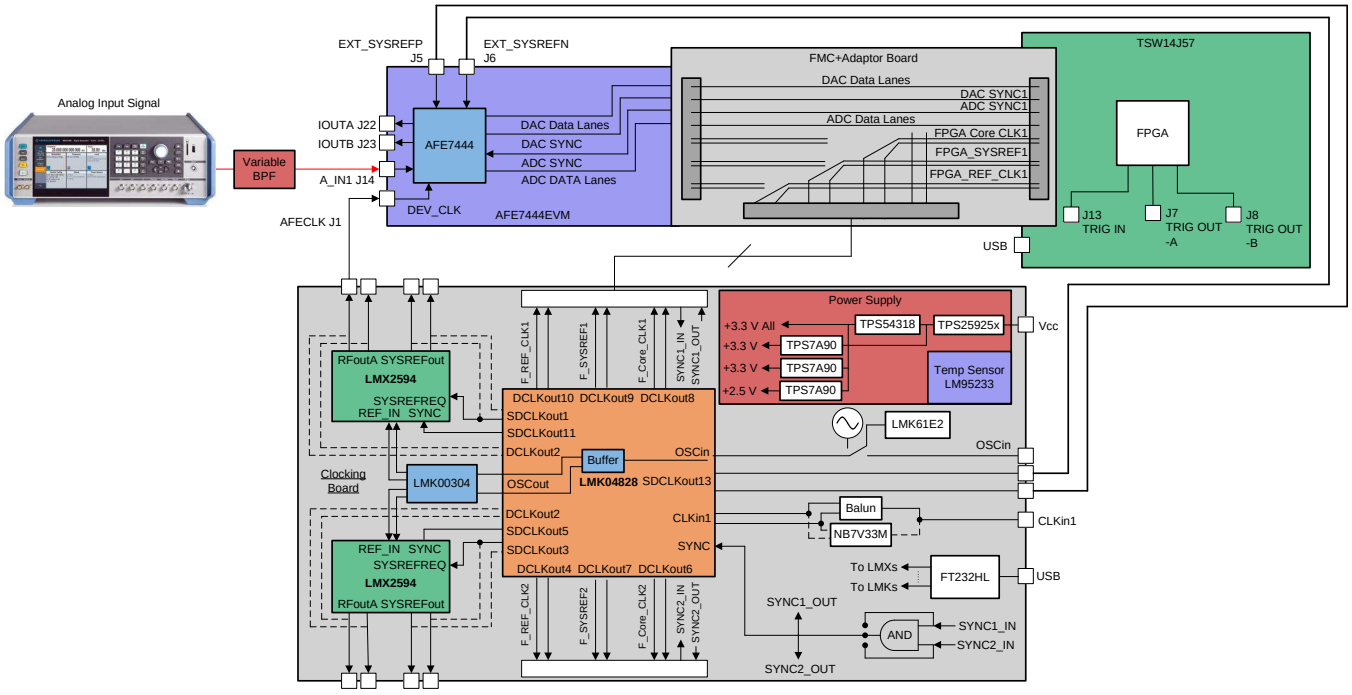
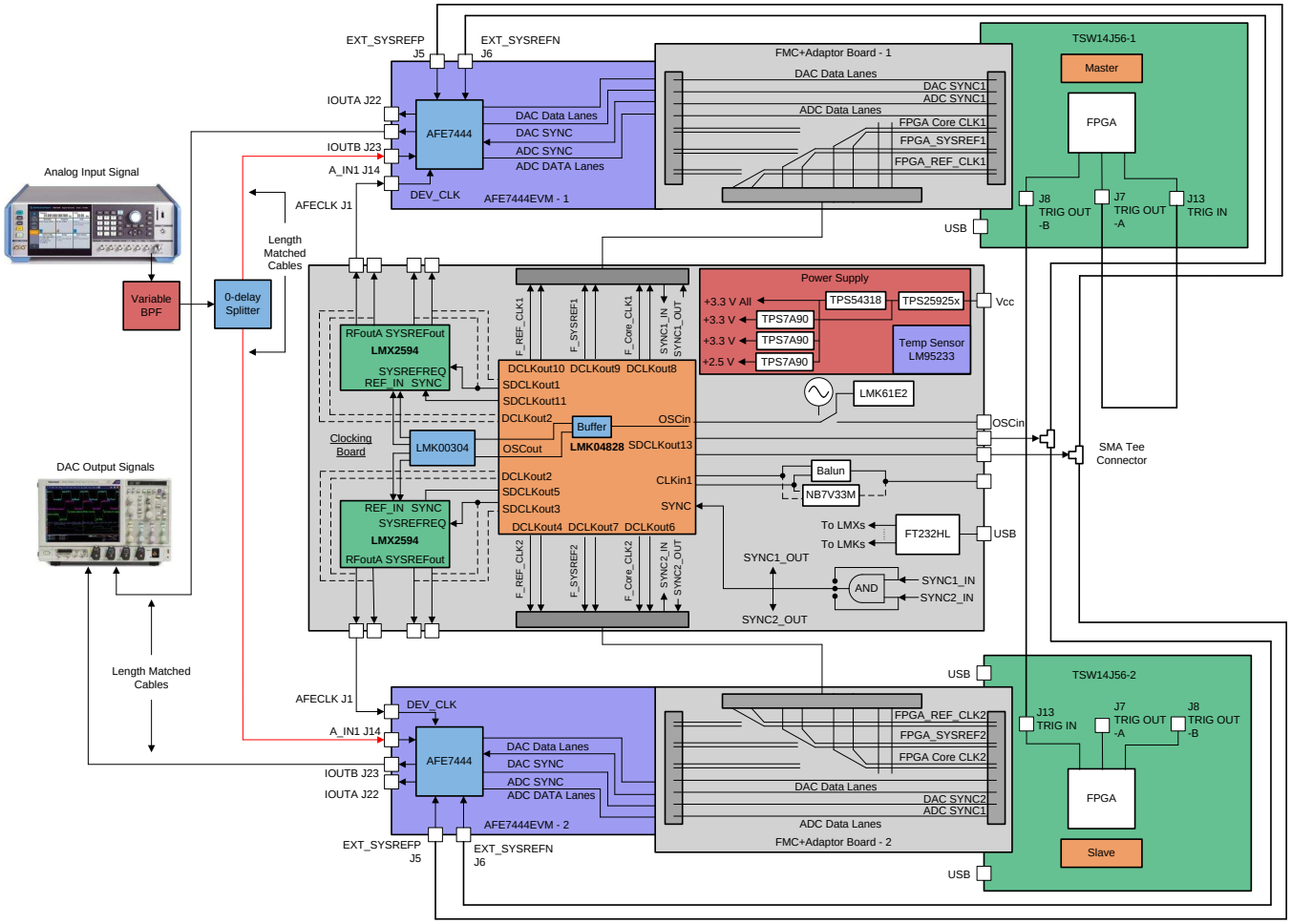


図 18. Test Setup for Two AFE7444 Analog Channel-to-Channel Skew Measurement



3.2.2 Test Results

3.2.2.1 Transmitter Performance

表 4 shows the measured transmitter performance results in terms of SFDR and IMD3 for mode 9 and an interpolation factor of 16. Measured SFDR and IMD3 of the AFE7444 with the proposed TIDA-010131 clocking solution is improved from the AFE7444EVM using the internal PLL clocks and is comparable with the external clock source from the signal generator.

表 4. Measured SFDR and IMD3 of Transmitter Output

PARAMETERS	CONDITIONS	UNIT	AFE7444 DATASHEET SPECIFICATION	TIDA-010131 MEASURED	AFE7444EVM MEASURED (EXT CLK)	AFE7444EVM MEASURED (INT PLL)
SFDR	SFDR for 0-FDAC/2 BW, DSA - 0 dB, -1 dBFS					
890 MHz		dBc	60	62.65	65.85	63.2
1800 MHz		dBc	55	60.89	59.3	58.29
2100 MHz		dBc	56	60.1	59.44	58.63
2600 MHz		dBc	58	66.5	66.63	66.54
SFDR	SFDR for Fout +/-250-MHz BW, DSA - 0 dB, -1 dBFS					
890 MHz		dBc	84	84.76	86.73	83.28
1800 MHz		dBc	74	82.89	82.27	82.54
2100 MHz		dBc	75	73.6	73.52	74.4
2600 MHz		dBc	74	72.78	73.48	74.47
IMD3	IMD3 for ±10-MHz tone offset, DSA - 0 dB, -7 dBFS each tone					
890 MHz		dBc	69	76.02	77.04	76.58
1800 MHz		dBc	69	74.64	74.67	75.07
2100 MHz		dBc	68	69.58	69.28	69.28
2600 MHz		dBc	68	69.82	70.34	70.35

3.2.2.2 Receiver Performance

表 5 shows the measured SNR performance of the AFE7444 receiver at various frequencies for mode 9 and a decimation factor of 16. Measured SNR of the receiver with the proposed TIDA-010131 clocking solution is improved compared to the AFE7444 internal PLL clocks and is comparable with the external clock source from the signal generator. 図 19 and 図 20 show spectrum results of the ADC at 1900-MHz and 2600-MHz input frequencies respectively.

表 5. Measured SNR of AFE7444 Receiver

INPUT FREQUENCY	CONDITIONS	UNIT	AFE7444 DATASHEET SPECIFICATION	TIDA-010131 MEASURED	AFE7444EVM MEASURED (EXT)	AFE7444EVM MEASURED (INT PLL)
1900 MHz	DSA - 0 dB, -3 dBFS input signal	dBFs	63.3	61	61.6	60.5
2600 MHz		dBFs	61.2	59.3	60.4	58.8

図 19. Spectrum at 1900-MHz Input Signal

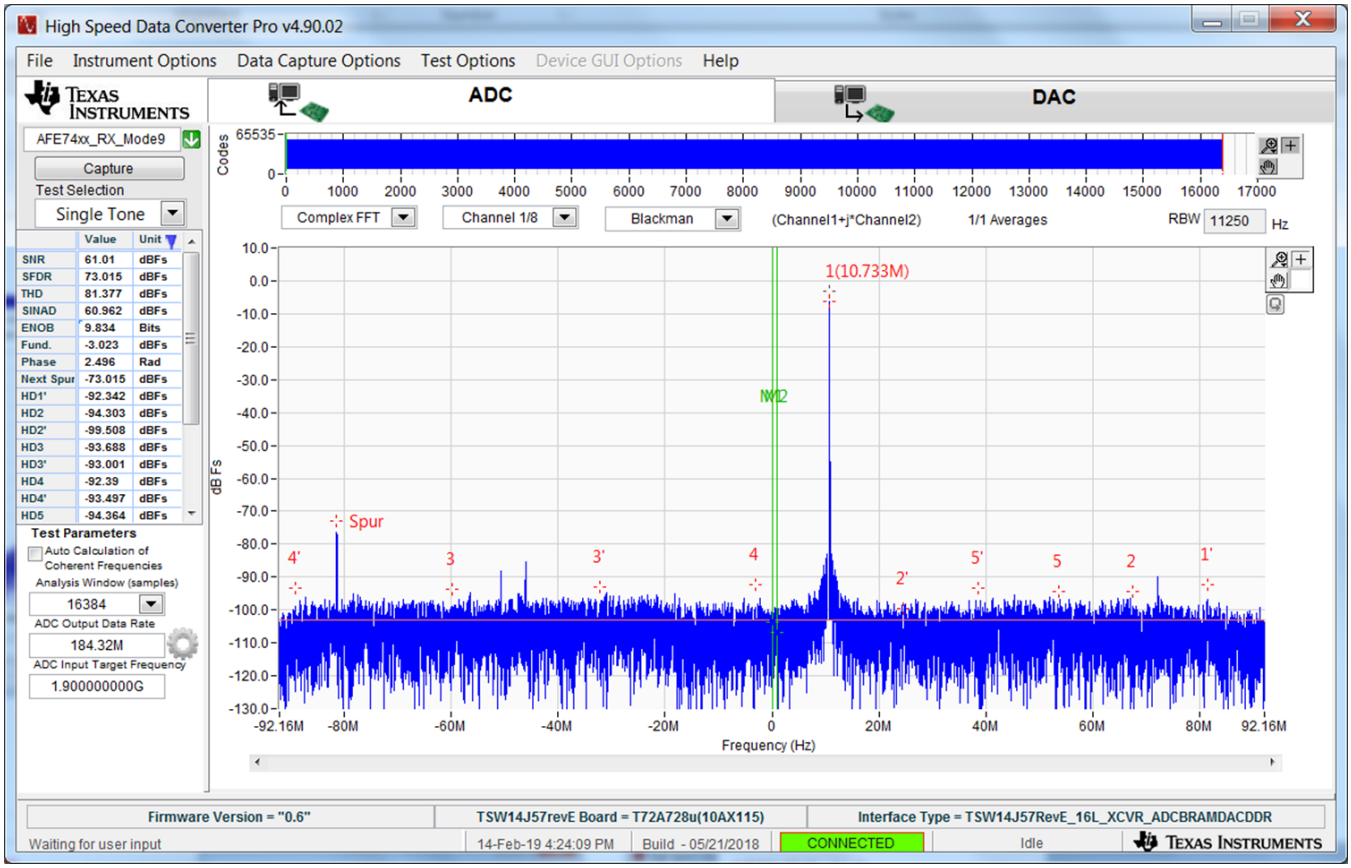
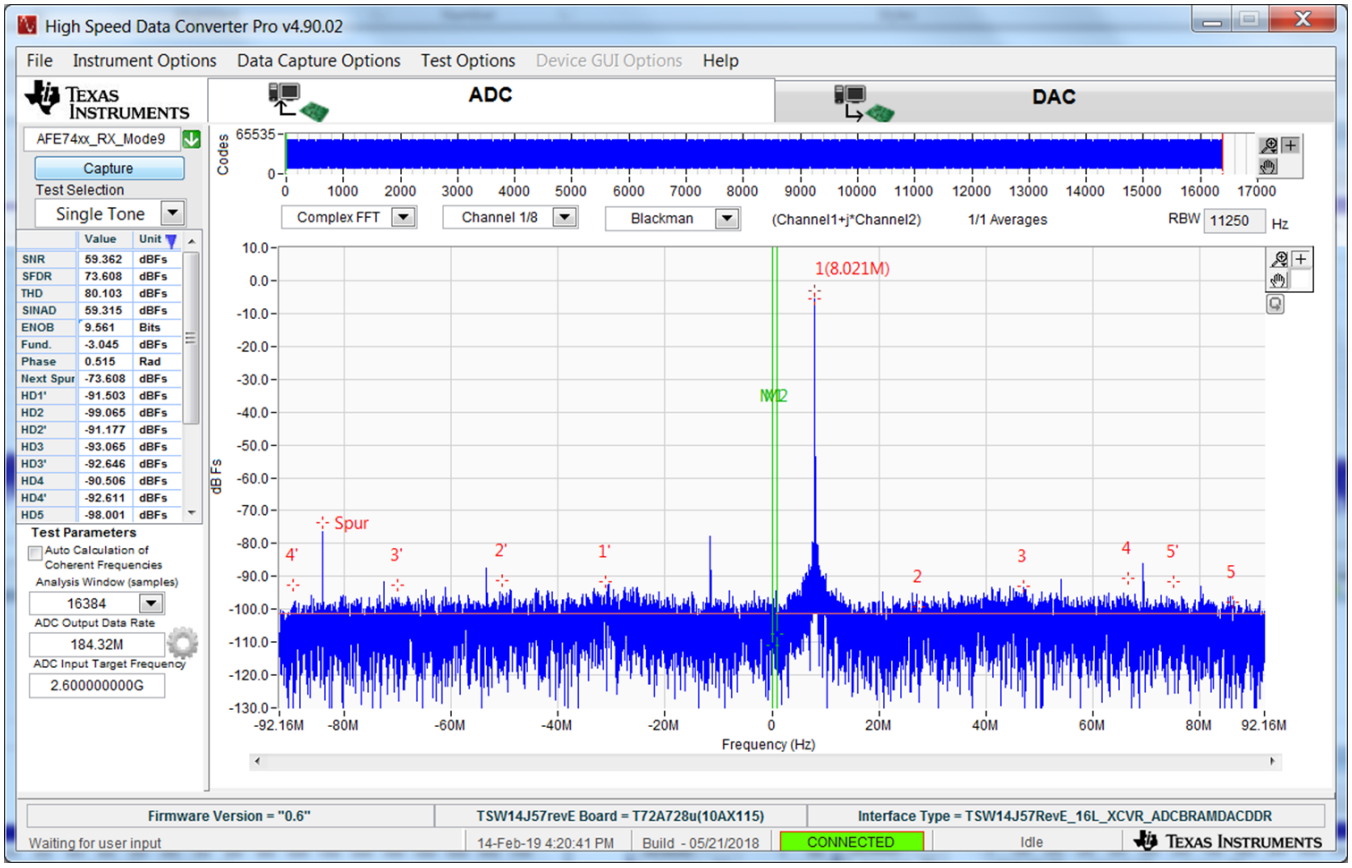


図 20. Spectrum at 2600-MHz Input Signal



3.2.2.3 *Multiple AFE7444s TX and RX alignment*

As explained in 2.2.1, synchronized clocks are critical for multichannel systems. This section shows the multichannel synchronized clocking performance while measuring the channel-to-channel skew between the transmitter and receiver of the two AFE7444EVMs respectively. The time-skew test is performed between the two channels of AFE7444EVMs at different frequencies operating in L and S band RADAR applications.

The transmitter channel's skew is evaluated by measuring skew between the generated outputs of each AFE's DAC in a high-speed oscilloscope. 表 6 shows the channel-to-channel skew at 5898.24-MHz DAC sampling frequency and the achieved skew was less than 10 ps for each output frequency. 図 21, 図 22, and 図 23 show the transmitter channel-to-channel skew at various output frequencies.

表 6. Measured Analog Channel-to-Channel Skew Between Transmitter Outputs

OPERATING FREQUENCY	MEASURED TIME SKEW (ps)
900 MHz	4
1800 MHz	-1
2100 MHz	-7

図 21. Captured Signals at 900-MHz Output

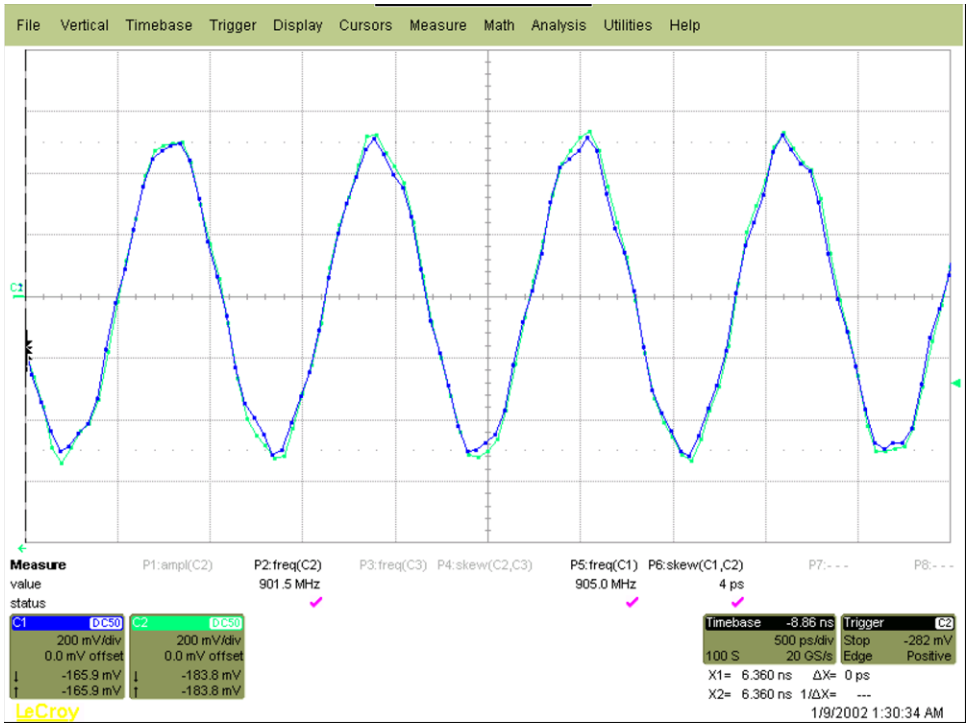


図 22. Captured Signals at 1800-MHz Output

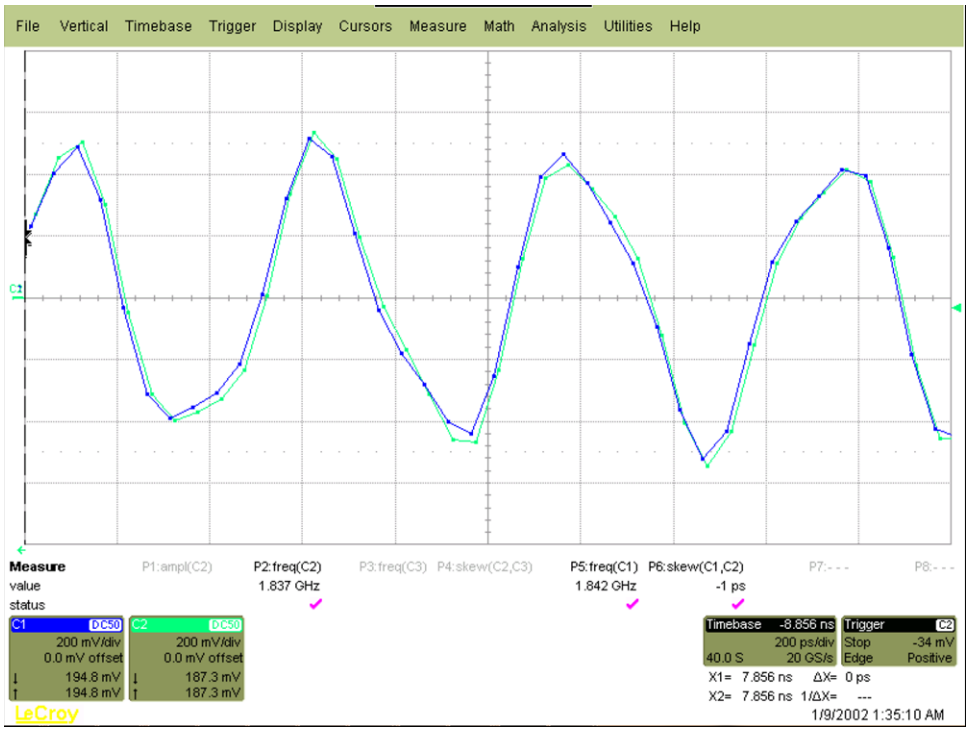
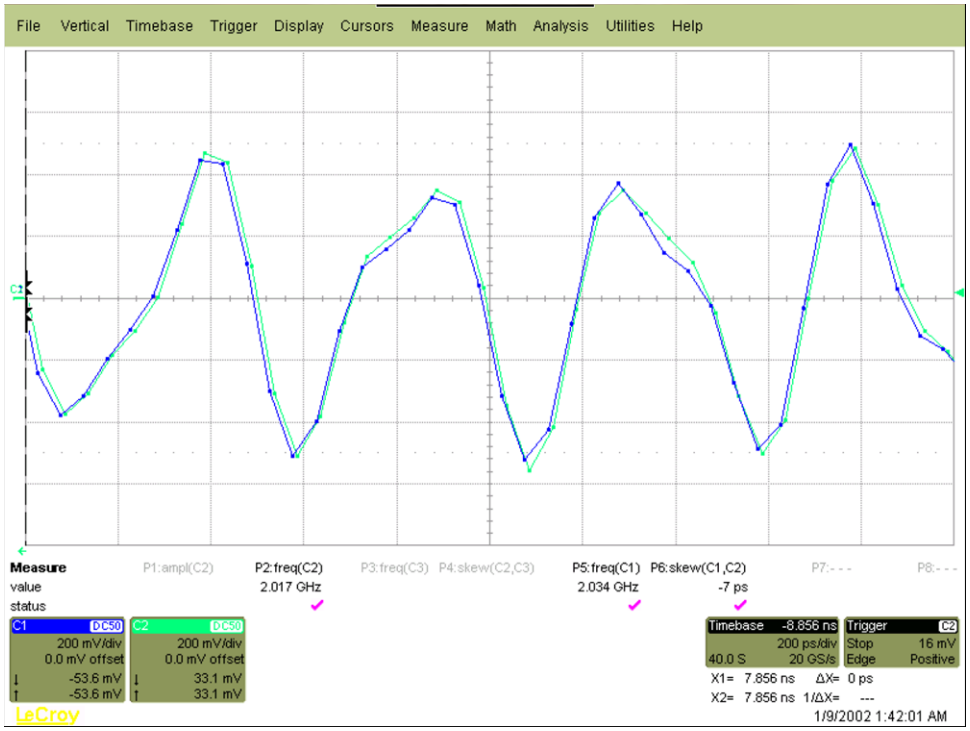


図 23. Captured Signals at 2100-MHz Output



The receiver channel's skew is evaluated by calculating the phase difference between signals captured from each AFE's ADC. 表 7 shows the channel-to-channel skew at a 2949.12-MHz sampling frequency. The measured time skew was less than 10 ps for each input frequency.

表 7. Measured Analog Channel-to-Channel Skew Between Receiver Inputs

OPERATING FREQUENCY	MEASURED TIME SKEW (ps)
900 MHz	2.28
1900 MHz	3.97
2600 MHz	4.82

図 24, 図 25 and 図 26 show the plot of the decimated output samples of the two AFE's ADCs for operating frequencies mentioned in the previous respective tables. The phase difference at each signal translates the channel-to-channel skew between AFE7444s at input frequencies, which are less than 10 ps.

図 24. Sampled Signals at 900-MHz Input

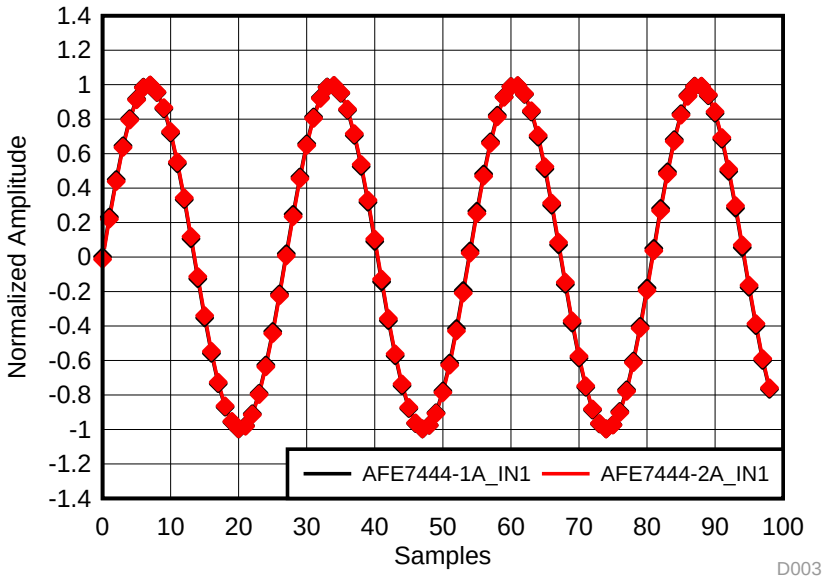


図 25. Sampled Signals at 1900-MHz Input

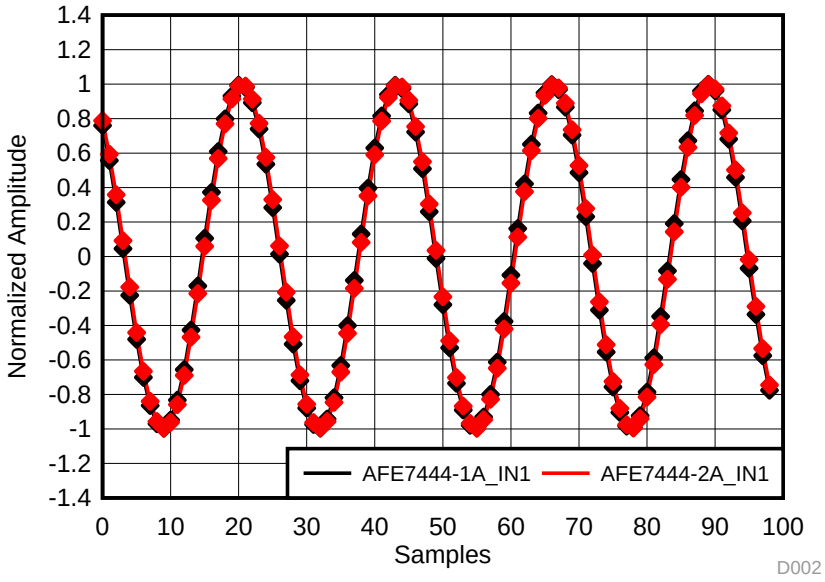
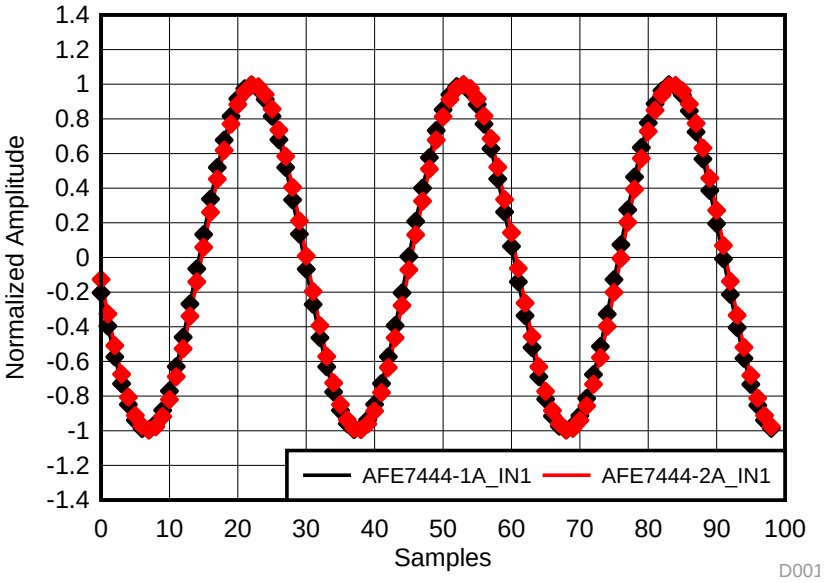


図 26. Sampled Signals at 2600-MHz Input



3.2.2.4 Summary and Conclusion

The TIDA-010131 is a JESD204B-compliant clocking reference design for a multichannel, RF-transceiver system, which is suitable for RADAR, wireless communication testers, and electronic warfare applications. This design demonstrates a high-performance phase synchronized clock with multiple RF transceivers without affecting the data converter's performance and shows the AFE7444 performance comparison with the proposed clocks, the external clock, and the internal PLL clocks. The system also shows deterministic latency behavior for every power on cycle with the analog channel-to-channel skew less than 10 ps.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010131.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010131.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010131.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010131.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010131.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010131.

5 Software Files

To download the software files, see the design files at TIDA-010131.

6 Related Documentation

1. Texas Instruments, DAC3xJ8x device initialization and SYSREF configuration application report
2. Texas Instruments, AFE74xxEVM user's guide
3. Texas Instruments, TSW14J56 JESD204B high-speed data capture and pattern generator card user's guide
4. Texas Instruments, TSW14J57 JESD204B high-speed data capture and pattern generator card user's guide
5. Texas Instruments, High speed data converter pro GUI user's guide

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7 About the Author

AJEET PAL is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the Aerospace & Defense and Test & Measurement sectors. Ajeet has eight years of experience in RF and wireless subsystem design for cellular and wireless systems. Ajeet earned his bachelor of engineering in electronics and communication engineering from the Institute of Technology & Management (ITM) University at Gwalior, India and his masters of technology in RF and microwave engineering from the Indian Institute of Technology (IIT) Kharagpur, India.

Appendix A

Example Matlab Program for Analyzing Receiver Channel to Channel Skew

```
%--------------------------------------------------------%
% Import Data %
%--------------------------------------------------------%
function varargout = SkewCheck_v5(varargin)
close all;
global N;
global samples_all;
global ax;
global num_bits;
global Fs;
global Fin;
global Decimation;
global popupA;
global popupB;
% Declare variables for imported data
data1 = xlsread('read_csv1.csv');
data2 = xlsread('read_csv2.csv');
Fs = 2949.12e6;
Fin = 900e6;
Fnco = 890.88e6;
Decimation = 12;
N = length(data1);
num_bits = 15;
%Removing DC in all the channels
samples_board_1 = data1;
samples_board_1 = samples_board_1 - repmat(mean(samples_board_1),size(samples_board_1,1),1);
samples_board_2 = data2;
samples_board_2 = samples_board_2 - repmat(mean(samples_board_2),size(samples_board_2,1),1);
samples_all = [samples_board_1 samples_board_2];
fig=figure('Units', 'normalized', 'Position',[0.1,0.1,0.5,0.8]);
set(0, 'CurrentFigure', fig);
for i = 1:size(samples_board_1,2)
waveDataSrc{i} = sprintf('File1_Ch%1d',i);
end
for k = 1:size(samples_board_2,2)
waveDataSrc{size(samples_board_1,2)+k} = sprintf('File2_Ch%1d',k);
end
```

```
popupA = uicontrol('Style', 'popup', 'Units', 'normalized',...
'String', waveDataSrc,...
'Position', [0.76,0.935, 0.2, 0.05],...
'Tag', 'PUA1', 'Callback', @setmap);
popupB = uicontrol('Style', 'popup', 'Units', 'normalized',...
'String', waveDataSrc,...
'Position', [0.76,0.905, 0.2, 0.05],...
'Tag', 'PUB1', 'Callback', @setmap);
ax(1) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
'CameraViewAngleMode', 'auto',...
'Units', 'normalized', 'Position', [0.06+0,0.06+0.48*1,0.9,0.38]);
ax(2) = axes('DataAspectRatioMode', 'auto', 'PlotBoxAspectRatioMode', 'auto',
'CameraViewAngleMode', 'auto',...
'Units', 'normalized', 'Position', [0.06+0,0.06+0.48*0,0.9,0.38]);
PlotData(1, 1)
CalcSkewData
end
function PlotData(PUPA, PUPB)
global samples_all;
global ax;
global N;
global num_bits;
global Fs;
global Fin;
global Decimation;
Fsd = Fs/Decimation;
global popupA;
global popupB;
popupAStr = get(popupA, 'String');
popupBStr = get(popupB, 'String');
samples_board_1 = samples_all(:,PUPA);
samples_board_2 = samples_all(:,PUPB);
subplot(ax(1));
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);
```

```
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));
%magitude correction
samples_board_1 = samples_board_1 * (mag_x/mag_y);
plot((0:length(samples_board_1)-1)*(1/Fsd),samples_board_1,...
((0:length(samples_board_2)-1)*(1/Fsd))-(0/(2*Fsd)),samples_board_2);
str_trace1 = sprintf('%s',popupAStr{PUPA});
str_trace2 = sprintf('%s',popupBStr{PUPB});
leg = legend(str_trace1, str_trace2);
set(leg, 'Interpreter', 'none');
title('Time Domain Plot');
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));
subplot(ax(2));
plot((0:N/2)*(Fsd/N), 20*log10(abs(X*2/N/A)), (0:N/2)*(Fsd/N), 20*log10(abs(Y*2/N/A)));
title('FFT Plot of ADC 1');
fprintf('\nIndex_x:%d; Index_y:%d\n',index_x, index_y);
% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_x));
% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff = mod(phase_diff, 2*pi);
%phase_diff_deg = mod(phase_diff / pi * 180, 360);
boardstring = '';
if phase_diff > pi
boardstring = 'Brd1 Lags Brd2';
phase_diff = 2*pi-phase_diff;
else
boardstring = 'Brd2 Lags Brd1';
phase_diff = phase_diff;
```

```
end
phase_diff_deg = phase_diff / pi * 180;
skew_ps = phase_diff_deg / (360*Fin) / 1e-12;
abc_title1 = sprintf('%s by %3.3f deg or %3.3f ps', boardstring, phase_diff_deg, skew_ps);
subplot(ax(1));
title(abc_title1);
abc_title2 = sprintf('Fin = %3.3f MHz', Fin*1e-6);
subplot(ax(2));
title(abc_title2);
end
function skewdata=CalcSkewData()
global samples_all;
global N;
global num_bits;
global Fs;
global Fin;
global Decimation;
Fsd = Fs/Decimation;
for row = 1:size(samples_all,2)
for col = 1:size(samples_all,2)
samples_board_1 = samples_all(:,row);
samples_board_2 = samples_all(:,col);
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));
%magitude correction
samples_board_1 = samples_board_1 * (mag_x/mag_y);
% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
```

```
A = 2^(num_bits-1);
% Find the bin with the largest amplitude. This is the sine wave.
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));
% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_x));
% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff_deg = phase_diff / pi * 180;
skew_ps = phase_diff_deg / (360*Fin) / 1e-12;
abc_title = sprintf('%3.3f°/%3.3fps', phase_diff_deg, skew_ps);
skewdata{row,col}=abc_title;
end
end
f = figure;
t = uitable(f,'Data',skewdata, 'Units', 'Normalized', 'Position',[0, 0, 1, 1], 'ColumnWidth',{150});
end
function setmap(source,callbackdata)
global popupA;
global popupB;
PlotData(get(popupA, 'Value'), get(popupB, 'Value'));
end
```

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