参考資料

デザイン・ガイド：TIDA-070001
OCP 用の冗長 eFuse 入力を持つ 3～7V_{IN}、宇宙グレード、ポイント・オブ・ロード (POL) のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

宇宙船用のアプリケーションには、信頼性向上のために多くの場合冗長性が取り入れられます。このリファレンス・デザインでは、2 つの TPS7H2201-SP 耐放射線強化 eFuse 負荷スイッチを使用して、ポイント・オブ・ロード (POL) 電源の入力に冗長性を組み込む方法を紹介します。2 つの負荷スイッチを使用することで、耐放射線性を強化した POL 降圧コンバータ TPS50601A-SP にプライマリ電圧と冗長電圧を供給できます。この負荷スイッチは過電流保護 (OCP) 制限値を変更可能であり、監視と保護が可能な電流センス出力ピンと調整可能な過電圧保護 (OVP) 機能も備えています。この POL コンバータは、短絡からの保護を強化する電流制限機能も備えています。

リソース

TIDA-070001	デザイン・ファイル
TPS7H2201-SP	プロダクト・フォルダ
TPS50601A-SP	プロダクト・フォルダ

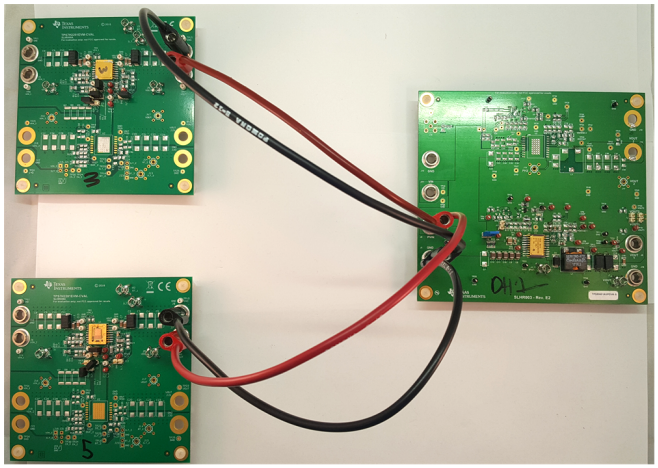
TI E2E™ Community　E2E™エキスパートに質問

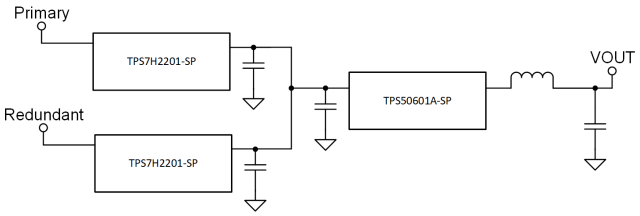
特長

- 可変の過電流保護 (OCP) 制限
- 可変の過電圧 (OVP) 制限
- 冗長化入力
- 構成可能なソフトスタート
- イネーブル / ディセーブル機能

アプリケーション

- コマンドおよびデータ処理
- 衛星用電源システム (EPS)
- 光イメージング・ペイロード
- レーダー・イメージング・ペイロード
- 通信ペイロード





1 System Description

The design consists of two TPS7H2201-SP load switches supplying input power for a TPS50601A-SP point of load converter in a redundancy configuration. The redundancy of the input voltage to the point of load converter is critical in keeping important power lines to high priority parts of a satellite such as an FPGA or microcontroller functioning.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	OPERATING SPECIFICATIONS	MAXIMUM SPECIFICATIONS	DETAILS
Input power supply	0 to 5 VDC	0 to 7 VDC	3.1.1
Input current requirement	0 to 3.5 A	0 to 7.5 A (set by load switch current limit)	3.1.1
Output voltage of POL converter	2.5 VDC	2.5 VDC	3.1.1
Output current of POL converter	0 to 6 A	0 to 13 A (set by POL current limit)	3.1.1
Operating temperature	25°C	–55°C to 125°C	3.1.1

2 System Overview

2.1 Block Diagram

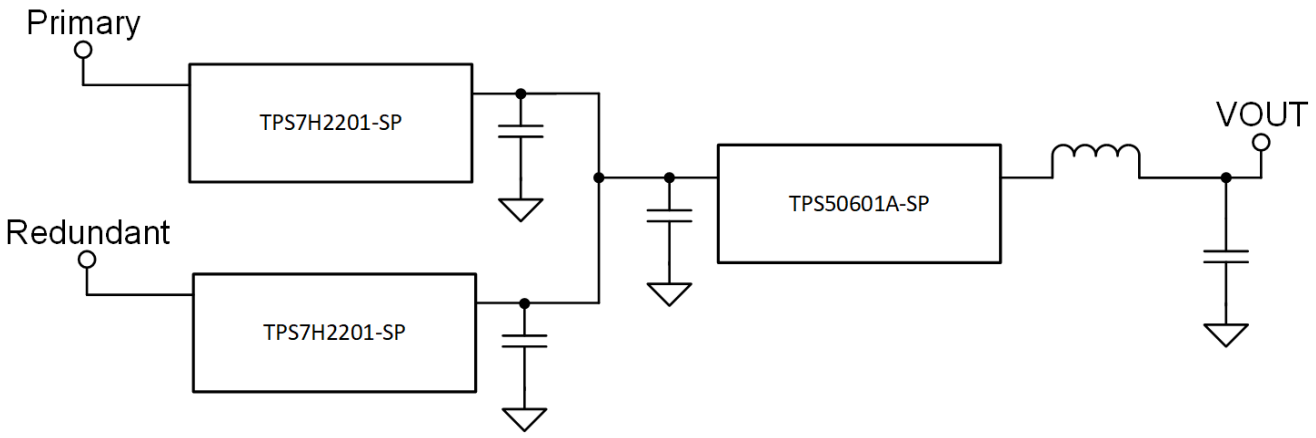


図 1. TIDA-070001 Block Diagram

2.2 Design Considerations

When using the TPS7H2201-SP as a current limiting load switch, the current limit must be calculated based on the duty cycle and efficiency of the TPS50601A-SP. Since the load switch is limiting the input and not the output current for the load switch, the input current will heavily depend on the duty cycle and efficiency of the converter. The output voltage of the TPS7H2201-SP will degrade slowly after the TPS50601A-SP turns off. The TPS50601A-SP has a minimum input voltage of 3 V. When the output voltage of the TPS7H2201-SP is below 3 V and disabled, the TPS50601A-SP will stop lowering the voltage and the charge stored on those capacitors will very slowly decrease. Enabling the TPS7H2201-SP during this time may result in the TPS50601A-SP turning on faster than anticipated.

2.3 Highlighted Products

2.3.1 TPS7H2201-SP

- Radiation Performance:
  - Radiation Hardness Assurance (RHA) up to TID 100 krad(Si)
  - Single Event Latch-up (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR) Immune to LET = 75 MeV-cm^2/mg
  - SEFI Immune to LET = 65 MeV-cm^2/mg
  - SET Characterized to LET = 65 MeV-cm^2/mg
- Integrated Single Channel Load Switch
- Input Voltage Range: 1.5 V to 7 V
- Low On-Resistance (R_{ON}) of 34-mΩ Maximum at 25°C and VIN = 5 V
- 6-A Maximum Continuous Switch Current
- Low Control Input Threshold Enables Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable Rise Time (Soft Start)
- Reverse Current Protection (TPS7H2201-SP)

- Programmable and Internal Current Limiting (FastTrip)
- Programmable Fault Timer (Current Limit and Retry Modes)
- Thermal Shutdown
- Ceramic Package With Thermal Pad

2.3.2 TPS50601A-SP

- Radiation Performance:
  - Radiation Hardened up to TID 100 krad(Si)
  - ELDRS Free 100 krad(Si) to 10 mrad(Si)/s
  - Single Event Latch-up (SEL) Immune to LET = 75 MeV-cm^2/mg
  - SEB and SEGR Immune to 75 MeV-cm^2/mg, SOA Curve Available
  - SET/SEFI Cross-Section Plot Available
- Peak Efficiency: 96.6% (VO = 3.3 V)
- Integrated 58-mΩ/50-mΩ MOSFETs
- Power Rail: 3 V to 7 V on VIN
- 6-A Maximum Output Current
- Flexible Switching Frequency Options:
  - 100-kHz to 1-MHz Adjustable Internal Oscillator
  - External Sync Capability: 100 kHz to 1 MHz
  - Sync Pin Can Be Configured as a 500-kHz Output for Master/Slave Applications
- 0.804-V ±1.5% Voltage Reference Overtemperature, Radiation, and Line and Load Regulation
- Monotonic Start-Up Into Prebiased Outputs
- Adjustable Soft Start Through External Capacitor
- Input Enable and Power-Good Output for Power Sequencing
- Power-Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout (UVLO)
- 20-Pin Ultra-Small, Thermally-Enhanced Ceramic Flatpack Package (HKH) for Space Applications

2.4 System Design Theory

The TPS7H2201-SP is a smart power load switch that allows multiple input voltages to supply the same TPS50601A-SP allowing for redundancy in input power supplies. The redundancy allows for a high reliability power supply for critical power rails. The TPS7H2201-SP also allows for current sensing of the input voltage of the TPS50601A-SP for monitoring the health of the power supply.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Two power supplies are needed to provide voltage to the TPS7H2201-SP, up to 7 V, which is the maximum voltage for the load switch. The power supplies in the following test setup need to supply up to 7.5 A of current set by the IL resistor of the individual load switches. The output load needs to be able to sink up to 13 A from the TPS50601A-SP when the device output is shorted. The TPS50601A-SP was set to an output of 2.5-V nominal. The surrounding temperature will be determined by the thermal maximum of the TPS50601A-SP and the TPS7H2201-SP, which have a temperature range of –55°C to 125°C.

3.2 Testing and Results

3.2.1 Test Setup

Tests were done with the following configuration, unless otherwise specified.

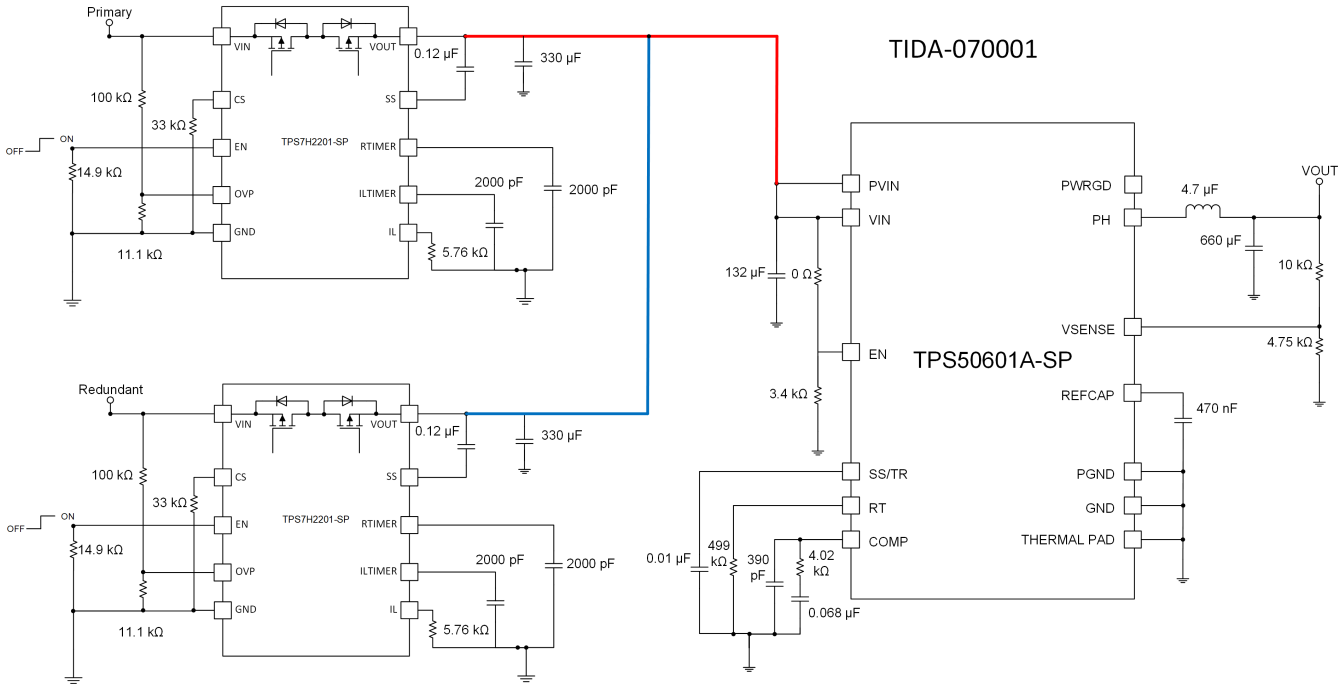


図 2. Test Setup

The tests were done with the following inputs/outputs, unless otherwise specified.

表 2. Key System Specifications

PARAMETER	SPECIFICATIONS
Input power supply	5 VDC
Output voltage	2.5 VDC
Output current	6 A
Operating temperature	25°C
LSW EN threshold	4.85 V
LSW OVP threshold	6 V
LSW current limit, IL	7.5 A
LSW current limit timer, ILTIMER	1 ms
LSW retry timer, RTIMER	1 ms
LSW soft start	9 ms
LSW maximum CS pin voltage	4.6 V
POL soft start	4 ms
POL UVLO threshold	2.75 V

3.2.2 Test Results

3.2.2.1 Leakage Current

Current flowing through disabled load switch was measured at no load and full load.

表 3. Test Data

TEST DONE	RESULT
Leakage current of disabled load switch with no load on POL converter	1.6 µA
Leakage current of disabled load switch with 6-A load on POL converter	0.75 µA
Operating temperature	25°C

3.2.2.2 Start-up

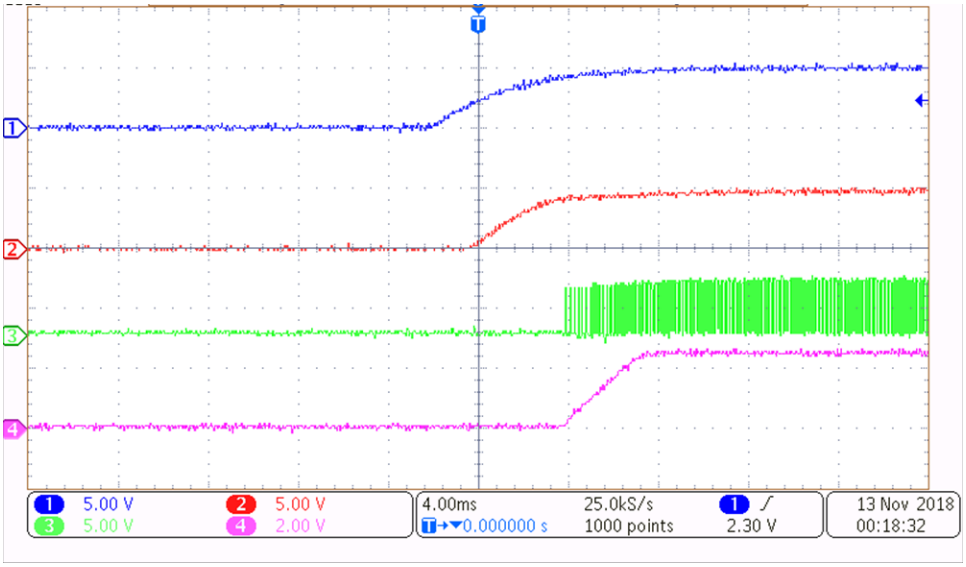


図 3. Start-up Waveform Full Load With Phase Node

表 4. Waveforms for 図 3

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	0 to 5 V
2	Output Voltage of Load Switch	0 to 5 V
3	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
4	Output Voltage of POL Converter	0 to 2.5 V

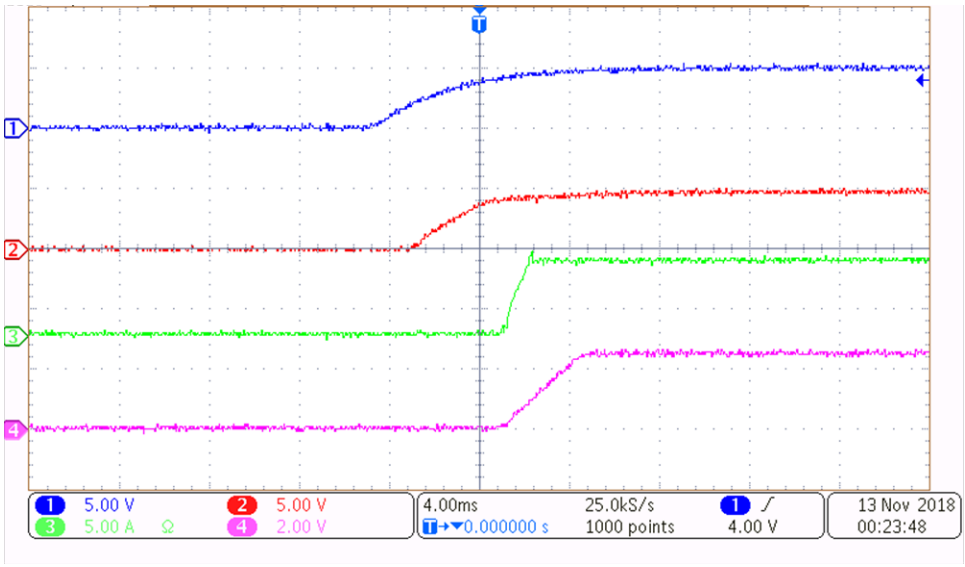


図 4. Start-up Waveform Full Load With Output Current

For the tests in 図 3 and 図 4, the input power to the load switch was ramped up with the load switch and the POL converter enabled. 6 A of current was drawn from the output of the POL converter.

表 5. Waveforms for 図 4

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	0 to 5 V
2	Output Voltage of Load Switch	0 to 5 V
3	Output Current of POL Converter	0 to 6 A
4	Output Voltage of POL Converter	0 to 2.5 V

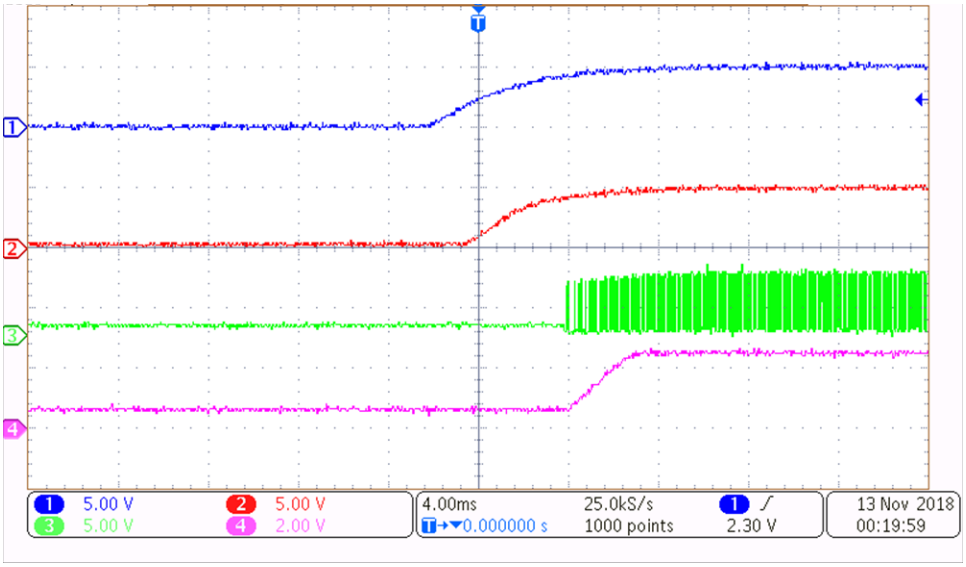


図 5. Start-up Waveform No Load With Phase Node

表 6. Waveforms for 図 5

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	0 to 5 V
2	Output Voltage of Load Switch	0 to 5 V
3	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
4	Output Voltage of POL Converter	0 to 2.5 V

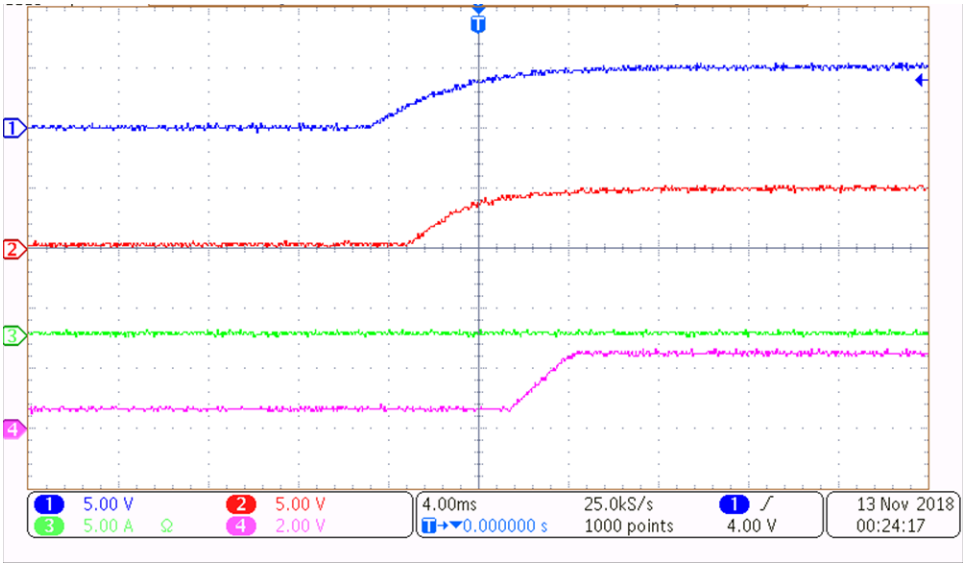


図 6. Start-up Waveform No Load With Output Current Node

For the tests in 図 5 and 図 6, the input power to the load switch was ramped up with the load switch and the POL converter enabled. 0 A of current was drawn from the output of the POL converter.

表 7. Waveforms for 図 6

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	0 to 5 V
2	Output Voltage of Load Switch	0 to 5 V
3	Output Current of POL Converter	0 A
4	Output Voltage of POL Converter	0 to 2.5 V

3.2.2.3 Shutdown

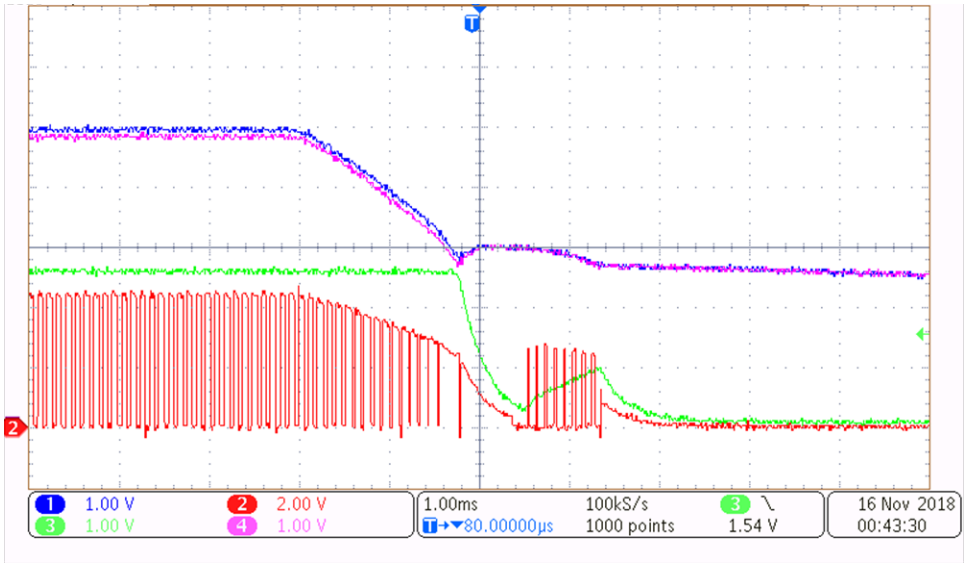


図 7. Shutdown Waveform Full Load With Phase Node

表 8. Waveforms for 図 7

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	5 to 2.5 V
2	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
3	Output Voltage of POL Converter	2.5 to 0 V
4	Output Voltage of Load Switch	5 to 2.5 V

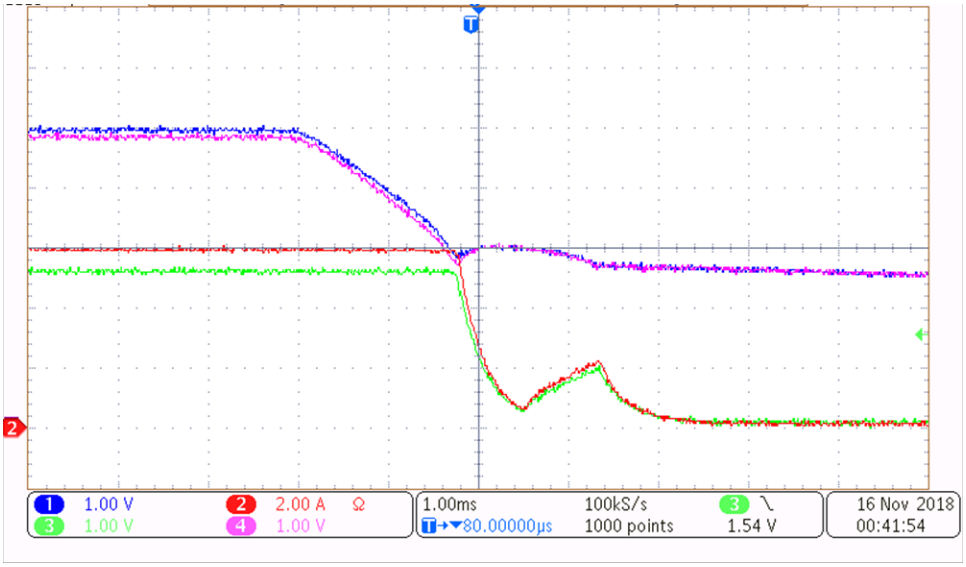


図 8. Shutdown Waveform Full Load With Output Current

For the test in 図 7 and 図 8, the input power to the load switch was ramped down. 6 A of current was drawn from the output of the POL converter using a resistive load. The input voltage of the POL converter dips below the UVLO and the device starts to turn off. The input voltage of the POL converter then starts to increase because of the large dip in output current. This increase causes the POL to switch a few times and discharge capacitors on the input of the POL converter.

表 9. Waveforms for 図 8

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	5 to 2.5 V
2	Output Current of POL Converter	6 to 0 A
3	Output Voltage of POL Converter	2.5 to 0 V
4	Output Voltage of Load Switch	5 to 2.5 V

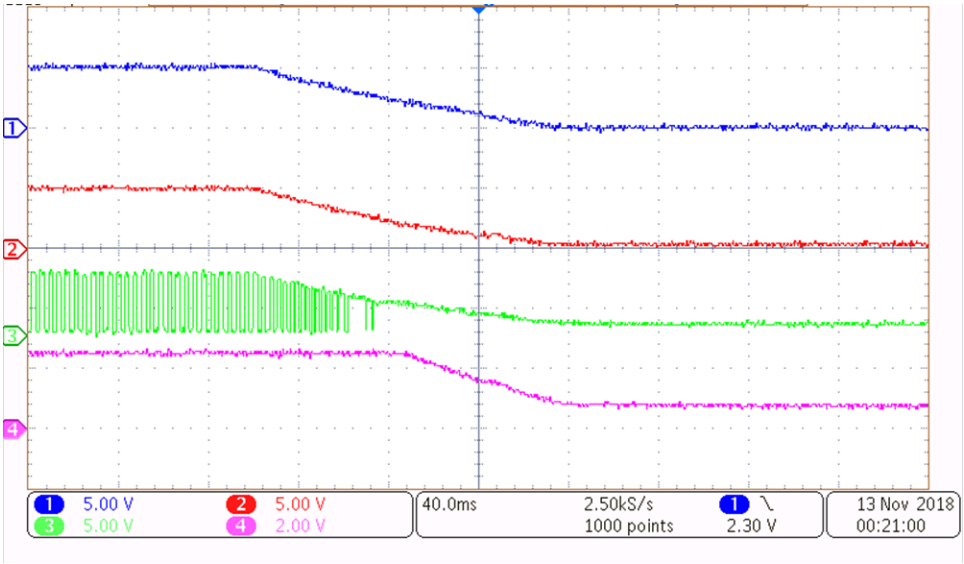


図 9. Shutdown Waveform No Load With Phase Node

表 10. Waveforms for 図 9

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	5 to 0 V
2	Output Voltage of Load Switch	5 to 0 V
3	Phase Node of POL Converter	5 to 0 V @ 100-kHz Switching Frequency
4	Output Voltage of POL Converter	2.5 to 0 V

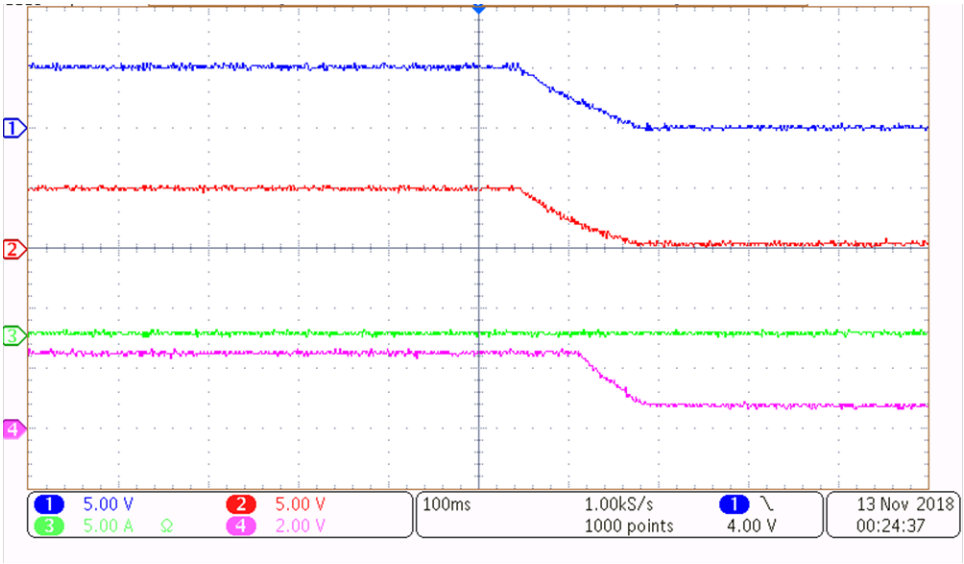


図 10. Shutdown Waveform No Load With Output Current

For the tests in 図 9 and 図 10, the input power to the load switch was ramped down. 0 A of current was drawn from the output of the POL converter.

表 11. Waveforms for図 10

Waveform Number	Signal	Values
1	Input Voltage to Load Switch	5 to 0 V
2	Output Voltage of Load Switch	5 to 0 V
3	Output Current of POL Converter	0 A
4	Output Voltage of POL Converter	2.5 to 0 V

3.2.2.4 Load Step

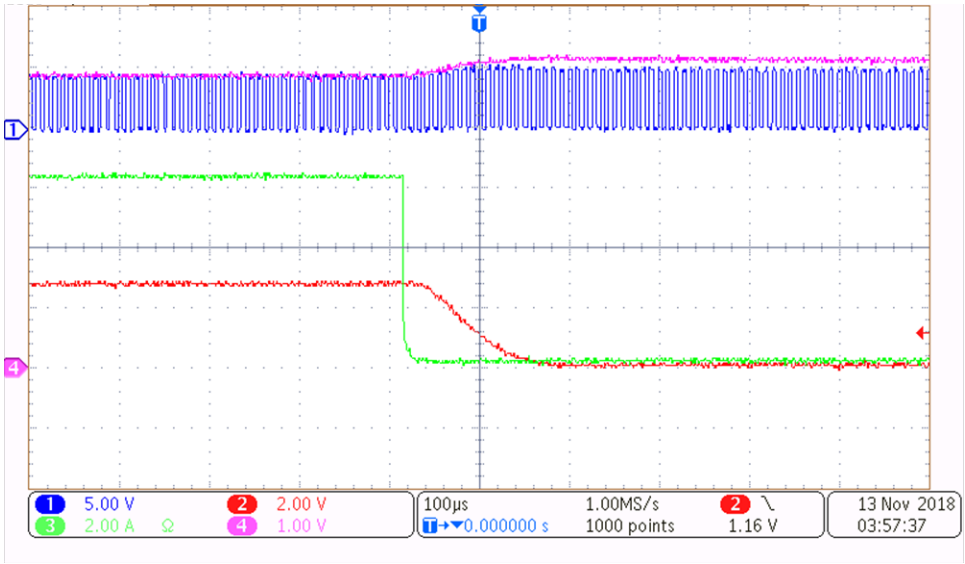


図 11. Negative Load Step With Phase Node

表 12. Waveforms for 図 11

Waveform Number	Signal	Values
1	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
2	CS Pin Voltage	2.36 to 0 V
3	Output Current of POL Converter	6 to 0 A
4	Output Voltage of Load Switch	4.8 to 5.2 V

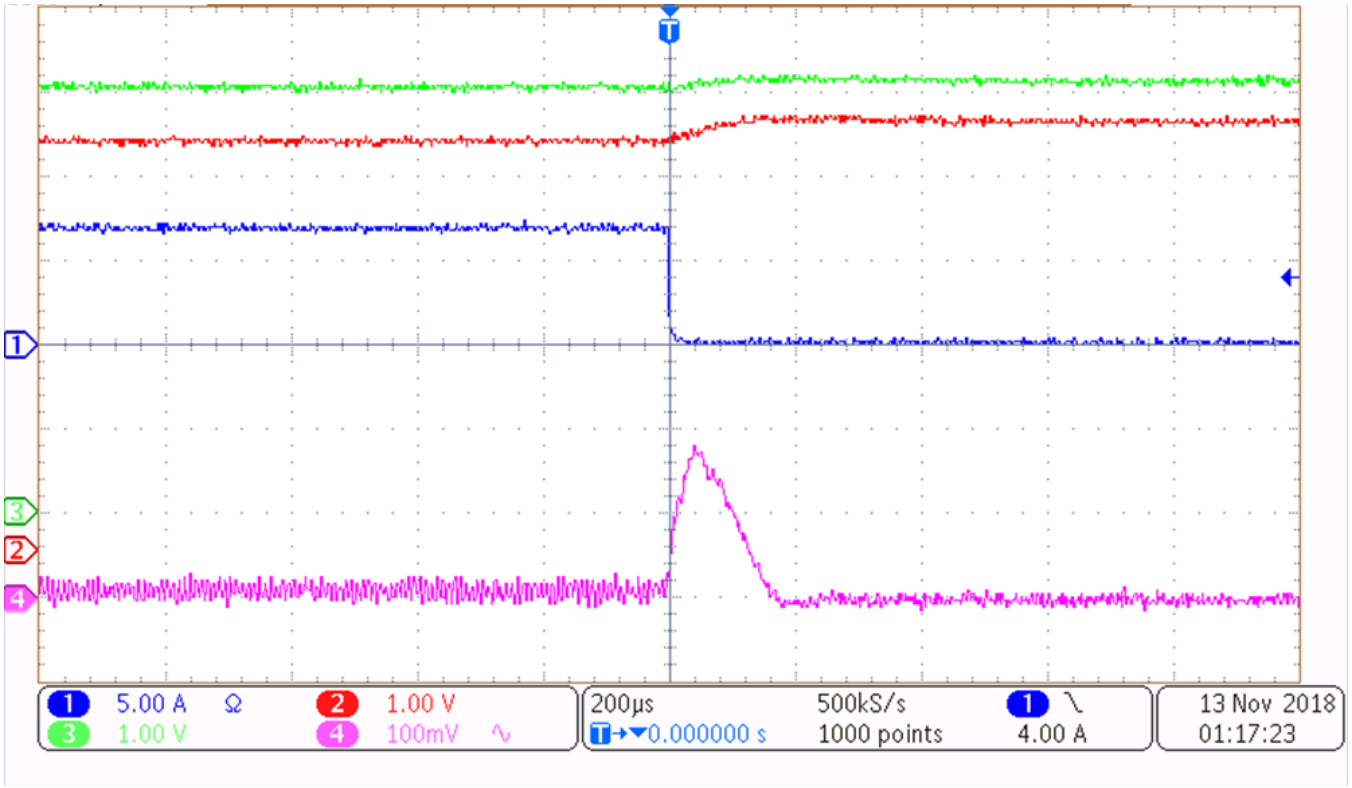


図 12. Negative Load Step With Input Voltage

For the tests in 図 11 and 図 12, the output current of the POL converter was stepped from 6 A to 0 A.

表 13. Waveforms for 図 12

Waveform Number	Signal	Values
1	Output Current of POL Converter	6 to 0 A
2	Output Voltage of Load Switch	4.8 to 5.2 V
3	Input Voltage of Load Switch	5 to 5.2 A
4	Output Voltage of POL Converter	170-mV Increase

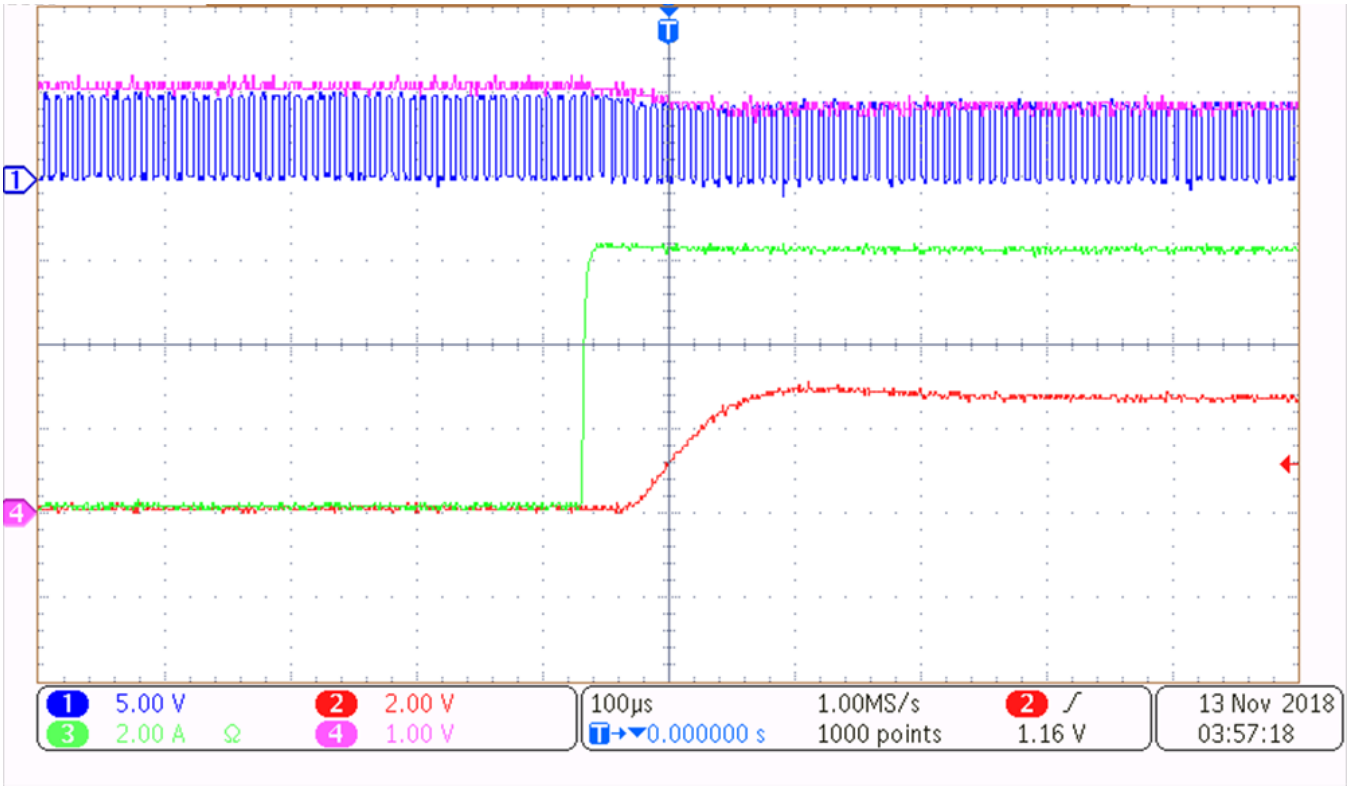


図 13. Positive Load Step With Phase Node

表 14. Waveforms for 図 13

Waveform Number	Signal	Values
1	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
2	Current Sense Pin of Load Switch	0 to 2.36 V
3	Output Current of POL Converter	0 to 6 A
4	Output Voltage of Load Switch	5.2 to 4.8 V

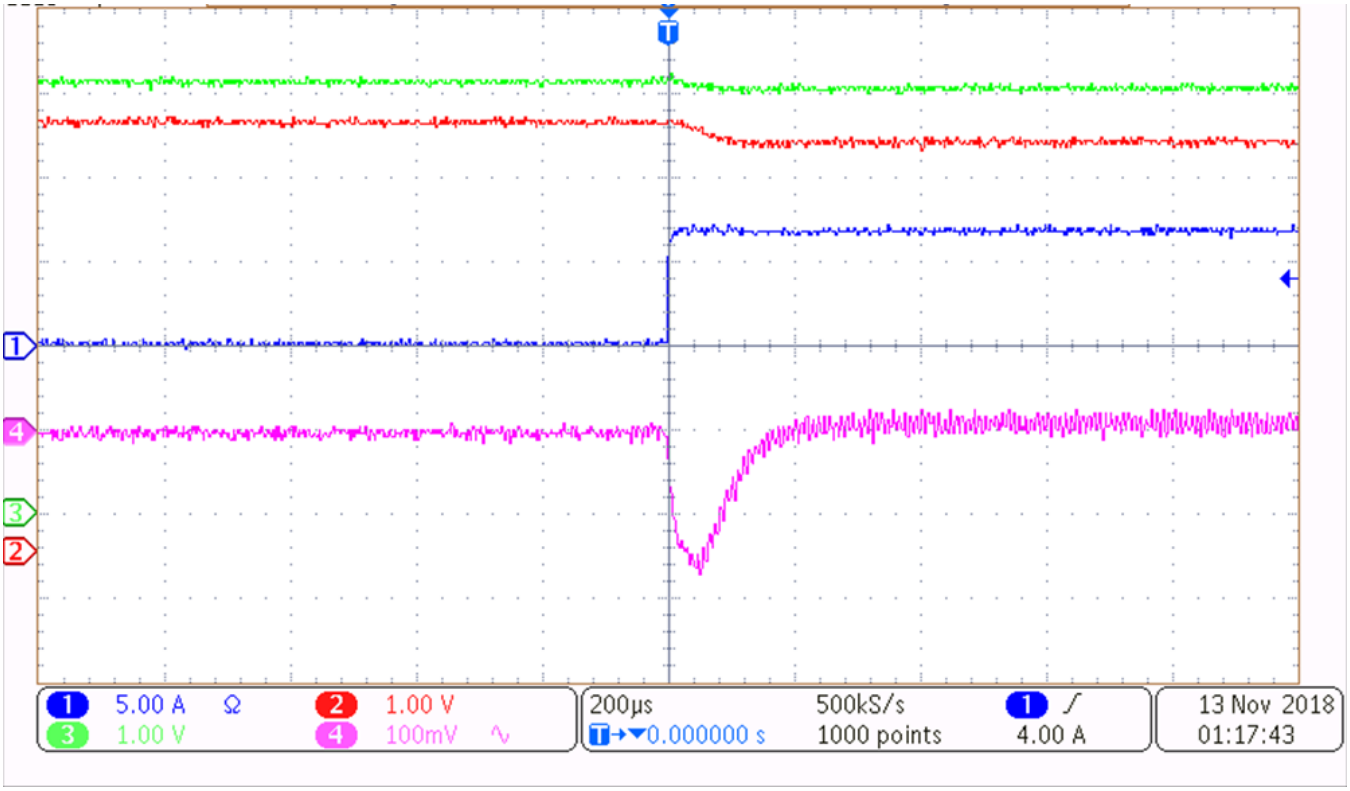


図 14. Positive Load Step With Input Voltage

For the tests in 図 13 and 図 14, the output current of the POL converter was stepped from 0 A to 6 A.

表 15. Waveforms for 図 14

Waveform Number	Signal	Values
1	Input Voltage of Load Switch	0 to 6 A
2	Output Voltage of Load Switch	5.2 to 4.8 V
3	Output Current of POL Converter	5.2 to 5 A
4	Output Voltage of POL Converter	180-mV Increase

3.2.2.5 Point of Load Converter Enable Toggle

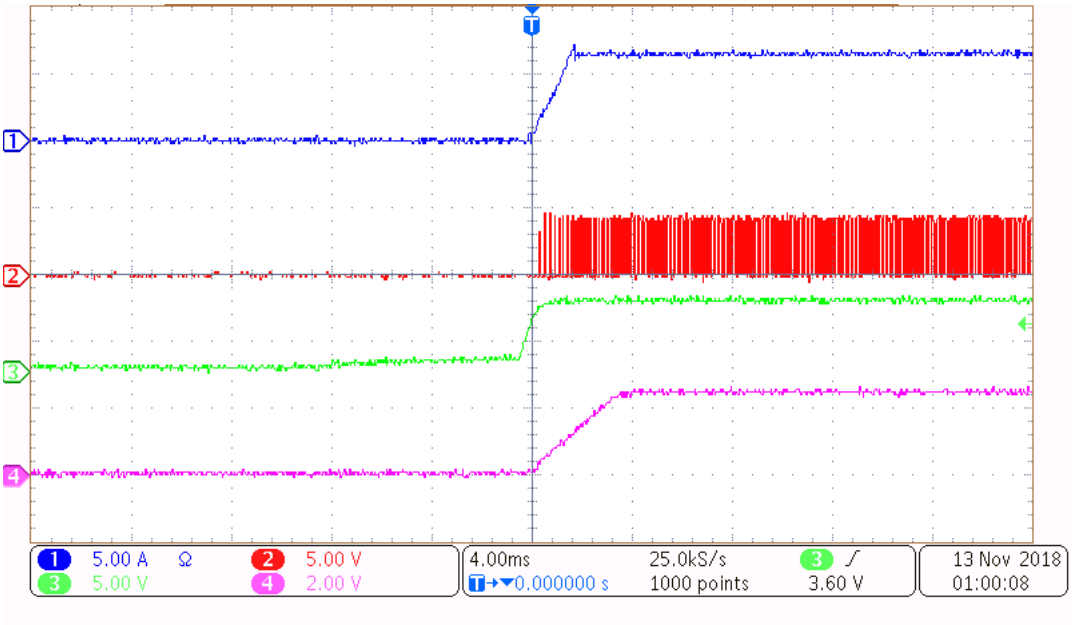


図 15. POL Enable Toggle High With Phase Node

表 16. Waveforms for 図 15

Waveform Number	Signal	Value
1	Output Current of POL Converter	0 to 6 A
2	Phase Node of POL Converter	4.8 V to 5 V
3	Enable Pin of POL Converter	5 to 0 V
4	Output Voltage of POL Converter	2.5 to 0 V

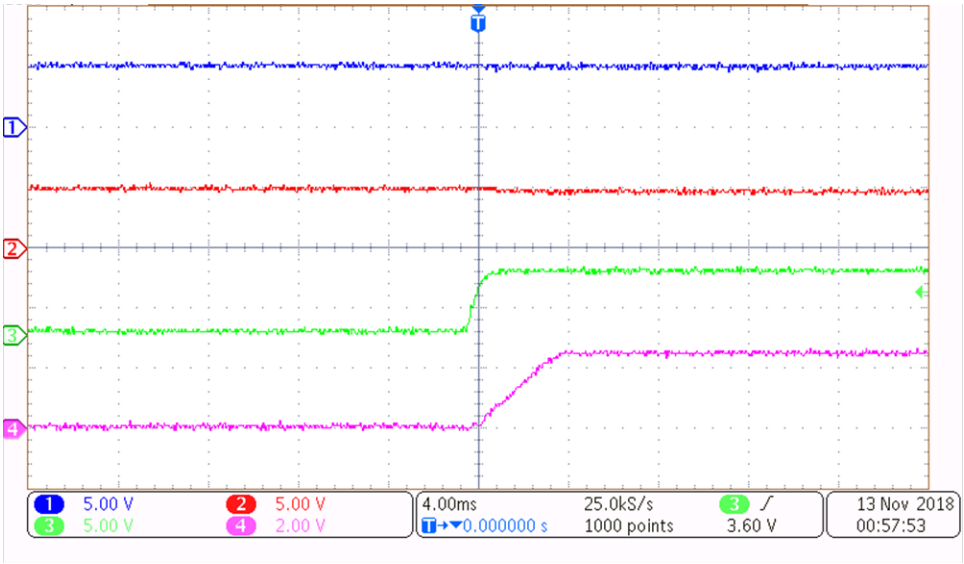


図 16. POL Enable Toggle High With Input Voltage

For tests in 図 15 and 図 16, the enable of the POL converter was brought high with the load switch already enabled.

表 17. Waveforms for 図 16

Waveform Number	Signal	Value
1	Input Voltage of Load Switch	5 V
2	Output Voltage of Load Switch	5 to 4.8 V
3	Enable Pin of POL Converter	0 to 5 V
4	Output Voltage of POL Converter	0 to 2.5 V

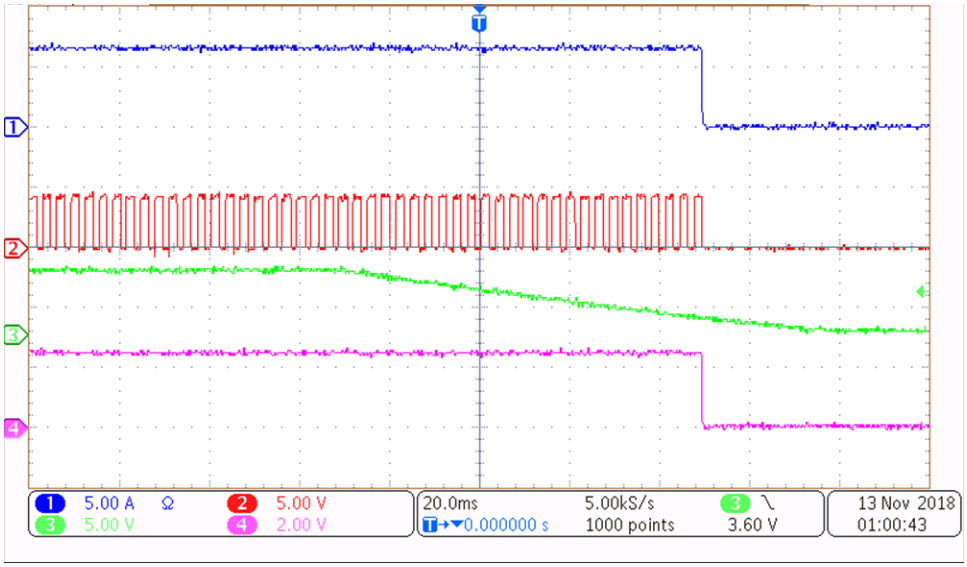


図 17. POL Enable Toggle Low With Phase Node

表 18. Waveforms for 図 17

Waveform Number	Signal	Value
1	Output Current of POL Converter	6 to 0 A
2	Phase Node of POL Converter	5 to 4.8 V
3	Enable Pin of POL Converter	0 to 5 V
4	Output Voltage of POL Converter	0 to 2.5 V

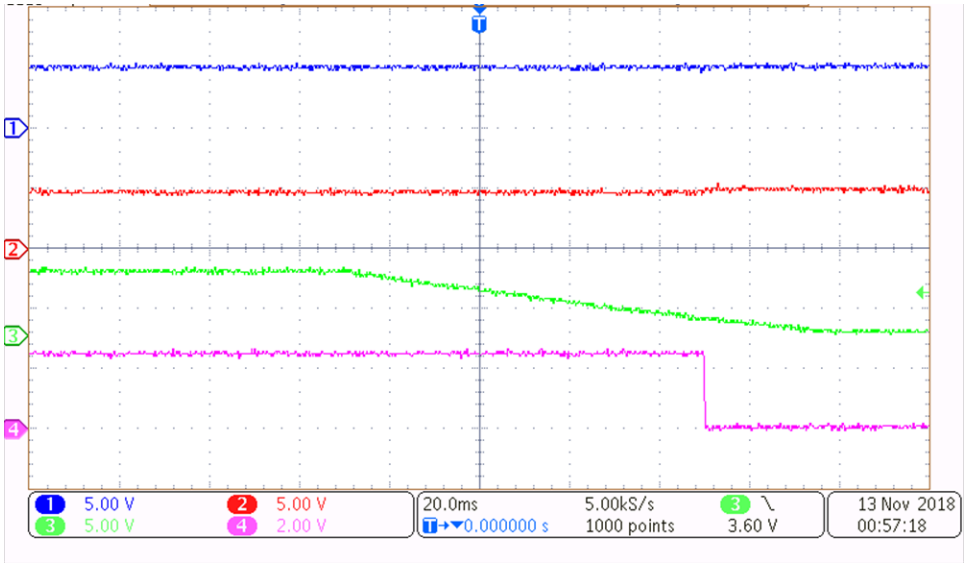


図 18. POL Enable Toggle Low With Input Voltage

For the tests in 図 17 and 図 18, the enable of the POL converter was brought low with the load switch enabled.

表 19. Waveforms for 図 18

Waveform Number	Signal	Value
1	Input Voltage of Load Switch	5 V
2	Output Voltage of POL Converter	4.8 to 5 V
3	Enable Pin of POL Converter	5 to 0 V
4	Output Voltage of POL Converter	2.5 to 0 V

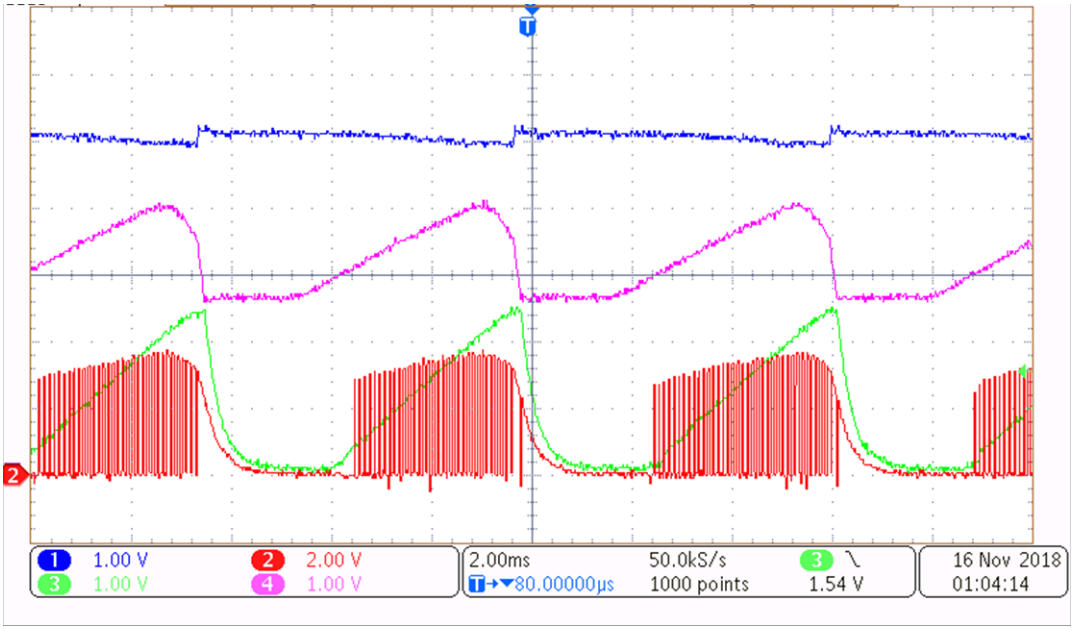


図 19. Load Switch Current Limit With Phase Node

表 20. Waveforms for 図 19

Waveform Number	Signal	Value
1	Input Voltage of Load Switch	5 and 5.2 V
2	Phase Node of POL Converter	0 to 4 V @ 100-kHz Switching Frequency
3	Output Voltage of POL Converter	0 to 2.5 V
4	Output Voltage of Load Switch	0.85 to 4 V

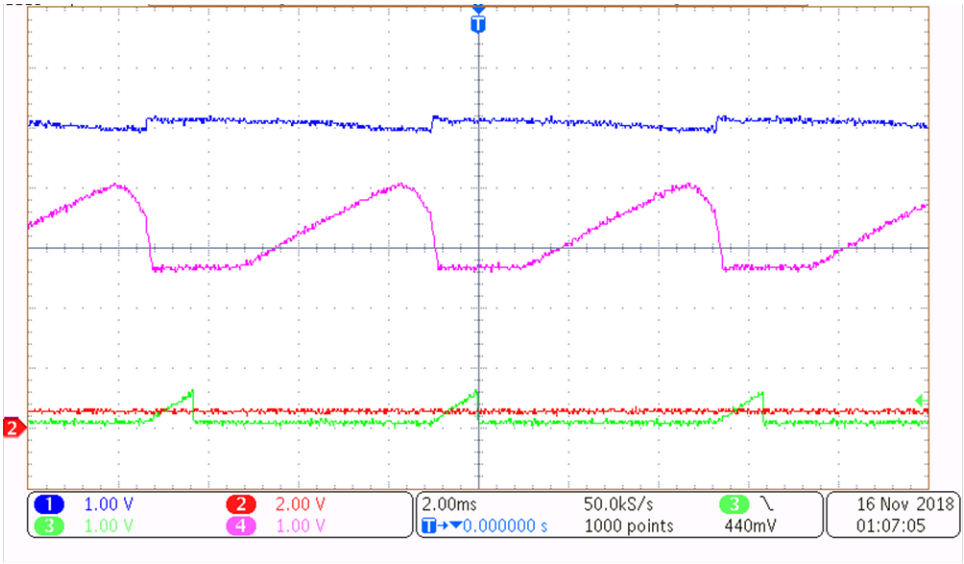


図 20. Load Switch Current Limit With Timer Pins

表 21. Waveforms for 図 20

Waveform Number	Signal	Value
1	Input Voltage of Load Switch	5 and 5.2 V
2	RLTimer Pin of Load Switch	0.5 V
3	ILTimer Pin of Load Switch	0 to 0.6 V
4	Output Voltage of Load Switch	0.85 to 4 V

For the tests in 図 19 and 図 20, the load switch current limit was set to 3 A by changing the IL resistor to 15.4 kΩ and the output current of the POL Converter was kept at 6 A. This behavior shown is the result of the load switch stopping current flow. Since the current flow is stopping the output voltage of the load switch will drop until it hits the undervoltage lockout of the POL converter. Once the undervoltage lockout of the POL converter is reached the POL converter will turn off stopping the short. Since the short on the output has stopped, the load switch will let current through again and increase the load switch output voltage. The output voltage of the load switch increases and turns on the POL converter. This process will repeat until either the short on the output goes away or one of the devices is disabled.

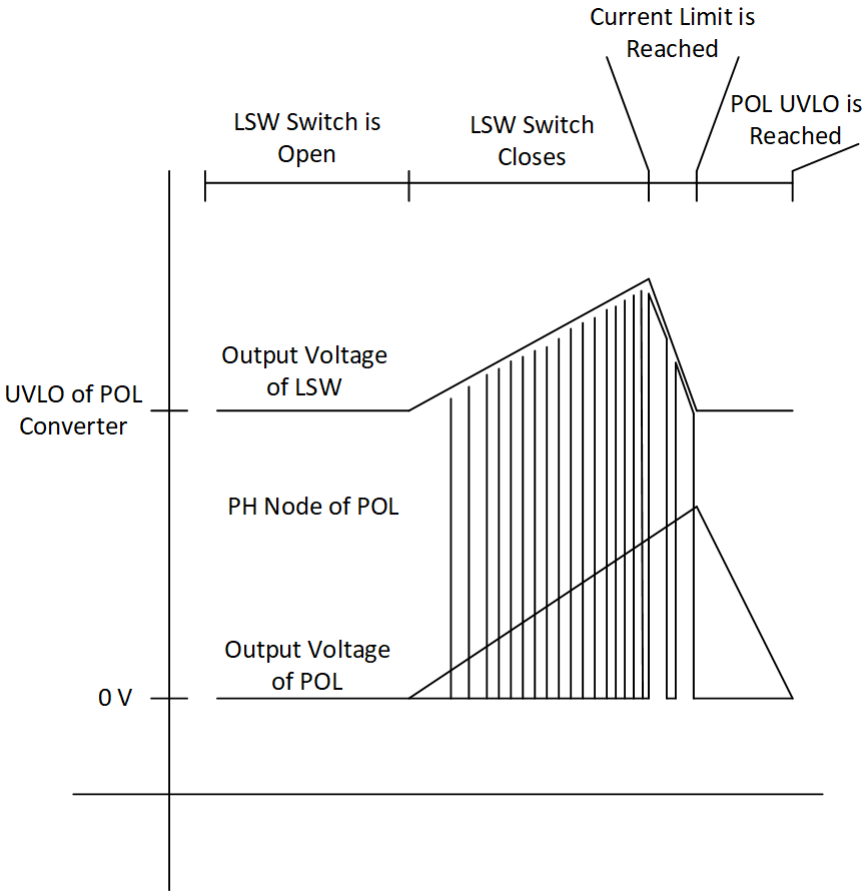


図 21. Breakdown of Load Switch Current Limit

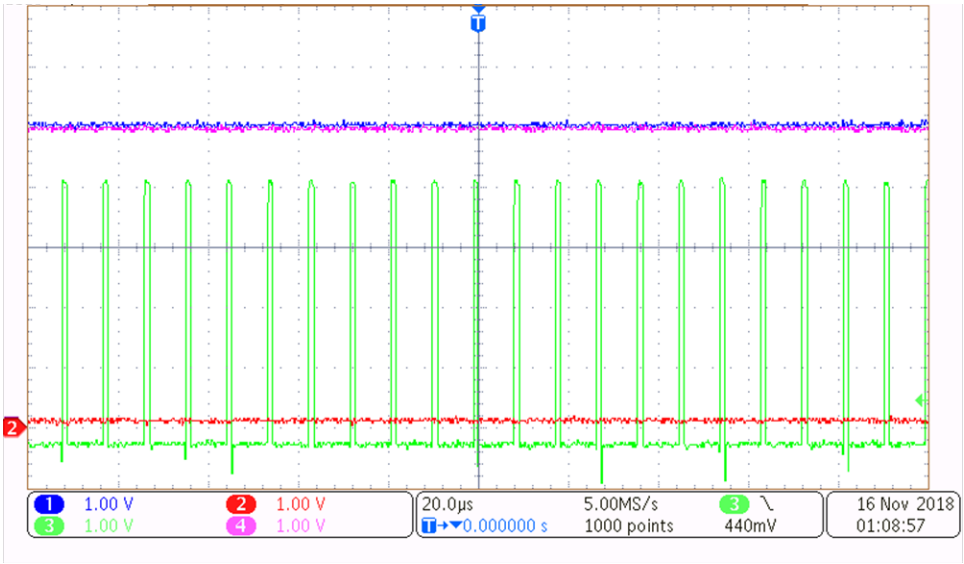


図 22. POL Current Limit With Phase Node

表 22. Waveforms for 図 22

Waveform Number	Signal	Values
1	Input Voltage of Load Switch	5 V
2	Output Voltage of POL Converter	0 V
3	Phase Node of POL Converter	0 to 5 V @ 100-kHz Switching Frequency
4	Output Voltage of Load Switch	5 V

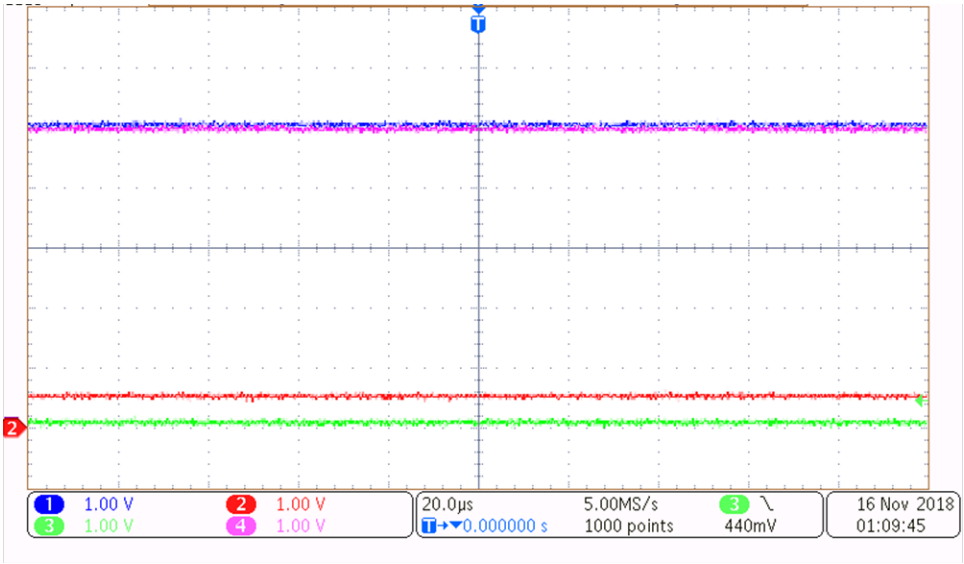


図 23. POL Current Limit With Timer Pins

In this test, the current limit of the load switch was set at 7.5 A. The POL converter has an internal current limit of 11 A to 13 A on the output that was tripped. This causes the POL converter to limit the input current to around 3 A with the output voltage of the POL converter dropping. Since the current limit of the POL converter limited the input current of the POL converter, the current limit of the load switch was not tripped and continued functioning. The duty cycle commanded will be determined by the minimum on time of the POL converter.

表 23. Waveforms for 図 23

Waveform Number	Signal	Values
1	Input Voltage of Load Switch	5 V
2	RLTimer Pin of Load Switch	0.5 V
3	ILTimer Pin of Load Switch	0 V
4	Output Voltage of Load Switch	5 V

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-070001.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-070001.

4.3 PCB Layout Recommendations

The TPS7H2201-SP EVM has power planes for VIN1, VIN2, VOUT, and GND on the top layer. Layers 2 and 3 are mostly all GND, with some signal routing on layer 3. Layer 4 contains more power planes for VIN1, VIN2, VOUT, and GND. Having multiple layers for each power plane allows for increased current carrying capacity and very low trace resistance. Vias are placed under the TPS7H2201-SP to allow for a thermal path from the top layer to the bottom layer.

For the TPS50601A-SP EVM that was used, it has PVIN, VIN, VOUT, and VPHASE all placed on the top layer. PVIN, VIN, and VOUT are also placed on the bottom of the board to increase current carrying capacity of the traces. The input decoupling capacitors (C8, C9, C10, C11, C12, C3, C4) are all located as close to the IC as possible. Placing the capacitors close is required to help with mitigating high frequency noise. The feedback resistors need to be placed as close to the FB pin as possible to prevent high frequency noise as well. The voltage set point divider, frequency set resistor, slow start capacitor, and compensation components are all routed to ground and placed close to a via to allow for high accuracy to the ground of the circuit board.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-070001.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-070001.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-070001.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-070001.

5 Related Documentation

1. *TPS7H2201-SP Radiation Hardened 1.5-V to 7-V, 6-A Load Switch*, SLVSDO0
2. *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter*, SLVSDF5

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年12月発行のものから更新 **Page**

- タイトルを「スイッチ付き入力の降圧コンバータのリファレンス・デザイン」から「OCP 用の冗長 eFuse 入力を持つ 3～7V_{IN}、宇宙グレード、ポイント・オブ・ロード (POL) のリファレンス・デザイン」に 変更 1
- 「概要」の段落 変更 1
- 「過電流制限、過電圧制限、入力電圧冗長性、ソフトスタート」を「可変の過電流保護 (OCP) 制限、可変の過電圧 (OVP) 制限、冗長化入力、構成可能なソフトスタート」に 変更 1
- FPGA、マイクロコントローラ、データ・コンバータ、ASIC 用の衛星電力分配、耐放射線強化アプリケーションと人工衛星ペイロード・アプリケーション 削除 1
- コマンドおよびデータ処理、衛星用電源システム (EPS)、光イメージング・ペイロード、レーダー・イメージング・ペイロード、通信ペイロード・アプリケーション 追加 1

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