参考資料

TI Designs: TIDA-010041
コンパレータまたはパワー・シーケンサとして使用する、広いV_{IN}（最大12V）のナノパワー・スーパーバイザのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、低消費電力リセットICとウォッチドッグ・タイマの各種使用例を紹介します。消費電流1µA未満のTPS3840デバイスは、コンパレータとして（単純な3ピン構成）、または汎用電源スーパーバイザとして（シーケンサとしてデイジー・チェーン接続が可能）動作するように構成できます。さらに、外付けコンデンサを使用して応答時間と遅延時間を設定できます。ウォッチドッグ動作が必要なアプリケーションでは、精度が±2.5%（標準値）のスタンドアロンのプログラム可能ウォッチドッグ・タイマとしてTPS3431デバイスを使用できます。

リソース

TIDA-010041	デザイン・フォルダ
TPS3840	プロダクト・フォルダ
TPS3431	プロダクト・フォルダ
TVS1400、TVS0500	プロダクト・フォルダ
OPA320	プロダクト・フォルダ
MSP432P4111	プロダクト・フォルダ

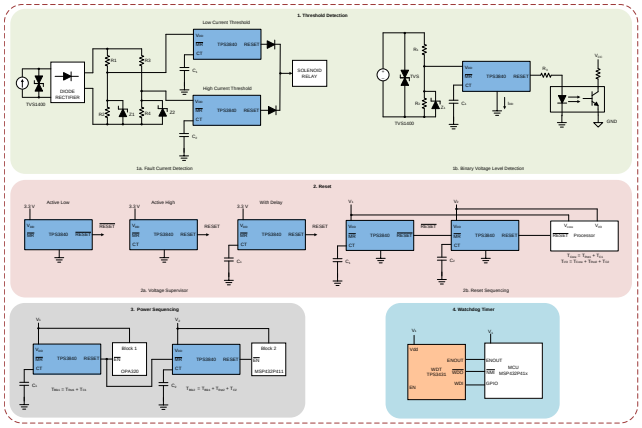
TI E2E™ Community　E2E™エキスパートに質問

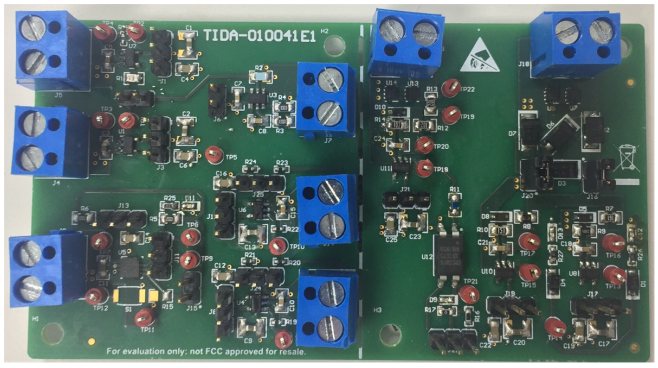
特長

- スレッショルド検出**(TPS3840)**：セルフパワーのスレッショルド検出器。電圧スーパーバイザをコンパレータ（3ピン構成で外部電源なし）として使用しています。
  - 超低静止電流（700nA未満）アーキテクチャ。スレッショルドを1.6V～4.9Vの範囲で0.1V刻みに設定でき、制御可能（外付けコンデンサにより80µs～600msの範囲）な応答時間で高速パワーオン（起動遅延250µs未満）が可能です。
- リセットによる電源管理およびシーケンシング**(TPS3840)**：マルチレール・リセット監視と起動シーケンシングに便利です。
  - アクティブLOWおよびアクティブHIGH構成。スレッショルド1.6V～4.9V、T_D80µs～600msで使用可能です。
- ウォッチドッグ・タイマ**(TPS3431)**：ユーザーが設定可能なタイマ。イネーブル・ピンを持ち、広い入力範囲に対応します。
  - 低消費電流：最大20µAでウォッチドッグ機能（外付け抵抗およびコンデンサでタイムアウトを設定可能）を実行します。

アプリケーション

- グリッド・インフラ
  - サーキット・ブレーカー：RCD、ACB、MCCB
  - PVインバータ、EV充電器
  - 変電所の自動化：保護リレー、スマート・メータ、フォルト・インジケータ、サーマル・ユニット
- ビルディング・オートメーション
- 家電製品





1 System Description

1.1 Threshold Detection

Some applications in grid infrastructure require threshold detection for safe and reliable operation of the end equipment. This could be monitoring for leakage current detection or for input voltage status detection.

Circuit Breaker: To prevent electrical hazards induced by leakage currents, circuit breakers are commonly used for detecting unsafe conditions by monitoring for any ground currents in a system. Such currents are continuously monitored as in a *Residual Current Detector* (RCD) and circuits tripped in the event when leakage currents exceeds certain thresholds. A key requirement for working of such equipment is the current consumption as they are always plugged in. As the fault current can cause severe damage or loss of life, the response time must be quick and the detection mechanism must be accurate and repeatable. They must have a smaller footprint because of the miniature size of the equipment.

EV Charger: Electric vehicles charged from EV charging stations (EVSE) through cables are required to have ground fault detection as a safety standard. These are often implemented either in EVSE or integrated within the charging cable. Leakage detectors should work for both AC and DC leakage currents.

Protection Relay: In addition to monitoring line voltages and currents, protection relay is used for voltage status detection. In particular, a *Digital Input Module* and *Binary Input Module* are used for battery monitoring, status indication, diagnostics, fault indication and changing configuration in applications such as substation battery monitoring, substation interlocking, breaker status indication, and so forth. The voltage threshold detector should be able to detect when the input voltage crosses certain threshold. A simple way of isolating between channels is required when multiple inputs are to be monitored.

1.2 Reset for Power Supply Supervision and Sequencing

A vast majority of the applications in grid use a micro-controller or micro-processor for processing input and output conditions. When the supply voltage dips below a certain threshold, the processor must be put in the reset condition from where it is able to restore critical settings and application data on power recovery.

Fault Indicator, Smart Meters, Monitoring Relay, Circuit Breaker: These applications predominantly use micro-controllers for their processing needs. It is not uncommon to loose system power in these equipment in the event of faults. Losing the settings and application data can be detrimental on subsequent processor restore. For this reason, supply voltage supervisor comes in handy to put the micro-controller in the reset configuration. Also, such a supervisor should operate at very low current levels during reset condition.

Multi-Function Relay, Terminal Units, EVSE, Data Concentrator: Applications requiring more processing bandwidth use micro-processors for their processing needs. Low power voltage supervisor is commonly used to prevent the processor from latching up by controlling the startup sequence as there are multiple rails that could turn-on at various time intervals.

1.3 Watchdog Timer

One of the ways to ensure reliable operation of micro-controllers in safety applications is for micro-controller to generate a periodic pulse signal. Watchdog timers are used to monitor such signals at regular intervals. A reset signal is asserted by the watchdog in the absence of a pulse. System designers need to be able to program the time window within reasonable accuracy while the part consumes low current.

The TIDA-010041 showcases the simplest configuration for:

- Voltage and current threshold detector using 3-pin configuration without using extra power supply
- Supply voltage supervisor for monitoring for voltage dips to prevent MCU or processor latch-up
- Sequencing of various blocks and subsystems during power-on condition to avoid damage to device
- Low power standalone watchdog timer

1.4 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Current threshold detection (RCD)	Threshold current: 30 mA, 300 mA	2.4.1
	Trip timing: 600 ms (30 mA), 6 ms (300 mA)	3.2.2.1
Voltage threshold detection (D/BIM)	Input voltage range: 0 V–20 V DC input resistance: 3 kΩ at 20 V DC	2.4.1
	Threshold voltage: 10 V DC	
	Hysteresis: 500 mV	3.2.2.1
	Current consumption: 4 mA at 20 V	3.2.2.1
	Isolation voltage: 5 kV_{RMS}	
Reset, power sequencing	Threshold voltage: 2.7 V	2.4.2
	Accuracy: 1% Typical (±2.5 % over -40°C to 125°C)	
Watchdog timer	Configuration 1: 10 kΩ between CWD and V_{DD}, timeout: 200 ms	2.4.4
	Configuration 2: CWD unconnected, Timeout: 1600 ms	
	Configuration 3: 10-nF capacitor between CWD and GND, timeout: 830 ms	

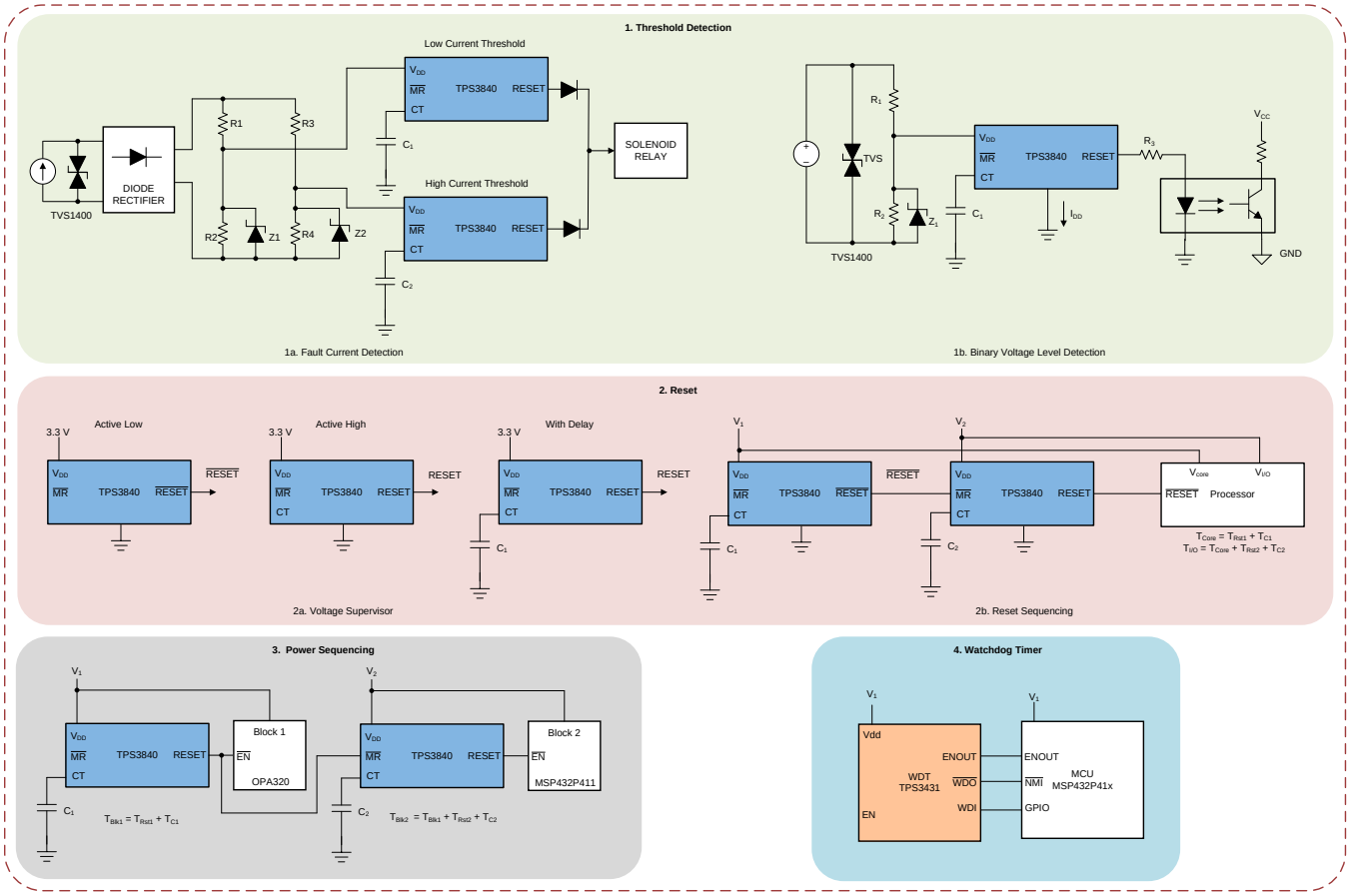
2 System Overview

2.1 Block Diagram

図 1 shows the TIDA-010041 block diagram highlighting the following four implementations:

- Threshold detection for overvoltage and current level
- Supply voltage supervision using RESET function
- Power sequencing
- Watchdog timer

図 1. TIDA-010041 Block Diagram



2.2 Design Considerations

Some of the key considerations for design of the TIDA-010041 are:

- Designing of fault current detection for the specified current threshold levels with an accurate response time
- Designing binary voltage level detector for the given input voltage range, threshold level and optimizing the overall power consumption
- Configuring supply voltage supervisors for different output stage requirements and delay timing
- Timing requirement for startup of multi-rail power supply or powering of different subsystems

2.3 Highlighted Products

This section provides details of some of the TI products used in this TI design.

2.3.1 TPS3840

The TPS3840 are family of voltage supervisors or reset part that offers voltage threshold detection while maintaining very low quiescent current. This part available in three different output configurations making it useful in variety of applications providing best combination of low power consumption, high threshold accuracy and low propagation delay. While configured for threshold detection, this simplifies the circuit design while using only three pins without the need of external power supply.

For more details, see the TPS3840 product page.

2.3.2 TPS3431

The TPS3431 device is a standard programmable watchdog timer with an enable feature for a wide variety of applications. The watchdog timeout features a 15% accuracy, high-precision timing (–40°C to +125°C) and 2.5% typical at 25ºC. The watchdog timeout can be programmed either by an external capacitor, or by factory-programmed default delay settings. The watchdog can be disabled via the Enable pin or the SET logic pins to avoid undesired watchdog timeouts during the development process.

For more details, see the *TPS3431 Standard Programmable Watchdog Timer with Enable* data sheet.

2.3.3 TVS1400, TVS0500

The TVSXX00 family of devices robustly shunts up to 43 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ±2 kV IEC 61000- 4-5 open circuit voltage coupled through a 42-Ω impedance. The TVS1400 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 20 V. Whereas, the TVS0500 device can clamp the voltage to below 10 V. The tight voltage regulation at the input ensures safe operation of the TPS3840 device by limiting the input voltage to below 12 V.

See *ESD protection & TVS surge diodes – Products* for more details on flat-clamp surge protection diodes.

2.3.4 OPA320

The OPA320 device is a precision, low-voltage CMOS operational amplifiers featuring rail-to-rail input operation optimized for very low noise e (7 nV/$\sqrt{\text{Hz}}$) and wide bandwidth (typical 20 MHz) while consuming very low quiescent current of 1.45 mA suitable for driving analog to digital converters (ADCs), signal conditioning and sensor amplification. The OPA320S device has a shutdown (enable) pin that can be used to further reduce the power consumption when the circuit is unused. This can also be used for power sequencing.

For more details, see the *OPAx320x Precision, 20-MHz, 0.9-pA, Low-Noise, RRIO, CMOS Operational Amplifier With Shutdown* data sheet.

2.3.5 MSP432P4111

The SimpleLink™ MSP432P4111 is a mixed-signal microcontroller that is optimized as wireless host MCUs with an integrated 16-bit precision ADC, delivering ultra-low-power performance including 100 µA/MHz in active power and 820 nA in standby power with FPU and DSP extensions. MSP432P411x MCUs are supported by a comprehensive ecosystem of tools, software, documentation, training, and support to get your development started quickly.

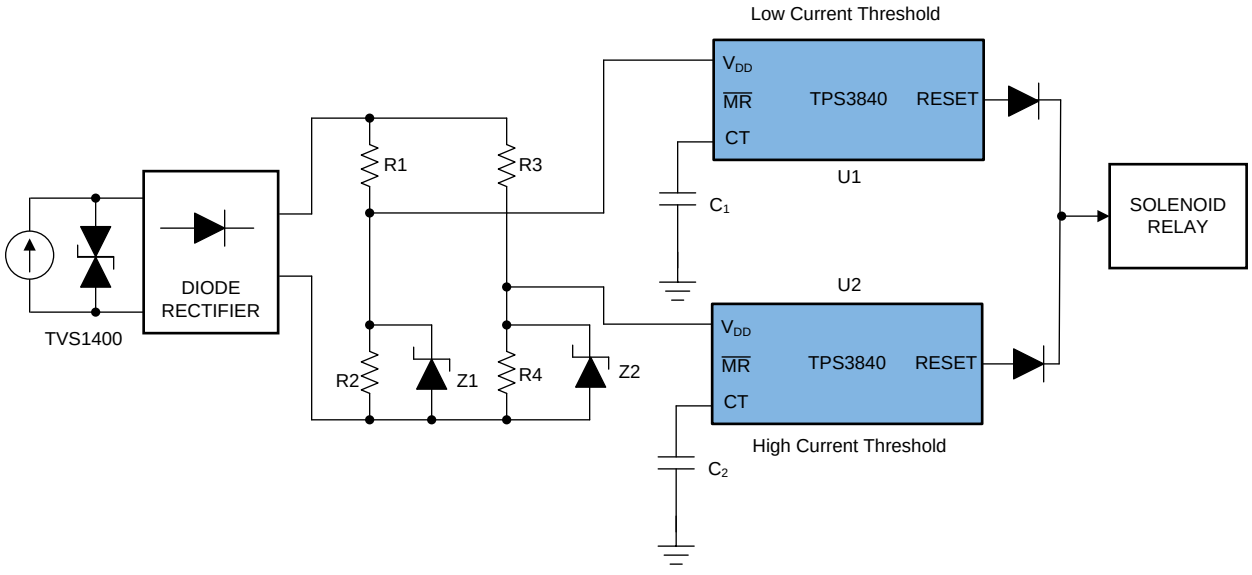
2.4 System Design Theory

2.4.1 Threshold Detection

This reference design simplifies the circuit implementation for threshold level detection. If the input to the system is a current source, as in a RCD, then current needs to be converted to voltage before comparing it with a reference. If the input to the system is a voltage source, then the input voltage needs to be attenuated according to the input voltage range. Monitoring for fault current or voltages is discussed in the following sections.

Fault current detection: In a typical leakage current detection system, ground leakage current is measured by sensing difference between incoming and outgoing current which is I_L - I_N. In this implementation, the input to the system is a current source which could be from a current sensor such as differential current transformer (CT) or ZCT. Output from the CT needs to be protected against sensor open condition using surge clamp diodes. Diode rectifier is used to rectify the AC signal to DC. Standards mandate various tripping times for different currents. In this design, two branches are shown in 図 2 with different response times for two current values.

図 2. Block Diagram for Multi-Branch Overcurrent Detection



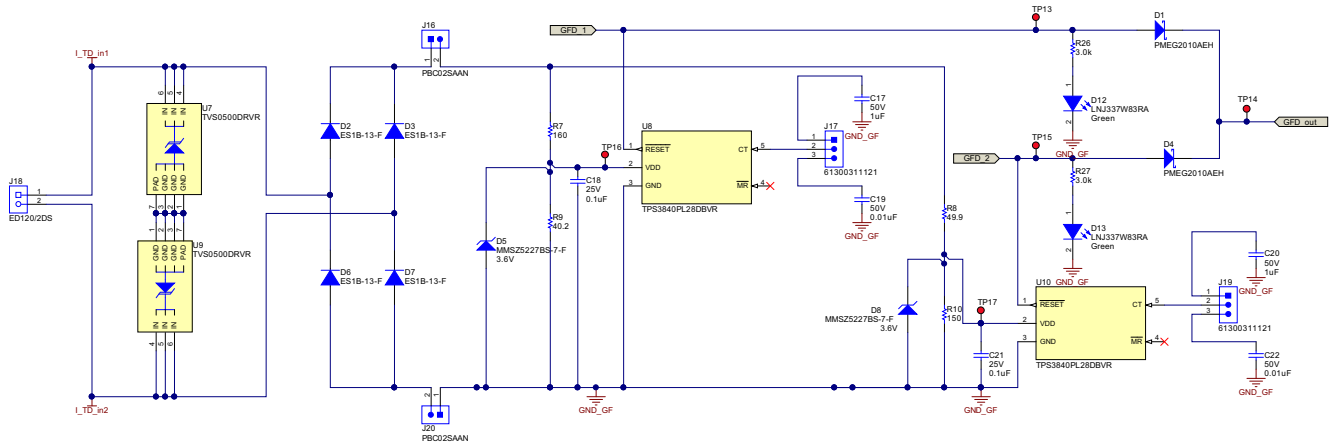
This can be designed for two different input current threshold values with different response times. This has two pairs of resistor dividers (R1-R2 and R3-R4) which correspond to two different levels of current thresholds. Threshold levels are detected using nano power voltage supervisor, TPS3840 in active-low configuration which gives high output when its V_{DD} reaches above the threshold voltage, V_{TH}. Selection of R1 and R2 are done such that voltage drop across R2 reaches the threshold value (V_{TH}) of U1 when the input current is at the lower current threshold. This ensures U1 taking action when the input current

reaches this threshold value. On the second branch, R3 and R4 are selected in such a way that voltage drop across R4 reaches V_{TH} of U2 when the input current reaches high current threshold value. Zener diodes, Z1 and Z2 are used across the V_{DD} of the TPS3840 device to prevent the voltages going above the safe operating level which is 10 V. This also enables to achieve higher ratio between lower and higher current threshold levels. Response times of the two branches are designed by selecting appropriate value of capacitance at the CT pin of U1 and U2. Capacitor values are calculated using 式 1.

$$T_D = 618937 \times C_{CT\_EXT} + 80\ \mu s \quad (1)$$

$$C_{CT\_EXT} = (T_D - 80\ \mu s) \div 618937 \quad (2)$$

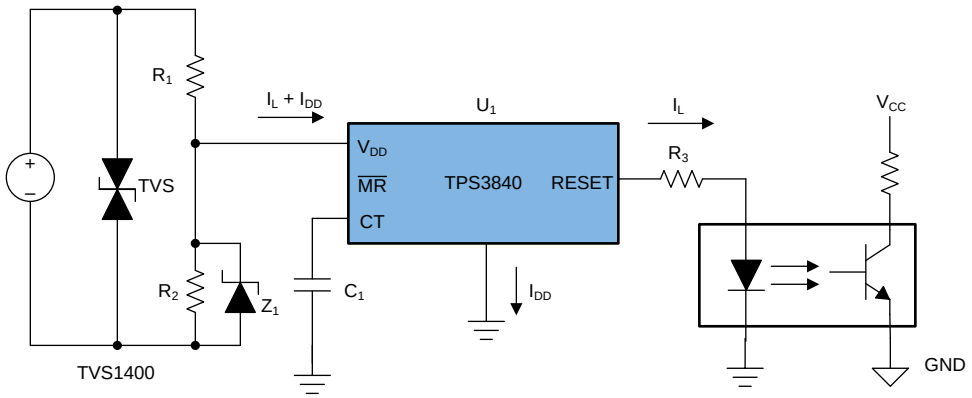
図 3. Circuit Diagram Showcasing Overcurrent Detection



Binary Voltage Level Detection: This section implements an overvoltage detection scheme using voltage supervisor. This is a generic architecture that can be used DC input. 図 4 shows a block diagram for both monitoring and isolating the output using an opto-coupler for a digital input module or binary input module. Input terminals are protected from lightning strikes, power source fluctuations using flat clamp surge protection diodes.

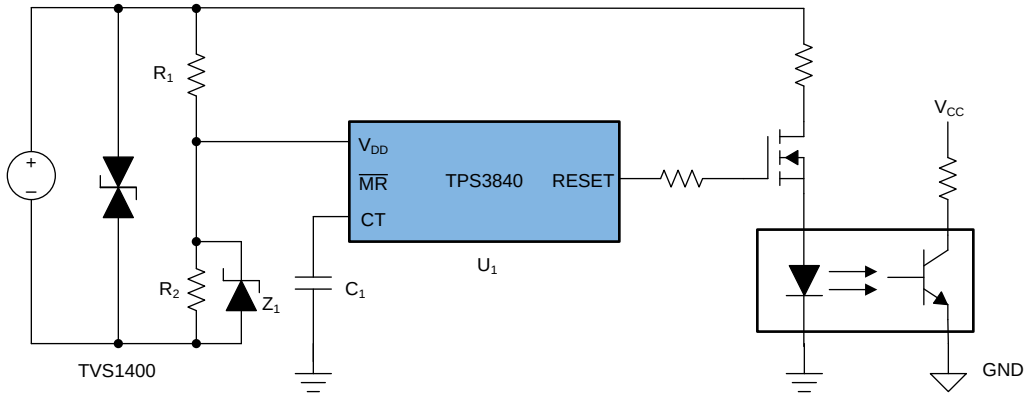
The voltage divider (R_1, R_2) can be estimated based on the voltage that needs to be monitored and the input voltage range of the TPS3840 device. The choice of the TPS3840 threshold is dependent on the ratio of input voltage threshold to the maximum monitoring voltage. Resistor R_3 is selected to provide enough bias current to the opto-coupler to trigger. The opto-coupler transmits the binary output signal across the isolation barrier.

図 4. Block Diagram for Binary Voltage Detection With Isolation



A slight modification is needed for the circuit shown in 図 4 as the load current I_L changes when the reset changes its state (when input goes above threshold in this case). This additional current introduces an error as it has to flow-through resistor R_1. To overcome this error, the load current that appears only when reset is high is routed through an alternate path using a switch and a resistor as 図 5 shows.

図 5. Alternate Circuit to Address Hysteresis Issue



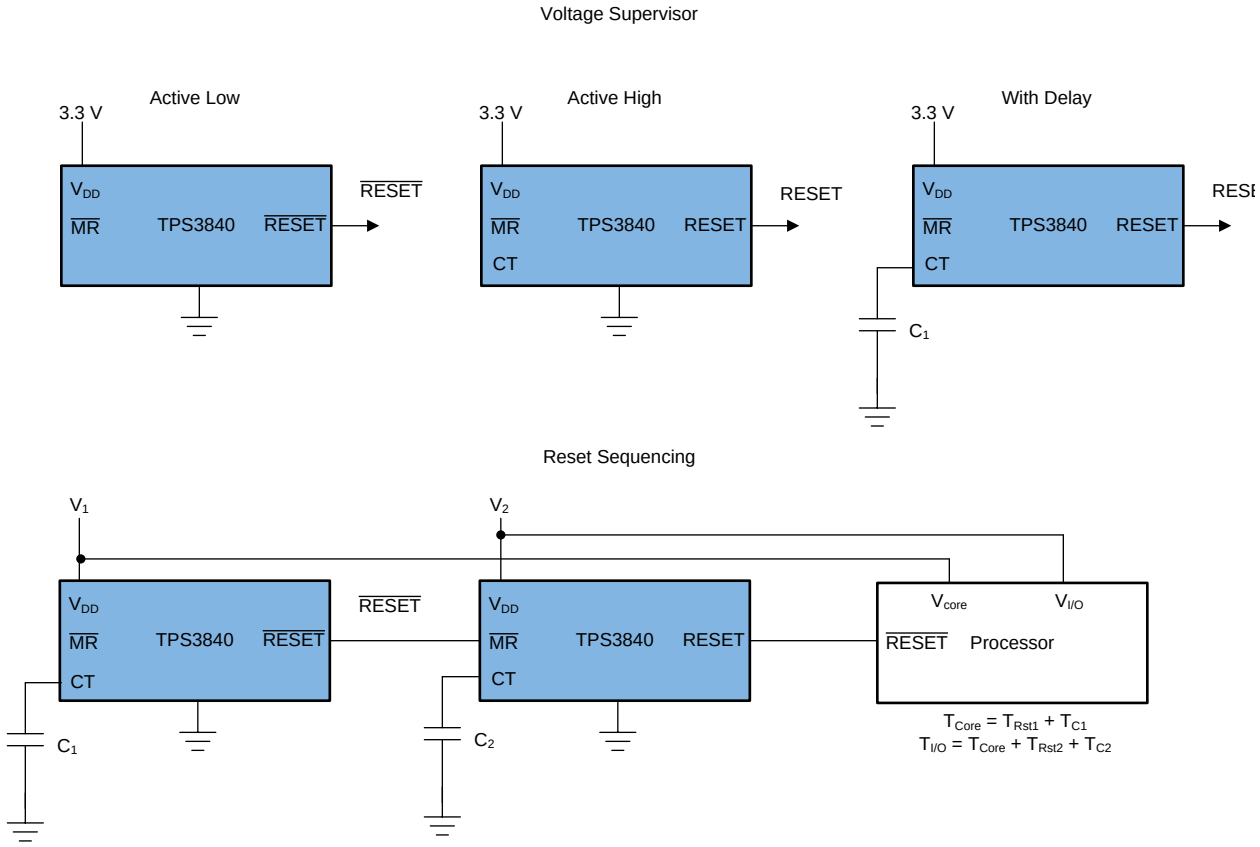
2.4.2 Voltage Supervision (RESET)

Voltage supervisors are used to ensure reliable functioning of a microprocessor or microcontroller during power supply dips and startup. This can be implemented either as an active high or active low signal.

Active low: RESET is asserted (low) when the input (V_{DD}) is below the threshold. It is de-asserted (high) when the input exceeds the threshold and the $\overline{MR}$ pin is above $V_{\overline{MR}\_H}$ or is left floating. There are two output options: open drain and push-pull. The open drain requires a pullup resistor to hold the RESET pin high. RESET can be pulled to any voltage up to 10 V, independent of the input voltage. In the push-pull configuration, RESET pin can only go as high as the input voltage due to absence of pullup resistor.

Active high: RESET is asserted (high) when the input is below the threshold. It is de-asserted (low) when the input exceeds the threshold and when the $\overline{MR}$ pin is above $V_{\overline{MR}\_H}$ or is left floating. This is available only in push-pull configuration.

図 6. Block Diagram Showcasing Different use Cases of Voltage Supervision



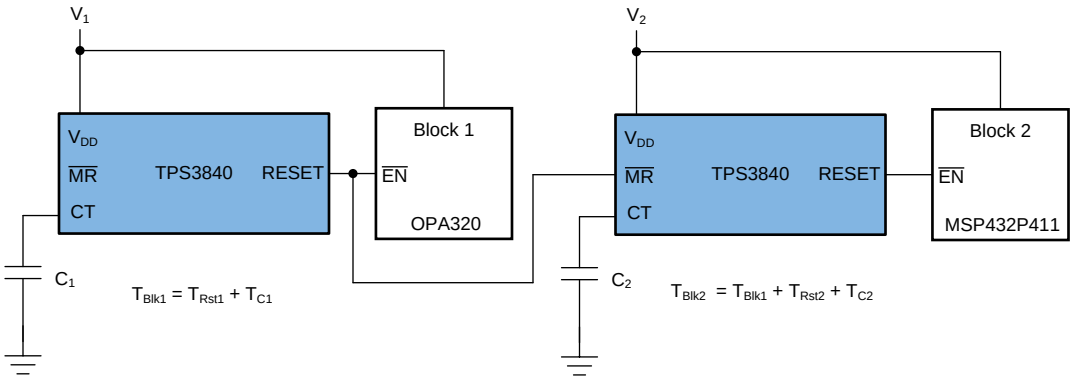
For the previous configurations, delay can be introduced by adding a suitable capacitor at the CT pin. The value of the capacitor is calculated using 式 1.

The voltage supervisor can also be used as a sequencer when multiple voltage rails are to be monitored as in the case of a processor. For example, if the separate voltage rails for the core and I/Os (input/outputs) have a different startup sequence, a voltage supervisor can be sequenced by cascading two in a daisy-chain mode as 図 6 shows. The variable delay between the two power supply startups can be compensated by choosing the right value of capacitors C_1 and C_2.

2.4.3 Power Sequencing

In applications having multiple subsystems powered by separate rails with different startup sequence, the previous concept is extended to control the powering on of different blocks. 図 7 illustrates this model.

図 7. Block Diagram for Demonstrating Power Sequencing



2.4.4 Watchdog Timer

With a watchdog timer such as the TPS3431 device, high-precision time control and the choice between fixed factory-programmed timing or user-programmable timing is available.

- Configuration 1: In this configuration, a 10-kΩ resistor is connected between CWD and V_{DD} of the part resulting in a standard watchdog timeout of 200 ms (170 ms to 230 ms)
- Configuration 2: If the CWD pin of the TPS3431 device is unconnected, a fixed watchdog timeout of 1600 ms (1360 ms to 1840 ms) can be obtained.
- Configuration 3: In this configuration, an user-programmable timeout delay is obtained by connecting a capacitor of desired value at the CWD pin. Relationship between the timeout delay and the capacitor value is given by, t_{WD} (ms) = 77.4 × C_{CWD} (nF) + 55 (ms)

図 8. Three Configurations of TPS3431 for Selecting the Timeout Delay

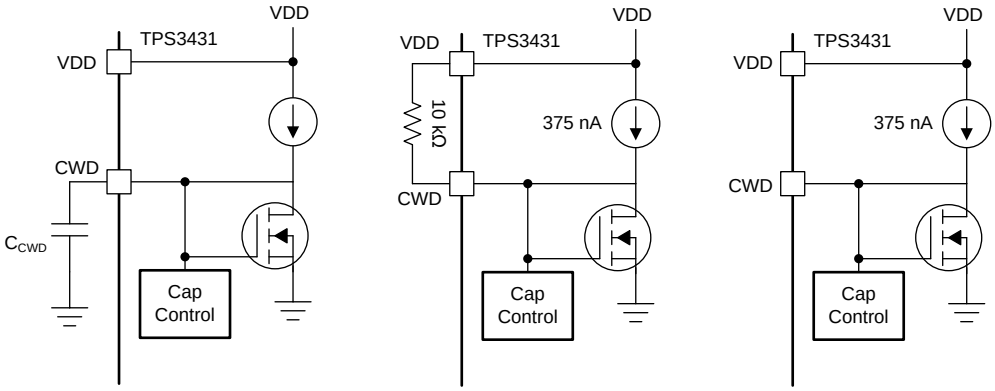
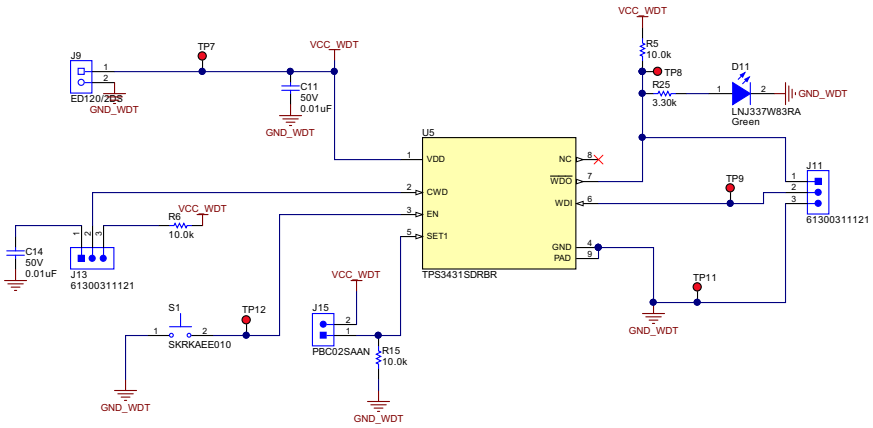


図 9. Circuit Diagram for Watchdog Timer



3 Hardware, Software, Testing Requirements, and Test Results

This section provides information on connecting this reference design for functional and performance testing. Developers can set up this platform to develop the application and evaluate the performance such as voltage threshold, response timing, and power consumption for different modes of applications.

3.1 Required Hardware and Software

3.1.1 Hardware

The following setup is required for the functional testing of TIDA-010041:

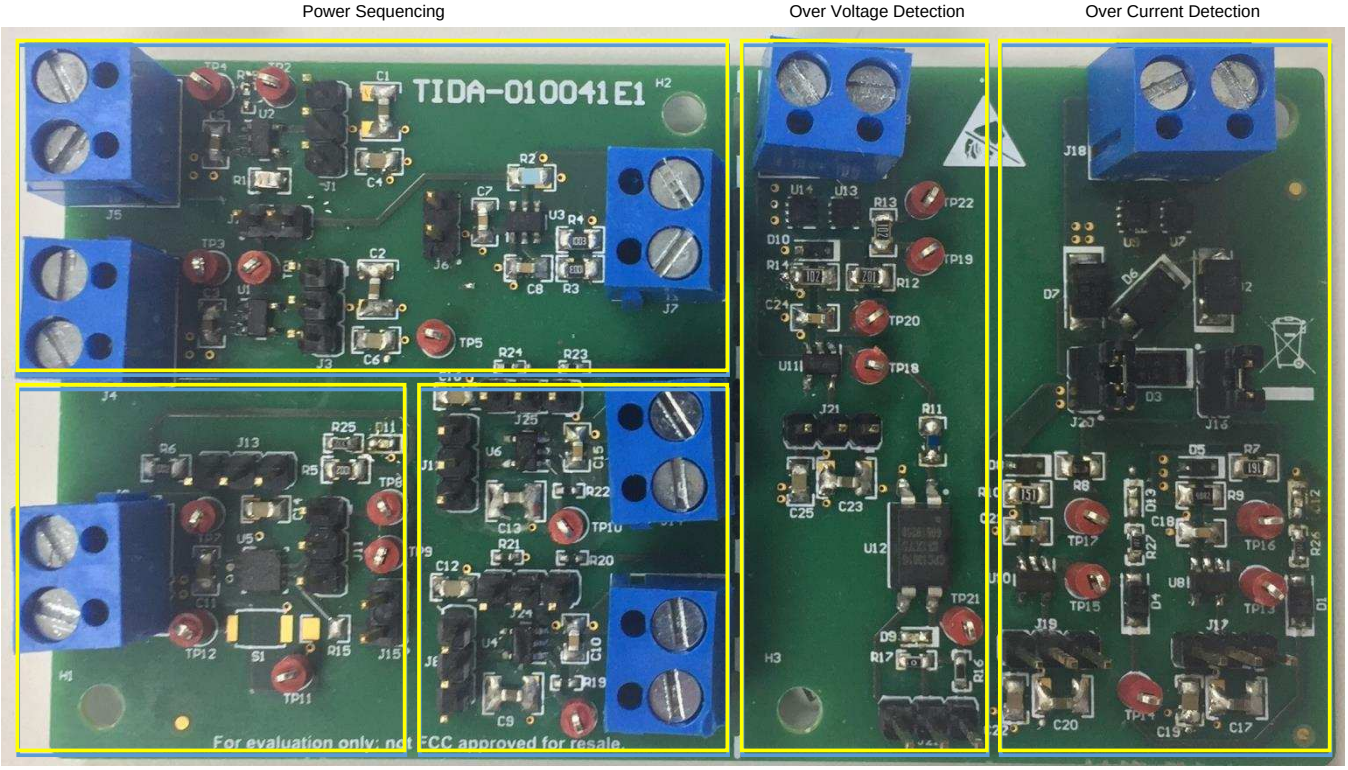
- Tested TIDA-010041 board
- Programmable DC voltage source capable of generating voltage up to 20 V
- Programmable DC current source capable of generating current up to 500 mA
- Programmable AC current source which is able to generate sinusoidal current of 50 Hz from 0 mA to 500 mA
- Digital multimeter for measuring the DC or AC voltages
- Digital oscilloscope for capturing the timing from the voltage waveforms

3.2 Testing and Results

3.2.1 Test Setup

図 10 shows the board layout for the TIDA-010041 used for testing and validating its performance. The board is sectionalized based on the implementations of various functions. Connectors are provided for plugging current and voltage sources to the corresponding sections. Jumpers are used for choosing different capacitors at the CT pins for adding delay in the response path.

図 10. Hardware for Validation



3.2.2 Test Results

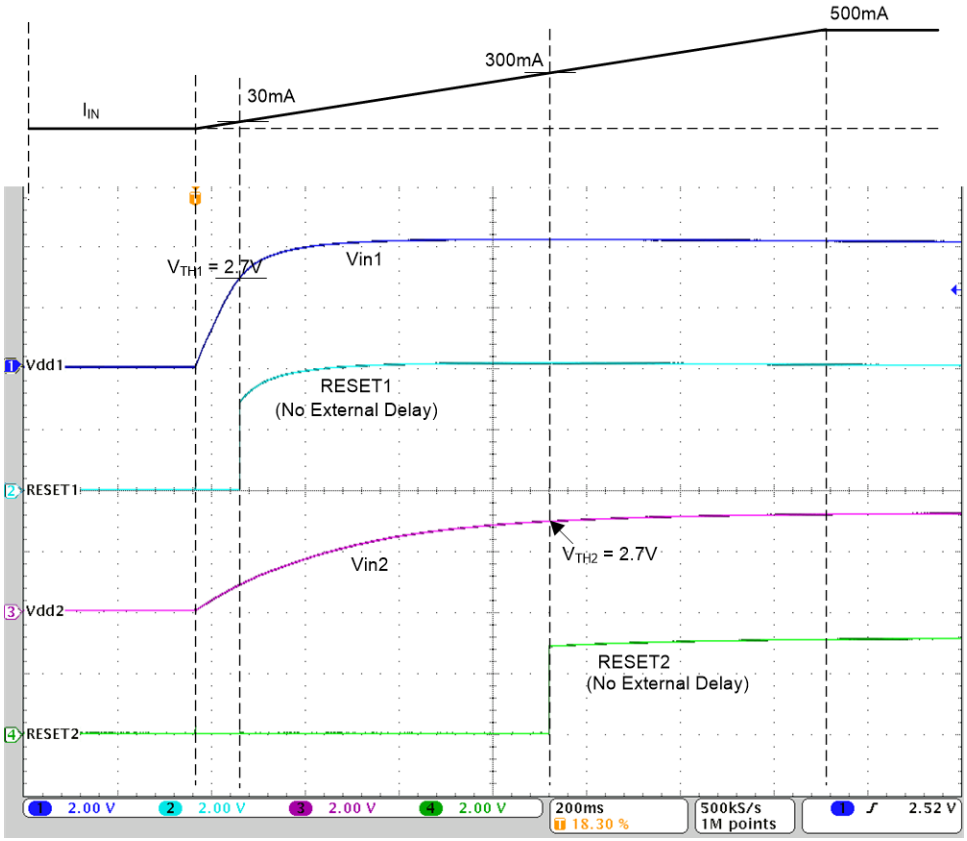
This section provides details of the functional tests done with TI design TIDA-010041 and observations.

3.2.2.1 Threshold Detection

Fault Current Detection: To capture the threshold levels for the fault current detection circuit, a DC current source is connected at the input (J16 and J20 on the board) bypassing the diode bridge rectifier for the circuit diagram shown in 図 3. DC current is swept from 0 to 500 mA and reset signal from both the low current threshold path (RESET1) and high current threshold path (RESET2) are observed. Threshold current levels for the two paths are set as 30 mA and 300 mA by choosing the right resistor values.

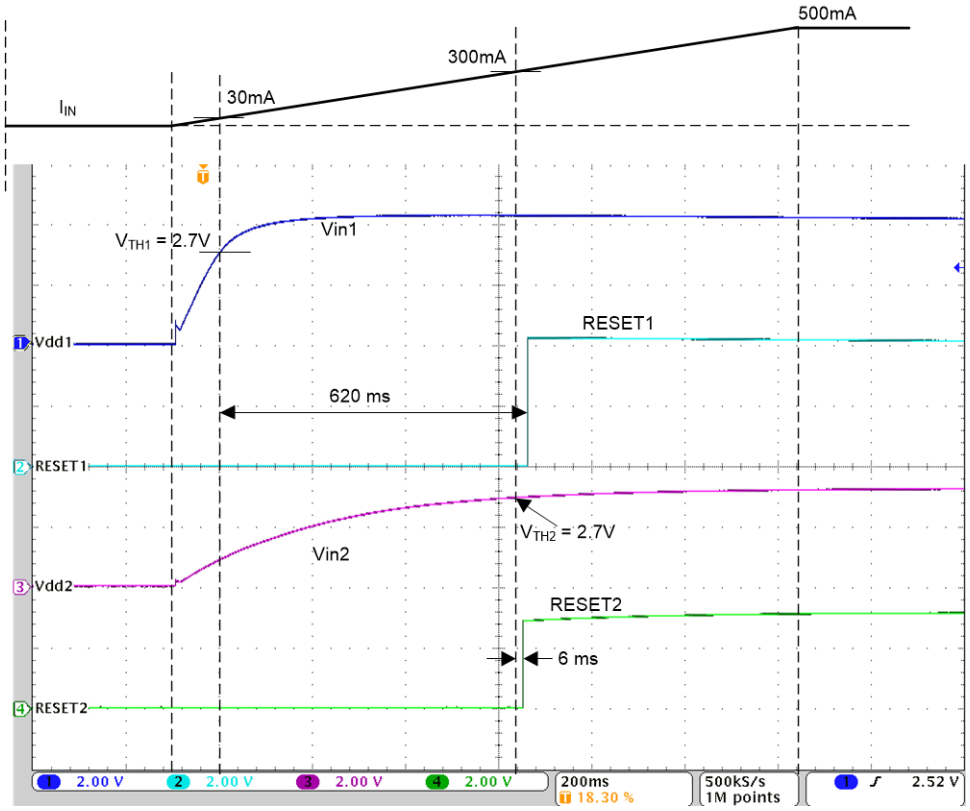
In the first evaluation, a ramp current source of 0 to 500 mA is connected at the input. 図 11 shows the voltage across the input and output of the two branches during this ramp input while keeping the CT pins of both the devices open. Voltage across the input of low current threshold branch increases linearly and reaches its threshold voltage, V_{TH1} when the input current increases from 0 mA to 30 mA. As the input current increases above 30 mA, voltage across its input goes above its threshold which immediately asserts its output to same as the input. Further increase in the input current clamps the input voltage, V_{in1} to around 4 V and its output voltage, RESET1 follows the input. Voltage across input of the second branch, V_{in2} increases linearly and reaches its threshold voltage, V_{TH2} as the input current changes from 0 mA to 300 mA. The TPS3840 device on the high threshold branch is asserted when the input current is above 300 mA and its output RESET2 follows same as its input V_{in2} as show in 図 11.

図 11. Response From Two Branches With Minimum Time Delay



For the same current input, the circuit has been modified by adding different response delays for the two branches. For the low current threshold branch, a delay of 620 ms is added by connecting 1-µF capacitor at the CT pin. Similarly for the high current branch, 10-nF capacitor is added introducing a delay of 6 ms. 図 12 shows the changes in response from both the branches when different delays are introduced. For branch-1, though its input goes above threshold when I_{IN} is 30 mA, RESET1 goes high after the delay of 620 ms. Whereas, RESET2 is asserted with 6-ms delay after V_{in2} goes above its threshold value.

図 12. Response From two Branches With the Introduction of Time Delay



When a step input current is 50 mA, only current detector on the lower threshold level operates with a response time of 620 ms as 図 13 shows. When the input current is above 300 mA, both the current detectors operates; however, the higher threshold detector responses quicker compared to lower threshold one as captured in 図 14.

図 13. Fault Current Detection for 50-mA DC Step Input

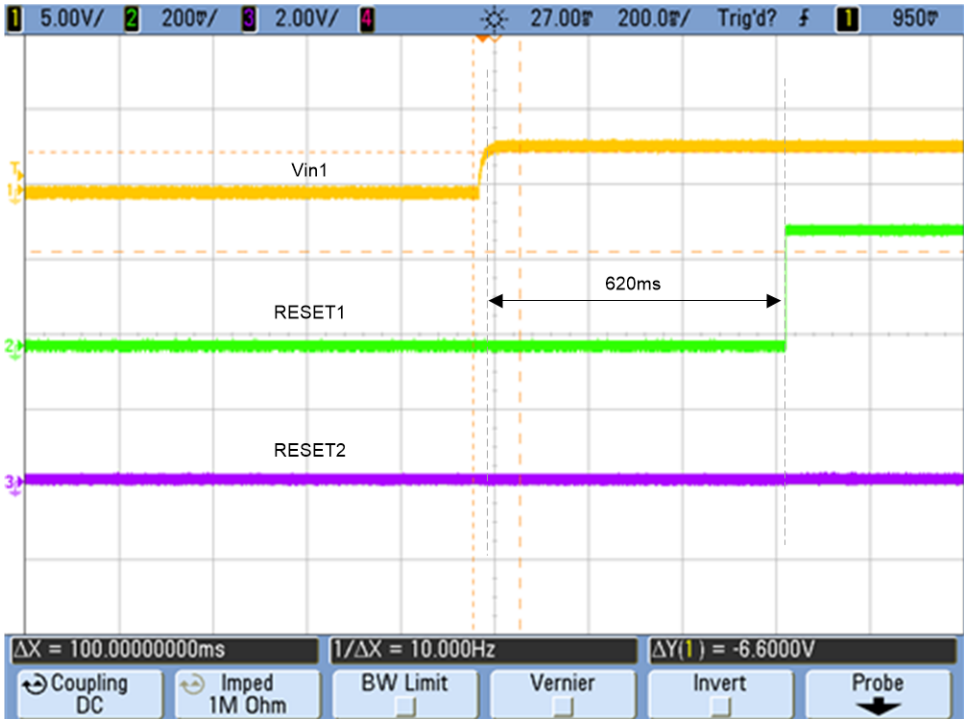
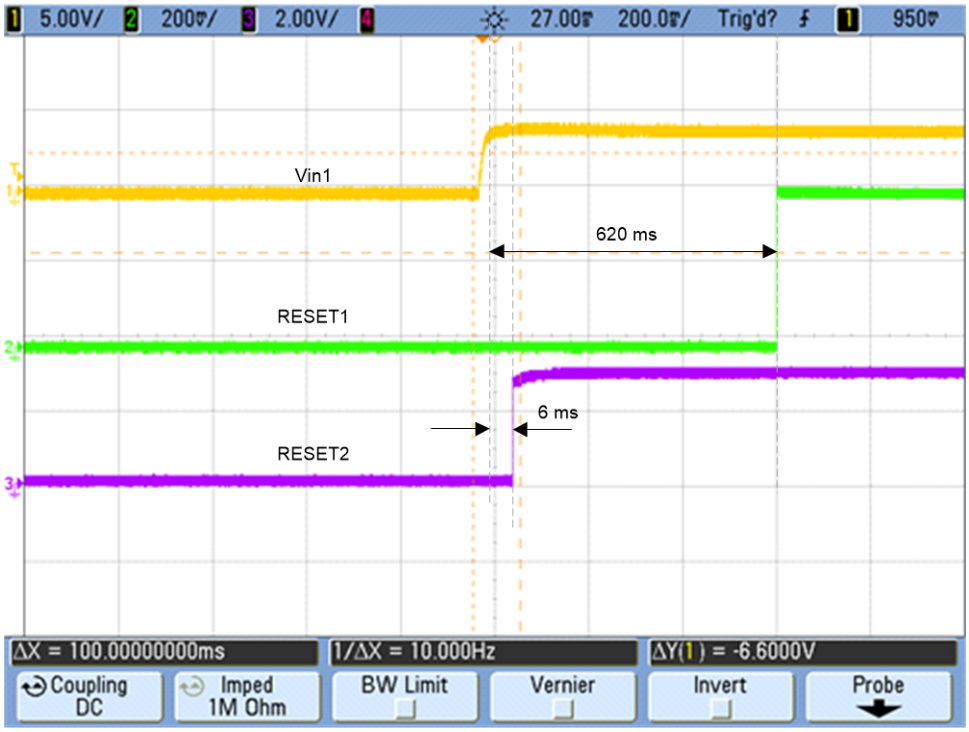
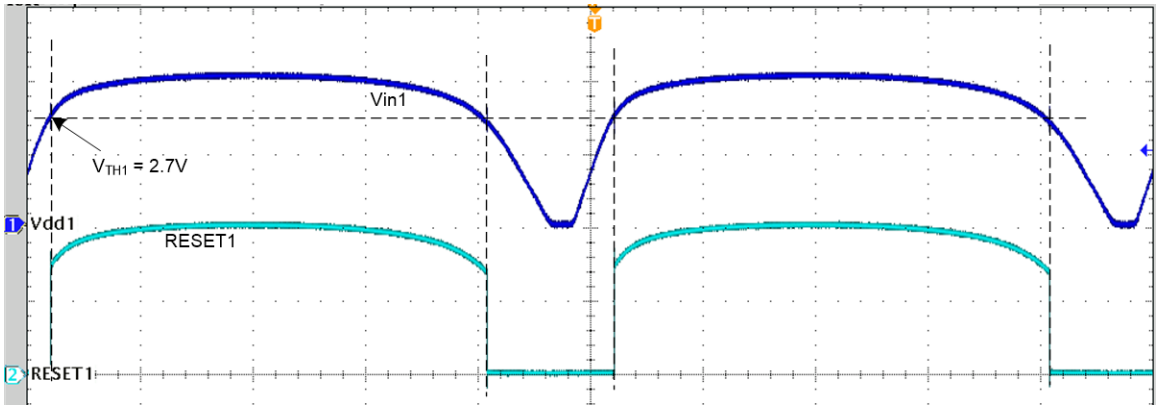


図 14. Fault Current Detection for 300-mA DC Step Input



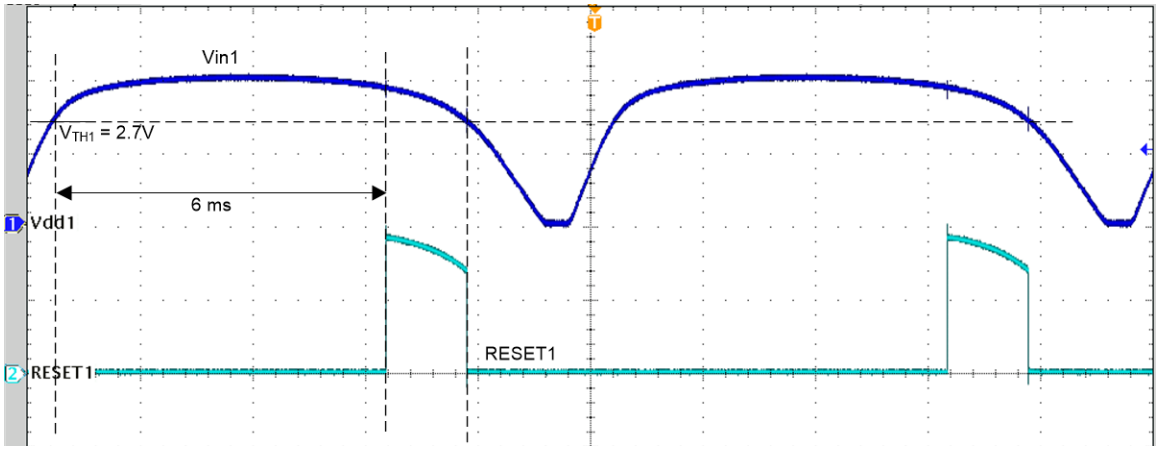
For the AC current detection, a 50-Hz current source is connected at the input (J18) and magnitude of the signal is swept from 0 mA to 300 mA. 図 15 shows the voltage at the input of branch-1 (with the low level current threshold which is 30 mA) and its output when input current of 100 mA RMS is applied. Whenever the input voltage crosses the threshold value, output is set high (same as the input) as the circuit is set to minimal delay of 80 µs. Input is being clamped by the zener to limit the voltage.

図 15. Response From Branch-1 for 100-mA RMS Input Without Delay



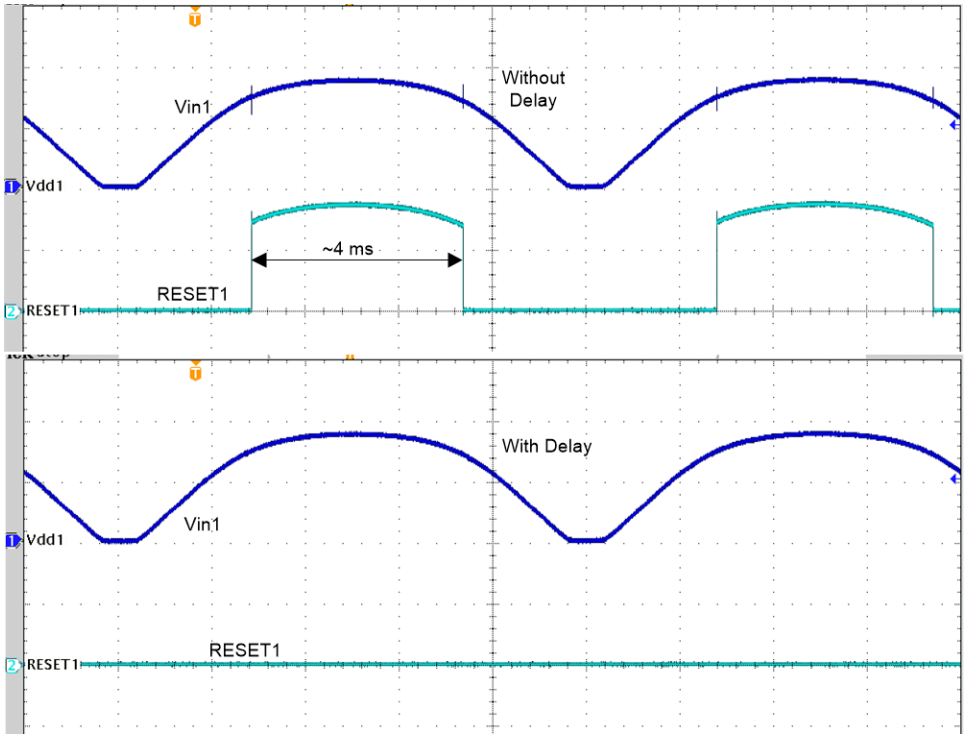
Same current input is applied introducing time delay of 6 ms and output (RESET) is pulled high with a delay from the instant V_{in} goes above V_{TH} and input voltage is still above the threshold shown in 図 16.

図 16. Response From Branch-1 for 100-mA RMS Input With Delay



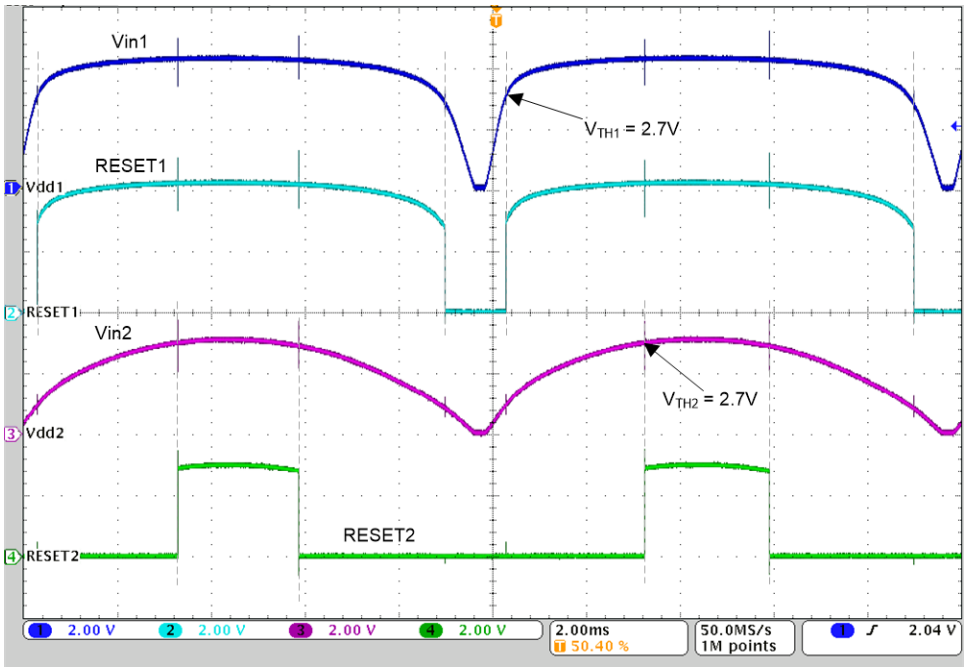
However, if the input current level is smaller with the time duration for which it stays above V_{TH} is lower than the delay time, then the output is going to stay at low without giving any trip signal as 図 17 shows. In this particular figure, an input current of 30 mA RMS is applied and output stays high for approximately 4 ms when it is configured for minimum delay. If the delay is set to 6 ms, then the device fails to detect an overcurrent level.

図 17. Responses for 30-mA RMS Input Without and With Delay



When the input current is above 300 mA threshold set by the second branch, both the branches are able to detect the overcurrent conditions the waveform in 図 18 shows for an input current of 220 mA RMS (310-mA peak).

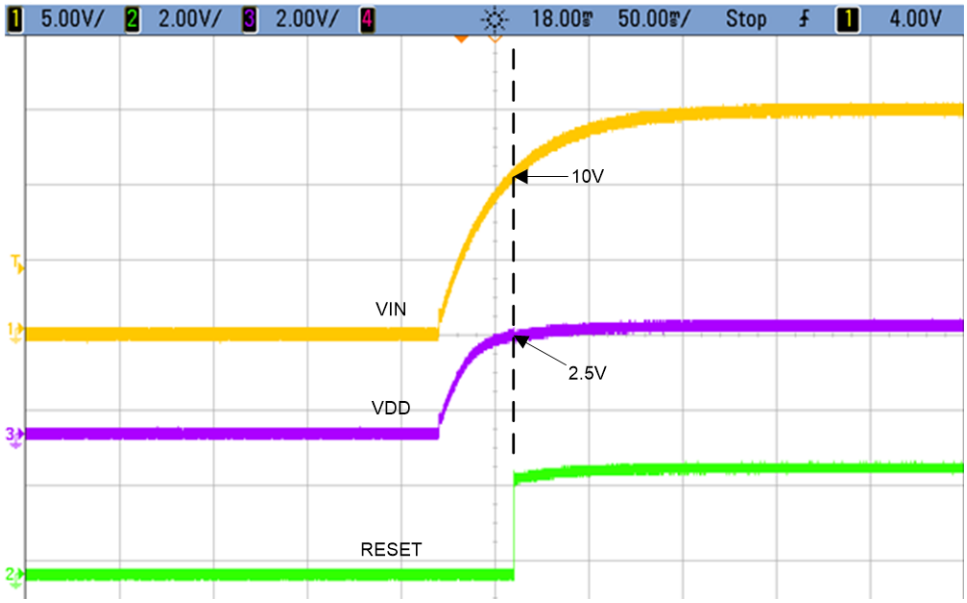
図 18. Responses From Two Branches for 220-mA RMS Input



Binary Input Voltage Detection: For the binary input voltage detection, a variable voltage source is applied at the input and varied in steps. Threshold value of the input is captured for which output state of the detector switches from low to high and is 10.599 V. Similarly, input voltage is decreased and its value is captured when the state changes from high to low at 10.099 V.

A step input voltage of 20 V is applied and voltage at the input of the supervisor, VDD, and reset signals are captured in 図 19.

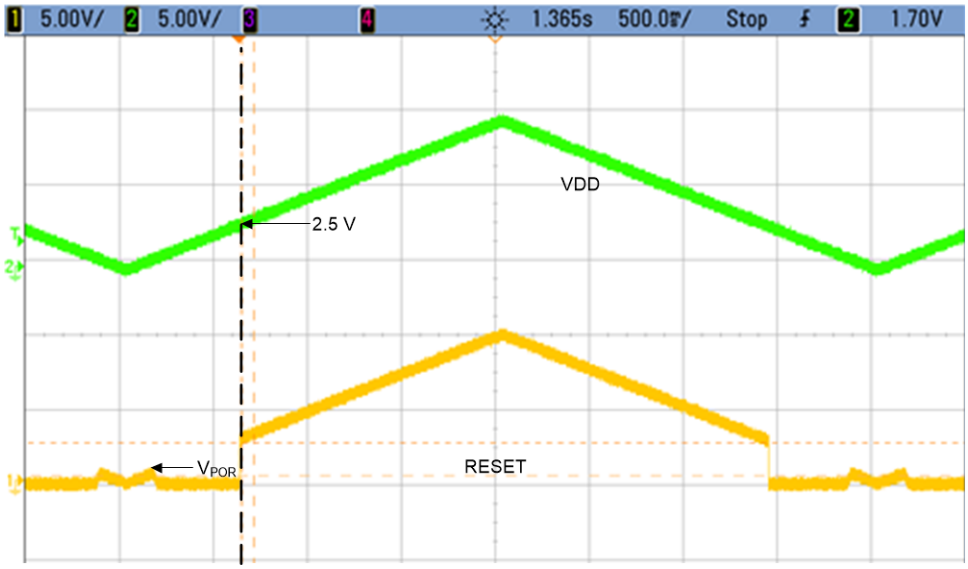
図 19. BIM: Voltages During Transition of Input Voltage From 0 V to 20 V



3.2.2.2 Voltage Supervision and Sequencing

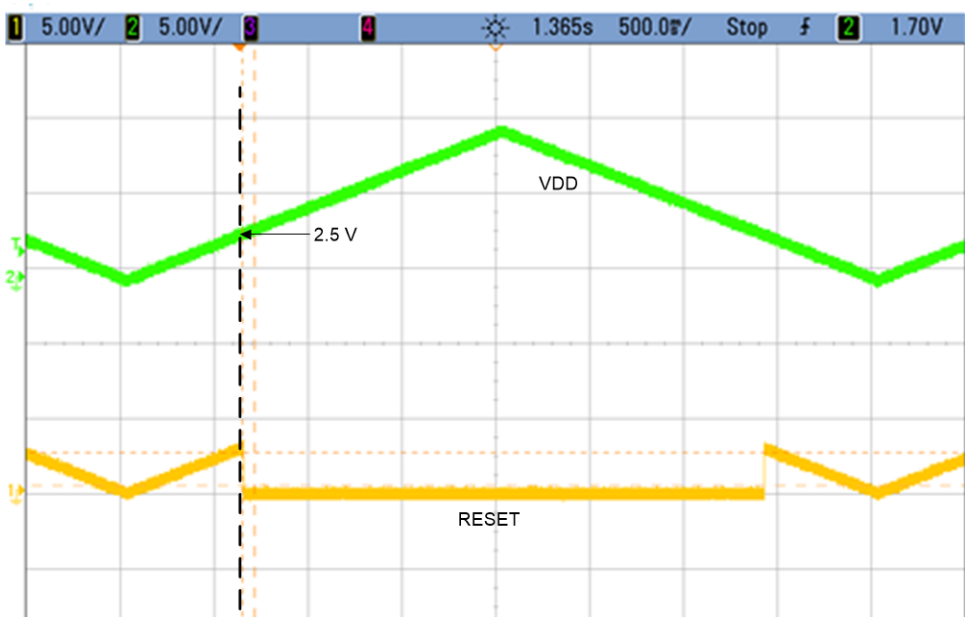
A triangle signal is applied across the input of an active low voltage reset part. 図 20 shows response of a push-pull (active low) topology where output of the part is driven same as the input voltage when it reaches above its threshold value. This also shows power on reset voltage (V_{POR}) of the device which is around 300 mV for which output is undefined.

図 20. Voltage Response of TPS3840 (Active Low)



Similarly for the active high device in push-pull configuration, the output (RESET) is low when the input voltage is above the threshold value as shown in 図 21.

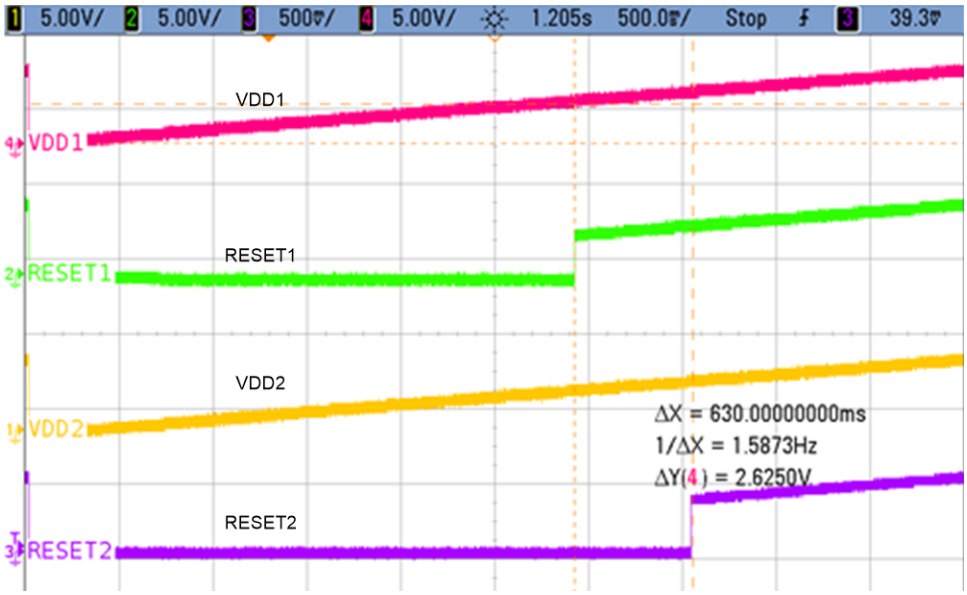
図 21. Voltage Response of TPS3840 (Active High)



Power Sequencing: In this test setup, two TPS3840 devices are cascaded together to monitor two supply rails, VDD1 and VDD2 and a delay of 6 ms has been added between RESET1 and RESET2.

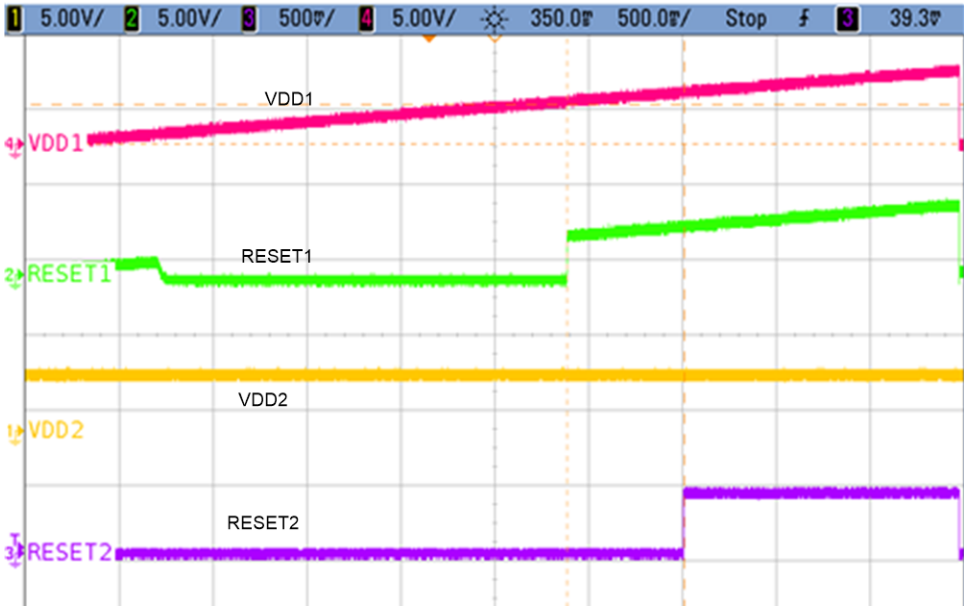
When both the input voltage rails ramp up together, output from the first device, RESET1 is enable whenever its input voltage is above the threshold setting of 2.7 V. Though this condition is true for the second device, its output is enabled only after 6 ms delay with respect to RESET1 going high as capture in 図 22.

図 22. Power Sequencing When Both VDD1 and VDD2 Comes up Together



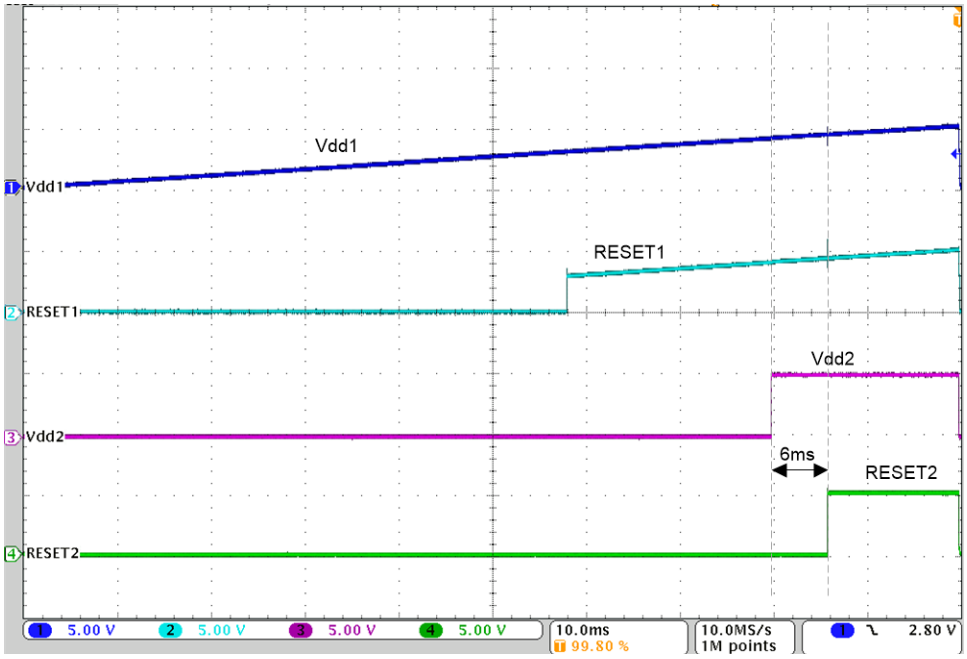
In a second test case, VDD2 comes up before VDD1 and RESET2 goes high after RESET1 going high with a delay of 6 ms as 図 23 shows.

図 23. Power Sequencing: VDD2 Coming Before VDD1



However, if Vdd2 comes up after Vdd1 has crossed its threshold value, and then RESET2 is going to wait until its input is above the set threshold value. Now the delay time is considered from the instant Vdd2 crossing the threshold level as 図 24 shows.

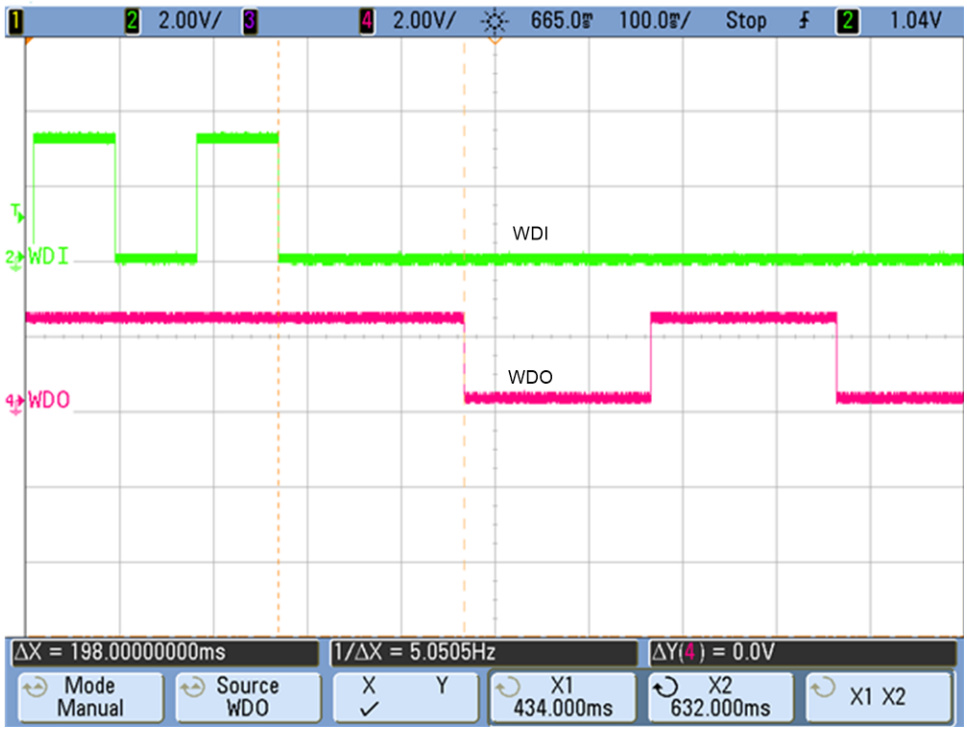
図 24. Vdd2 Comes on After Vdd1



3.2.2.3 Watchdog Timer

Configuration 1: The TPS3431 device is configured in mode 1 by connecting a 10-kΩ resistor between the CWD pin and V_{DD}. 図 25 shows the timeout of 198 ms and watchdog reset delay of 200 ms.

図 25. WDT Configuration 1: Timeout of 200 ms



Configuration 2: While keeping the CWD pin unconnected, a timeout of 1.6 s is obtained with the watchdog reset delay for 200 ms as 図 26 shows.

図 26. WDT Configuration 2: Timeout of 1600 ms

Configuration 3: Any other timeout value is achieved by connecting a specific capacitor at the CWD pin. As an example, a 10-nF capacitor is connected and timeout delay of 830 ms is obtained as 図 27 shows. 表 2 summarizes timing values for all the three configuration of watchdog timer.

図 27. WDT Configuration 3: Timeout of 830 ms

表 2. Timeout Delay for TPS3431

	EXPECTED TIMEOUT (ms)	MEASURED TIMEOUT (ms)
Configuration 1	200	198
Configuration 2	1600	1586
Configuration 3	830	824

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010041.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010041.

4.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010041.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010041.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010041.

5 Related Documentation

1. Texas Instruments, *EMC-Compliant Digitally Isolated 2-Channel, Wide DC Binary Input Module Reference Design*
2. Texas Instruments, *Size and Cost-Optimized Binary Input Module Reference Design Using Digital Isolator With Integrated Power Reference Design*
3. Texas Instruments, *EMC Compliant, Isolated, 2-Channel Binary or Digital Input Module for Wide AC/DC Input Reference Design*
4. The RCD Handbook *BEAMA Guide to the selection and application of residual current devices*, September 2010.
5. Texas Instruments, *Optimizing Resistor Dividers at a Comparator Input Application Report*

5.1 商標

5.2 Third-Party Products Disclaimer

6 Terminology

BIM— Binary Input Module

DIM— Digital Input Module

MCU— Microcontroller Unit

RCCB— Residual Current Circuit Breaker

RCD— Residual Current Detector

SVS— Supply Voltage Supervision

WDT— Watchdog Timer

7 About the Author

PRASANNA RAJAGOPAL is a systems engineer at Texas Instruments Dallas where he is responsible for developing reference design solutions for Grid Infrastructure in Industrial Systems. Prasanna brings to this role his expertise in power electronics and mixed signal systems. Prasanna earned his PhD from IISc, Bangalore, India

HARSH MISRA is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for Grid Infrastructure in Industrial Systems. Harsh completed his B.E.(hons) in Electrical and Electronics engineering from BITS Pilani, India

7.1 Acknowledgments

KALLIKUPPA MUNIYAPPA SREENIVASA, Systems Architect at Texas Instruments, for his inputs and feedback on system architecture, requirements, and technical inputs.

AMIT KUMBASI, Systems Manager at Texas Instruments, for his inputs and feedback on system architecture, requirements, and technical inputs.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。