参考資料

TI Designs: TIDA-080001
携帯3Dスキャナ用、小さな外形の構造化光パターン・ジェネレータのリファレンス・デザイン

概要

この超低コスト3Dスキャンのリファレンス・デザインにより、構造化光の三角測量法を使用する携帯3Dスキャナおよびマシン・ビジョンのアプリケーションを短期間で開発できます。この方式では、DLP®テクノロジを使用して柔軟性の高いパターンを物体に投影できます。

このTI DesignはDLP Picoの0.2インチTRP WVGA DMD (DLP2010)と、新しいディスプレイおよび光コントローラDLPC3470を使用します。DLP2010は小型であるため、小さな外形と低消費電力であることが重視される携帯機器に最適です。このリファレンス・デザインには、サンプルの光エンジン設計が付属し、電子部品や光学部品と、3Dスキャン設計に使用される各種の光パターンを生成するためのソフトウェアが含まれています。これと同じ電子設計は、DLP2010NIR DMDでも使用でき、700nm～2500nmの範囲の波長に対応するNIR光源として使用できます。

リソース

TIDA-080001	デザイン・フォルダ
DLP2010 (DMD)	プロダクト・フォルダ
DLPC3470	プロダクト・フォルダ
DLPA2005	プロダクト・フォルダ

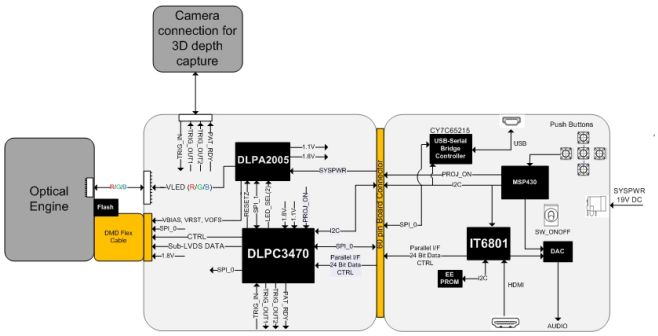
TI E2E™ Community　E2E™ エキスパートに質問

特長

- DLPC3470ディスプレイおよび光コントローラ、および完全に統合されたDLPA2005 PMIC/LEDドライバを搭載
- 電子的設計でDLP2010とDLP2010NIRの両方をサポート - 可視光線とNIR波長
- DLP2010、DLP2010NIR - 854×480のアルミ製のマイクロメートル・サイズ・ミラーを直交配置し、柔軟で高精度な光制御を実現
- DLP2010EVM-LCレイアウトで使用
- モノクロおよびRGBパターンを表示でき、柔軟なトリガでカメラを制御
- すぐに量産可能な光エンジンと、プログラム可能なLEDドライバ(0～650mA)が付属
- PCソフトウェアのGUIにより、あらゆる種類のパターンを光エンジンへ送信

アプリケーション

- パーソナル・エレクトロニクス:
  - 3Dカメラ
  - 歯科用口腔内3Dスキャナ
  - マシン・ビジョン
  - ロボット・ビジョン
  - 顔面認証などの生体認証



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1 System Description

The 3D sensor market is fragmented with the required features depending on the application and object being scanned, whether it is dental scanning, facial recognition or optical PCB inspection. 表 1 lists typical requirements for a 3D scanner.

表 1. 3D Scanner System Typical Requirements

DLP FEATURE	Requirement
Camera Type	0.3 Mpix to 12 Mpix resolutions, global shutter, 30 -– 1000 fps, trigger input
Scan Speed	100 Hz - 1 KHz
Resolution	0.1 mm - 1.0 mm (x, y, z)
Range and Field of View	10 cm - 1 m
Scan Time	≤ 1.0 sec (3D scan time = capture + processing)
Wavelength	400 - 700 nm, 850 nm (indoor), 940 nm (outdoor)
Pattern	Binary code or sinusoidal fringe patterns or other new techniques
Contrast	Camera limit (8-bit: 255-0) optical system MTF should allow for high frequency fringe patterns to be displayed clearly.

A typical block diagram of 3D printing system using the stereolithography (SLA) technique is shown in 図 1.

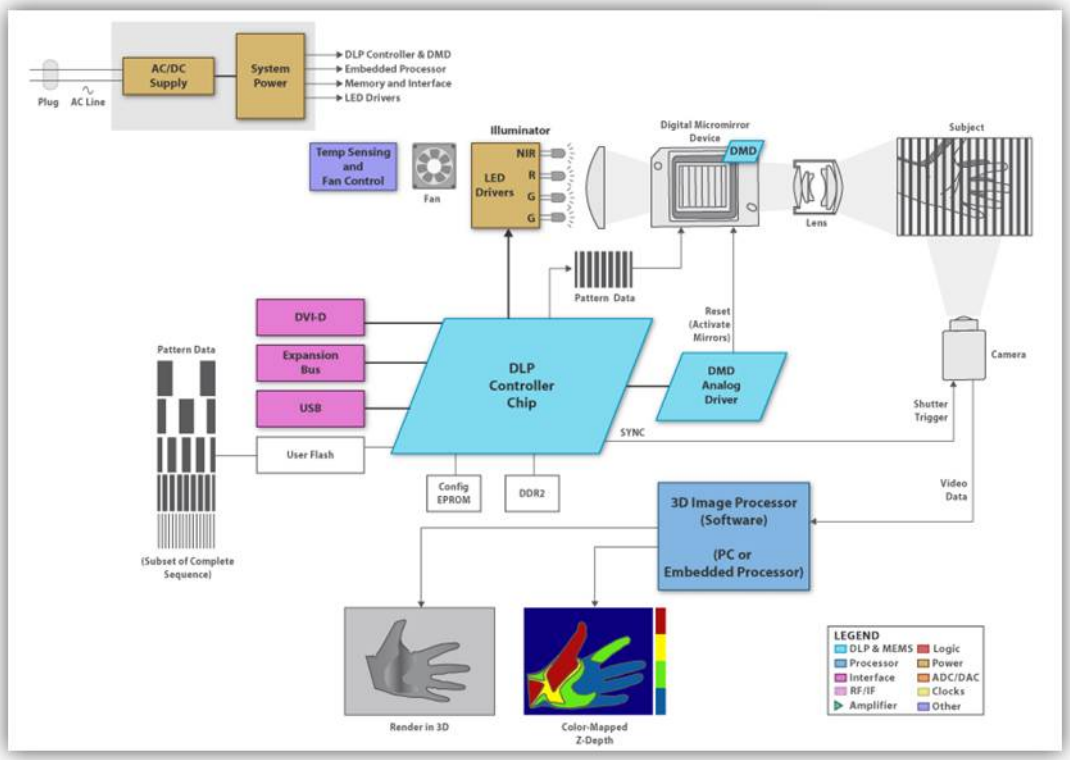


図 1. 3D Scanner System Block Diagram

1.1 Applications for Mobile Smart TVs and Mobile Projectors

This 3D scanning TI Design has several applications across consumer, medical, and industrial markets such as:

- 3D cameras
- Intra-oral dental 3D scanners
- Robotic vision
- Machine vision
- Biometrics such as facial recognition

図 2. Different 3D Scanning Applications

DLP technology is highly flexible in terms of generating different types of light patterns at high speed and while working with different wavelengths of light. 表 2 lists the key features of DLP technology and the corresponding benefits in 3D scanning applications.

表 2. DLP Technology Benefits for 3D Scanning

DLP FEATURE	DESIGN BENEFIT
Optical MEMS device	Inherently **non-invasive** approach
High speed pattern rates	Real-time 3D acquisition
Flexible pattern control	Micron-level accuracy and resolution
External triggers	Easy synchronization to cameras and other system control
Extended wavelength support (405 nm to 2500 nm)	Enables diverse applications with visible and near-infrared light

2 System Overview

2.1 Block Diagram

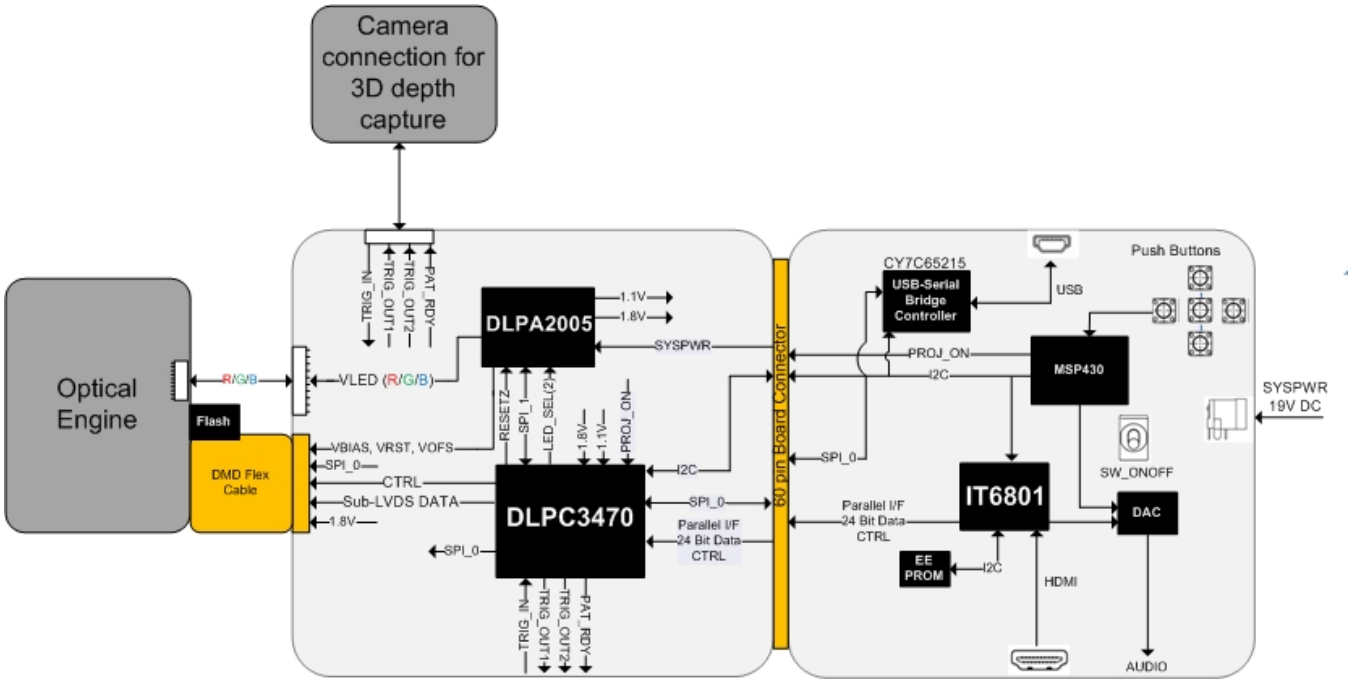


図 3. TIDA-080001 Block Diagram

2.2 Design Considerations

See the following documents for considerations in DLP system design:

- *TI DLP® Pico™ System Design: Optical Module Specifications*
- *TI DLP® System Design: Brightness Requirements and Tradeoffs*

2.2.1 Functional Description

Structured light is an active, non-contact optical method that projects a set of patterns onto an object and captures them with an imaging sensor, offset from the projector. The image sensor is typically a global or rolling shutter camera or a compatible open CV camera (such as a webcam). This technique takes advantage of the known camera-to-projector separation to locate a specific point on the object and compute its depth with triangulation algorithms. Programmable pattern structured light can obtain greater depth accuracy with the use of multiple patterns and the ability to adapt the patterns in response to ambient light, the object's surface, and optical reflection.

2.2.1.1 Pattern Codification Techniques

Programmable pattern structured light utilizes the following pattern codification techniques:

- Multiple temporal pattern set. In this technique, each point in the image is encoded by the temporal sequence of intensities of the pattern set. Typical pattern sets include:
  - **Binary Code**: It is composed of a series of progressively thinner black and white stripes. The first pattern has half of the array black with the other half white. The second pattern divides each black and white stripe in half, with each stripe converted to half black and half white. The third pattern

further divides the stripes until the pattern is an alternating set of black and white stripes one pixel wide.

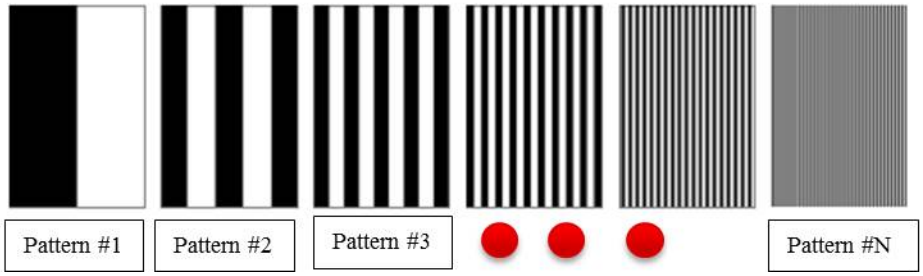


図 4. Typical Binary Pattern Set

If only the first row in each pattern is drawn, the pattern sequence looks like 図 5.

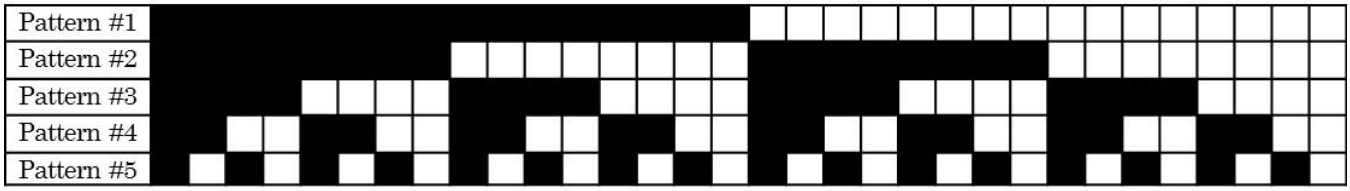


図 5. Typical Binary Pattern Set - Row 1

– **Gray Code**: Similar to binary code, but adjacent stripes only differ by 1-bit. It follows the sequence as shown in 図 6.

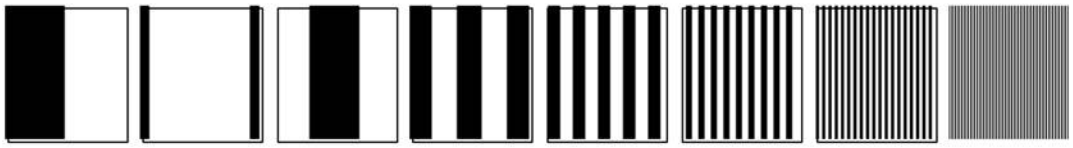


図 6. Gray Code Sequences

If only the first row in each pattern is drawn, the pattern sequence looks like 図 7.

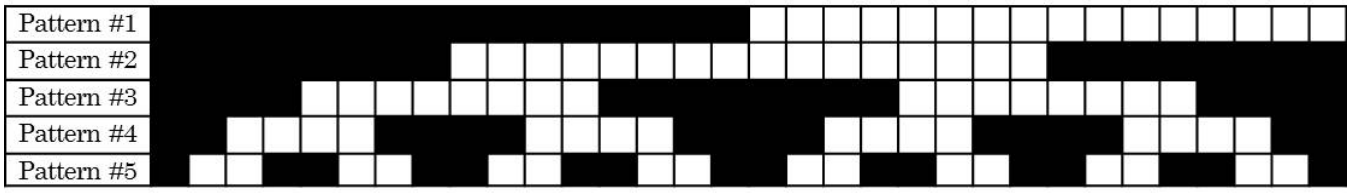


図 7. Gray Code Sequences - Row 1

– N-ary codes: Use multi grey levels instead of binary to encode m symbols in mn stripes. m = grey levels, n = # patterns

– Phase shift or sinusoidal: A set of three sinusoidal intensity patterns, which is phase shifted by $2\pi/3$ on each subsequent pattern as shown in 図 8.

- Pattern #1 = $\cos(\varphi - 2\pi/3)$
- Pattern #2 = $\cos(\varphi)$
- Pattern #3 = $\cos(\varphi + 2\pi/3)$

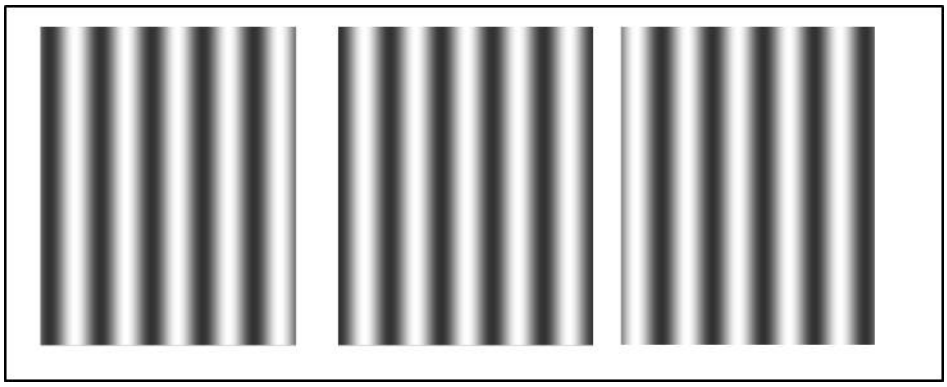


図 8. Phase Shift Patterns Example

A pattern set is a set of patterns that share the same exposure time, bit-weight (binary or gray-scale), frame period, trigger control, and pattern source (external or internal). During a 3D scan, multiple pattern sequences are used for best resolution capture. For example, a 3D scan might have 3 sinusoidal patterns followed by a set of binary patterns followed by a different set of sinusoidal patterns.

There are several other techniques employing a variety of patterns and a variety of sequences in the literature and is an ongoing innovation in this market space. The DLPC3470 controller used in this TI design supports flexible pattern generation capability with both DLP2010 and DLP2010NIR DMD chips.

2.2.1.2 Pattern Streaming Modes

Typical electronics block diagram with DLPC3470 is shown in 図 9.

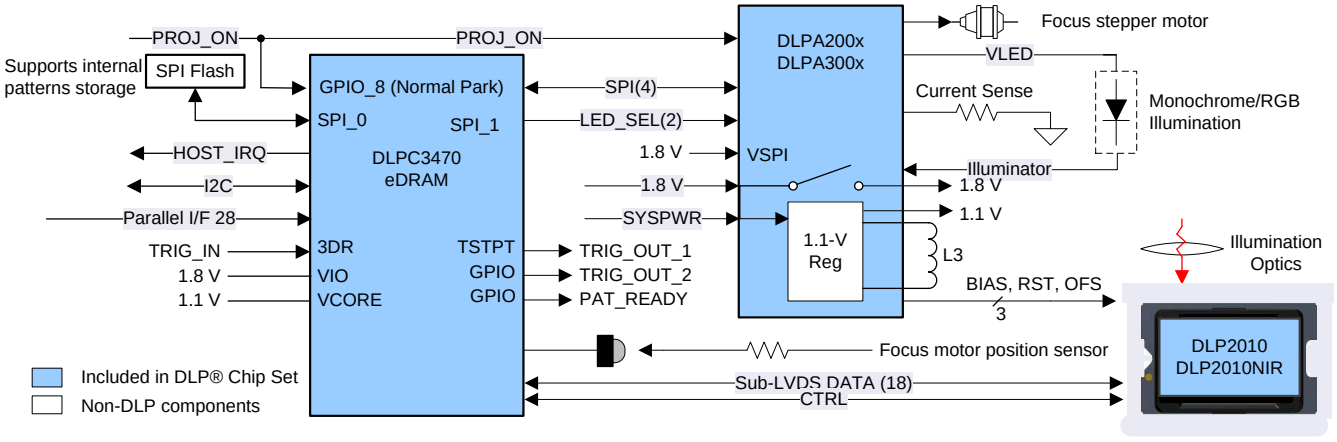


図 9. Internal Pattern Streaming Timing Diagram

2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.2 WVGA DLP chipset. For a list of these documents, see 6.

3 Hardware, Software, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Assuming default conditions as shipped.

1. Power up the DLP2010 Light Control EVM by applying an external DC power supply (19 V DC, 3.42 A) to the J10 connector. The P5V_VIN (D5) and P3P3V_SB (D6) LED will turn on to indicate that 5-V and 3.3-V standby power is applied.
   External Power Supply Requirements:
   - Nominal output voltage: 19 VDC
   - Minimum output current: 3 A; Maximum output current: 3.42 A
   - Efficiency level: VI

   NOTE: TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, etc.
   NOTE: The system is designed to operate also with an external 12-V DC power supply.
2. Move the SW_ONOFF switch to the ON position to turn the DLP2010 Light Control EVM on. When the DLP2010 Light Control EVM is turned on, the PROJ_ON LED D3 will turn on.
3. After the DLP2010 Light Control EVM is turned on, the projector will default to displaying a DLP Light Control splash image.
4. The focus of the image can be adjusted with the focus wheel on the optical engine.

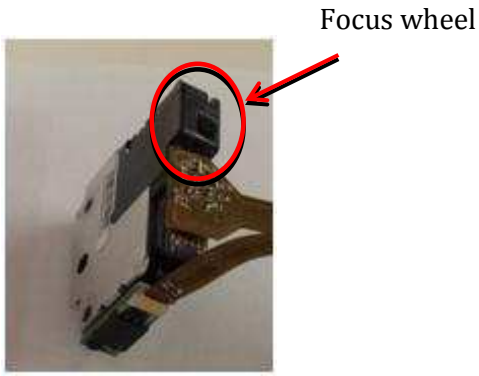


図 10. Optical Engine With Focus Wheel

5. Connect USB to the DLP2010 Light Control EVM and open the DLP Display and Light Control EVM Graphical User Interface (GUI) on your computer. If needed, connect an HDMI source to the EVM and communicate to the EVM over the GUI software.
6. Using the GUI, the EVM can be set into Video Display Mode or Light Control Mode. Install Jumper J11 to set Trigger IN/OUT voltage on the EVM (**jumper Is not included by default**). Refer to the GUI User's Guide for further description.
7. When turning off the projector, turn off the SW_ONOFF switch prior to removing power cable.
   Note: To avoid potential damage to the DMD, it is recommended to turn off the projector with the SW_ONOFF before disconnecting the power.
8. There are ten indicator LEDs on the DLP2010 Light Control EVM, and they are defined in 表 3:

表 3. LEDs on the DLP2010 Light Control EVM

LED Reference	Signal Indication	Description
D1	HOST_IRQ	ON during DLPC3470 boot OFF when projector is running. Indicates DLPC3470 boot-up completed and ready to receive commands
D2	RESETZ	OFF when projector is turned on via SW_ONOFF

表 3. LEDs on the DLP2010 Light Control EVM (continued)

LED Reference	Signal Indication	Description
D3	PROJ_ON	On when projector is turned on via SW_ONOFF
D5	P5V_VIN	5-V power applied
D6	P3P3V_SB	Regulated 3V3 power on
D7	MSP2	ON when HDMI cable plugged in, and external video detected. OFF when external video is not detected.
D8	ACK	ON when Cypress CY3420 is I^2C master OFF when MSP430 is I^2C master
D9	REQ	ON when Cypress CY3420 requests the MSP430 to give Cypress master control of the I^2C bus
D10	GPIO1	Blinking when PC is communicating to flash over SPI
D11	GPIO0	Blinking when PC is communicating to DLPC3470 over I^2C

3.1.2 Light Engine

The optical engine in the EVM is developed by Asia Optics and is production ready.

The light engine consists of the following components:

- 0.2-inch WVGA DMD (DLP2010)
- OSRAM red, green, and blue LED – LE BA Q6WM and LCG H9RM

表 4. Optical Engine Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Brightness		25		lumens
LED Current		650		mA
Brightness Uniformity	75%			
Throw Ratio		1.65		
Offset		100%		

The dimensions of the optical engine are shown in 図 11:

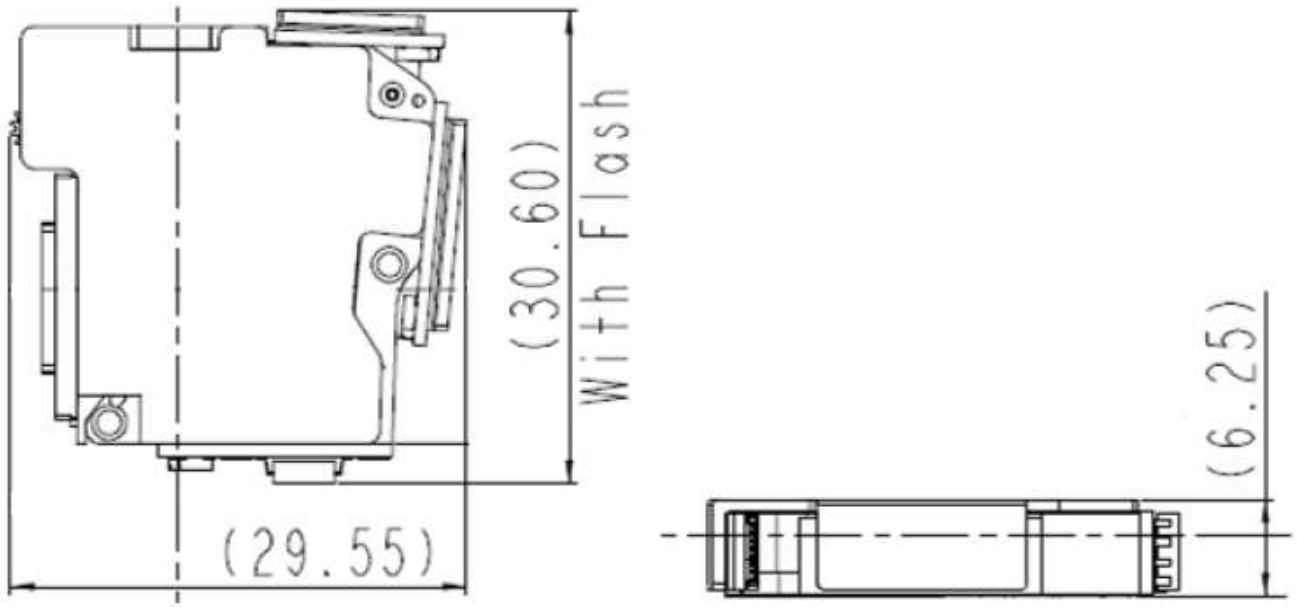


図 11. Dimensions of Optical Engine

3.1.3 Software

The software required for this reference design is available for download on the DLP2010EVM-LC tool folder.

3.2 Testing and Results

For 3D scanning application, typically a mono-chrome sequence is used unlike an RGB sequence for a display application. DLPC3470 controller is designed with these requirements in consideration. The patterns could be streamed in two modes.

3.2.1 External Pattern Streaming Mode

In this mode, the patterns are streamed through the external RGB interface. For 3D scanning, typically, a monochrome sequence is used. A typical timing diagram is shown in 図 12.

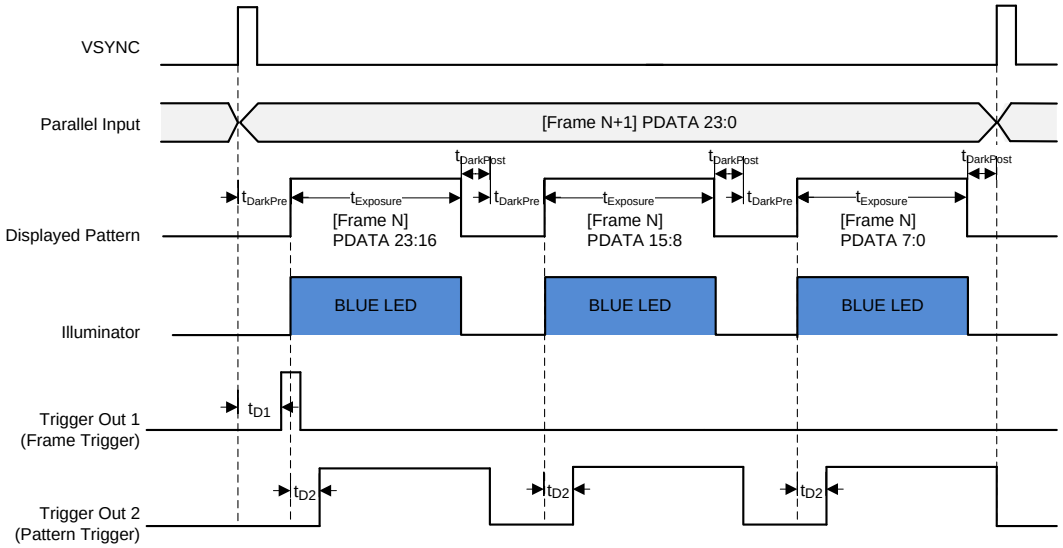


図 12. External Pattern Streaming Timing Diagram

3.2.2 Internal Pattern Streaming Mode

In this mode, the patterns are all stored in the flash memory and there is no need for streaming the patterns from external RGB interface. This will result in a much simpler electronics useful for a portable and ultra-low-cost application. Internal Pattern Streaming Mode is shown in 図 13.

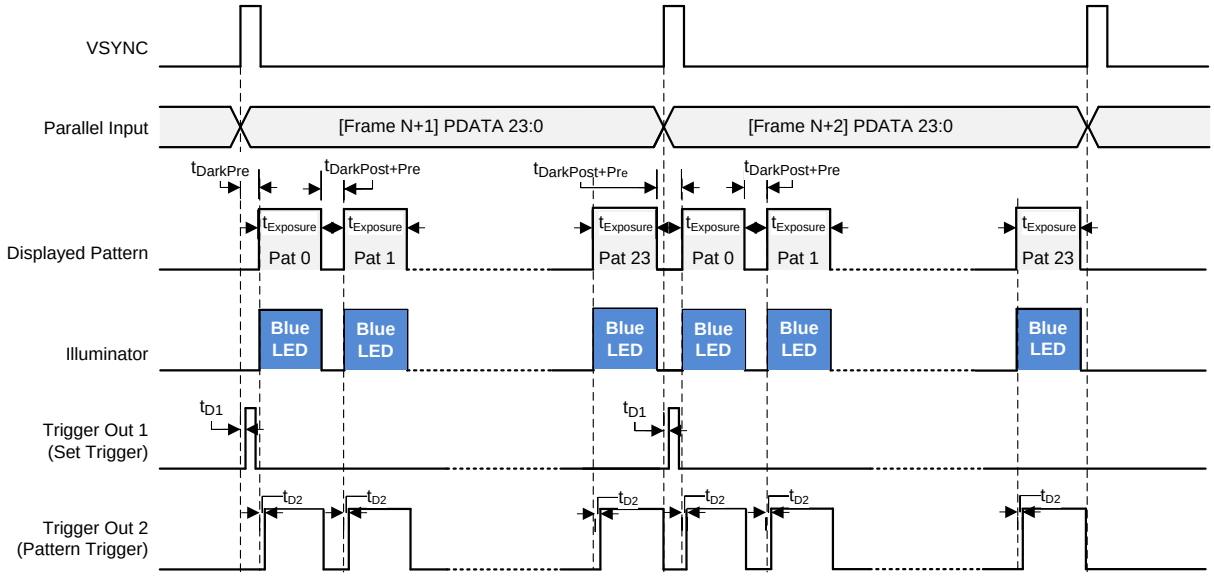


図 13. Internal Pattern Streaming Timing Diagram

This sequence is verified with the DLP2010 light control EVM. 図 14 shows the Trigger Out1 and Trigger Out2 timing diagram.

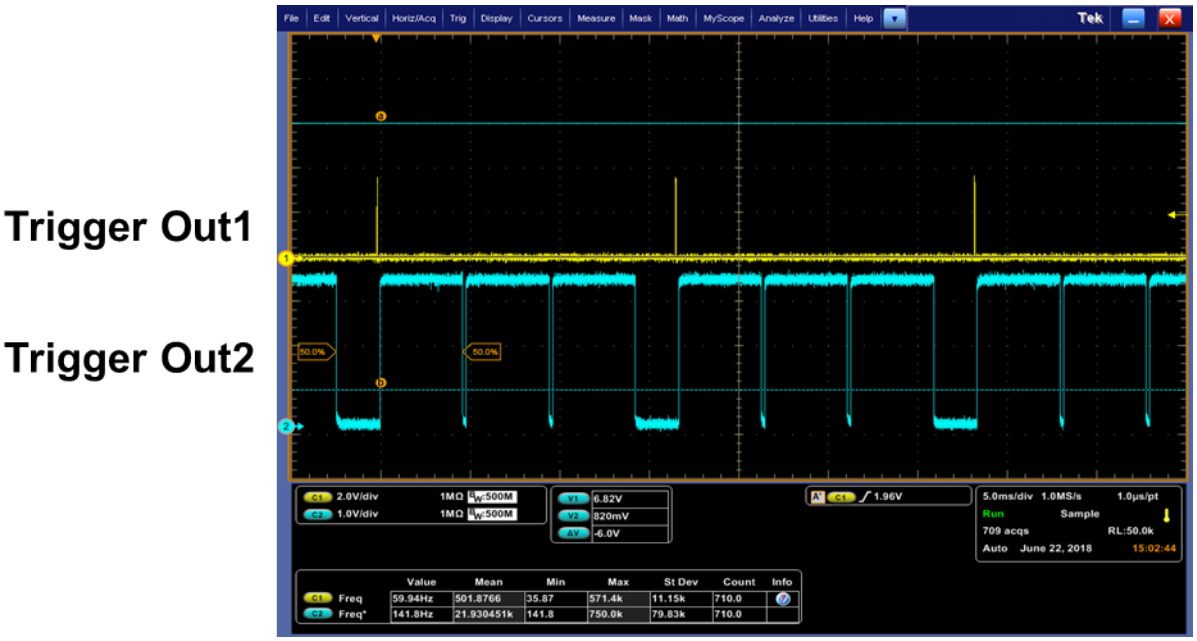


図 14. Scope Plots of Trigger Out1 and Trigger Out2 (24-bit Monochrome)

Different types of mono-chrome and RGB images as shown in 図 15 and 図 16 are tested on the light engine for good image quality.

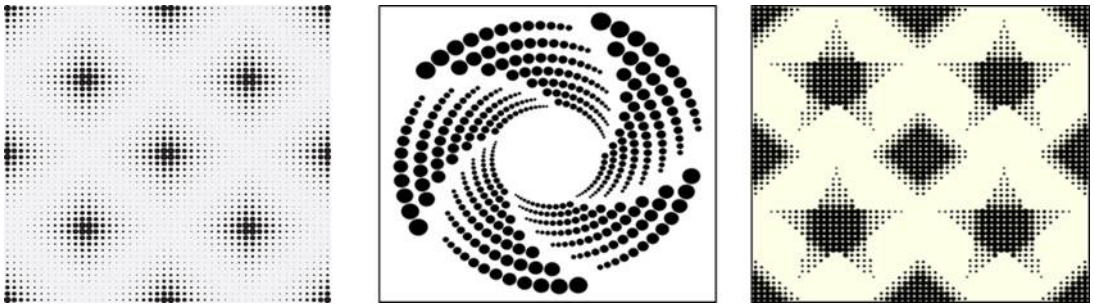


図 15. Different Bit Patterns

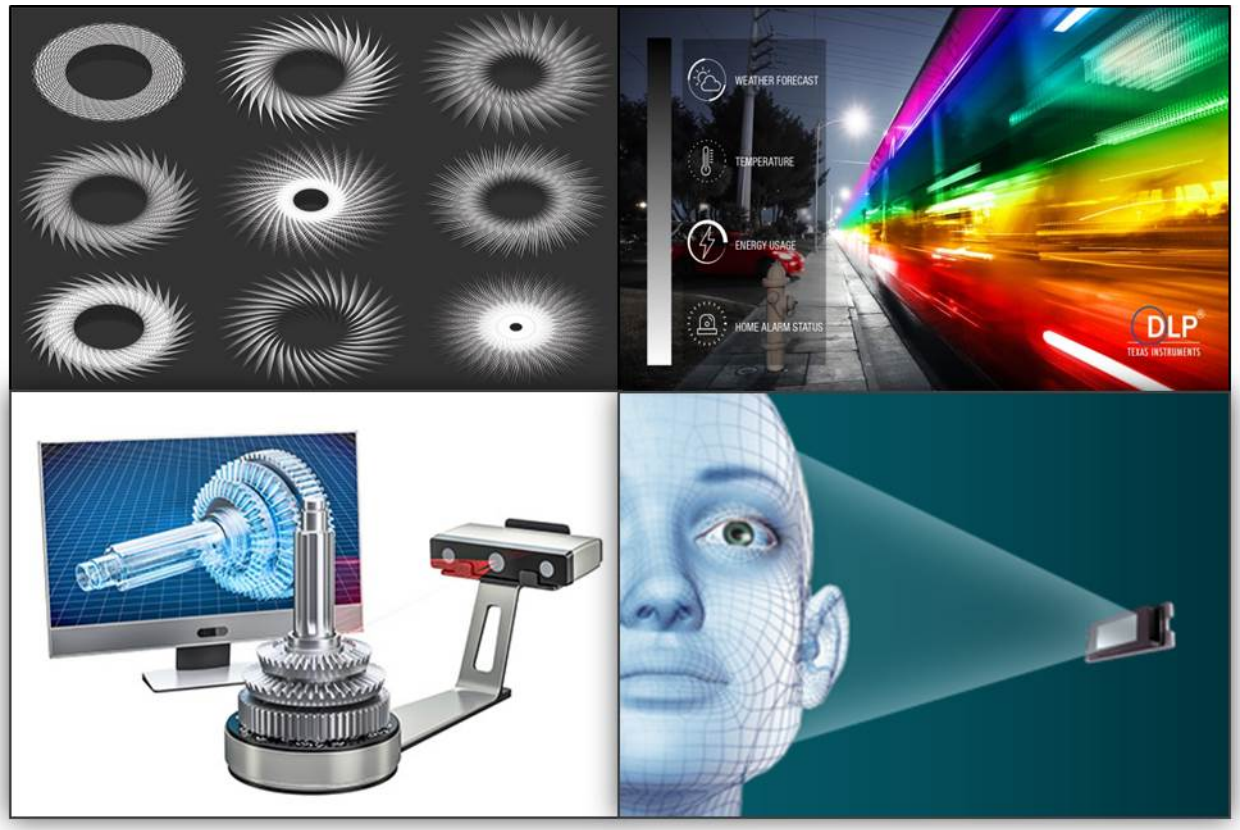


図 16. Monochrome and RGB Image Testing

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-080001.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-08001.

4.3 PCB Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3470, DLP2010, and DLPA2005 data sheets.

4.3.1 DLPC3470 Layout Guidelines

4.3.1.1 Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC3470 contains two internal PLLs, which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins must be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. Place all four components as close to the ASIC as possible, however it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors must be connected across VDD_PLLM and VSS_PLLM/VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3470 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

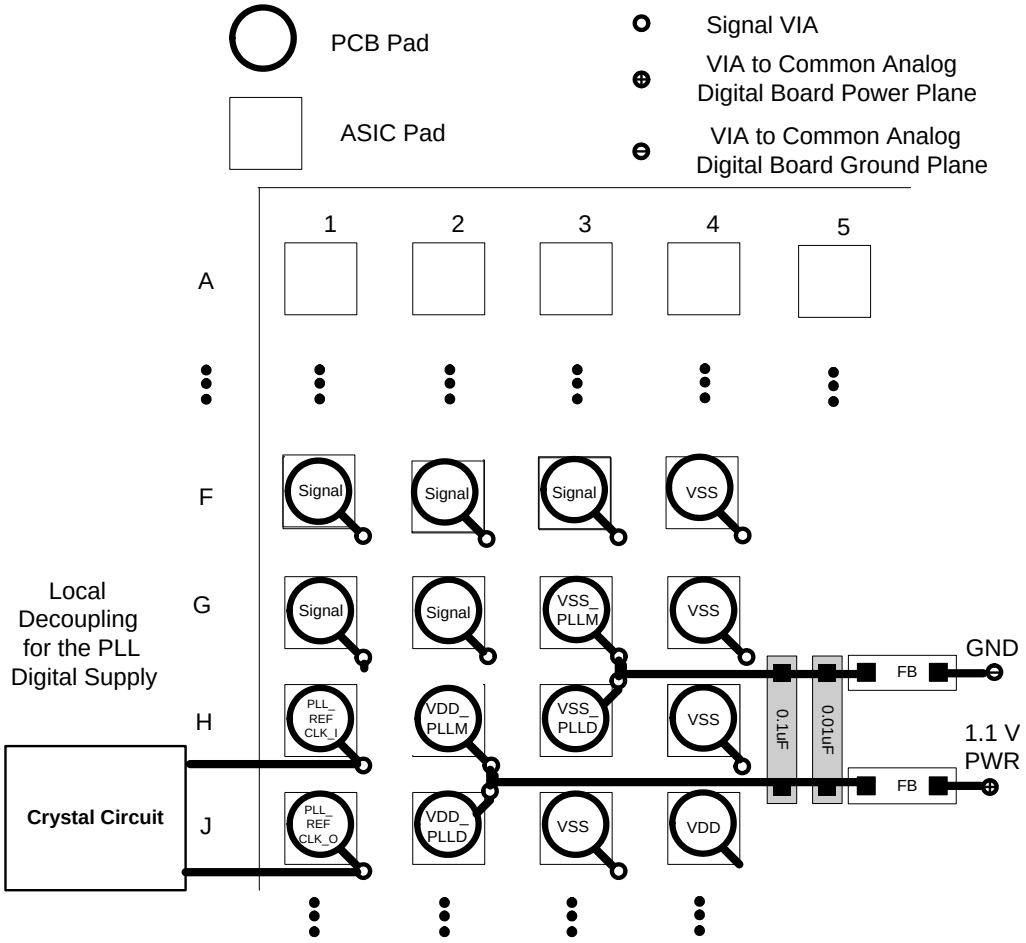


図 17. PLL Filter Layout

4.3.1.2 I²C Interface Performance

Both DLPC3470 I²C interface ports support a 100-kHz baud rate. By definition, I²C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

4.3.1.3 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3470 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

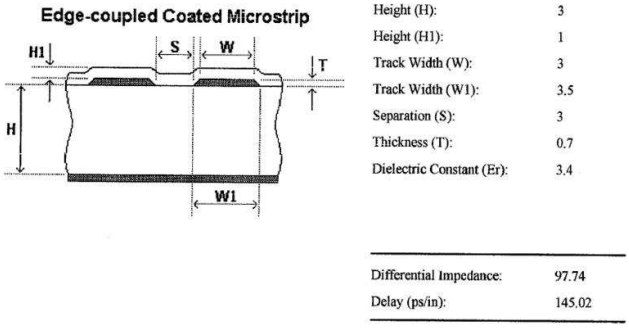
Setup Margin = (DLPC3470 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time Margin = (DLPC3470 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

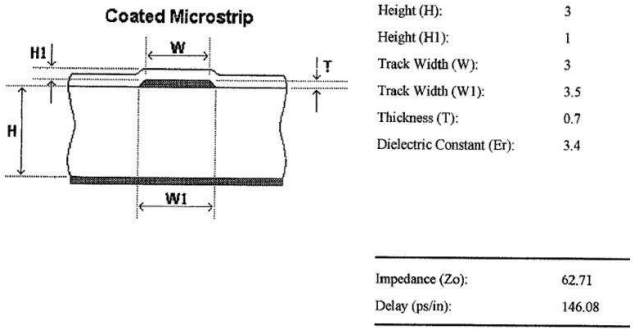
where PCB SI degradation is signal integrity degradation due to PCB effects, which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

DLPC3470 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations can also work, but must be confirmed with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals



DMD_LS Signals

図 18. DMD Interface Board Stack-Up Details

4.3.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends tying unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown resistor to ground. For ASIC inputs with internal pullup or pulldown resistors, do not add an external pullup or pulldown resistor unless specifically recommended.

注: Internal pullup and pulldown resistors are weak and must not be expected to drive the external line. The DLPC3470 device implements very few internal resistors, and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins can become an input, then the pins must be pulled up (or pulled down) using an appropriate, dedicated resistor.

4.3.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

表 5. Max Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See (3)	inch (mm)
DMD_LS_WDATA	6.5 165.1	See (3)	inch (mm)
DMD_LS_RDATA	6.5 165.1	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See (3)	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

表 6. High Speed PCB Signal Routing Matching Requirements(1)(2)(3)(4)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH(5)**	**UNIT**
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC3470 or the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance for a signal group is always with respect to reference signal.

4.3.1.6 *Number of Layer Changes*

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

4.3.1.7 *Stubs*

- Avoid stubs.

4.3.1.8 *Terminations*

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths must include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path must include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

4.3.1.9 *Routing Vias*

- Minimize the number of vias on DMD_HS, DMD_LS_CLK, and DMD_LS_WDATA signals to not

exceed two.

- Any and all vias on these signals must be located as close to the ASIC as possible.

4.3.2 DLPA2005 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

図 19 shows an example layout that has critical parts placed as close as possible to the pins they are connected to. Here are recommendations for the following components:

R1	is RLIM and is connected via a wide trace (low resistance) to the system ground. The analog ground at pin 5 should be star connected to the point where RLIM is connected to the system ground. Aim on a wide and low-ohmic trace as well, although this one is less critical (tens of mA).
L1	is the big inductor for the VLED that is connected via two wide traces to the pins
C4	are the decoupling capacitors for the VLED and they are as close as possible placed to the part and directly connected to ground.
L3/C20	are components used for the VCORE BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin
L2	This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2005 using wide PCB traces.

4.3.2.1 Layout Example

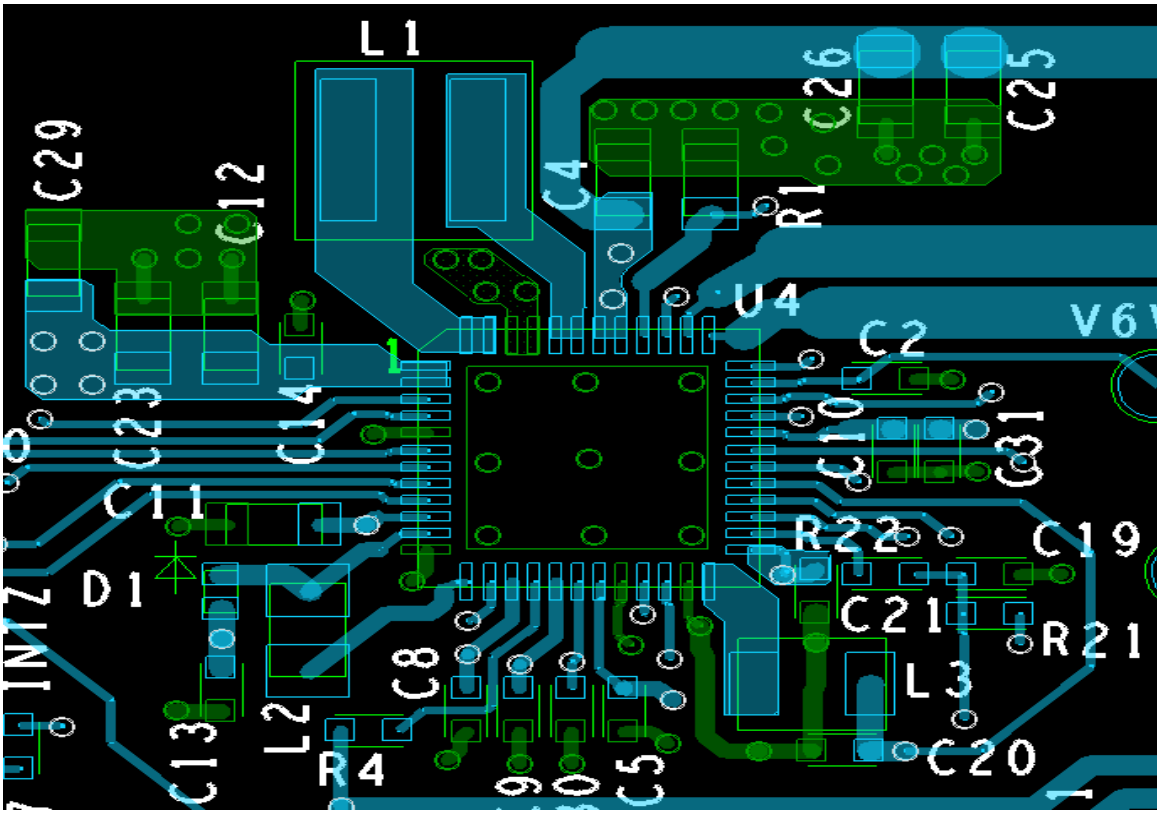


図 19. Example Layout of DLPA2005

4.3.2.2 Thermal Considerations

An important consequence of the efficiency numbers shown in 図 20 is that they enable DLPA2005 thermal calculations.

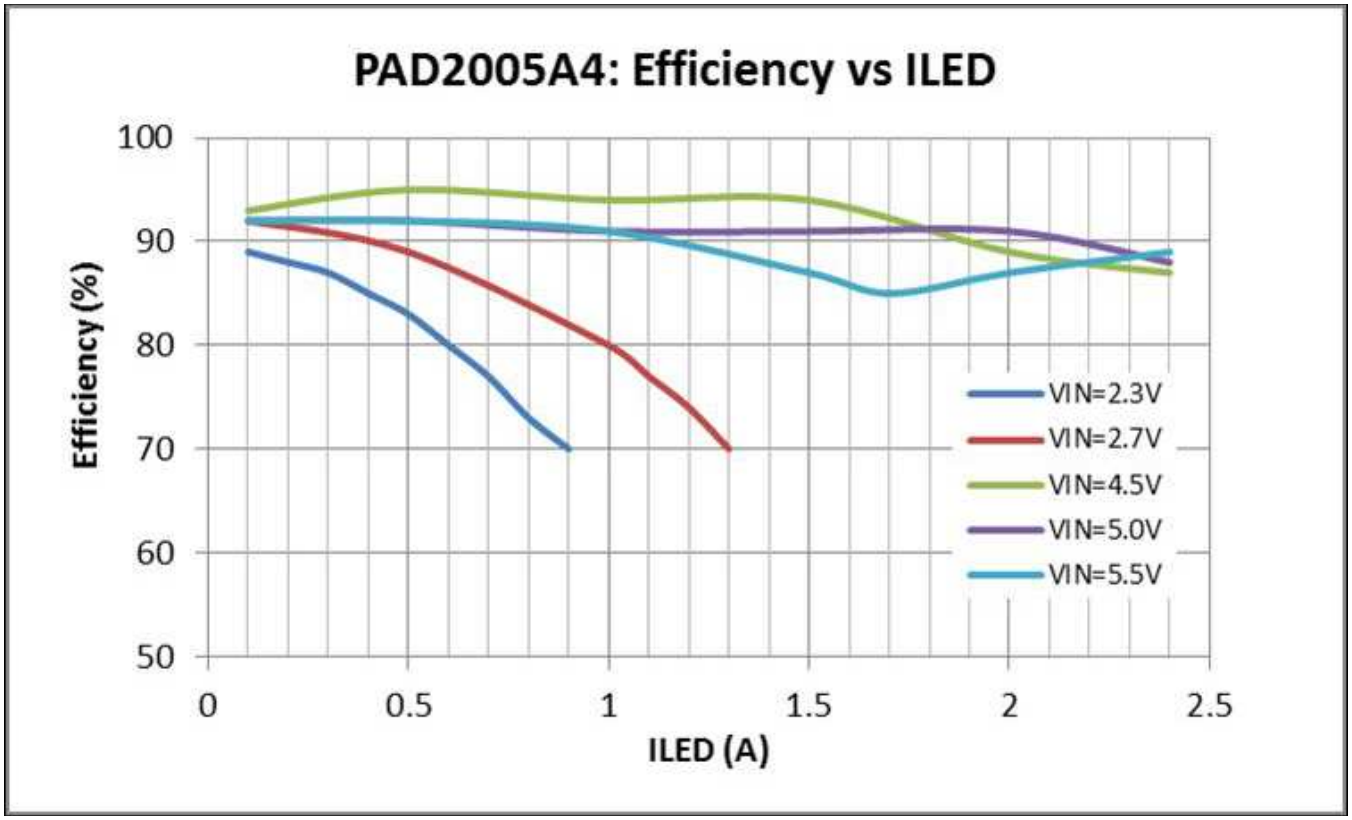


図 20. Measured Typical Power Converter Efficiency as a Function of ILED for Several Supply Voltages (V_{OUTmax} = 4.8 V for Each Supply)

Since the efficiency is not 100%, power is dissipated in the DLPA2005 chip. Due to that dissipation die temperature will rise. For reliability reasons, use die temperatures that are as low as possible. Using a heat sink and airflow are efficient means to keep die temperature reasonably low. In cases that airflow or a heat sink is not feasible, the system designer should specifically pay attention to the thermal design. The die temperature for regular operation should remain below 120°C.

The following is an example of a thermal calculation. The calculation starts with summarizing all blocks in the DLPA2005 that dissipate. Clearly, the buck-boost converter supplying the LED power is the main source of dissipation. For illustrating purposes here we assume this buck-boost converter to be the only block that dissipates significantly. For the example assume: V_{OUT} = 4.8 V (for all three LEDs), I_{OUT} = 2.4 A, and V_{IN} = 5 V. From 図 20, the derived related efficiency is about n_{eff} = 88%.

The power dissipated by the DLPA2005 is then given by:

$$P_{DISS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{100\%}{\eta_{eff}} - 1\right) = 4.8V \cdot 2.4A \cdot \left(\frac{100\%}{88\%} - 1\right) = 1.6W$$

The rise of die temperature due to this power dissipation can be calculated using the thermal resistance from junction to ambient, θ_{JA} = 27.9°C/W. This calculation yields:

$$T_{JUNCTION} = T_{AMBIENT} + P_{DISS} \cdot \theta_{JA} = 25°C + 1.6W \cdot 27.9°C/W = 69.6°C$$

It is also possible to calculate the maximum allowable ambient temperature to prevent surpassing the maximum die temperature. Assume again the dissipation of P_{DISS} = 1.6 W. The maximum ambient temperature that is allowed is then given by:

$$T_{AMBIENT-\max} = T_{JUNCTION-\max} - P_{DISS} \cdot \theta_{JA} = 120°C - 1.6W \cdot 27.9°C/W = 75.4°C$$

It is again stressed here that for proper calculations the total power dissipation of the DLPA2005 should be taken into account. On top of that, if components that are close to the DLPA2005 also dissipate a significant amount of power, the (local) ambient temperature can be higher than the ambient temperature of the system.

If calculations show that the die temperature will surpass the maximum specified value, two basic options exist:

- Adding a heat sink with or without airflow. This will reduce θ_{JA}, yielding lower die temperature.
- Lowering the dissipation in the DLPA2005 implying lowering the maximum allowable LED current.

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-080001.

4.4 Cadence Project

To download the Cadence project files, see the design files at TIDA-080001.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-080001.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-080001.

5 Software Files

To download the software files, see the design files at DLP2010EVM-LC.

6 Related Documentation

1. Texas Instruments, *DLP2010 Light Control EVM User's Guide*
2. Texas Instruments, *DLPC3470 Display and Light Controller Data Sheet*
3. Texas Instruments, *DLP2010 (0.2 WVGA DMD) Data Sheet*
4. Texas Instruments, *DLPA2005 PMIC and LED/Lamp Driver IC Data Sheet*

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