参考資料

TI Designs: TIDA-010014
光電子測定サブシステム用の低電圧IR LEDドライバのリファレンス・デザイン

概要

このリファレンス・デザインでは、光電子測定サブシステム用のIR LEDドライバの設計サンプルを紹介します。ここで紹介するサブシステムには、オペアンプを基礎とする電圧から電流へのコンバータと、アクティブ・パス・デバイス用のMOSFETトランジスタが含まれ、正確かつプログラム可能な電流シンク機能の基盤を形成します。この回路でMOSFETトランジスタを使用することには、以下で説明するいくつかの利点があります。最も重要なことは、低電圧のバッテリ駆動システムで優れた電流レギュレーションが可能になることです。同様に、帰還におけるオペアンプの高い入力インピーダンスと高いオープン・ループ・ゲインにより、温度範囲全体にわたって回路の応答がフラットになり、電源電圧の変化による出力電流の変動も最小限に抑えられます。

リソース

TIDA-010014	デザイン・フォルダ
TINA-TI™	SPICEシミュレータ
TLV9062	プロダクト・フォルダ
TLV9002	プロダクト・フォルダ
CSD17483F4	プロダクト・フォルダ

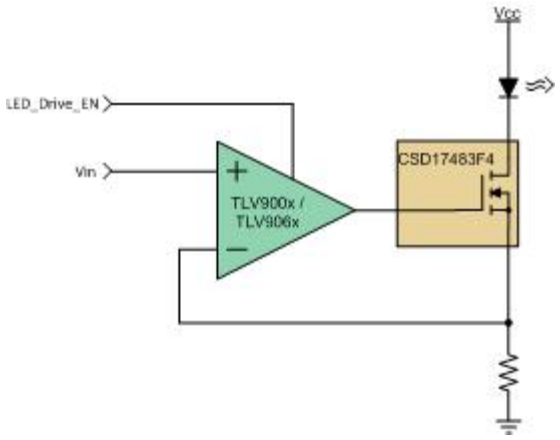
TI E2E™ Community　E2E™ エキスパートに質問

特長

- 3Vバッテリを使用するアプリケーション向けの低電圧動作
- 高速なイネーブル時間と最小限のオーバーシュートにより、LEDの「オン」時間を最小化
- 「オフ」状態での低い消費電流
- 出力電流の可変範囲が広く、線形的
- 小フットプリント

アプリケーション

- 煙および熱感知器
- 大気環境とガスの検出
- 近接センシング
- 改ざん防止保護



1 System Description

Photoelectric sensors have a wide variety of applications ranging from barcode readers to proximity sensing and smoke detectors. A key component of any photoelectric sensor subsystem is the LED driver.

In smoke detector applications, detection of scattered light is used to sense the amount of smoke in the air. As such, a large amount of photons must be generated by the transmitter (IR LED) so that there is enough scattered light to be detected by the receiver (photodiode). This requirement means high forward current through the LED. Additionally, due to recent changes in standards, long battery life and better sensitivity is required. For the LED driver, this requirement means faster turnon time and the ability to run at low supply voltage without losing accuracy in the forward current setting. Air quality and gas detection applications operate in a similar fashion with the only difference being the physical size of the particles being detected. Thus, the advantages of this LED driver design will be equally beneficial for air quality and gas detection.

Proximity sensing and tamper protection applications can be implemented with a variety of different circuit technologies. However, both are commonly implemented using photoelectric sensing. Because proximity sensing and tamper protection are functions that need to be continually active, low power operation is key. This is especially important for the LED driver since the LED is continually flashed at a low duty cycle. The fast turnon time and accurate current setting achieved with this LED driver design allow lower duty cycles and low operating voltage, thereby realizing substantial power savings for these applications.

Use of the low-cost, general-purpose family of TI op amps such as the TLV900x and TLV906x allow for operation down to ~2.5 V with an IR LED and a wide dynamic range for the input voltage to LED current conversion. These devices also offer low LED driver shutdown current and ensure enable times through the use of dedicated shutdown pin options.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Operating voltage	2.5 V to 5 V	2.4.1
IR LED current adjustment range	40 mA to 350 mA	2.5.3
Enable time	< 5 µs	2.5.4.2
Disable time	< 50 µs	2.5.4.2
Operation temperature	0°C to 70°C	2.3

2 System Overview

2.1 Block Diagram

図 1 illustrates the TIDA-010014 block diagram.

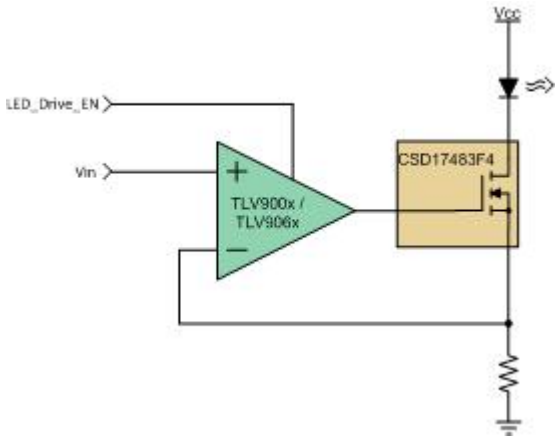


図 1. TIDA-010014 Block Diagram

2.2 Design Considerations

Photoelectric measurement subsystems typically rely on the sensing of reflected photons from illuminated objects. To create enough photons to produce a signal with enough signal-to-noise ratio (SNR), the LED current is typically driven on the order of hundreds of milliamps. For reliability and power savings, the LEDs are pulsed at a low duty cycle, thus requiring minimal overshoot and fast turnon times to achieve the most efficient LED operation. Further, the LED wavelength required depends on the particle size being illuminated, that is, smaller particles need shorter wavelengths of light for illumination.

Most systems allow for adjustment of the LED drive current through firmware to accommodate calibration routines, certain algorithms requiring different LED current set points, or to compensate for environmental changes such as temperature or even component aging. The LED driver subsystem should have a large adjustment range for the output current to maintain system flexibility.

Several considerations must be taken into account for this particular design:

- The op amp should feature rail-to-rail operation on the output. At a minimum, operation will be to negative rail but preferably to both rails on the input to maximize the upper adjustment range.
- The op amp input offset should be at least 10 times lower than the minimum input voltage.
- The op amp overload recovery time will impact turnon time going from an off state where V_{in} = 0 V to an on state. This time needs to be less than the required turnon time specification. Generally, the op amp overload recovery time should be 2 times to 10 times lower than the required turnon time.
- The op amp bandwidth requirement will also largely depend on the turnon time and settling time specifications, especially where the step sizes between programmed output current values are small. That is, small step size requires higher bandwidth to achieve a given turnon time and settling time.
- The MOSFET transistor R_{DS_ON} should be low so that the minimum supply voltage is met at the maximum LED current set point with the transistor operating in its linear region.
- The MOSFET transistor V_{TH} should be much less than the minimum supply voltage minus the maximum input voltage to the circuit to allow for tolerances in the threshold voltage, as well as

changes in threshold voltage and gate-to-source overdrive voltage due to changes in output current.

The remainder of this design guide will illustrate use of devices meeting the criteria set forth previously.

2.3 Highlighted Products

2.3.1 TLV9062

The TLV906x series is a family of low-power, rail-to-rail input and output op amps designed for cost-optimized systems. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and are designed for driving sampling analog-to-digital converters (ADCs).

The device features include:

- Rail-to-rail input and output
- Low input offset voltage: ±0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: 10 nV/ √ Hz
- Low Input Bias Current: 0.5 pA
- Low quiescent current: 538 μA/channel
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version: TLV906xS
- Extended temperature range: –40°C to +125 °C

図 2 shows the TLV9062 functional block diagram.

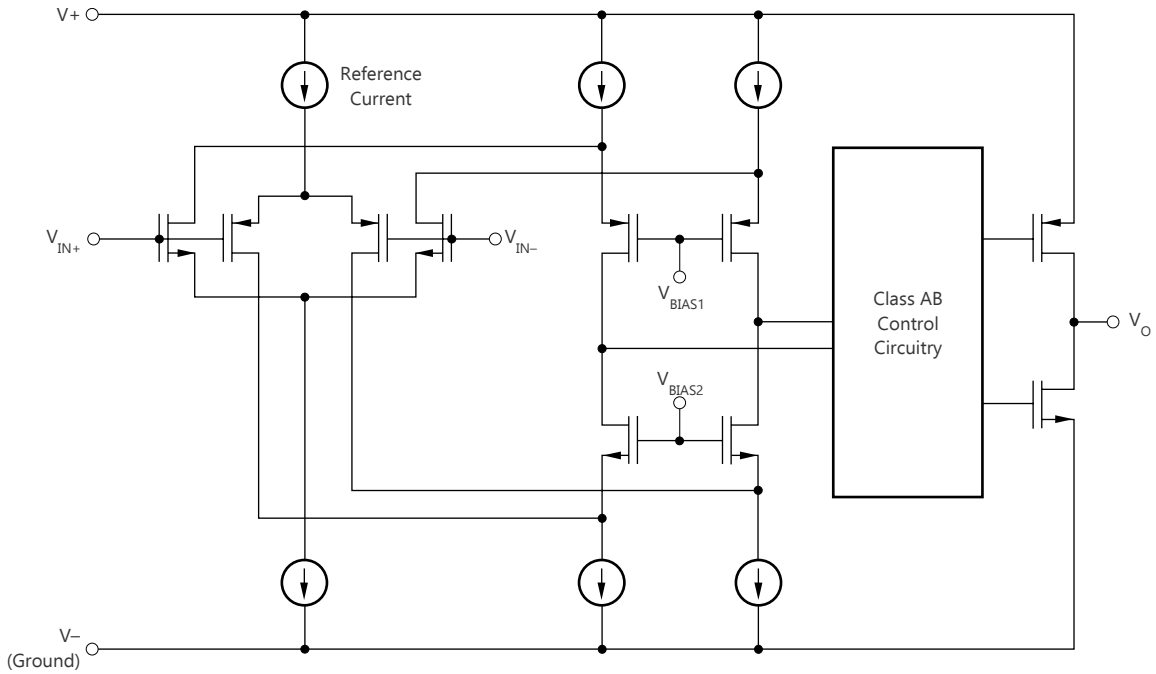


図 2. TLV9062 Functional Block Diagram

2.3.2 TLV9002

The TLV900x series is a family of low-power, rail-to-rail input and output op amps designed for cost-optimized systems. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

The device features include:

- Rail-to-rail input and output
- Low input offset voltage: ±0.4 mV
- Unity-gain bandwidth: 1 MHz
- Low broadband noise: 27 nV/ √ Hz
- Low input bias current: 5 pA
- Low quiescent current: 60 μA/Ch
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Extended temperature range: –40°C to +125 °C

図 3 shows the TLV9002 functional block diagram.

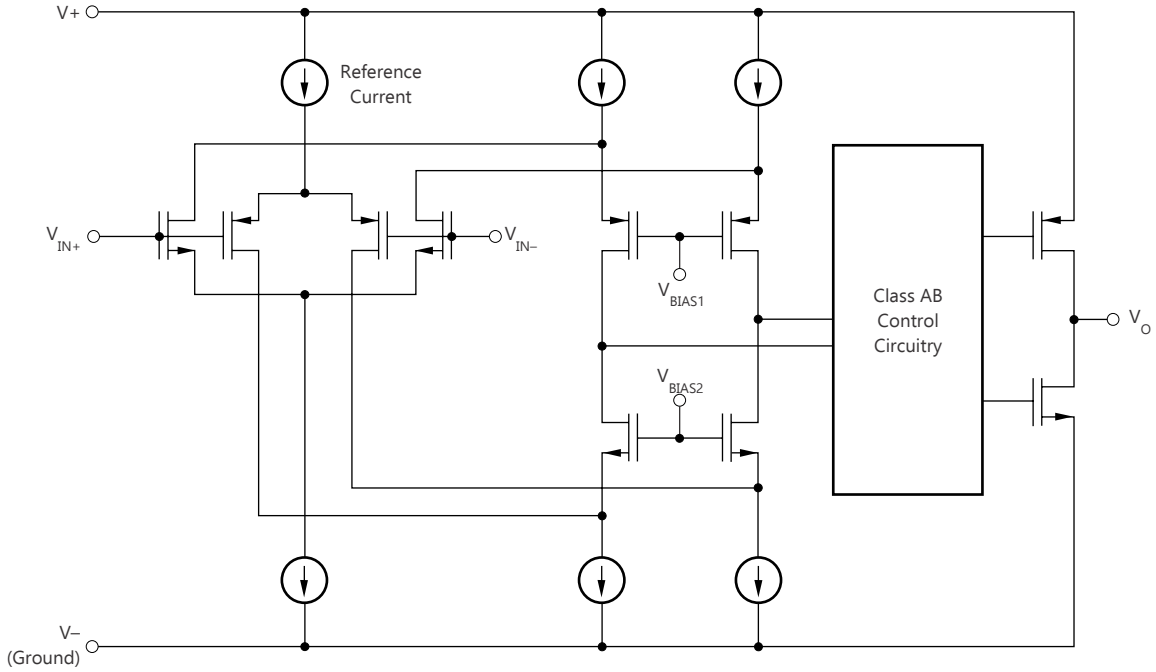


図 3. TLV9002 Functional Block Diagram

2.3.3 CSD17483F4

This 200-m Ω , 30-V N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

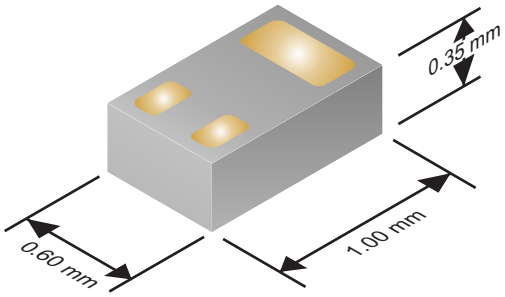


図 4. CSD17483F4 Typical Part Dimensions

The device features include:

- Low on-resistance
- Low Q_g and Q_{gd}
- Low-threshold voltage
- Ultra-small footprint (0402 case size)
  - 1.0 mm × 0.6 mm
- Ultra-low profile
  - 0.35-mm height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

図 5 shows the CSD17483F4 functional block diagram.

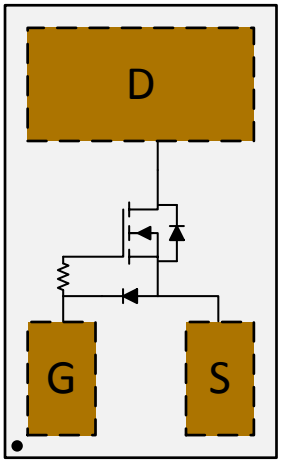


図 5. CSD17483F4 Functional Block Diagram

2.4 System Design Theory

The circuit illustrated in 図 1 shows the basic schematic concept for the LED driver subsystem. The function of this circuit is a voltage-to-current converter arranged as a constant current sink. The transfer function of this circuit is $I_{LED} = V_{in} / R$. Due to the high input impedance of the op amp, the voltage across the current setting resistor will be equal to the voltage applied at V_{in} while the open loop gain of the amplifier provides loop gain for the resulting control loop. The loop gain in turn increases the output impedance of the circuit by $A_{loop} * r_{o\_FET}$ which results in a nearly-ideal current sink function. Intuitively, the op amp controls the gate voltage of the FET so that the equation for I_{LED} is true for changes in V_{in} as well as the supply voltage. For low supply voltage operation, or in cases where the load has a large voltage drop for the programmed current value, the FET will be forced into linear operation. However, as long as the supply voltage is greater than or equal to $V_{F\_LED} + I_{LED} * R_{DS\_ON\_FET} + V_{in}$ the circuit will continue to operate as a high impedance current sink, assuming $V_{OH\_Op\text{-}Amp} + V_{GS\_FET} < V_{F\_LED} + I_{LED} * R_{DS\_ON\_FET}$. The design considerations listed in 2.2 ensure that the minimum operating voltage is not limited by the chosen op amp or FET input characteristics.

Because the circuit shown in 図 1 implements a control loop, additional components are necessary for stable circuit operation. 図 6 shows the complete circuit schematic.

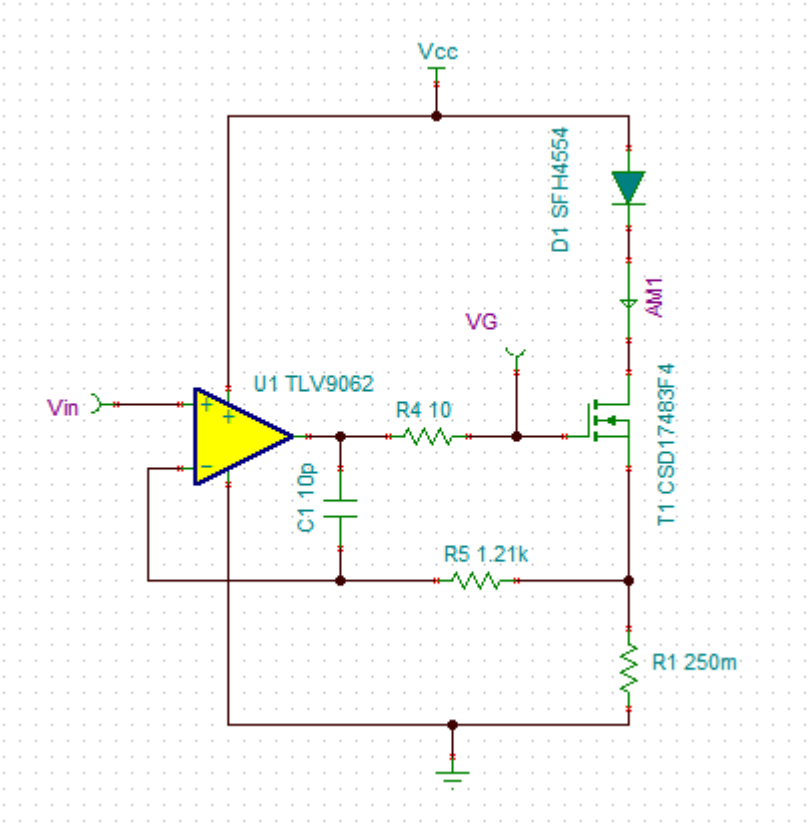


図 6. TIDA-010014 LED Driver Schematic

Components R4, R5, and C1 make up the compensation network for the LED Driver circuit, and all three components must be included to properly compensate the loop. R4 is used to isolate the op amp output from the high capacitance load of the MOSFET, while C1 bypasses the MOSFET at high frequencies. R5 is used to set the frequency where C1 begins to bypass the output network. Because this type of double loop compensation does not have a closed form solution for determining the exact component values, an

intuitive approach is required. The approach taken in this design is as follows: First, R4 should be sized based on the op amp's data sheet recommendations based on the estimated capacitive load presented by the MOSFET being used. Second, initial values of 10 kΩ for R5 and 10 pF for C1 are chosen. Due to op amp parasitics and other stray capacitances, 10 pF represents a minimum value for C1. AC small signal stability simulations along with transient stability simulations can be used to dial in the desired performance. Alternatively, bread boarding can also be used to determine the final component values, however, simulations provide a good alternative to making many PCB modifications. Any simulation-derived solution, ideally, must be verified at the PCB level. Use the following guidelines for adjusting the component values for desired performance:

- Increasing the value of R4 results in decreased phase margin and longer rise time and settling time.
- Increasing the value of C1 results in increased phase margin at the expense of slower transient response.
- For fixed R4 with adequate phase margin and transient response, the value of C1 and R5 can be adjusted as long as C1*R5 is kept constant.
- For C1 > 100 pF, an additional resistor in series with C1 may be needed if overshoot and ringing begin to increase with increases in C1.

There are a couple of different ways that the input to the LED driver is generated. The first of these uses a DAC followed by a voltage divider to maximize the dynamic range of the DAC. This circuit is illustrated in 図 7. The second method, commonly used to drive the input, is to use a PWM followed by a simple RC filter. This circuit is illustrated in 図 8.

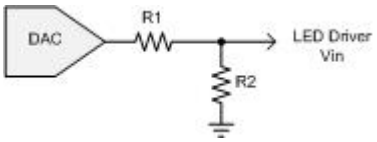


図 7. DAC Driven Input Circuit

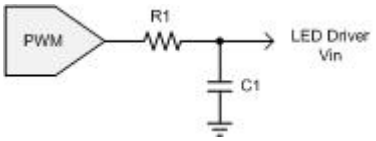


図 8. PWM Driven Input Circuit

The DAC-driven approach generally provides a solution for applications requiring high-resolution output current steps. The PWM approach can be used for cost-constrained applications where high-resolution output current steps are not required. The PWM approach also has the flexibility of providing a high-resolution design if using an MCU with high-resolution timers.

Another important aspect of this LED driver circuit is that, due to the feedback and op amp high-impedance input, this circuit exhibits a flat response over temperature.This response means that with a constant input voltage applied, the output current value will be constant across temperature. In many applications, especially smoke detectors, it is preferred that the final output of the photoelectric measurement system provide a constant output across temperature. One way of generating this temperature independent output is to adjust the LED current to compensate for the temperature

dependence of the entire signal chain. Using the topology shown in 図 6 along with either of the input circuits described, all that is needed is a temperature measurement taken prior to the LED turnon pulse and knowledge of the signal chain temperature coefficient to adjust the LED driver output current value. Using an LED driver circuit with a zero temperature coefficient simplifies the compensation calculation saving power and processing time as well as memory space for firmware in the overall system design.

2.4.1 Circuit Design

Aside from the design of the compensation network previously covered, there is only one component value to design in this circuit, which is R1 shown in 図 6. With the minimum supply voltage and maximum output current known, R1 can be determined by using the following equations:

$$V_{R1} = V_{Supply\_min} - I_{Out\_max} \times R_{DS\_ON\_FET}\big|_{VG = V_{Supply\_min}} - V_{F\_LED} \quad (1)$$

$$R1 = \frac{V_{R1}}{I_{Out\_max}} = \frac{\left(V_{Supply\_min} - V_{F\_LED}\right)}{I_{Out\_max}} - R_{DS\_ON\_FET}\big|_{VG = V_{Supply\_min}}$$

式 2 assumes that the chosen op amp has the ability to drive the gate of the FET all the way to the positive rail and that the sum of the voltage drops for the LED and MOSFET are less than the minimum supply voltage. In most cases, the forward voltage drop of the LED at the maximum output current will be known because this is the component for which this circuit is designed to drive. This leaves the choice of FET to satisfy one of the main underlying assumptions.

The LED shown is an 860 nm wavelength narrow beam angle device typically used in smoke detector applications. For this design, the forward voltage drop of the LED at 350 mA is roughly 2.2 V leaving 0.3 V for the voltage drop across the FET and R1. With R1 = 250 mΩ, the voltage drop across R1 will be ~90 mV, so the choice of FET for this design must drop less than 210 mV at 350 mA output current, or equivalently have an R_{DS_ON} value less than 600 mΩ at V_{GS} = 2.41 V. The chosen CSD17483F4 data sheet shows a maximum resistance of 310 mΩ at V_{GS} = 2.5 V, so the requirements of the circuit are therefore met with margin.

The minimum output current specification, with the value of R1 fixed, will determine the minimum input voltage by $V_{in\_min} = I_{Out\_min}$*R1. The op amp input offset voltage should be low compared to V_{in_min} so that output current error is minimized. The op amps highlighted in this reference design, TLV9062 and TLV9002, both have typical input offset voltage less than 0.5 mV, whereas V_{in_min} as designed is 10 mV.

Lastly, the chosen FET should have an output voltage rating equal to V_{Supply_max}. The CSD17483F4 is a 30 V rated device which is more than adequate for a 5 V supply. (2)

2.4.1.1 Component Selection

2.4.1.1.1 Amplifier Selection

As discussed in 2.4.1, the op amp in this design should feature rail-to-rail operation on the output and at least to negative rail on the input. Preferably, operation to both rails on the input is needed to maximize the upper end of the adjustment range. The op amp input offset should be at least 10 times lower than the minimum input voltage as described in the design section.

To satisfy the turnon time specification for this design, op amp overload recovery and unity gain bandwidth parameters will have an impact. The op amp overload recovery time will impact turnon time going from an off state where V_{in} = 0 V to an on state. This needs to be less than the required turnon time specification. The op amp unity gain bandwidth requirement will largely impact the turnon time and settling time specifications, especially where the step sizes between programmed output current values are small. That is, small step size requires higher bandwidth to achieve a given turnon time and settling time. The difference in turnon time due to the effects of these two op amp parameters will be illustrated in simulations shown in 2.5.4.1.

2.4.1.1.2 FET Selection

As described in 2.4.1, the MOSFET transistor R_{DS_ON} must be low so that the minimum supply voltage is met at the maximum LED output current set point. The MOSFET transistor V_{TH} parameter must be much less than the minimum supply voltage minus the maximum input voltage to the circuit to allow for tolerances in the threshold voltage as well as changes in threshold voltage and gate-to-source overdrive voltage due to changes in output current. This requirement also assumes the output of the op amp is able to drive the MOSFET gate to positive rail. If the op amp does not have this capability, then the MOSFET V_{TH} required must be reduced by the op amp V_{OH} value. The MOSFET V_{DS} voltage rating must be greater than the maximum supply voltage specification.

2.4.1.1.3 Passive Component Selection

Standard metal film 1% resistors are sufficient for this design. The exception may be R1, where a tighter tolerance may be desired for higher accuracy output current settings. Ceramic X7R capacitors are sufficient for this design. Although not shown in the simulation schematics for this reference design, a supply decoupling capacitor for the op amp should be included. Refer to the appropriate op amp data sheet for guidance on decoupling capacitor values.

2.5 Simulation and Results

2.5.1 AC Small Signal Stability

図 9 shows the TINA-TI schematic used to simulate the AC small signal stability of the LED driver.

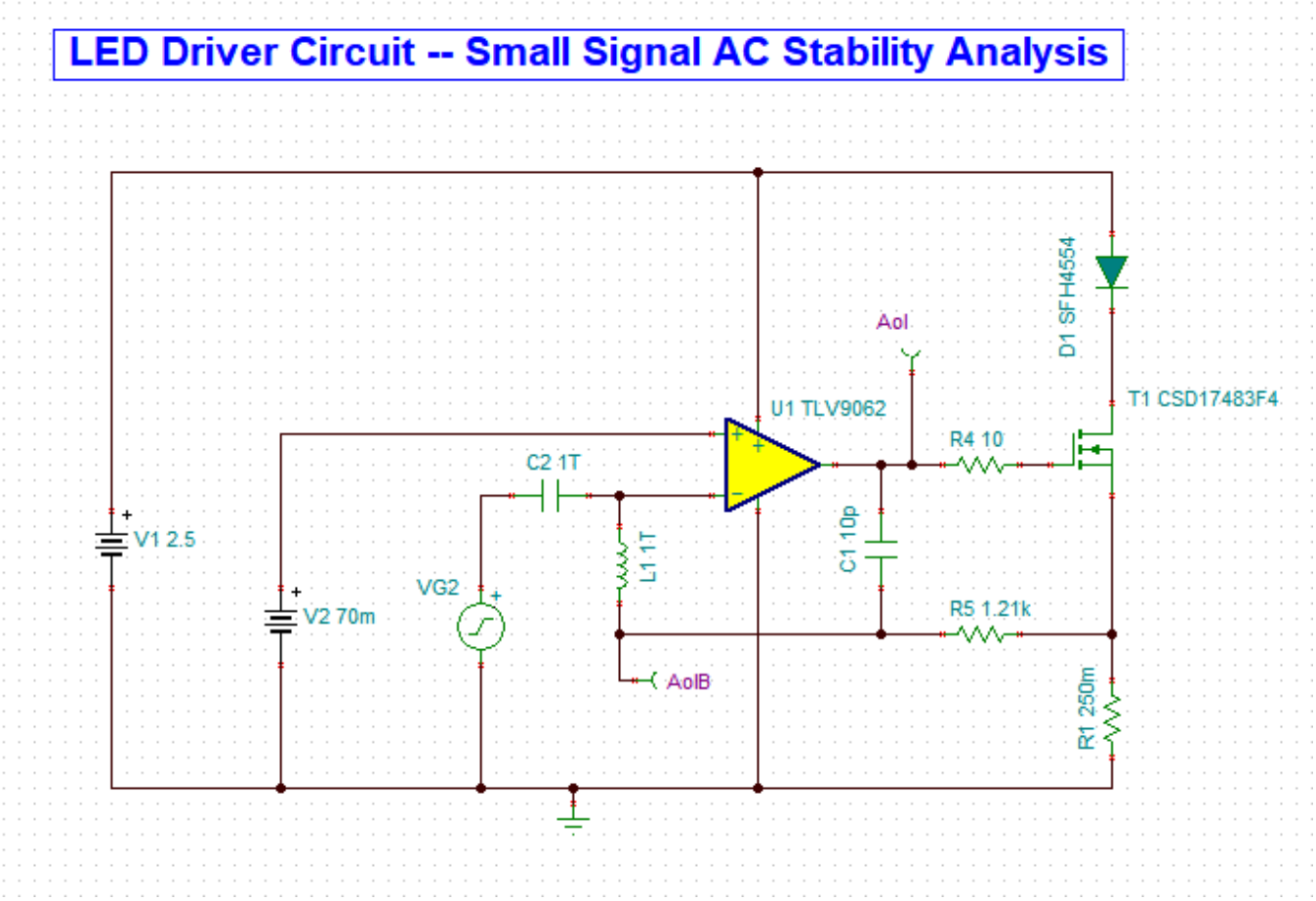


図 9. AC Small Signal Stability Simulation Schematic

The main components for this test bench are L1 and C2 with AC source VG2. C2 provides an open circuit at DC where L1 provides a short circuit to close the loop and establish the DC operating point. Under AC conditions, C2 will be a short circuit while L1 will be an open circuit, thereby opening the loop for stability analysis. Probe A_{ol}, as the name implies, will show the open loop gain response of the op amp, while probe AolB will show the loop gain of the circuit. Similarly, AoI / AolB will show the response of 1/β for the feedback loop.

図 10 shows the small signal stability frequency response of the circuit. As shown, the circuit is very stable with close to 90° of phase margin.

One caveat of breaking the feedback at the location shown for AC analysis is that the effect of the op amp input capacitance on the loop response is neglected. This capacitance can be added between node AolB and ground to observe the effect. In this case, the phase margin decreases to 84.2 degrees with a 0-dB crossing frequency of 3.43 MHz compared to what is shown in 図 10.

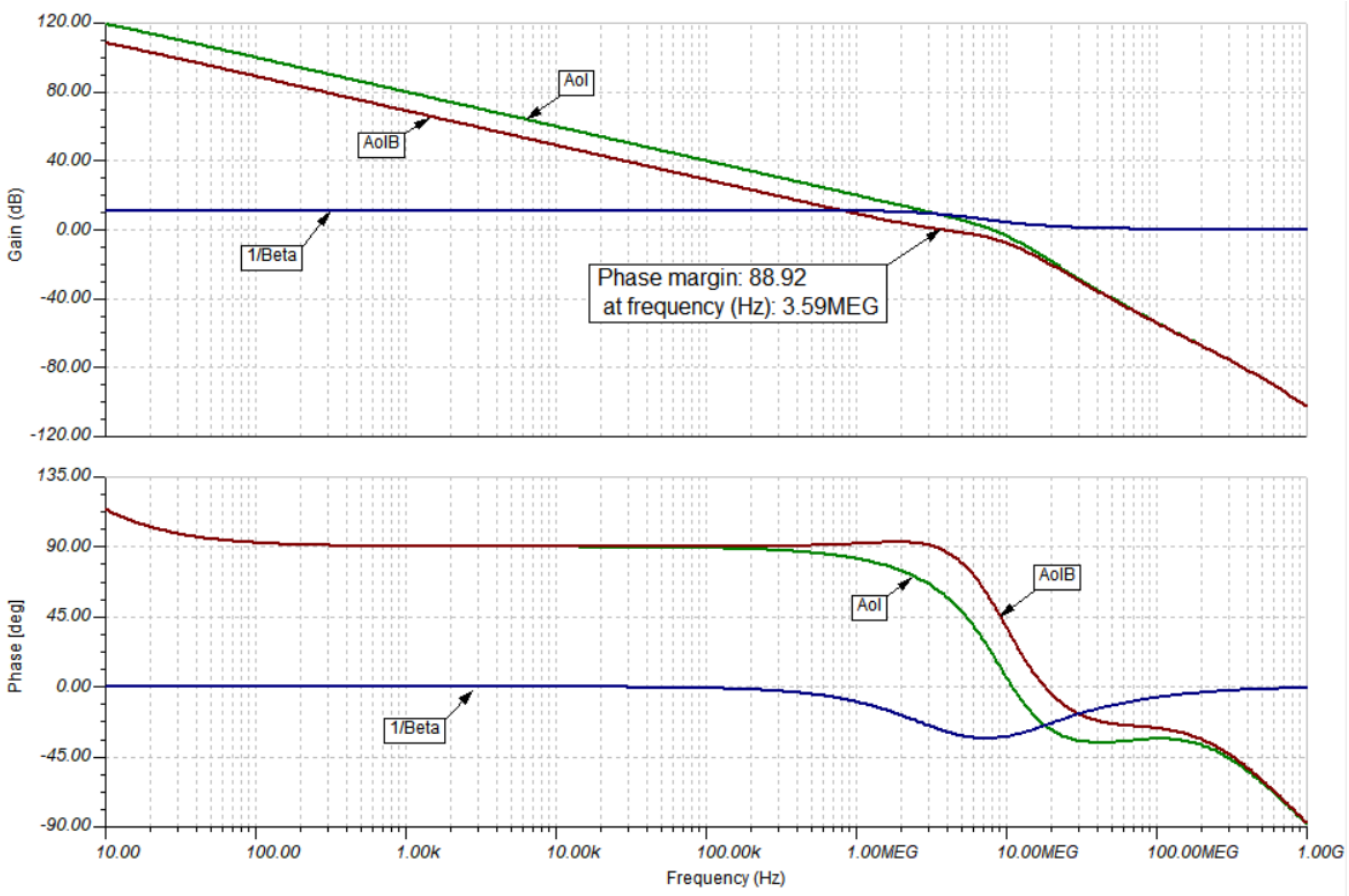


図 10. AC Small Signal Stability Analysis Results

2.5.2 Transient Step Response (Stability)

To reinforce the results of the AC small signal stability analysis, transient step response simulations should always be performed. For this design, two different step response simulations are performed. The first is a large amplitude step from a 0-V input while the second is a low amplitude step from the minimum input voltage (or any input value in the operating range). The value for the low amplitude test is typically 1 mV to 10 mV. The value is 1 mV in this case, however, the point is that the step size is within the linear range of the input pair of the amplifier which is usually less than 100 mV.

The low amplitude step response generally is a good confirmation of results from the AC response. Exercising this simulation at different initial points allows evaluation of any stability dependence on the DC operating point. A similar analysis can be performed in the frequency domain by varying V2 in 図 9.

The purpose of the large amplitude step response is to look for possible stability problems by taking the amplifier out of its linear region of operation due to effects such as internal or external slewing.

2.5.2.1 Large Amplitude Response

The TINA-TI simulation schematic for the large amplitude transient step response is shown in 図 11.

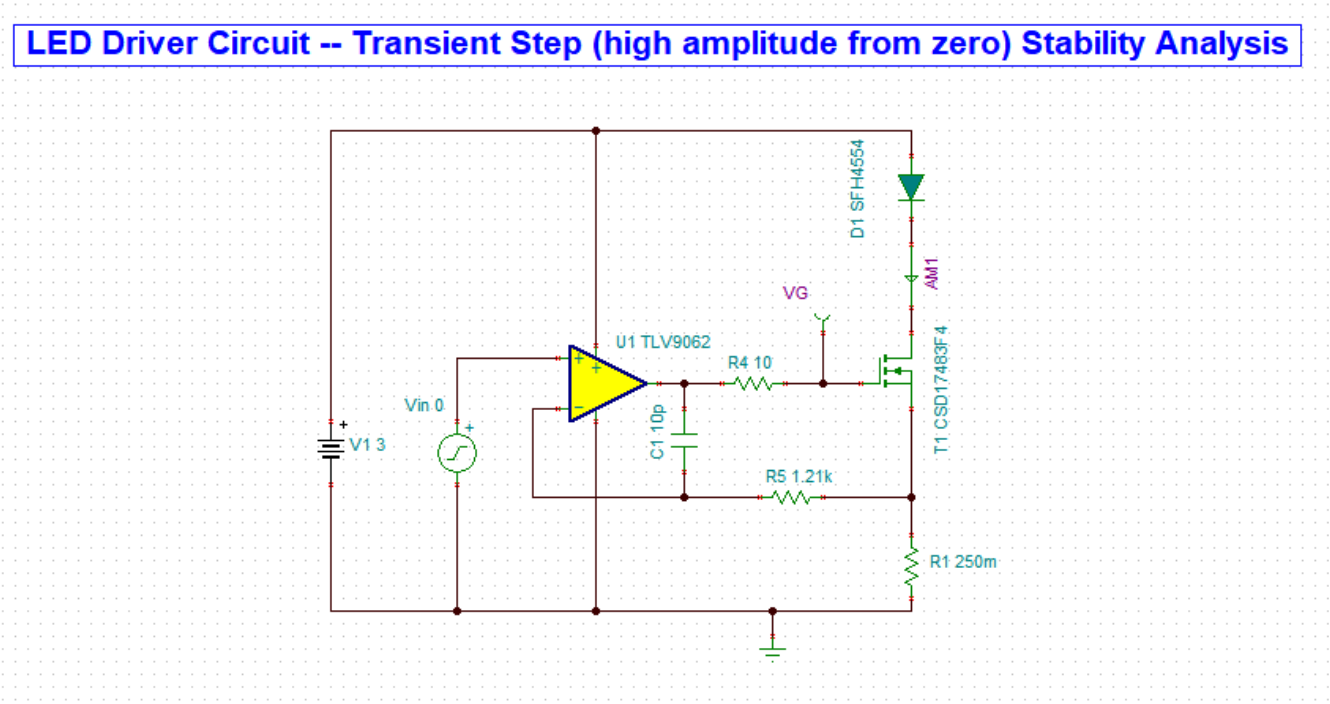


図 11. Large Amplitude Transient Step Response Simulation Schematic

図 12 shows the results for the large amplitude transient step response. As shown, there appears to be no large signal stability issues with good agreement with the small signal AC results.

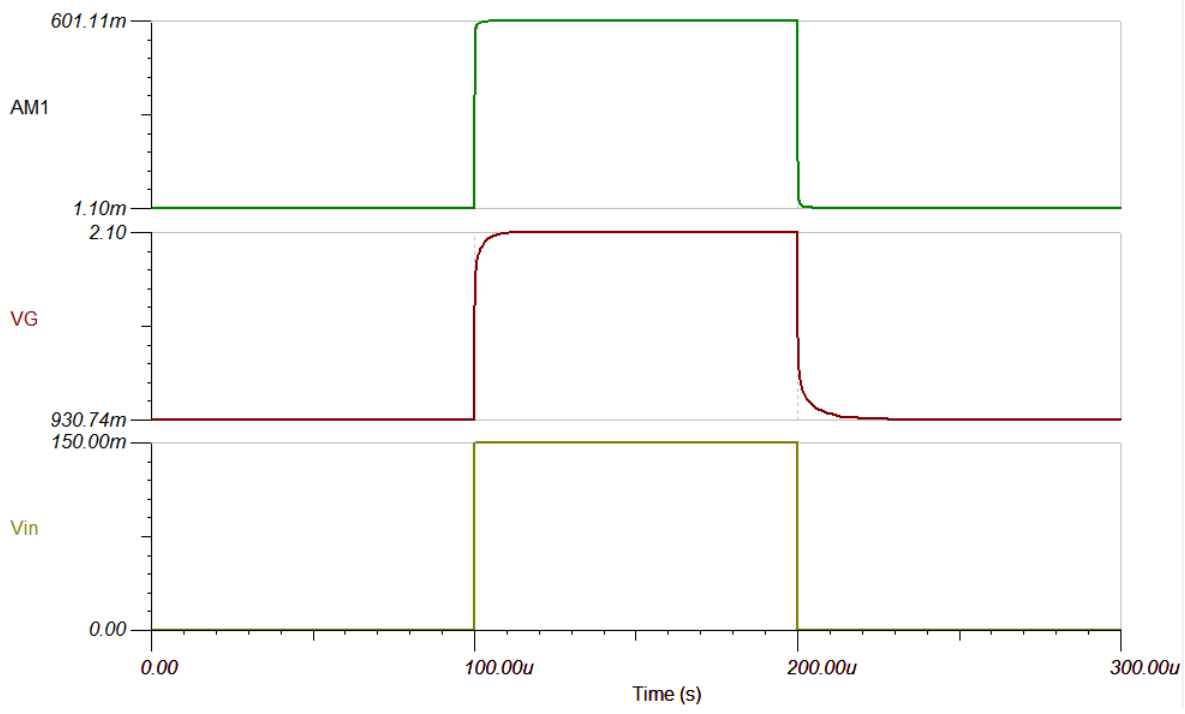


図 12. Large Amplitude Transient Step Response

2.5.2.2 Low Amplitude Response

The TINA-TI simulation schematic for the low amplitude transient step response is shown in 図 13.

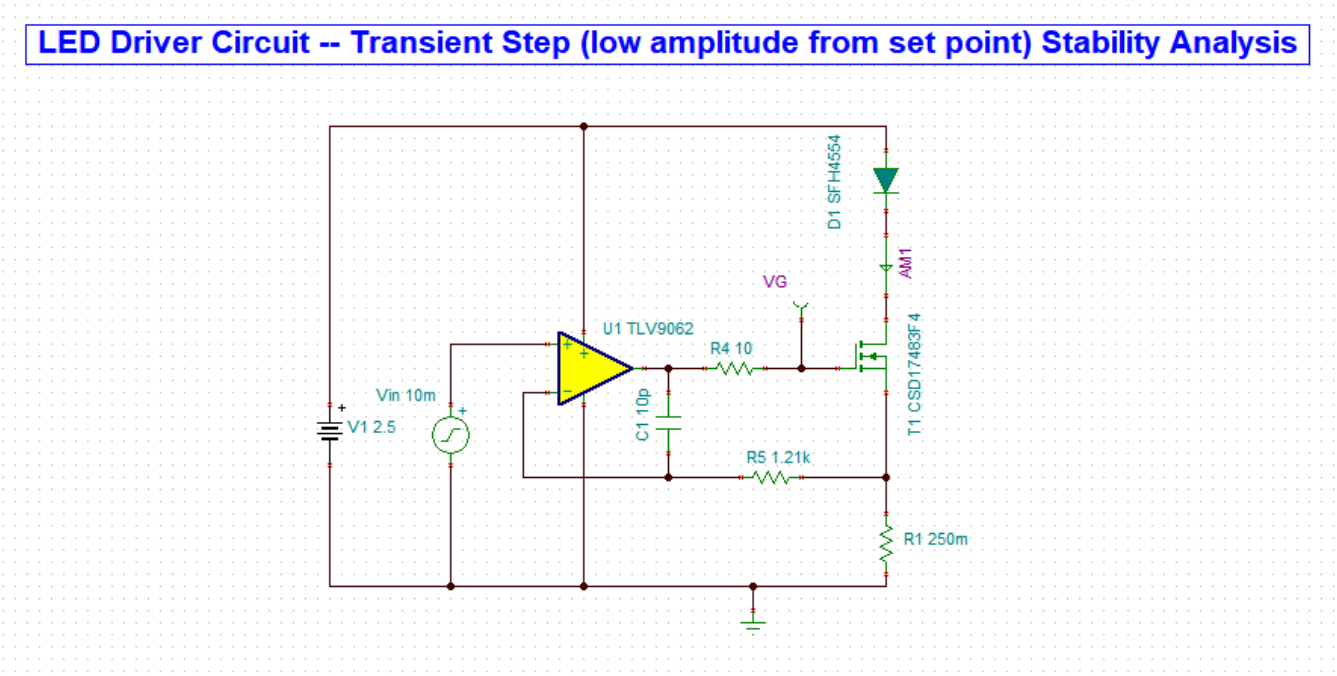


図 13. Low Amplitude Transient Step Response Simulation Schematic

図 14 shows the results for the low amplitude transient step response. As shown, there appears to be good agreement with the small signal AC results.

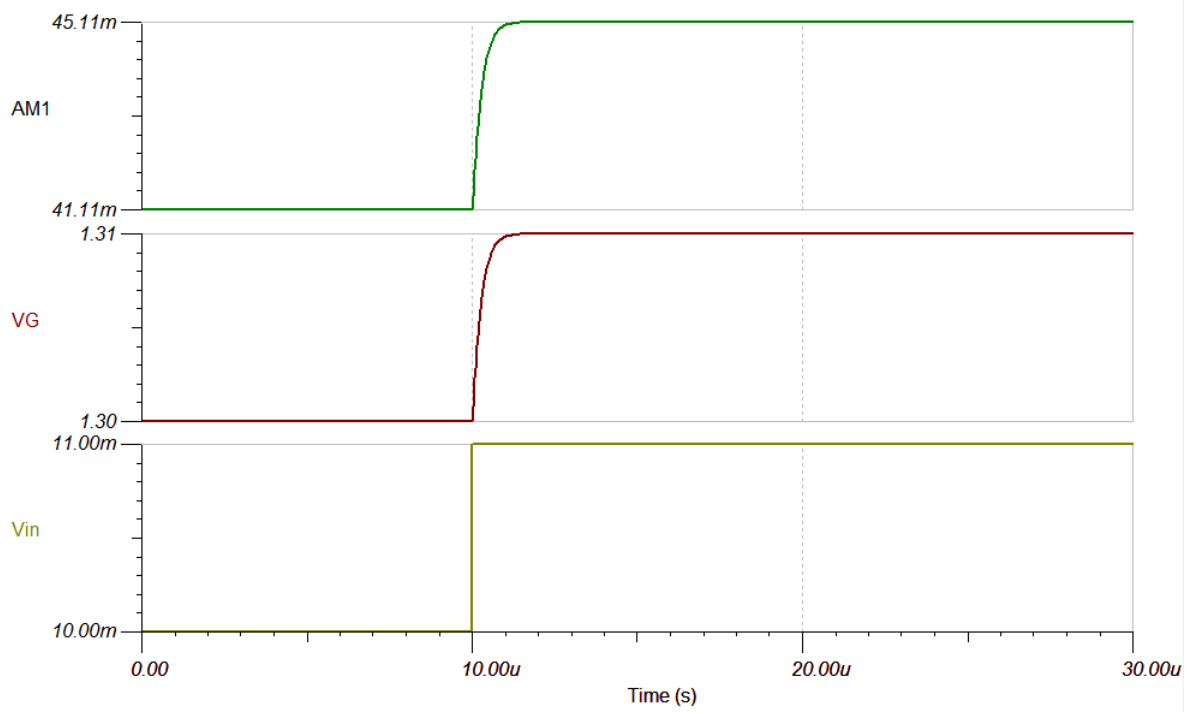


図 14. Low Amplitude Transient Step Response

2.5.3 DC Response

Two aspects of the DC response for the LED driver circuit are the response to changes in V_{in} which illustrates the DC transfer function and the response to changes in V_{supply} which illustrates the supply rejection of the circuit. The TINA-TI simulation schematic for the DC response is shown in 図 15.

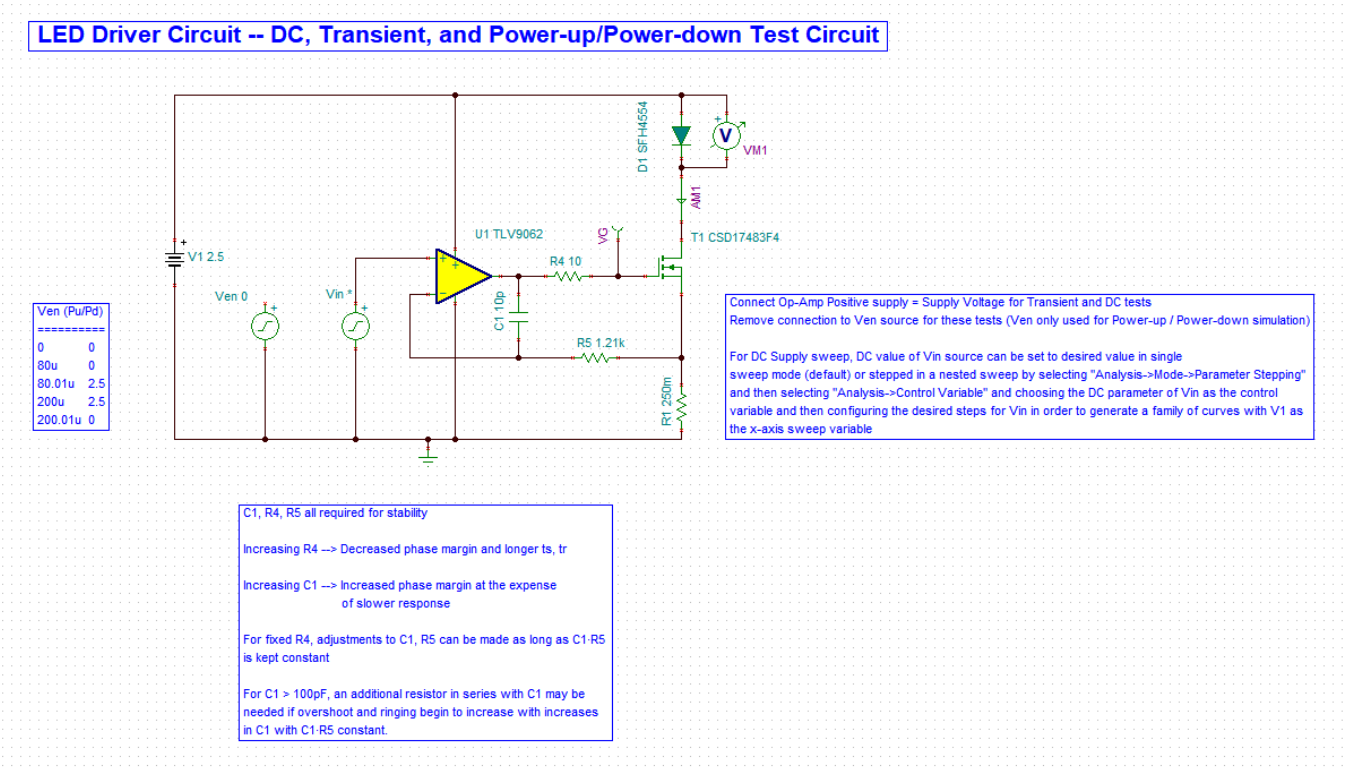


図 15. DC and Transient Response Simulation Schematic

図 16 shows the DC response as the input voltage, V_{in}, is swept through the design input range. As expected, the response is very linear throughout the operating range.

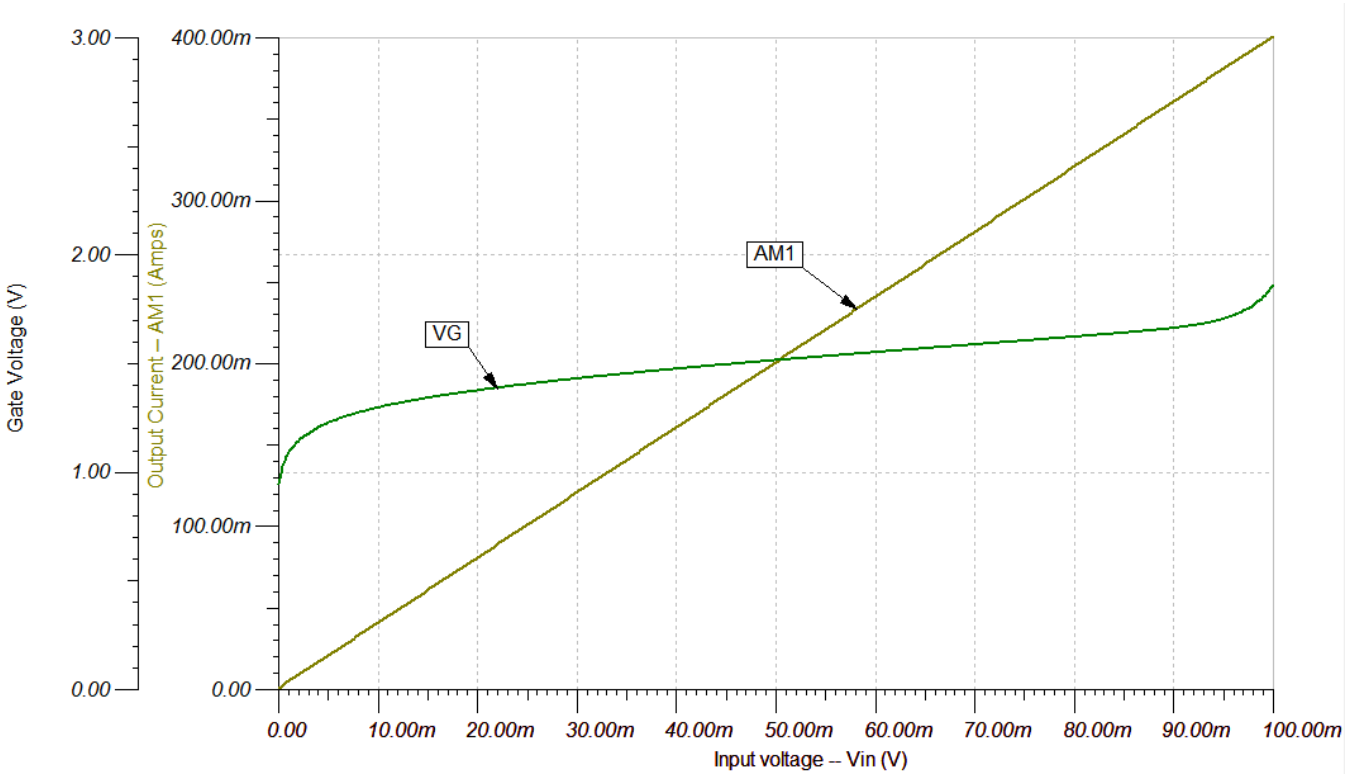


図 16. DC Response, I_{out} vs V_{in}

図 17 shows the DC response as the supply voltage is varied from 0 V to V_{supply_max} with V_{in} at the two extremes of the design input range. As described in 2.4, for supply voltage greater than or equal to 2.5 V, the output current remains constant which indicates a high output impedance looking into the current sink and consequently excellent DC supply rejection.

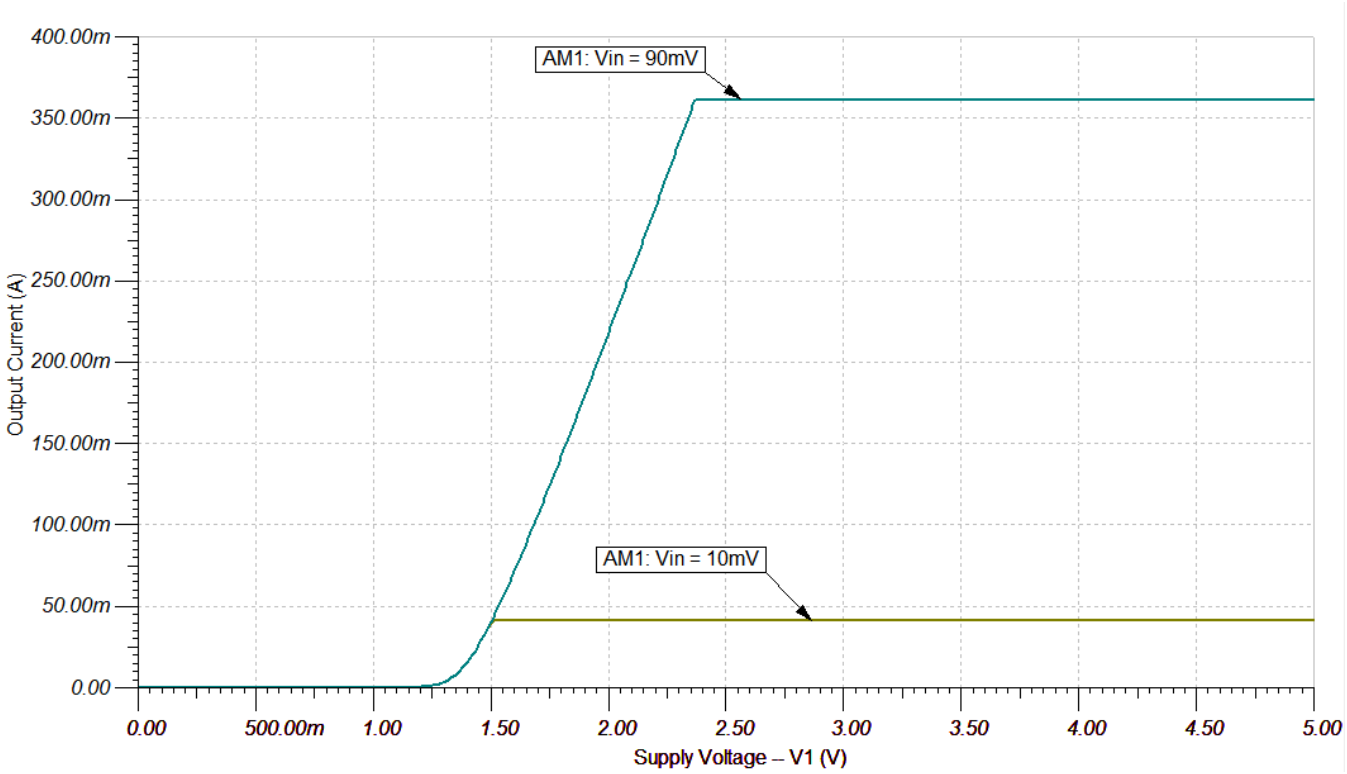


図 17. DC Response, I_{out} vs V_{supply}

2.5.4 Transient Response (Functional)

There are two other transient response simulations for this circuit that are required to verify functionality. The first transient simulation is basically a step response on the input from 0 V to V_{in_min} and V_{in_max} separately to measure the expected turnon and turnoff times of the circuit. This particular simulation is performed with the op amp powered to isolate performance variables. The second transient simulation checks the power-up and power-down functionality. This is where the op amp is powered up and down with V_{in} pulsed while the op amp is powered. This simulation is designed to most closely match the operation of the real circuit in applications such as smoke detectors, where the LED is pulsed at high current for a fixed time duration with very low duty cycle. Ideally, the result of these two simulations should match when the signal timing is correct.

2.5.4.1 Timing Verification

The schematic used for the circuit timing verification is the same as what is shown in 図 15. The results of the timing verification simulations for t_{on} using the TLV9062 amplifier are shown in 図 18 and 図 19.

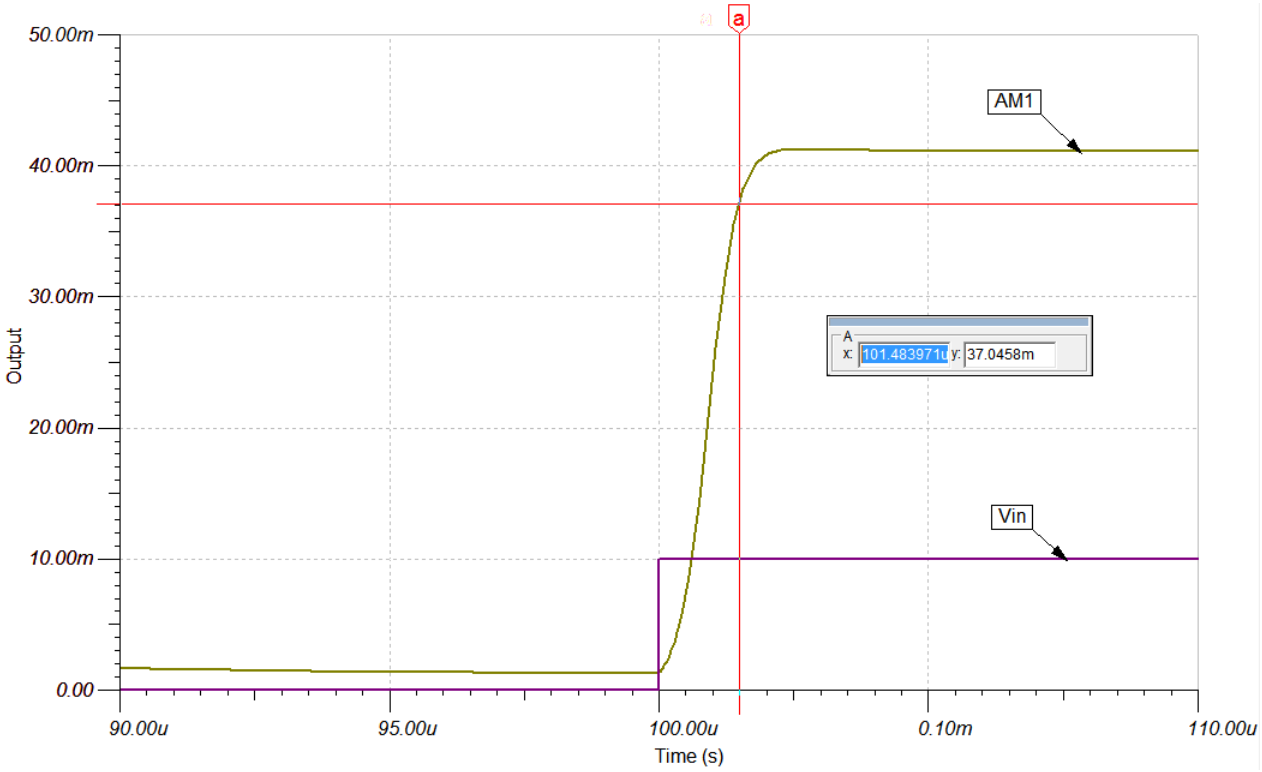


図 18. Transient Response for 90% t_{on} With Minimum Input Step Using the TLV9062 Amplifier

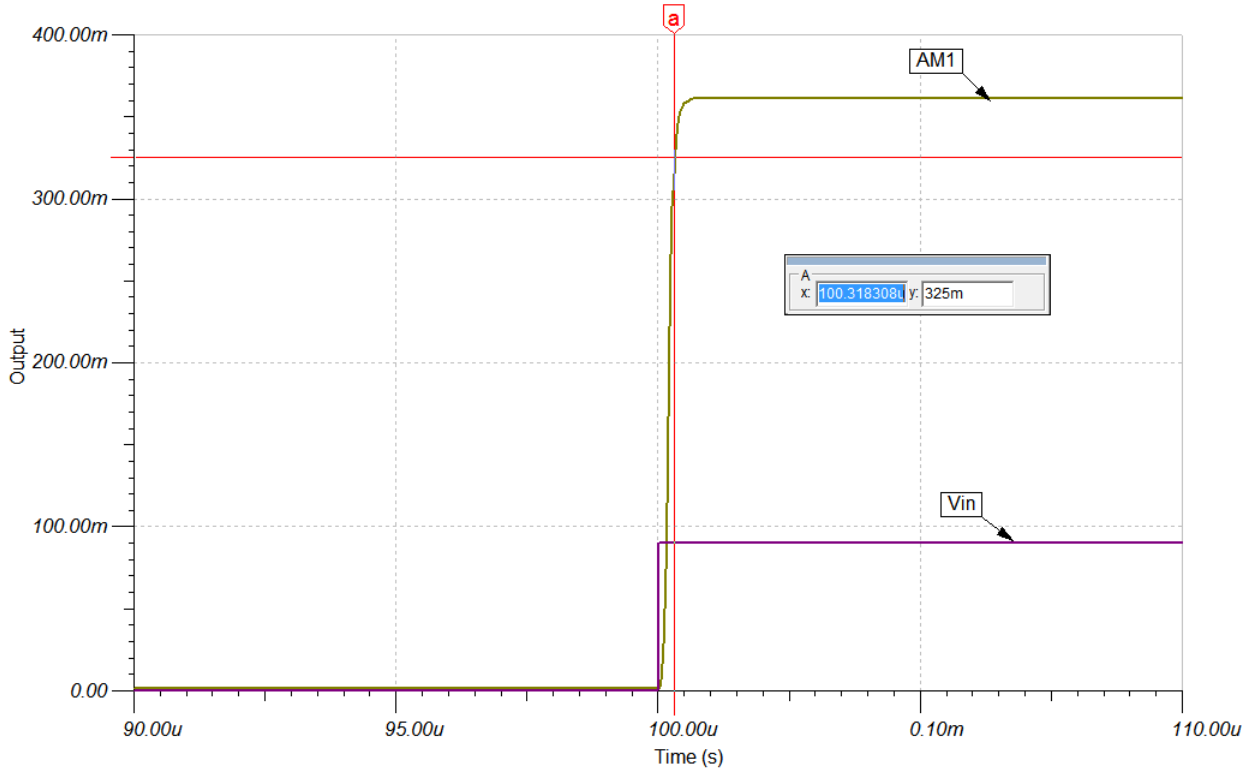


図 19. Transient Response for 90% t_{on} With Maximum Input Step Using the TLV9062 Amplifier

The results shown in 図 18 and 図 19 are consistent with previous simulations. While these turnon times are quite fast, lab results have consistently shown even better performance.

When comparing different op amps for this circuit, in particular the TLV9062 and TLV9002, the main difference shows up in the timing simulation due to the differences in unity gain bandwidth and overload recovery time. There is a slight difference in small signal AC performance while using the same compensation network design for the TLV9062 with the TLV9002. However, because the simulation used to verify timing is essentially a step response, the small difference in phase margin will be seen as increased overshoot in the output current waveform. Because most of the simulation result differences are slight between these two amplifiers, only the main differences are shown in this design guide.

図 20 shows the TINA-TI simulations schematic used for the transient timing verification using the TLV9002 amplifier. The only difference in this schematic compared to 図 15 is the op amp instance.

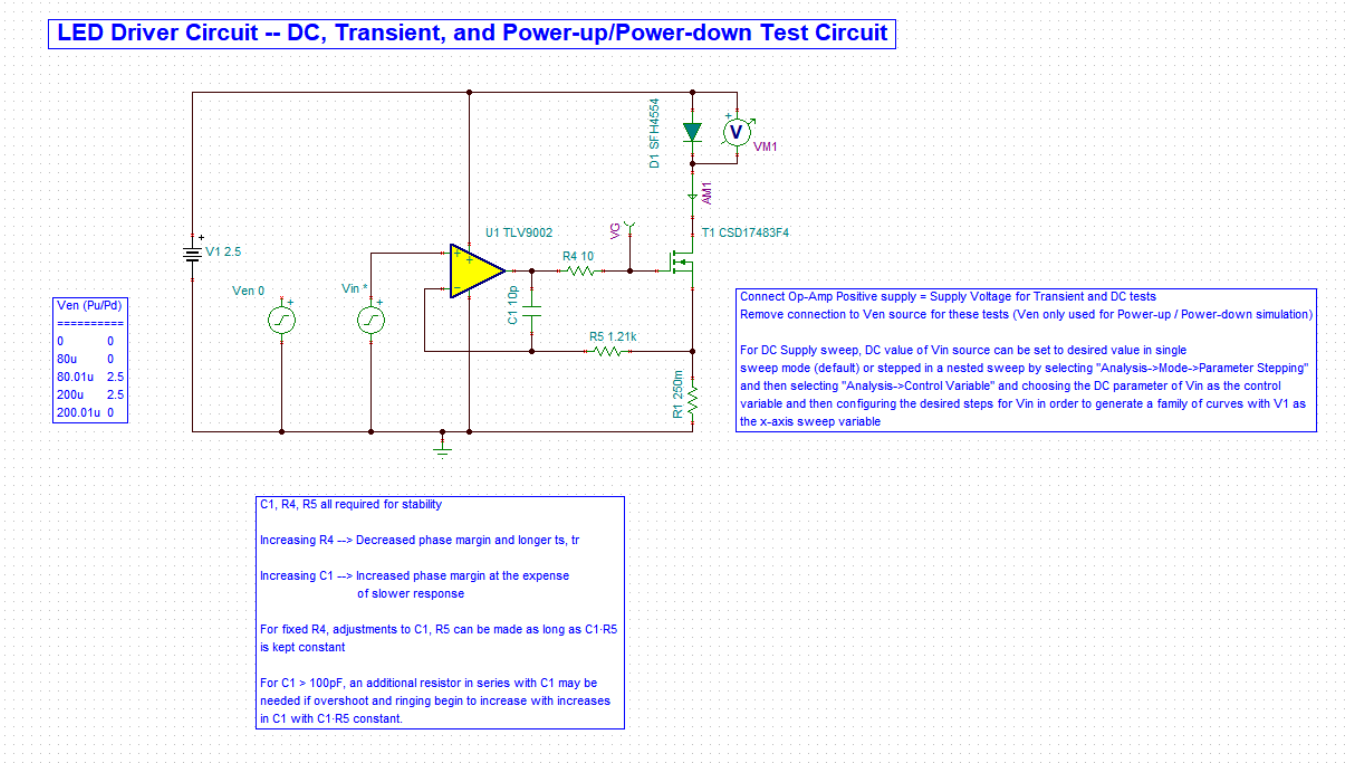


図 20. Transient Response Simulation Circuit Using TLV9002 Amplifier

The results of the timing verification simulations for t_{on} using the TLV9002 amplifier are shown in 図 21 and 図 22.

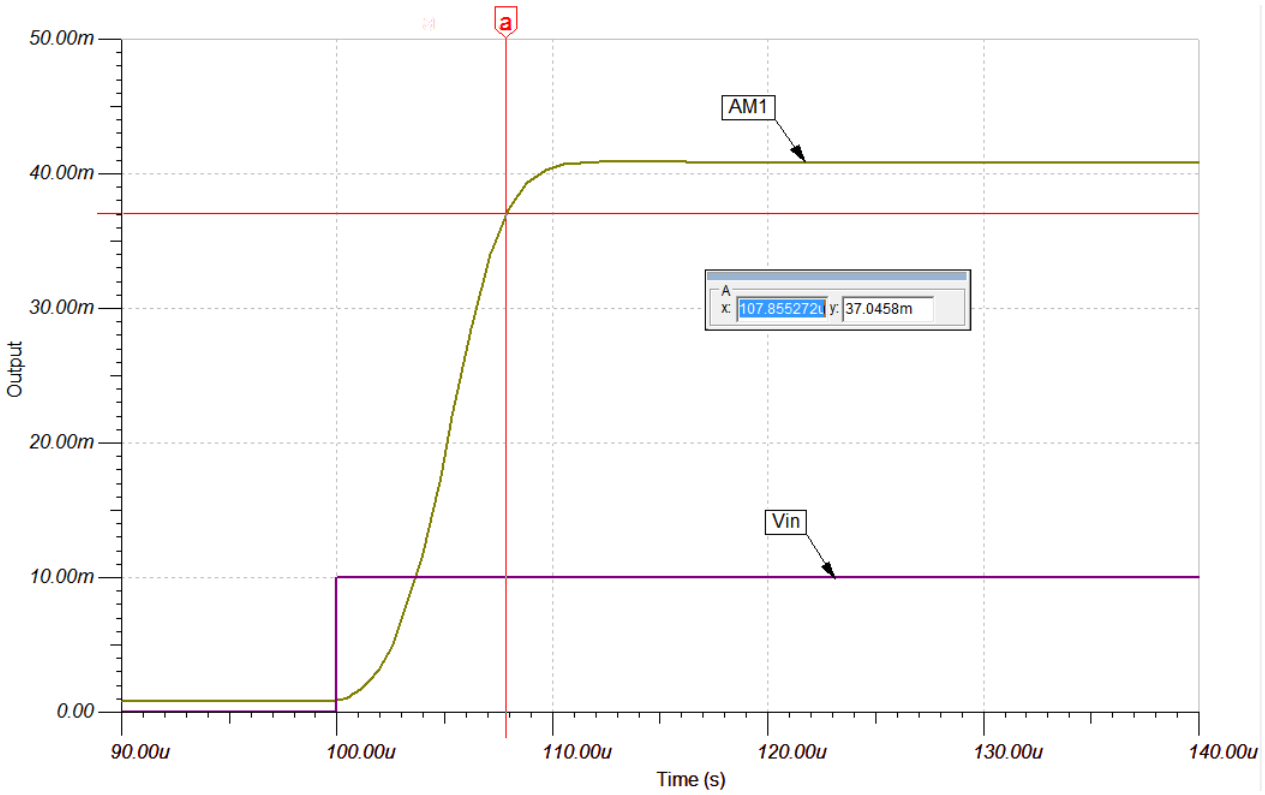


図 21. Transient Response for 90% t_{on} With Minimum Input Step Using the TLV9002 Amplifier

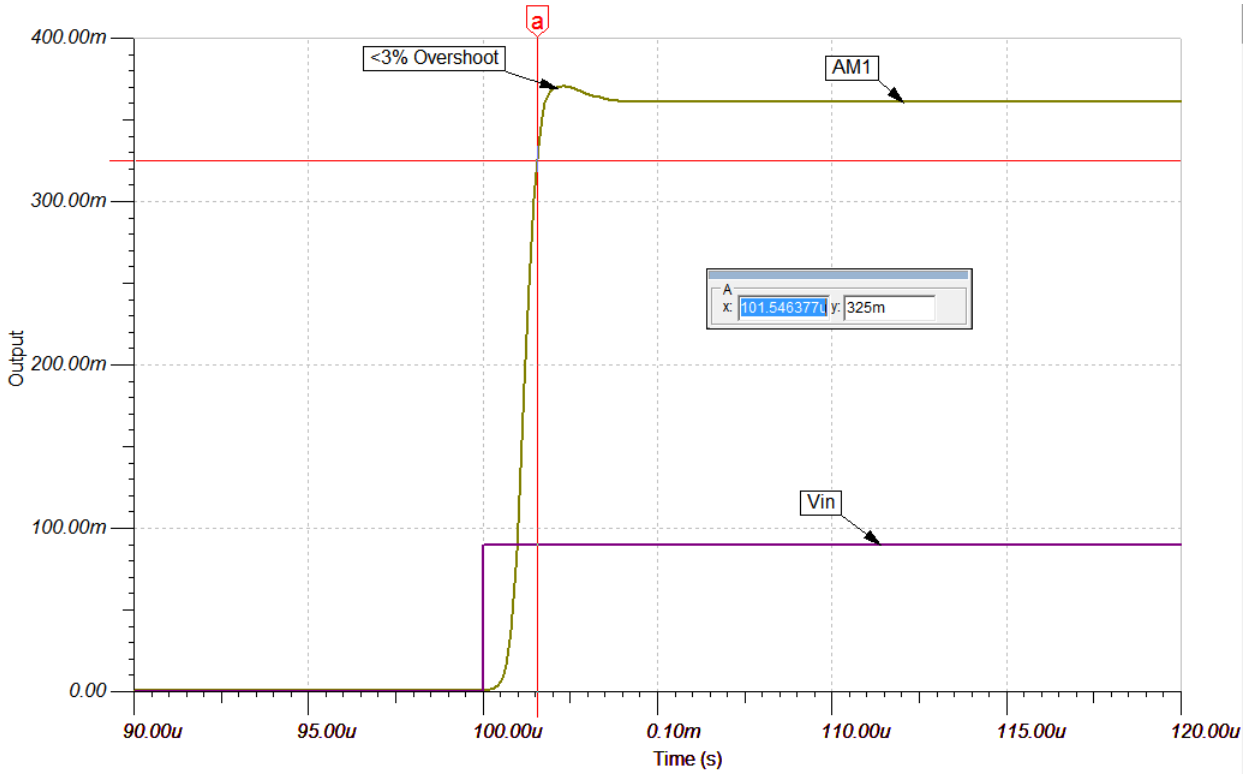


図 22. Transient Response for 90% t_{off} With Maximum Input Step Using the TLV9002 Amplifier

As expected, the turnon time results using the TLV9002 are slower compared to results using the TLV9062, but the operation with the same compensation network still produces stable operation. The effect of the op amp overload recovery time can be seen in comparing the results in 図 21 with 図 18. The 7.86 µs t_{on} for the TLV9002 versus the 1.48 µs t_{on} for the TLV9062 is a direct effect of the difference in unity gain bandwidth (1 MHz vs 10 MHz) and in overload recovery time (850 ns typical vs. 200 ns typical).

Because t_{off} performance is slower for the circuit using the TLV9002 amplifier compared to the results using the TLV9062, only the TLV9002 results are shown in 図 23 and 図 24.

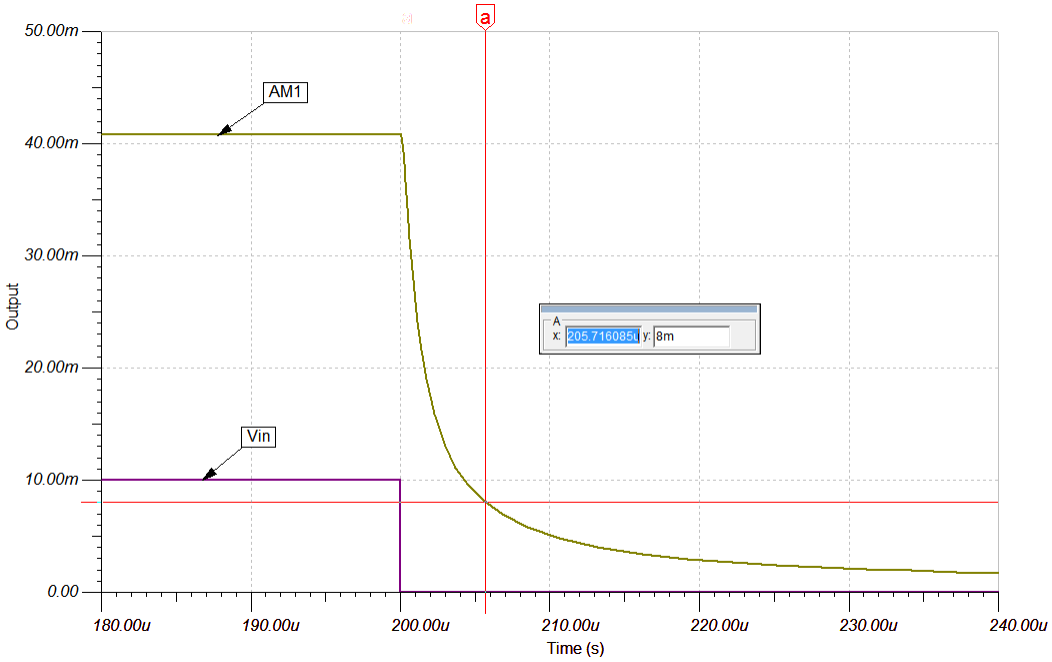


図 23. Transient Response for 20% t_{off} With Minimum Input Step Using the TLV9002 Amplifier

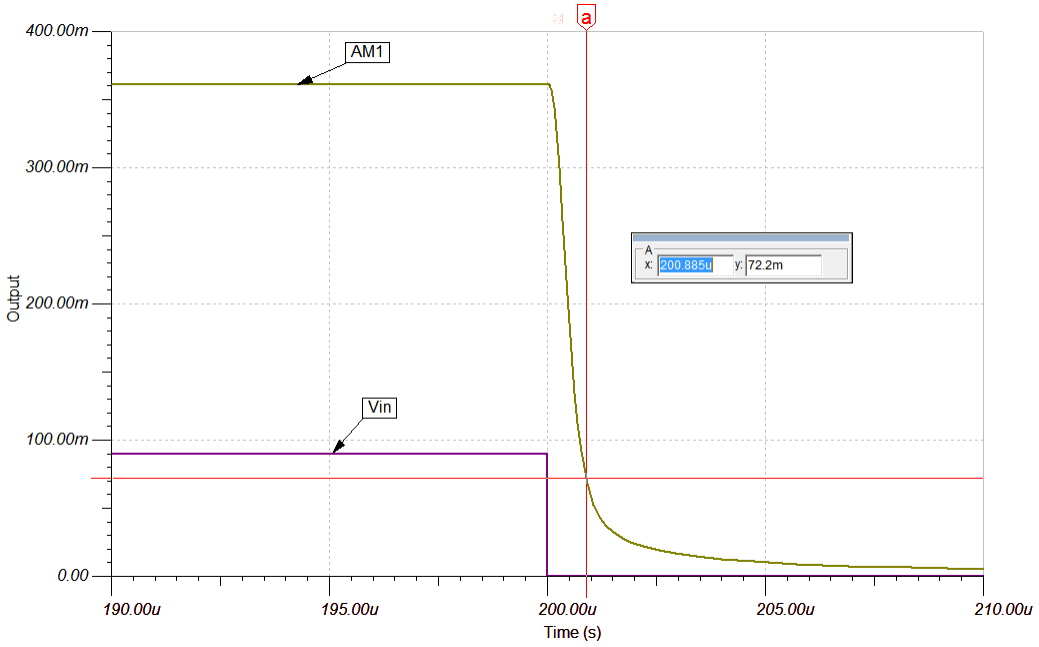


図 24. Transient Response for 20% t_{off} With Maximum Input Step Using the TLV9002 Amplifier

2.5.4.2 Power-Up and Power-Down Functionality

The TINA-TI schematic used to simulate the power-up and power-down functionality of the circuit using the TLV9062 amplifier is shown in 図 25.

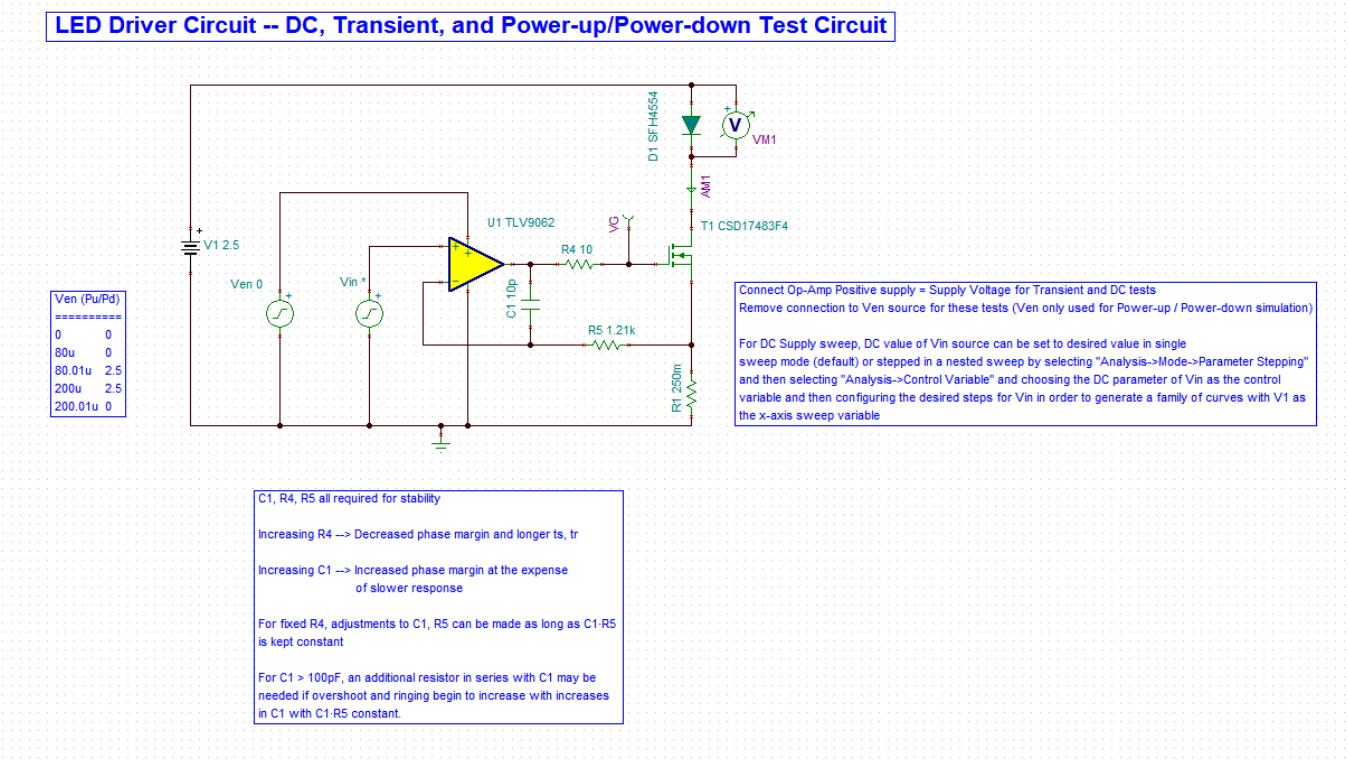


図 25. Power-Up and Power-Down Simulation Circuit

図 26 shows the results of the power-up and power-down simulation.

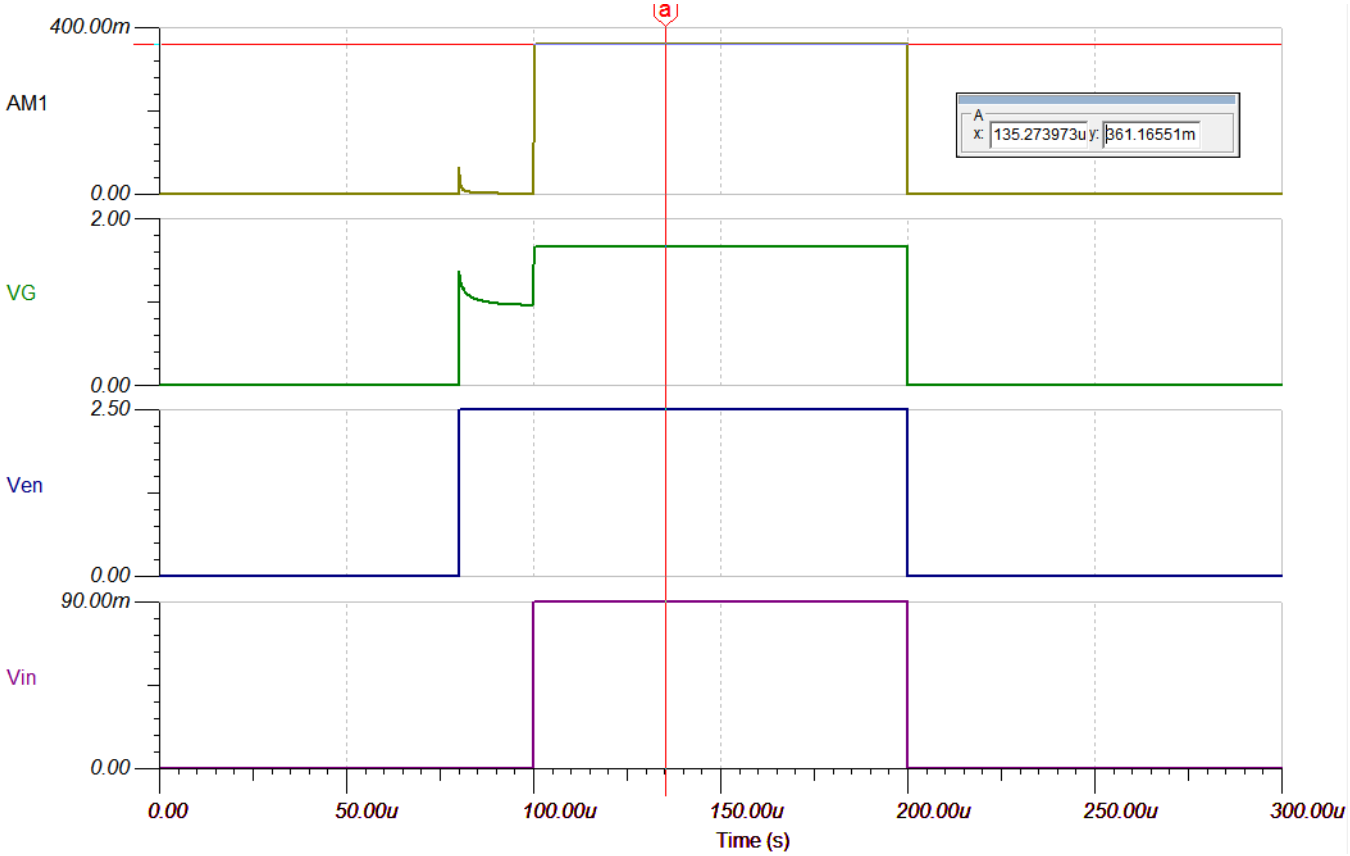


図 26. Power-Up and Power-Down Simulation Results

As shown, the op amp is powered up 20 µs prior to the input voltage step being applied to give the op amp time to turn on and settle. In some application, the op amp and input voltage can be toggled together to save some time that the op amp needs to be powered as well as any system MCU which is responsible for controlling the system timing. Another alternative which allows predictable on/off timing and which can be driven with lower output current digital control signals is to use an op amp with a separate shutdown pin such as what is available with the TLV9062S device.

Lastly, the spikes seen at the output of the op amp and the resulting spike in the output current in 図 26 is due to capacitive coupling between the supply and output pins of the op amp due to the parasitic capacitance of the op amp output device between these two pins while in the off condition. Once the op amp powers up completely, these two outputs will settle to their correct values. A lower slew rate on the Enable signal at power-up will help to reduce the peak amplitude of these spikes.

2.6 Design Files

2.6.1 Simulation Files

To download the TINA-TI simulation files, see the design files at TIDA-010014.

2.7 Related Documentation

1. Texas Instruments, *TLV906xS 10-MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems Data Sheet*
2. Texas Instruments, *TLV900x Low-Power, Rail-to-Rail In and Out, 1-MHz Operational Amplifier Data Sheet*
3. Texas Instruments, *CSD17483F4 30-V N-Channel FemtoFET™ MOSFET Data Sheet*
4. Texas Instruments, *Low-Side V-I Converter Reference Design, 0 to 5 V Input, 0 mA to 500 mA Output*
5. Texas Instruments, *High-Side V-I Converter, 0-2V to 0-100mA, 1% Full Scale Error*
6. Texas Instruments, *TI Precision Labs - Op Amps*

2.7.1 商標

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2.8 About the Author

DAVID STOUT is a systems designer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. David has over 18 years of experience designing Analog, Mixed-Signal, and RF ICs with more than 14 years focused on products for the industrial semiconductor market. David earned his bachelor of science in electrical engineering (BSEE) degree from Louisiana State University, Baton Rouge, Louisiana and a master of science in electrical engineering (MSEE) degree from the University of Texas at Dallas, Richardson, Texas.

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