参考資料

TI Designs: TIDA-01403
サーマル・イメージング・カメラ用の74dB SNR、10MSPS、14ビットのアナログ・フロントエンドのリファレンス・デザイン

概要

このリファレンス・デザインは、電子画像処理システムを念頭に構築されています。今日のイメージ・センサは、優れた画像品質を保証し、経時劣化による歪みを避けるため、ADCに対する厳しい要求があります。たとえば、優れた直線性(DNL < 0.5 LSBかつINL < 4 LSB)、高分解能(12～18ビット)、高速(最高20MSPS)、高SNR (> 74dB SNR)などです。このリファレンス・デザインでは、TI製の低ノイズ高速アンプ、完全差動アンプ(FDA)、高速ADC、低ノイズLDOを利用して、サーマル・イメージング・カメラのピクセル出力信号をデジタル化するための高性能アナログ信号チェーンを設計する方法を紹介します。

リソース

TIDA-01403	デザイン・フォルダ
TINA-TI	ツール・フォルダ
ADS4142	プロダクト・フォルダ
OPA2626	プロダクト・フォルダ
THS4551	プロダクト・フォルダ
TPS717	プロダクト・フォルダ

TI E2E™ Community

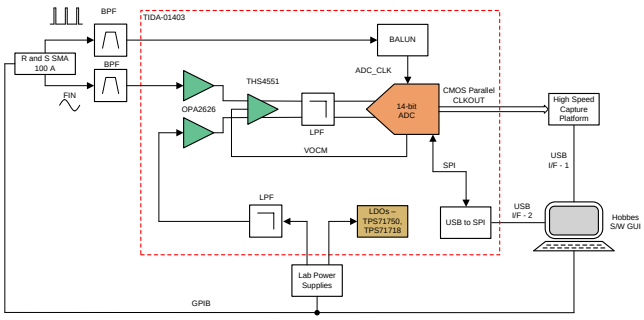
E2E エキスパートに質問

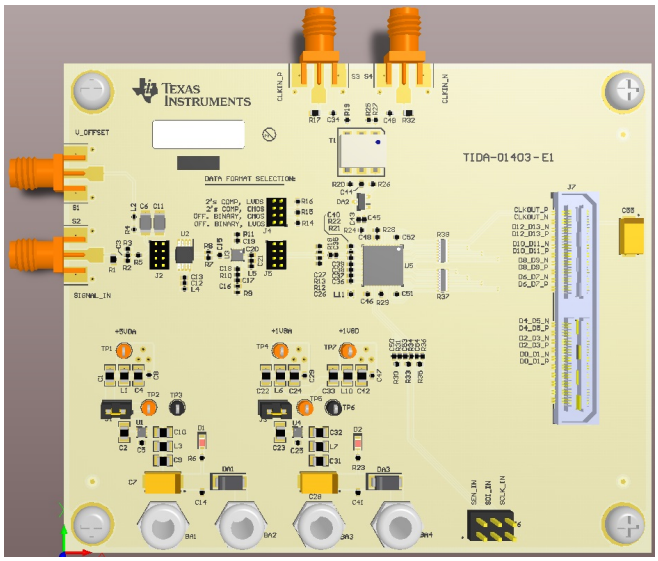
特長

- サンプリング速度: 10MSPS以下に最適化されたフロントエンド回路
- アナログ入力の種類: ユニポーラのシングルエンド信号
- ADCの分解能とフルスケール範囲(FSR): 14ビットおよび2V_{PP}差動
- 出力データ・インターフェイス: 1.8VパラレルCMOSまたはDDR LVDS
- 積分非直線性(INL) < 1 LSBかつ微分非直線性(DNL) < 0.5 LSB (標準値)
- SNR、ENOB、THD: > 74dB、12ビット、< -84dB
- 合計消費電力: 80mW未満

アプリケーション

- セキュリティと監視: サーマル・イメージング・カメラ
- 医療用画像処理
- 試験/測定機器
- 車載用ナイト・ビジョン
- 航空宇宙/防衛





1 System Description

Virtually every imaging system includes an image sensor, AFE circuit, and digital signal processor (DSP). Every electronic imaging system starts with an image sensor. The AFE conditions the pixel-output signal from the image sensor in the analog domain and converts it to digital by employing an ADC. The digitized-pixel data is easily interfaced to a broad range of DSPs, including the DaVinci™ and Sitara™ processors from TI, with an integrated image pipe for enhanced video and image processing. As the interface between the analog core and DSP, ADCs are the second most performance-critical component in the complete-image signal-processing chain, after the image sensor. Image sensors of today force heavy demands on ADCs, in terms of excellent linearity (DNL < 0.5 LSBs and INL < 4 LSBs), high resolution (12 to 18 bits), high speed (up to 20 MSPS), and high SNR (> 74-dB SNR) to assure superior image quality and freedom from distortion over time.

The rich product portfolio of TI covers a broad spectrum of image-capture applications with diverse requirements. Portfolio offerings, reference-design support, product quality, and manufacturing excellence lets system designers customize imaging systems for specific applications with confidence. The imaging products from TI are optimized to work together, yet also let designers mix-and-match with third-party components when required. As modern imaging systems become more portable and compact, TI is committed to solving challenges that manufacturers face when designing these increasingly complex systems.

Enabled by the low-noise, high-speed amplifier, fully differential amplifier (FDA), high-speed ADC, and low-noise LDO from TI, this reference design demonstrates how to design a high-performance, analog-signal chain for thermal imaging cameras. This design guide was written to describe key system-performance requirements that are translated into the specifications of the signal-chain components, to achieve optimal performance by making correct choices. The scope of this TI reference-design subsystem is to give system designers a head start in designing the complete-image signal-processing chain responsible for digitizing the pixel-output signal from the sensor, using low-noise amplifiers and a high-speed sampling ADC with excellent linearity (DNL and INL), high SNR, and low distortion, giving superior imaging performance. This reference design provides a complete set of downloadable documents such as the comprehensive design guide, schematic, Altium PCB layout files, bill of materials (BOM), test results, and Gerber files, which aid system designers in the design and development of their end-equipment systems.

System performance requirements must be translated into the specifications of the key signal-path components, to achieve the best tradeoffs between performance, power consumption, size, and ease of use (see 表 1). The following subsections describe the various blocks within the TI reference-design system and what characteristics are most critical to best implementing the corresponding function.

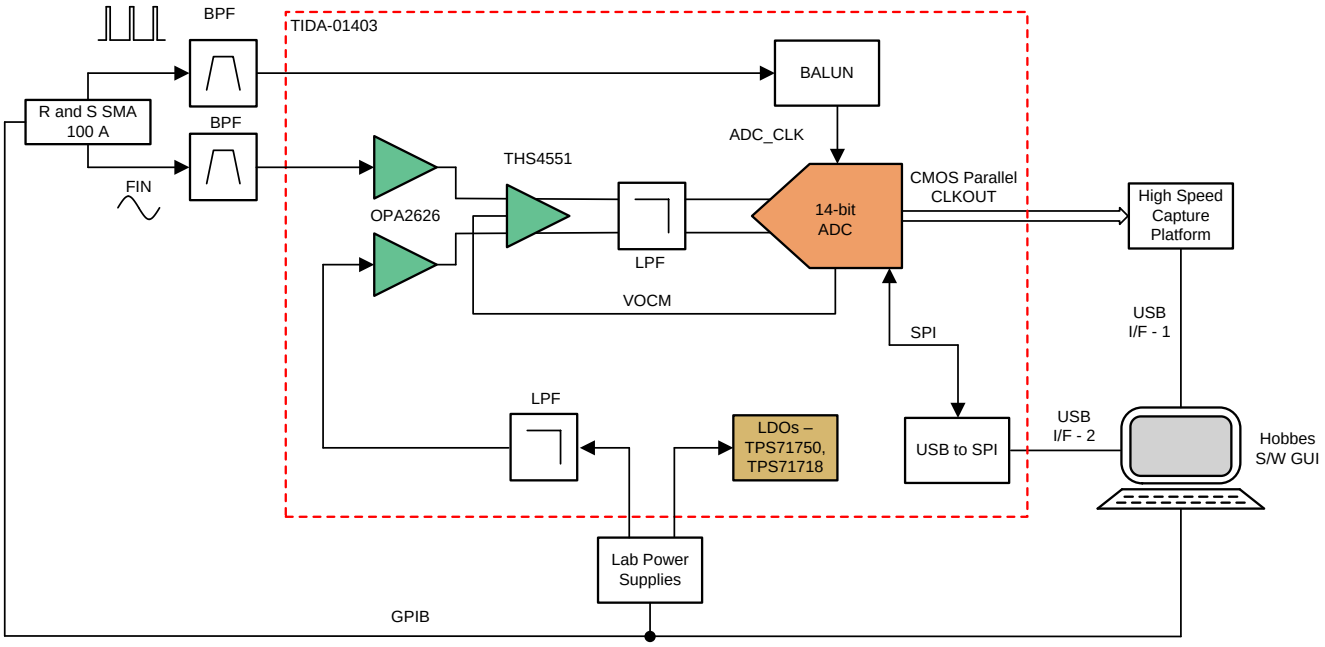
1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATION
Number of analog inputs	One
Input range and type	Unipolar, single-ended
ADC full-scale input range	2 V_{PP} differential
ADC architecture	Pipeline
Resolution	14 bit
SNR	> 74 dB using the DC-input histogram method
ENOB	> 12 bit
THD	< -84 dB
INL	< 1 LSB
DNL	< 0.5 LSB
Sampling frequency	ADC can sample frequencies up to 65 MSPS, however, the AFE has been optimized for 10 MSPS or less
Operating voltage	External supplies: 5.5-V DC and 3.3-V DC
Power consumption	Approximately 80 mW
Connector	One SMA connector for the analog input signal
	One SMA connector for the common-mode input voltage
	Two SMA connectors for the single-ended or differential clock
	One 40 × 2, Samtec connector for the data capture card

2 System Overview

2.1 Block Diagram



2.2 Highlighted Products

At a high level, this reference-design subsystem consists of high-speed, low-noise, front-end amplifiers, a high-speed, 14-bit pipeline ADC, and power management devices. The high-speed ADC digitizes the conditioned analog-image signal to the digital domain, allowing for additional processing by a FPGA or DSP. The ADS4142 is a 14-bit, fully-differential, pipeline ADC (low-speed variant of the ADS41xx family), offering the advantages of good common-mode rejection and low-distortion products. In any imaging system, the AFE electronics must not be the limiting factor in performance, so for high-end imaging applications, a 14-bit ADC is necessary. One of the most common ways to drive a differential-input ADC is with a transformer. However, there are applications such as imaging systems, where the ADC cannot be driven with transformers, because the frequency response to the DC is also expected. Although an ADC can be driven single-ended, a fully-differential driver usually optimizes overall performance. The signal from the image sensor must be conditioned before being sent to the ADC. The front-end, ADC driver circuitry is basically a single-ended-to-differential conversion stage. In the front end there is the OPA2626, a high-speed, high-precision, low-noise amplifier presenting high-input impedance to the output of the sensor, followed by the THS4551, a high-speed, precision, low-noise FDA, providing low impedance and fast-signal settling when differentially driving ADC inputs. The TIDA-01403 design features the following devices.

2.2.1 ADS4142

The ADS412x and ADS414x devices are lower-sampling, speed variants in the ADS41xx family of ADCs (see 図 1). These devices use innovative design techniques to achieve high-dynamic performance, while consuming extremely low power at 1.8-V supply. The devices are well suited for multicarrier, wide-bandwidth, communication applications.

The ADS412x and ADS414x devices have fine-gain options that can be used to improve SFDR performance at lower full-scale input ranges, especially at high-input frequencies. They include a DC-offset correction loop that can be used to cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

The ADS412x and ADS414x devices are available in a compact, VQFN-48 package and are specified over the industrial temperature range (–40°C to +85°C). The ADS412x and ADS414x devices have the following features:

- Ultra-low power with 1.8-V single supply:
  - 103-mW total power at 65 MSPS
  - 153-mW total power at 125 MSPS
- High-dynamic performance:
  - SNR: 72.2 dBFS at 170 MHz
  - SFDR: 81 dBc at 170 MHz
- Dynamic power scaling with sample rate
- Idle channel SNR: 74.8 dBFS (ADS414x)
- Output interface:
  - Double data rate (DDR), LVDS with programmable swing and strength:
    - Standard swing: 350 mV
    - Low swing: 200 mV
    - Default strength: 100-Ω termination
    - 2× strength: 50-Ω termination
  - 1.8-V parallel CMOS interface also supported
- Programmable gain up to 6 dB for SNR, SFDR trade-off
- DC offset correction
- Supports low-input clock amplitude, down to 200 mV_{PP}

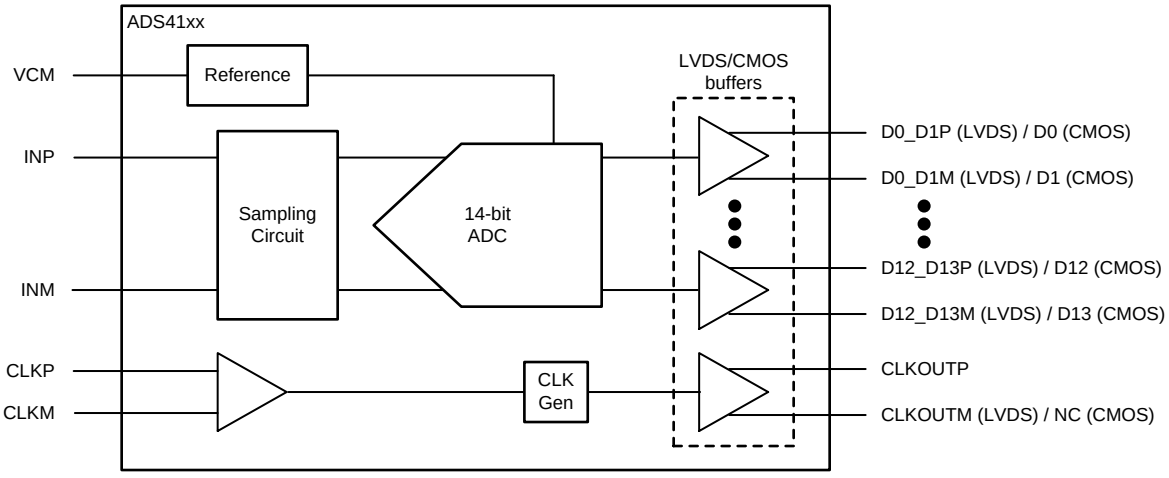


図 1. ADS41xx Block Diagram

2.2.2 OPA2626

The OPAx626 family of operational amplifiers (op amps) are 16-bit and 18-bit, high-precision, successive-approximation register (SAR), ADC drivers, with low total harmonic distortion (THD) and noise (see 図 2). This family of precision op amps is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). With a high-DC precision of only 100-µV offset voltage, a wide gain-bandwidth product of 120 MHz, and a low-wideband noise of 2.5 nV/√Hz, this family of devices is optimized for driving high-throughput, high resolution, SAR ADCs, in applications such as the ADS88xx family of SAR ADCs.

The OPAx626 family is available in 5-pin SOT and 8-pin VSSOP packages and is specified for operation from –40°C to +125°C. The OPAx626 family has the following features:

- Excellent dynamic performance:
  - Low distortion: –122 dBc for HD2 and –140 dBc for HD3 at 100 kHz
  - Gain bandwidth (G = 100): 120 MHz
  - Slew rate: 115 V/µs
  - 16-bit settling at 4-V step: 280 ns
  - Low-voltage noise: 2.5 nV/√Hz at 10 kHz
  - Low-output impedance: 1 Ω at 1 MHz
- Excellent DC precision:
  - Offset voltage: ±100 µV (maximum)
  - Offset voltage drift: ±3 µV/ºC (maximum)
  - Low-quiescent current: 2 mA (typical)
- Input common-mode range includes negative rail
- Rail-to-rail output
- Wide temperature range: fully specified from –40°C to +125°C

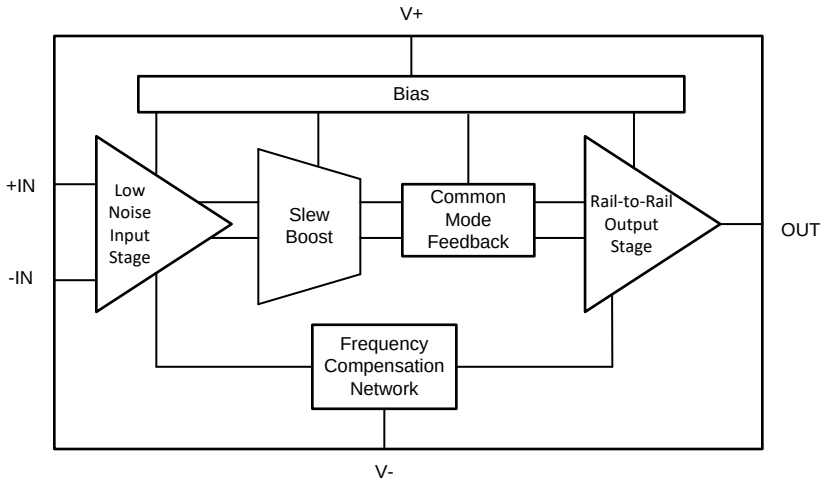


図 2. OPAx262 Functional Block Diagram

2.2.3 THS4551

The THS4551 fully-differential amplifier (see 図 3) offers an easy interface, from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive-load driving, this device is well suited for data-acquisition systems where high precision is required, along with the best SNR and spurious-free dynamic range (SFDR), through the amplifier and ADC combination.

The THS4551 device features the negative-rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply, differential-input ADC. Low DC error and drift terms support the emerging 16- to 20-bit SAR input requirements. A wide-range, output common-mode control supports the ADC running from 1.8-V to 5-V supplies, with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

The THS4551 device is characterized for operation over the wide temperature range of –40°C to +125°C, and is available in 8-pin VSSOP, 16-pin VQFN, and 10-pin WQFN packages. The THS4551 device has the following features:

- Bandwidth: 150 MHz (G = 1 V/V)
- Differential output slew rate: 220 V/µs
- Gain bandwidth product: 135 MHz
- Negative rail input (NRI), rail-to-rail output (RRO)
- Wide-output common-mode control range
- Single-supply operating range: 2.7 V to 5.4 V
- Trimmed-supply current: 1.37 mA at 5 V
- 25°C input offset: ±175 µV (maximum)
- Input offset voltage Drift: ±1.8 µV/°C (maximum)
- Differential input voltage noise: 3.3 nV/√Hz
- HD2: –128 dBc at 2 V_{PP}, 100 kHz
- HD3: –139 dBc at 2 V_{PP}, 100 kHz
- < 50-ns settling time: 4-V step to 0.01%
- 18-bit settling time: 4-V step, < 500 ns

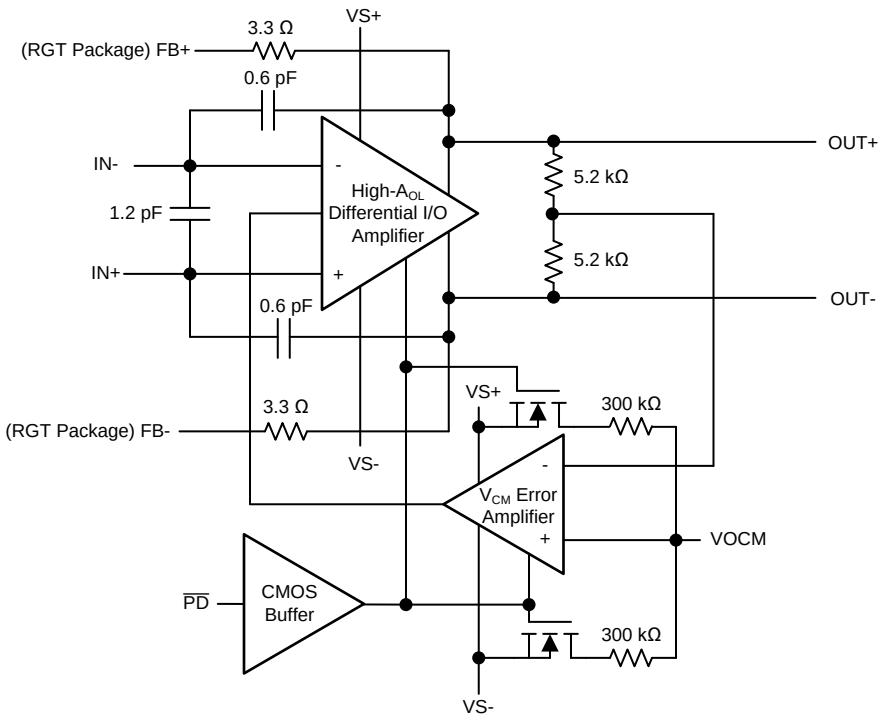


図 3. THS4551 Functional Block Diagram

2.2.4 TPS717xx

The TPS717 family of low-dropout (LDO), low-power, linear regulators offers high power-supply rejection (PSRR), while maintaining low, 45-μA ground current in an ultra-small, five-pin, SOT package (see 図 4). The family uses an advanced BiCMOS process and a PMOS pass device to achieve fast start-up, low noise, excellent transient response, and excellent PSRR performance. The TPS717 device is stable with a 1-μF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. The device family is fully specified from T_J = –40°C to 125°C and is offered in a small SOT (SC70-5) package, a 2-mm × 2-mm WSON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm WSON-6 package, which are ideal for small form factor portable equipment (such as wireless handsets and PDAs). The TPS717xx device has the following features:

- Input voltage: 2.5 V to 6.5 V
- Available in multiple output versions:
  - Fixed output with voltages from 0.9 V to 5 V
  - Adjustable output voltage from 0.9 V to 6.2 V
- Ultra-high PSRR:
  - 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent load and line transient response
- Low dropout: 170 mV at 150 mA (typical)
- Low noise: 30 μV_{RMS} (typical), 100 Hz to 100 kHz
- Small 5-pin SC-70, 2-mm × 2-mm WSON-6, and 1.5-mm × 1.5-mm WSON-6 packages

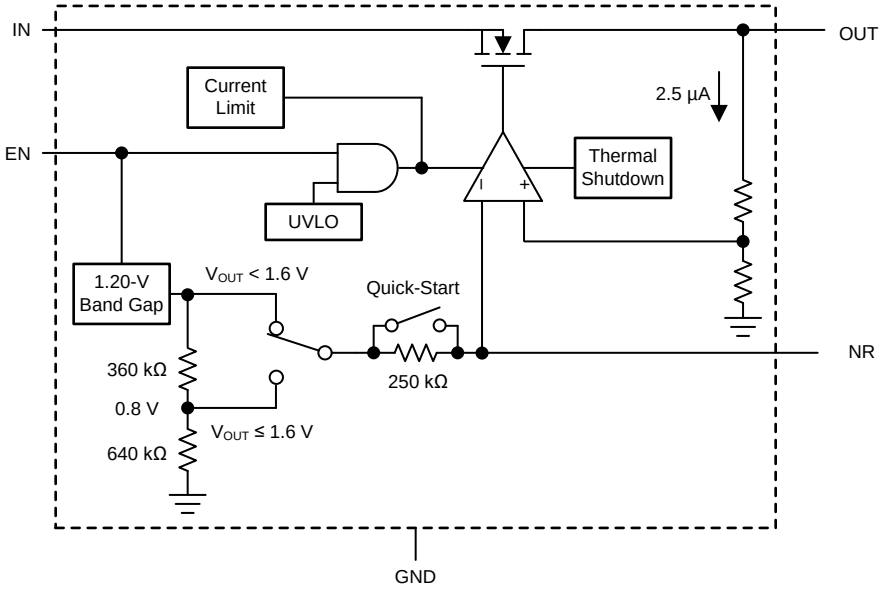


図 4. TPS717xx Functional Block Diagram

3 System Design Theory

Usually, image-sensor manufacturers may not be experts in designing ADCs. Consequently, sometimes ADC manufacturers are not aware of the critical requirements that ADCs must satisfy for pixel output digitization. Improving the speed and resolution of ADCs sometimes requires performance tradeoffs, and these tradeoffs must be made in favor of the imaging applications. Typically, any ADC is used in one of three modes of operation: DC conversion, multiplexing (time domain), and signal reconstruction (frequency domain). Before proceeding further, it is important to understand how an electronic-imaging system differs from signal-reconstruction applications. Focal plane arrays (FPA) used in IR-imaging applications typically output single-ended, ground-referenced, signal-containing pixel information that is read pixel-by-pixel by the read out integrated circuit (ROIC). Therefore, analog-video output of an image sensor is not a continuous, periodic waveform. The output is actually a pseudo-DC waveform that resembles a series of steps with different amplitudes. The characteristics of such a video waveform dictate time rather than frequency. The ADC samples the analog-video signal only during the relatively slow-moving portion of the waveform, preferably in the end when the pixel is most settled. Therefore, electronic imaging differs from signal reconstruction applications, because it is strictly a multiplexed-input time-domain data-acquisition application. That characteristic means a designer should not focus more on optimizing the THD, which is a frequency-domain specification. A high-THD specification is irrelevant for most of the imaging applications. In time-domain applications, spectral purity is not that important. The AFE circuit is the crucial link for establishing and maintaining good system performance. The design of an AFE circuit, for an imaging application, depends on many factors, like the type of sensor being used, dynamic range, image resolution, speed, noise performance, power consumption, and form-factor requirements. 図 5 shows the basic architecture of the electronics of a camera.

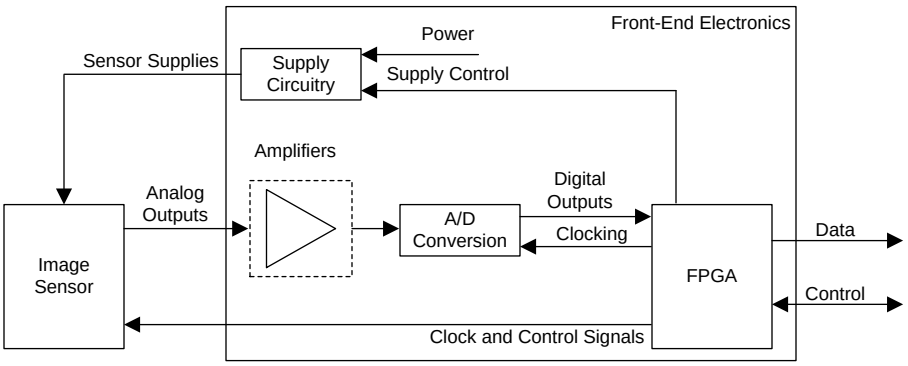


図 5. Basic Architecture of Camera Electronics

The linearity of the AFE can impact the imaging system performance. The nonlinearities of a real ADC can cause artifacts in the digitized image, which are easily noticeable to human eyes. The human-vision system has excellent edge, or discontinuity-detection capability, and therefore can pick-up different geometric shapes quite comfortably. In imaging applications, the AFE must be designed while keeping in mind the capabilities of the human-vision system. Improper selection of the ADC and the driver amplifiers in imaging applications may create edges or discontinuities that do not exist or eliminate edges that do exist, and our eyes can spot such artifacts instantly. Therefore, an imaging system must do the following:

- Not introduce discontinuities where they do not exist in the scene – more related to selection of the ADC
- Preserve discontinuities wherever they exist in the scene – more related to selection of driver amplifier circuitry

3.1 Selecting an ADC

An imaging system must not introduce discontinuities where they do not exist in the scene – This requirement is more related to the nonlinearity of the ADC. ADCs, by nature, add discontinuities (DNL and INL). It is difficult to predict how ADC nonlinearity impacts final imagery, due to the strong dependence on scene details. Therefore, to surface any impact due to ADC imperfections, electronic-imaging systems are tested or calibrated with a continuous-tone wedge, which is a gradual linear excursion of gray tones from white to black or black to white (see 図 6). The DNL of the ADC is the most critical specification for imaging, because a DNL error results in edge distortion. In an ideal converter, the step width or analog increment of each conversion value is the same, and the DNL is zero. Such an ideal converter would translate increasing light intensity into digital values that an ideal D/A converter could reconvert to resemble perfectly stepped wedges of increasing intensity. If the DNL is not zero, then each step has a different width. This imperfection affects intensity fidelity and causes improper gradation of the image scale with local imperfections. A large, positive DNL error would look like a flat spot, where color stays the same for many stepped wedges. A large, negative DNL error would look like a sudden color jump. A DNL error greater than 0.5 LSB usually creates objectionable artifacts.

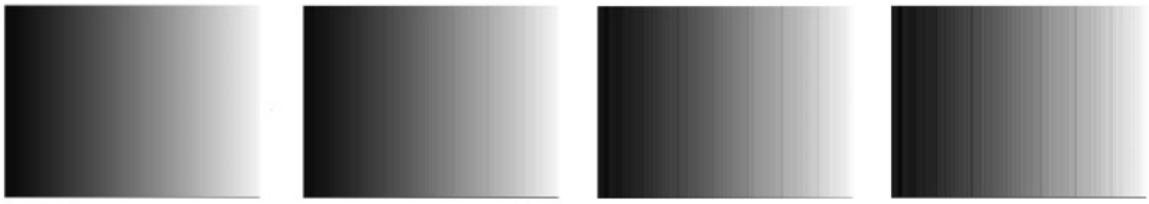


図 6. Smooth Gradient Scene With Increasing DNL Error

In addition, small DNL values can add to a significant error in INL. Erroneous INL corrupts the entire image scale with a gradual nonlinearity. The human eyes are generally less sensitive to this type of error than to DNL-induced edge problems. However, more INL errors results in color artifacts that may cause deceptive results. The detector was placed in front of a black body with uniform temperature, and images were captured with different ADCs with INL specifications from 1 LSB to 5 LSB. An INL error greater than 3 LSB creates noticeable color artifacts.

Not all ADCs are created equal. There are different architectures to accomplish the task. Different architectures bring different strengths and weaknesses and lend themselves to the optimization of different applications. With ADCs, as with any circuit, designers face many tradeoffs. The ADC is a performance-critical component in the image-signal processing chain. To establish accurate and detailed images of scanned objects, these applications employ larger arrays with more pixels and longer frame-update times. The ADC must provide high resolution with excellent linearity, low noise, low drift, and low offset. All this performance is necessary to assure image quality, color purity, and freedom from distortion over time. The pipelined ADC is the architecture of choice for imaging applications, because pipeline ADCs provide an optimum balance of noise, linearity, speed, resolution, power dissipation, and size.

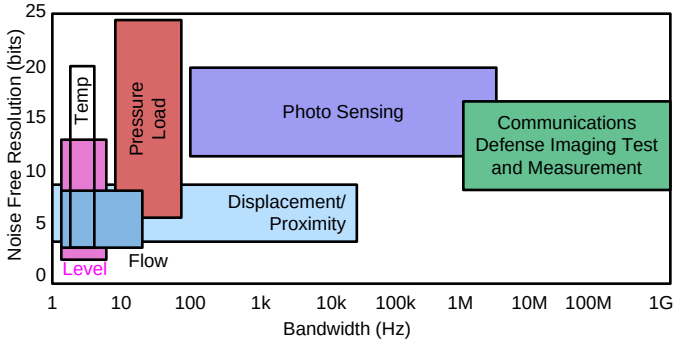


図 7. Noise-Free Resolution Versus Bandwidth

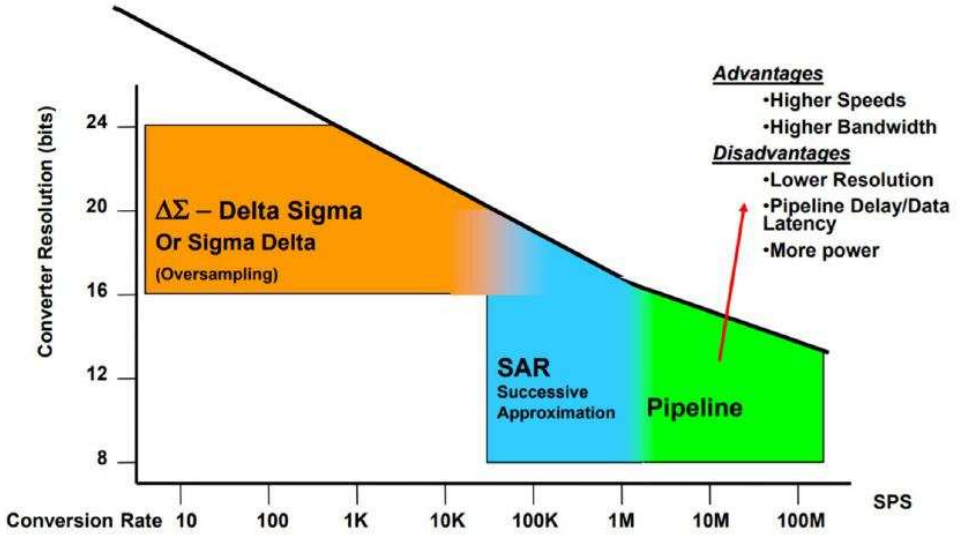


図 8. Converter Resolution Versus Conversion Rate

With the system specifications provided, designers can begin working on the center of the input-signal path — the ADC. Key specifications and properties identified for a high-speed ADC follow:

- **ADC channels:** Number of channels must be equal to the number of video outputs in the image sensor. Generally, image sensors up to QVGA resolution come with only one video output.
- **Need for speed:** Sampling rate must be greater than the sensor resolution (M × N) times the frame rate (frames per second). For a QVGA-resolution (320 × 240 pixels) sensor with a 100-Hz frame rate, the sampling rate is greater than 320 × 240 × 100 = 7.68 MSPS.
- **SNR:** Noise generated within the AFE circuitry directly affects the dynamic range of the imaging system. Therefore, the SNR of the ADC must be 6 to 10 dB greater than the SNR of the image sensor. If the SNR of an image sensor is unknown, the SNR of the ADC must be 10 dB higher than the dynamic range (DR) of the image sensor. For an image sensor with a DR of 1.25 mV_{PP} to 2 V_{PP} or 64 dB, the minimum SNR of the ADC must be 74 dB (64 dB + 10 dB).
- **Resolution of ADC:** Most of the image-processing algorithms output 8 to 10 bits for the display. Therefore, the resolution of the ADC must be 2 to 4 bits greater than the number of bits in the final image after digital image processing. Advanced, digital, image-processing algorithms require more bits from the ADC, allowing extra headroom in image manipulation and editing, ensuring minimal loss of image integrity. The more bits in a camera, the smoother the digitization process. More bits also mean higher accuracy and more information. With enough bits, the human eye can no longer determine the difference between a continuous grayscale and its digital representation. Continuing deeper, the effective resolution (ENOB) of the ADC should be such that it digitizes the entire DR (see 式 1).

$$\mathrm{DR} = 10^{\frac{\mathrm{DR(dB)}}{20}} = 10^{\frac{64\ \mathrm{dB}}{20}} = 1585$$
$$\mathrm{ENOB} = \log_2(\mathrm{DR}) = \log_2(1585) = 10.6\ \mathrm{bit} \quad (1)$$

In this case, the resolution of the ADC must be higher than the ENOB (10.6 bits), considering the noise introduced by the analog signal-processing circuitry and digitization process. Designers may also want to keep the maximum signal from the sensor smaller than the ADC full scale range (FSR), to avoid clipping anywhere is the signal path. This step helps in eliminating the risk of overdrive. A 12-bit ADC

cannot meet the SNR requirement. With all of this considered, a 14-bit ADC with 74-dB SNR or greater is a good choice for high-end imaging applications.

- **DNL:** DNL of the ADC must be less than 0.5 LSBs
- **INL:** INL of the ADC must be less than 3 LSBs
- **Low-power consumption:** In general, AFE circuitry is placed close to the image sensor, inside a closed camera housing. Heat generated by the AFE may interfere with IR energy coming in through the lens from the scene. Therefore, power consumption of the design must be minimized.
- **Small package:** Security cameras are compact. Space is always a challenge. Sometimes, it is possible that an ADC with the best specifications cannot be used, simply because it has a bigger package.

Go to www.ti.com to see ADC options.

TI Home → Data Converters → Analog-to-Digital Converters (ADCs) → High Speed ADCs (> 10 MSPS)

Compare	Part Number	Resolution (Bits)	Sample Rate (Max) (MSPS)	# Input Channels	SNR (dB)	ENOB (Bits)	SFDR (dB)	Power Consumption (Typ) (mW)	Input Range (Vp-p)	Interface	Operating Temperature Range (C)	Analog Input BW (MHz)	Input Buffer	Package Group	Package Size: mm2:W x L (PKG)	Approx. Price (US$)	Architecture	DNL (Typ) (+/- LSB)	INL (Typ) (+/- LSB)	Reference Mode
	Filter by part number																			
☐	ADS4142 - 14-bit, 65 MSPS, Analog-to-Digital Converter (ADC)	14	65	1	72.3	11.7	88	95	2	DDR LVDS, Parallel CMOS	-40 to 85	800	No	VQFN	49 mm2: 7 x 7(VQFN)	18.65 | 1ku	Pipeline	0.5	1.5	Int
☐	ADS4145 - 14-Bit, 125-MSPS Analog-to-Digital Converter (ADC)	14	125	1	72.2	11.5	88	136	2	DDR LVDS, Parallel CMOS	-40 to 85	800	No	VQFN	49 mm2: 7 x 7(VQFN)	36.90 | 1ku	Pipeline	0.5	1.5	Int
☐	ADS6142 - 14-Bit, 65-MSPS Analog-to-Digital Converter (ADC)	14	65	1	74.6	12	86	285	2	DDR LVDS, Parallel CMOS	-40 to 85	500	No	VQFN	25 mm2: 5 x 5(VQFN)	20.50 | 1ku	Pipeline	0.5	2	Ext, Int
☐	ADS6143 - 14-Bit, 80-MSPS Analog-to-Digital Converter (ADC)	14	80	1	74.4	12	89	318	2	DDR LVDS, Parallel CMOS	-40 to 85	500	No	VQFN	25 mm2: 5 x 5(VQFN)	29.50 | 1ku	Pipeline	0.5	2	Ext, Int

図 9. ADC Selection

The ADS4142 device meets all the necessary requirements – linearity, speed, and accuracy. The ADS4142 device is a 14-bit, 65-MSPS, pipeline ADC, which operates from 1.8-V analog and 1.8-V digital power supplies with low-power consumption of 65 mW at 10 MSPS. The ADS4142 device is a single-channel ADC that has the same, excellent, 14-bit performance and low power, with parallel outputs that can simplify the FPGA code required to collect data. The ADS4142 device gives users the flexibility to include the choice of CMOS or DDR LVDS outputs, with programmable digital-output timing and LVDS drive strength. The ADS4142 device is available in a RoHS compliant, 7 mm × 7 mm, QFN48 package. The ADS4142 device has additional specifications that are important to note as the rest of the signal path is designed. First, the input characteristics of the ADC. Its full-scale differential-input range is 2 V_{PP}, common-mode voltage (VCM) is 0.95 V, and differential-input capacitance is 4 pF. The ADS4142 device uses differential inputs to reject common-mode noise and interference, increase DR, and improve overall performance due to balanced signaling.

3.2 Selecting the Amplifiers

An imaging system must preserve discontinuities wherever they exist in the scene – This requirement is more related to the step response of ADC-input circuitry (including the front-end amplifier, if any). As already discussed, the video output of the sensor is a pseudo-DC signal. Therefore, it is possible to encounter a full-scale change between adjacent pixels (or two consecutive conversions). The frequency content of the resulting waveform can greatly exceed the Nyquist frequency derived from the ADC sampling rate. These high-frequency contents in the waveform do not contain any information of interest, but must be processed by the front-end amplifier and input circuitry of the ADC. The insufficient BW and slew rate of the amplifier and ADC input circuitry may result in degradation of the system performance.

The signal must settle within 0.5 LSB at the input of the ADC for the worst-case, full-scale change in the given sampling period. This condition is critical to maintain the overall linearity performance of the ADC. Typically, amplifier data sheets specify output-settling performance only from 0.1% to 0.01%, which may not be sufficient for high-resolution converters (> 14 b). Therefore, the designer must verify the input-driver settling behavior, with simulators such as TINA-TI, to assist in amplifier selection.

The ADC AFE circuitry must be designed to complement the performance of the ADC and mainly consists of two parts: a driving amplifier and a flywheel RC filter, as shown in 図 10. Important functions in this key block include:

- Filtering to remove unwanted high-frequency signals
- Low-output impedance, which provides a buffer between the signal source and the ADC input
- Single-ended to differential conversion
- Amplification, to match signal levels to the ADC-input range
- Level shifting, to match the ADC common-mode input level

Select components which minimize the component count in this block. The next step is to look at one of the more demanding requirements for the analog signal-processing block – optimizing the bandwidth of the circuit. This design uses a simple, passive, single-pole, low-pass filter between the amplifier stage and ADC. The filter bandwidth is primarily driven by the following requirements:

- The RC-filter bandwidth must be low enough to band-limit the noise fed into the input of the ADC, thereby increasing the SNR of the system.
- The overall system bandwidth must be large enough to accommodate optimal settlings of the input signal at the ADC input before the start of the conversion.

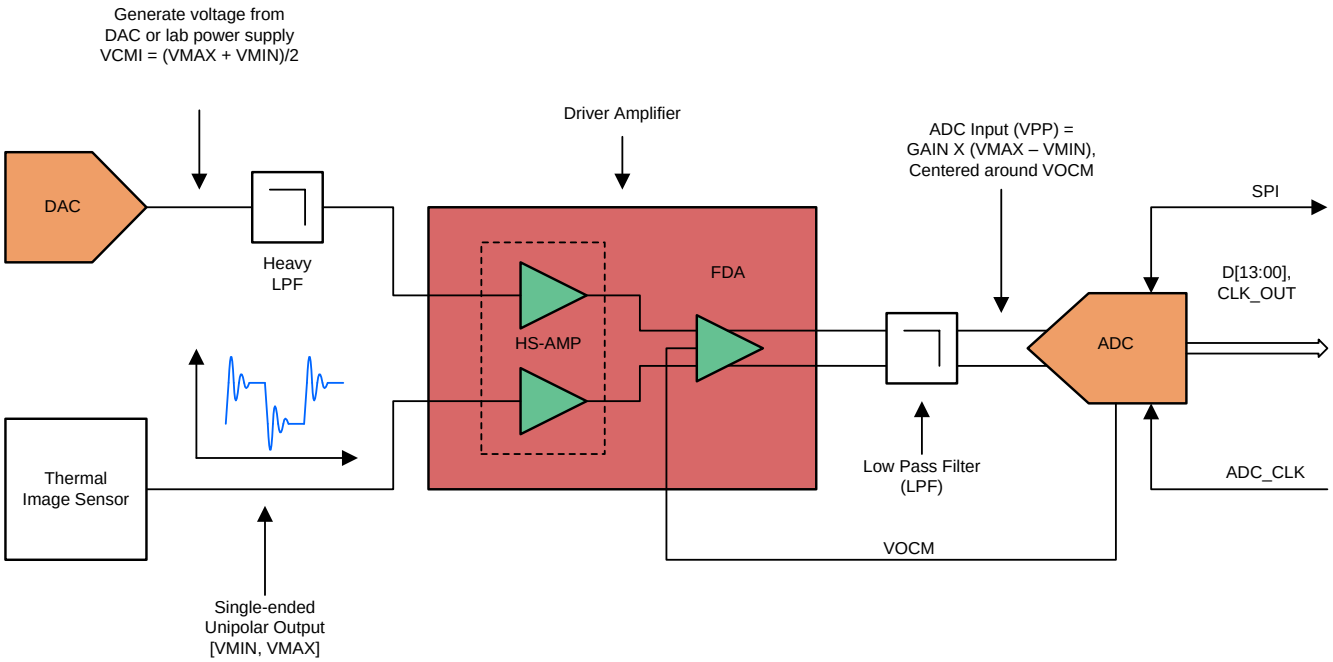


図 10. Conceptual Schematic of AFE Circuit for IR Imaging Applications

The settling time available to the amplifier may not equal an entire clock cycle. The source may dictate this, but there is a disturbance produced by the ADC on the opposite edge of the clock, and this event gives the filter only a ½-clock cycle to settle, even if the amplifier is not otherwise disturbed. If the amplifier is disturbed by this event, it does not leave as much time for the filter to settle. Theoretically, a simple RC requires about 10.4 time constants to settle to 14 bits, and for 10 MSPS, it results in a bandwidth of about 33 MHz. 式 2 gives the step response of the simple, first-order system for the worst-case full-scale change (ΔV).

$$v_{ADC}(t) = \pm \Delta V \left(1 - e^{-2\pi BWt}\right) \quad (2)$$

where

- BW is the 3-dB bandwidth of the system.

The settling error at the end of the ½-clock cycle (t = Ts / 2) is ΔV – 0.5 LBS, see 式 3.

$$BW \geq \frac{\ln\left(2^{N+1}\right)}{\pi Ts} = \frac{\ln\left(2^{N+1}\right)}{\pi} \times Fs = \frac{\ln\left(2^{14+1}\right)}{\pi} \times 10\,MHz = \sim 33.112\,MHz$$

$$BW \geq \sim 33.112\,MHz \quad (3)$$

where

- Ts is the sampling period.
- Fs is the sampling frequency.

図 11 shows the equivalent circuit for the analog input of the ADS4142 device, consisting of a switched-capacitor-based, differential, sample-and-hold architecture. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input, the INP and INM pins, must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP}, differential-input swing. The input-sampling circuit has a full-power bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Although the input structure of the ADS4142 device is completely differential, this ADC can be either single-ended or differentially driven. Optimum performance can be achieved by using a fully-differential driver amplifier.

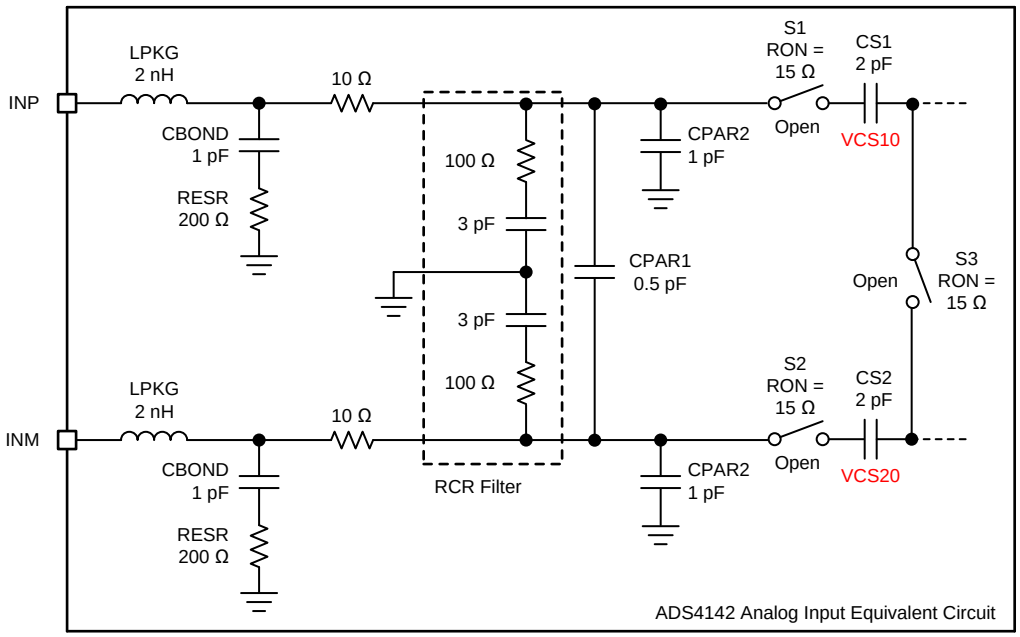


図 11. ADS4142 Analog Equivalent Circuit

The two distinctive stages to ADC operation are the track and hold phases. In the track phase, the sampling switches S1, S2, and S3 are closed and the sampling capacitors (CS1 and CS2) track the input signal with a certain RC-time constant. During the next clock phase (or the hold phase), the sampling switches S1, S2, and S3 are open and the sampling capacitors (CS1 and CS2) are held at the constant value of the input signal, that ideally corresponds to the last value of the track instant. These sampling switches (S1, S2, and S3) open or close at the sampling frequency (Fs), as shown in 図 12.

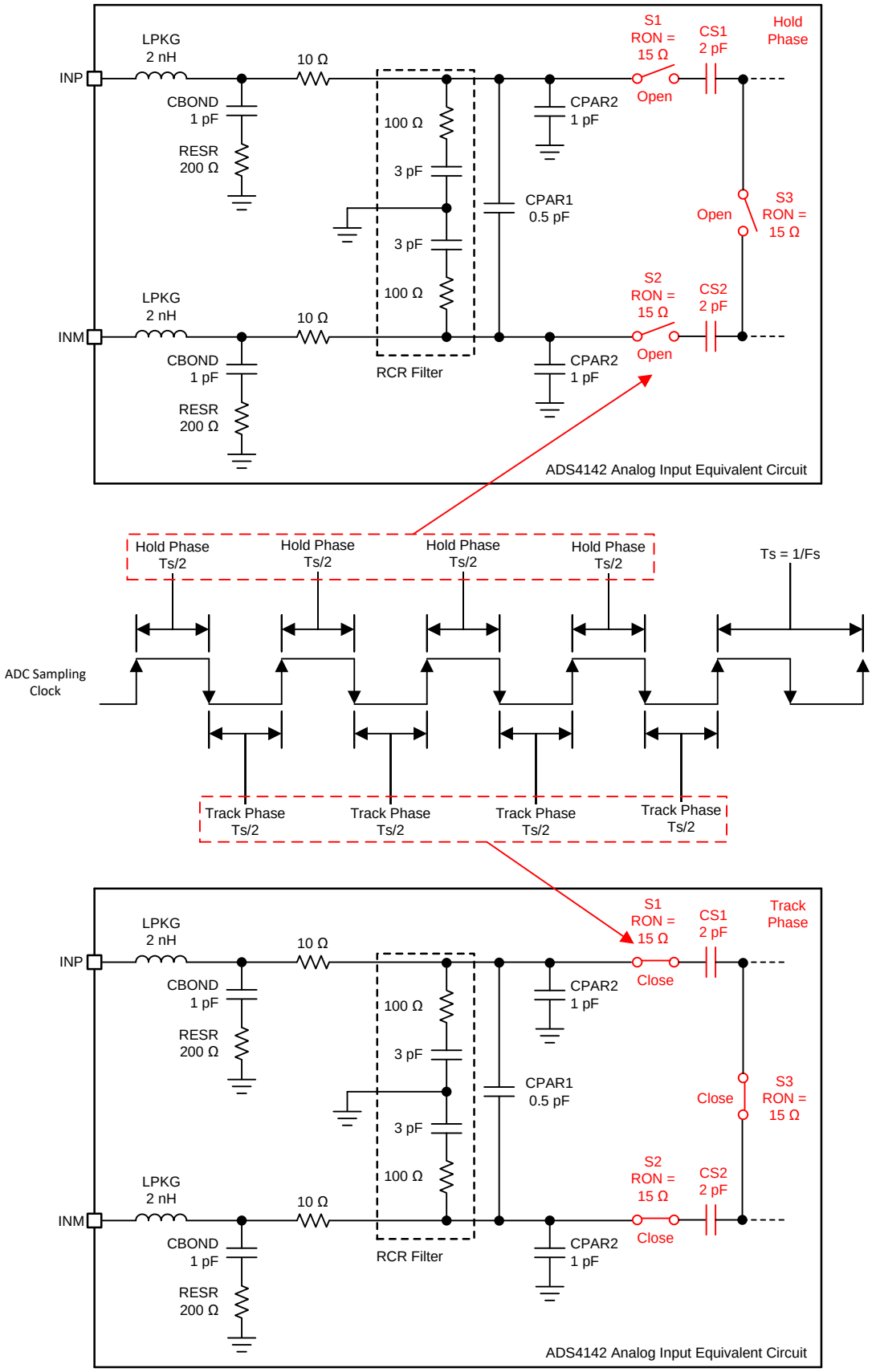


図 12. Sampling Switches S1 and S2

The ADC takes the sample of the input signal at the rising edge of the sampling clock, also known as track-to-hold mode transition. In 図 14, all the pixel outputs are time-multiplexed to the input of a global ADC to provide the digital output. The sensor output changes soon after the ADC takes a sample. The input of the driver amplifier may see a full-scale change between adjacent pixels immediately after the track-to-hold mode transition. When the ADC enters the hold phase, the sampling capacitor is not tracking the input signal. During this time, it is a good opportunity for the output of the driver amplifier to quickly settle and start acting like a DC source. Considering the correct sampling process, output of the driver-amplifier stage must continue to act like a DC source throughout the track phase. At the hold-to-track mode transition, the sampling switches reconnect to the source to recharge the sampling capacitors to a new value, by the external filter capacitors. This results in charge kick-back transients at the input of the ADC, as 図 14 shows. This occurrence is the most critical moment that determines the accuracy of the design, because the voltage across the sampling capacitors must settle to a ±0.5-LSB error band around the final value before the sampling switches open (or, track-to-hold mode transition).

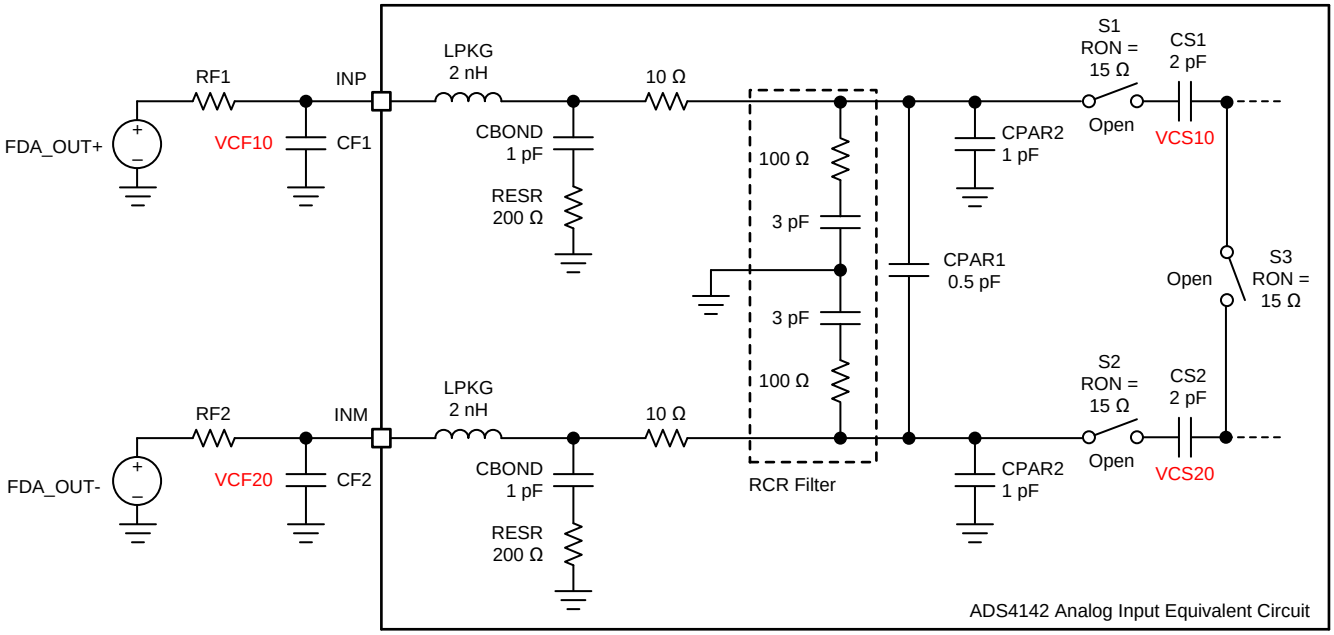


図 13. ADS4142 Analog Equivalent Circuit

From 図 13, assuming VCF10 > VCS10, users can see that at first the sampling capacitor (CS1) is quickly charged by the energy of the external input capacitor (CF1) through RS1 at the start of the track phase. The process of charging the sampling capacitance (CS1) causes a voltage drop across external input capacitor (CF1). The subsequent process of charging the sampling capacitor (CS1) is much slower due to this higher input impedance. Therefore, the external-RC filter component must be properly set, considering the time constant of the sampling capacitor charging in a given time period. 式 4 gives the magnitude of the voltage drop across the input capacitor (CF1), at the time that the sampling switches are closed.

$$\Delta V = \frac{C_{S1}}{C_{F1} + C_{S1}} \times \left(V_{CF10} - V_{CS10}\right) = \frac{1}{\frac{C_{F1}}{C_{S1}} + 1} \times \left(V_{CF10} - V_{CS10}\right) \quad (4)$$

A higher ratio between the input capacitor and sampling capacitor produces a smaller voltage drop. The input capacitor, CF, helps to reduce the kickback noise at the ADC input and provides a charge bucket to quickly charge the sampling capacitor during the track phase. The value of CF must be chosen such that the voltage droop (ΔV) on the external filter capacitor is less than 10% of the input voltage. Therefore, the generalization given in 式 4 can be used to estimate the necessary size of the external capacitor, CF.

- $C_F \geq 15\ C_S$
- C_{F1} and $C_{F2} \geq 33$ pF

For low distortion, the external filter capacitors (CF1 and CF2) must be a C0G or NP0 type. C0G-type capacitors exhibit minimal change in capacitance over input voltage, frequency, temperature, and so on, and are typically available in values of 10 nF or less. Thus, a C0G-type capacitor with a value of CF1 and CF2 = 33 pF is selected for this TI reference design. At this point, it is important to understand the tradeoffs involved in selecting the values of CF and RF. If the value of CF is high, it provides better attenuation against kickback noise when the sampling switches are closed. However, CF cannot be made arbitrarily high, because it degrades the phase margin of the driving amplifier, thus making it unstable. The series resistor, RF, acts as an isolation resistor, which helps to stabilize the driving amplifier. A higher value of RF is helpful from the amplifier stability perspective, but it degrades AC performance and must be balanced with the amplifier stability, to ensure that the distortion does not exceed the required specifications. Distortion happens due to the nonlinear input impedance of the ADC, and it increases with source impedance, input signal frequency, and amplitude. The maximum value of RF depends upon the fact that by the end of the track phase (TS/2), the sampling capacitor (CS) must be charged to an acceptable level of the measured input voltage. That statement means the signal must settle within 0.5 LSB at the input of the ADC for the worst-case, full-scale change at the end of acquisition time. 式 5 gives the value of the required external-filter resistance.

$$\left(R_F + R_{SH}\right) \times \left(C_F + C_S\right) \leq \frac{t_{TRACK}}{k1} \tag{5}$$

where

- k1 is number of time constants for the kick-back transient to settle, as defined in 式 7.
- R_{SH} represents the total series resistance from the ADC input pin to the sampling capacitor.

$$k1 = \ln\left(\frac{\left(V_{IN} - V_{CSH0}\right)}{\left(1 + \frac{C_F}{C_S}\right)V_{FSR}} \times 2^{(N+1)}\right) \tag{6}$$

For this design, the values of the parameters used in 式 6 follow:

- t_{TRACK} = 50 ns
- C_F = 27 pF
- C_S = 2 pF
- $V_{INP} = V_{CM} + 0.5$ V
- $V_{CSH0} = V_{CM} - 0.5$ V
- V_{FSR} = 1 V
- N = 14
- RSH = 10 Ω + 15 Ω + 7.5 Ω = 32.5 Ω

After inserting these values in 式 6, RF should be less than 200 Ω. The minimum value for RF depends on the output impedance of the amplifier, based on stability considerations. First select the driver amplifiers and then use the TINA simulations to further refine the values of the filter components.

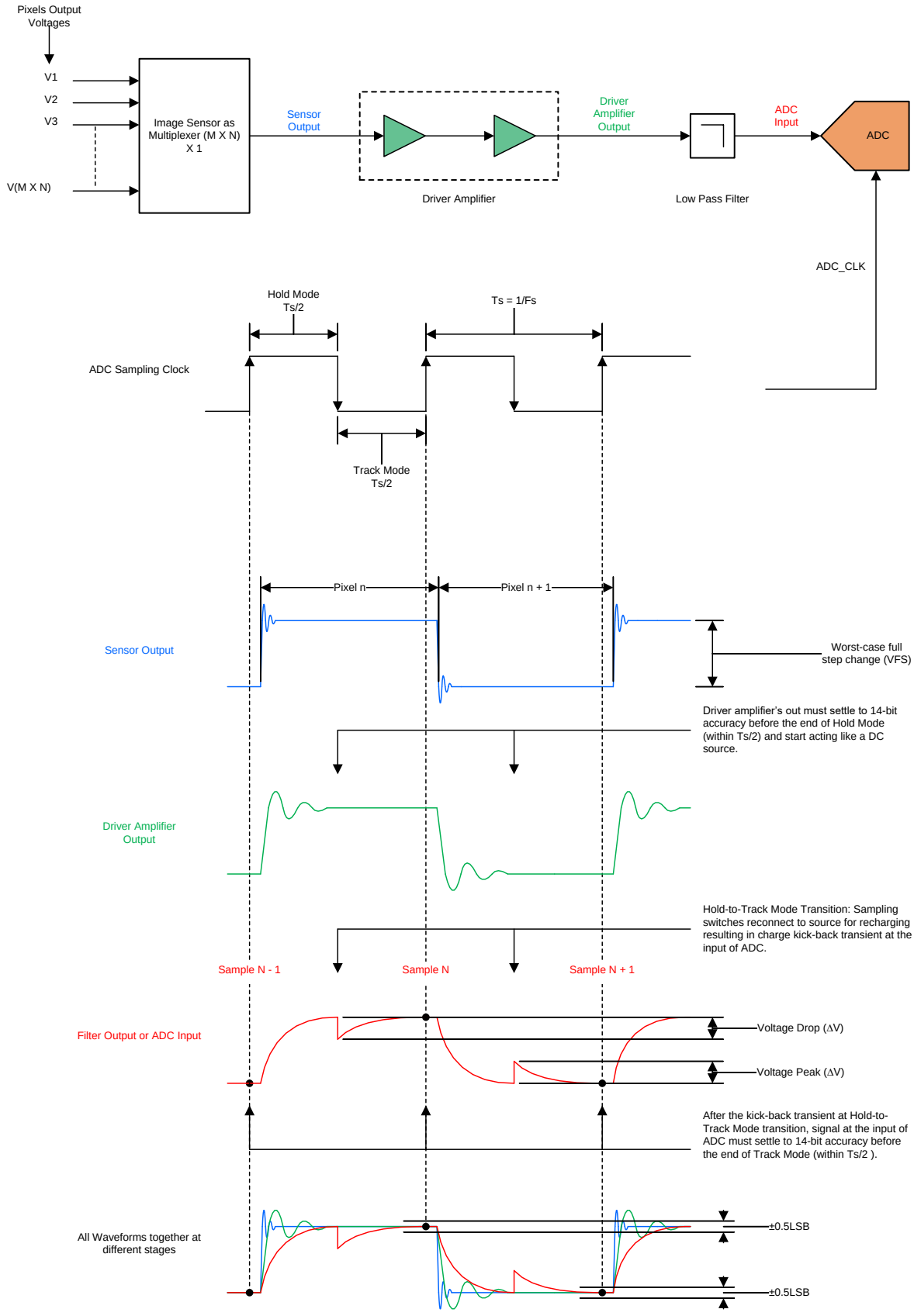


図 14. Waveforms at Different Stages in the Signal Chain

The process of selecting suitable amplifiers for driving the high-speed ADC with differential inputs may be a challenging task. Multiplexed applications, such as pixel-by-pixel reading in imaging systems, exercise the slewing capability and bandwidth capability of the driving amplifier. Bandwidth and slew rate requirements are significantly increased by operating in a multiplexed mode, and care must be taken in selecting a component for this application. The settling time of an amplifier mainly consists of dead time, slew time, recovery time, and linear settling time, as shown in 図 15.

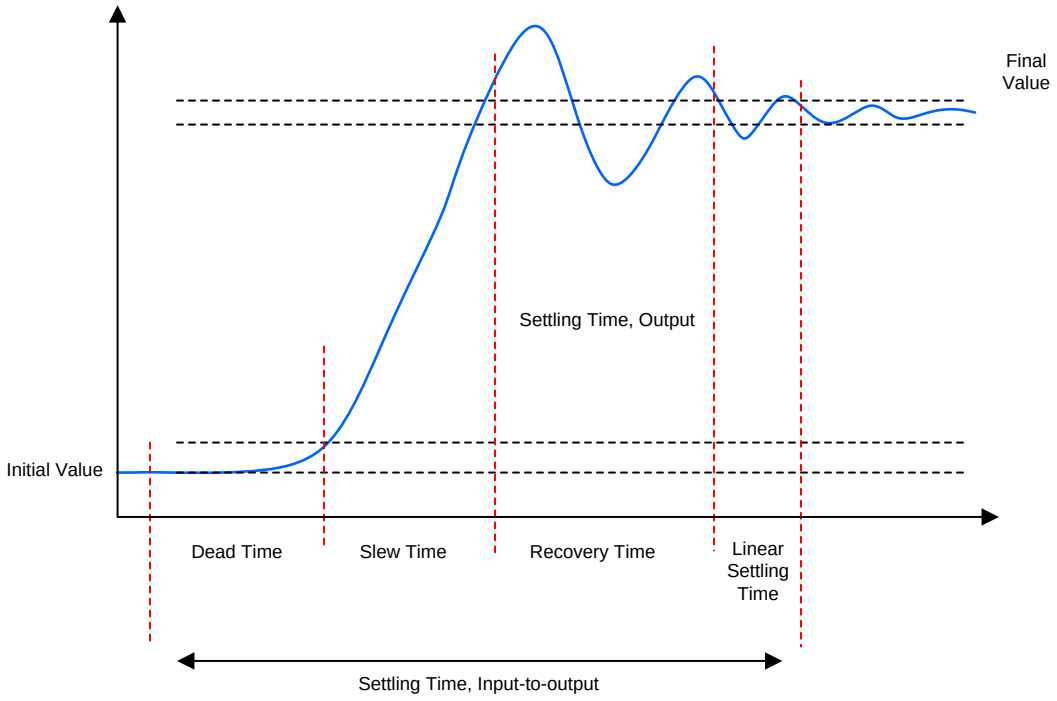


図 15. Settling Time

In 図 15, the high-speed amplifier (HS-AMP), FDA, and filter must settle to 0.5 LSB for a worst-case, full-step change (VFSR) within a given sampling period. Assuming each stage is a simple, first-order system, then 式 7 can give the number of time constants (k2) required for N-bit settling.

$$k2 = (N + 1) \ln 2 \quad (7)$$

where

- N is the resolution of the ADC.

When the amplifier is out of slew, and if the input is not changing significantly, then the amplifier perceives the input as small signal. Therefore, 式 8 and 式 9 give the individual settling times of the HS-AMP, FDA, and filter.

$$t_{HS-AMP} = \frac{\Delta V}{SR_{HS-AMP}} + \frac{k}{2\pi \times SSBW_{HS-AMP}}$$

where

- t_{HS-AMP} is settling time of the HS-AMP.
- SR_{HS-AMP} is slew rate of the HS-AMP.
- $SSBW_{HS-AMP}$ is small-signal bandwidth of the HS-AMP. (8)

$$t_{FDA} = \frac{\Delta V}{SR_{FDA}} + \frac{k}{2\pi \times SSBW_{FDA}}$$

where

- $t_{FDA}$is settling time of the HS-AMP.
- $SR_{FDA}$is slew rate of the HS-AMP.
- $SSBW_{FDA}$ is small-signal bandwidth of the FDA. (9)

For a cascaded configuration, 式 10 gives a close approximation of the overall settling time.

$$\text{Settling Time of Driver Amplifier} = t_{Settling} = \sqrt[2]{t_{HS-AMP}^{\ 2} + t_{FDA}^{\ 2}} \quad (10)$$

The settling time of the driver amplifier should be smaller than the duration of the hold phase (T_S/2), as given in 式 11.

$$t_{Settling} < \frac{T_S}{2} = \frac{100\ ns}{2} = 50\ ns \quad (11)$$

Now, select the HS-AMP and FDA such that 式 11 is satisfied.

Go to www.ti.com to find a FDA (see 図 16).

TI Home → Amplifiers → Operational Amplifiers (Op Amps) → Fully Differential Amplifiers

Compare	Part Number	Number of Channels (#)	Total Supply Voltage (Min) (+5V=5, +/-5V=10)	Total Supply Voltage (Max) (+5V=5, +/-5V=10)	BW @ Acl (MHz)	Acl, min spec gain (V/V)	Slew Rate (Typ) (V/us)	Vn at Flatband (Typ) (nV/rtHz)	Iq per channel (Typ) (mA)	Rail-to-Rail	Vos (Offset Voltage @ 25C) (Max) (mV)	Rating	Operating Temperature Range (C)	Package Group	Approx. Price (US$)	Output Current (Typ) (mA)	2nd Harmonic (dBc)	3rd Harmonic (dBc)	Package Size: mm2:W x L (PKG)
☐	THS4551 - Low Noise, Precision, 150MHz, Fully Differential Amplifier	1	2.7	5.4	150	1	220	3.3	1.35	In to V-, Out	0.175	Catalog	-40 to 125	QFN, VQFN, VSSOP	1.39 | 1ku	45	128	139	4 mm2: 2 x 2(QFN), 9 mm2: 3 x 3(VQFN), 15 mm2: 4.9 x 3(VSSOP)
☐	THS4531 - Ultra low power 0.25mA, RRO, fully differential amplifier	1	2.5	5.5	36	1	220	10	0.25	Out	1	Catalog	-40 to 125	QFN, SOIC, VSSOP	1.32 | 1ku	26	128	137	4 mm2: 2 x 2(QFN), 29 mm2: 6 x 4.9(SOIC), 15 mm2: 4.9 x 3(VSSOP)
☐	THS4531A - Ultra Low Power, RRO, Fully-Differential Amplifier	1	2.5	5.5	36	1	220	10	0.25	In to V-, Out	0.4	Catalog	-40 to 125	QFN, SOIC, VSSOP	1.10 | 1ku	26	129	138	4 mm2: 2 x 2(QFN), 29 mm2: 6 x 4.9(SOIC), 15 mm2: 4.9 x 3(VSSOP)
☐	THS4521-HT - High Temperature, Very Low Power, Negative Rail Input, Rail-to-Rail Output, Differential Amp - Hi-Rel	1	2.5	3.6	40.7	1	39	19.95	1.1	In to V-, Out	11.5	High Temp	-55 to 175, -55 to 210	CFP, SOIC		33	96	91.5	See datasheet (CFP), 29 mm2: 6 x 4.9(SOIC)

図 16. High-Speed, Fully-Differential Amplifier Comparison

Go to www.ti.com to find a HS-AMP (see 図 17).

TI Home → Amplifiers → Operational Amplifiers (Op Amps) → High-Speed Op Amps (GBW ≥ 50MHz)

Compare	Part Number	Number of Channels (#)	Architecture	Total Supply Voltage (Min) (+5V=5, +/-5V=10)	Total Supply Voltage (Max) (+5V=5, +/-5V=10)	BW @ Acl (MHz)	Acl, min spec gain (V/V)	Slew Rate (Typ) (V/us)	Vn at Flatband (Typ) (nV/rtHz)	Vn at 1kHz (Typ) (nV/rtHz)	Iq per channel (Typ) (mA)	Vos (Offset Voltage @ 25C) (Max) (mV)	Rail-to-Rail	Features	Rating	Operating Temperature Range (C)	Package Group	Approx. Price (US$)	Package Size: mm2:W x L (PKG)	Input Bias Current (Max) (pA)	GBW (Typ) (MHz)
☐	OPA2684 - Dual, Low Power, Current Feedback Operational Amplifier	2	Bipolar, Current FB	5	12	210	1	820	3.7	3.7	1.7	3.5	No	Small Size, Shutdown	Catalog	-40 to 125	SOIC, SOT-23	2.58 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23)	10000000	210
☐	OPA2683 - Very Low Power, Dual Current Feedback Operational Amplifier	2	Bipolar, Current FB	5	12	145	1	210	4.4	4.4	0.79	3.5	No	Shutdown	Catalog	-40 to 85	SOIC, SOT-23, VSSOP	2.01 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23), 15 mm2: 4.9 x 3(VSSOP)	4000000	145
☐	OPA2836 - Dual, Very Low Power, Rail to Rail out, Negative Rail in, VFB Op Amp	2	Bipolar, Voltage FB	2.5	5.5	205	1	560	4.6	4.6	1	0.4	In to V-, Out	Small Size, Shutdown	Catalog	-40 to 125	QFN, SOIC, UQFN, VSSOP	1.50 | 1ku	4 mm2: 2 x 2(QFN), 29 mm2: 6 x 4.9(SOIC), 4 mm2: 2 x 2(UQFN), 15 mm2: 4.9 x 3(VSSOP)	1000000	120
☐	OPA2835 - Dual, Ultra Low Power, Rail to Rail Out, Negative Rail In, VFB Amplifier	2	Bipolar, Voltage FB	2.5	5.5	56	1	160	9.3	10	0.25	0.5	In to V-, Out	Shutdown	Catalog	-40 to 125	QFN, SOIC, UQFN, VSSOP	1.35 | 1ku	4 mm2: 2 x 2(QFN), 29 mm2: 6 x 4.9(SOIC), 4 mm2: 2 x 2(UQFN), 15 mm2: 4.9 x 3(VSSOP)	400000	30
☐	LM6172 - Dual High Speed, Low Power, Low Distortion Voltage Feedback Amplifiers	2	Bipolar, Voltage FB	5.5	36	160	1	3000	12	12	2.3	1.5	No	N/A	Catalog	-40 to 85	PDIP, SOIC	2.17 | 1ku	See datasheet (PDIP), 29 mm2: 6 x 4.9(SOIC)	1500000	160
☐	LM6172QML-SP - Dual High Speed, Low Power, Low Distortion Voltage Feedback Amplifiers - Hi-Rel	2	Voltage FB, Bipolar	5.5	36	80		3000	12	12	2.3	1.5		N/A	Space	-55 to 125	CDIP, CFP		See datasheet (CDIP), See datasheet (CFP)		80
☐	LM6172QML - Dual High Speed, Low Power, Low Distortion Voltage Feedback Amplifiers - Hi-Rel	2	Voltage FB, Bipolar	5.5	36	80		3000	12	12	2.3	1.5		N/A	Military	-55 to 125	CDIP, CFP		See datasheet (CDIP), See datasheet (CFP)		80

図 17. High-Speed Amplifier Comparison

For this design, the OPA2626 and THS4551 devices seem to be better choices in terms of bandwidth, slew rate, noise, IQ, distortion, and device package. Other FDAs also satisfy the settling-time requirement and available in smaller packages, for example, the THS4541 device, with low noise (2.2 nV/√Hz), high bandwidth (approximately 620 MHz) and high-slew rate (approximately 1500V/µs), but at the cost of a higher operating current (approximately 10.1 mA). With a high DC precision of only 100-µV offset voltage, a wide gain-bandwidth product of 120 MHz, and a low wideband noise of 2.5 nV/√Hz, the OPAx626 family of devices is optimized for driving high-throughput, high-resolution ADCs. The OPA2626 device is available in an 8-pin VSSOP package. In cascaded configuration, the OPA2626 and THS4551 devices settle to 0.5 LSB for a worst-case, full-step change (VFSR) within 38 ns. That occurrence means the output of the driver-amplifier circuitry starts acting like a constant DC source, even before the ADC enters into the track phase.

3.3 *Refining Values of Filter Components: Parameter Stepping Technique in TINA-TI Simulation*

The resistor-capacitor combination can be optimized slightly for the circuit and input signal being converted by simply varying the R-C combination; however, remember that having the incorrect combination will limit the linearity performance of the ADC. Also, increasing the bandwidth as seen by the ADC introduces more noise.

図 18 shows the TINA schematic of driver amplifier and analog input equivalent circuit for the ADS4142 device. The analog input equivalent circuit in TINA schematic is slightly different from the one in the ADS4142 data sheet. For example, in the TINA schematic, all the switches have been replaced by voltage controlled switches, so that these switches can be controlled to model the track and hold process of the ADC. On the left-hand side is the OPA2626 op amp, THS4551 FDA, and RC-charge bucket circuit. V_{TRACK} and V_{HOLD} are signal sources used to control the timing of the switches. The timings of these sources were configured for a 10-MSPS sampling rate.

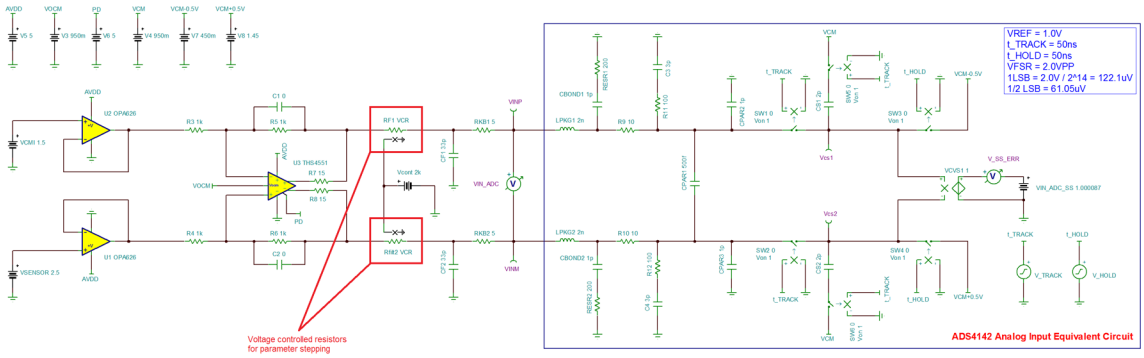


図 18. TINA Schematic for Parameter Stepping

The settling-error meter must be configured to read zero error when the voltage across the sample capacitor has settled to the steady-state output of the amplifier. This reading is achieved by running DC analysis and setting the voltage source, VIN_ADC_SS, to a DC voltage equal to the steady-state output of the amplifier, VIN_ADC, as shown in 図 19. The voltage-controlled voltage source VCVS1 translates the voltage across the sample capacitors from differential to single-ended. This voltage is compared to a steady-state voltage source to compute the settling error.

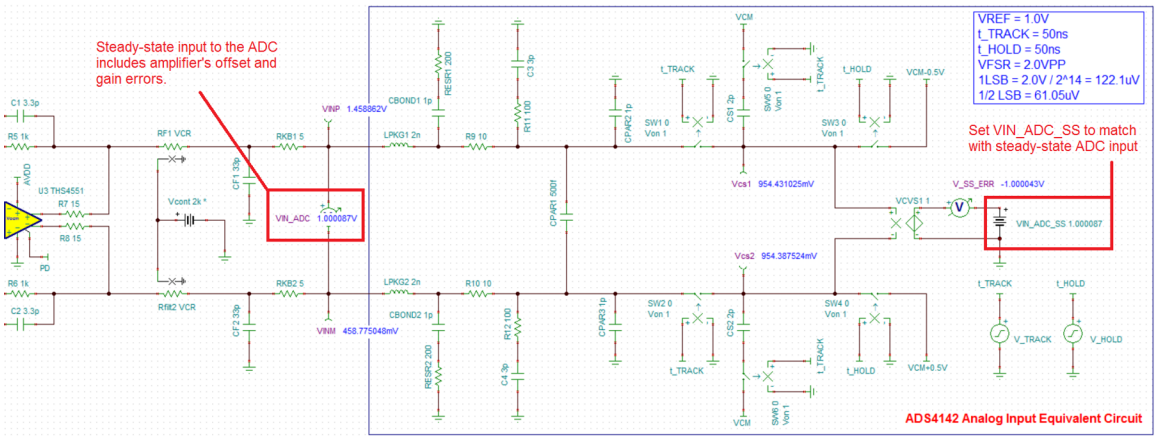


図 19. Run DC Analysis for Steady State ADC Input Voltage

The TINA-TI SPICE simulator was used to optimize the RC-charge bucket circuit and to verify that the error target is achieved. As a reminder, we know the filter capacitor value is 33 pF and the maximum filter resistance value is 200 Ω. Filter resistance cannot be too low; otherwise the stability of the THS4551 FDA may become a concern. The parameter-stepping technique was used to find the best resistance for a given fixed-filter capacitor. To start, the range of the filter-resistor values can be from 90 Ω to 200 Ω. Parameter stepping sweeps the values of the filter resistor. However, parameter stepping does not allow for two equal components to be simultaneously stepped. A way around this limitation is to use a voltage-controlled resistor. 図 20 shows two voltage-controlled resistors controlled by the source, Vcont. The resistance is equal to the control source, so each resistor in this example is set to 1 kΩ, because Vcont is 1 kV. Vcont was configured to run 15 different simulations, with resistor values ranging from 90 to 200 Ω, using either the linear sweep type or list of standard resistor values. Run the transient analysis for several conversion cycles. 図 20 shows a graph containing 15 sets of curves – one for each resistance value in the parameter step. To make the simulation results easier to look at, adjust the vertical and horizontal axis scaling. The main curves to look at here are the error curves – V_SS_ERR [1] through V_SS_ERR [15].

The error curves should ideally settle to 0 V, so set the vertical range accordingly for zooming in on the error. On the horizontal axis, always ignore the first cycle, because some start-up behavior invalidates these results. After adjusting the curves, 図 20 shows what the graphs look like. There is one error curve for each resistance value, for a total of 15 different curves. The legend lists the curve name, parameter step value for that curve, time, and value of the curve at that time. So, for example, the curve V_SS_ERR[10] is the error voltage source measured with a 145-Ω resistor, at 500 ns, with an error of –28.748462 µV. Remember, the parameter being stepped is actually a voltage source that is used to set resistance, so the 145-Ω resistor shows up as a voltage.

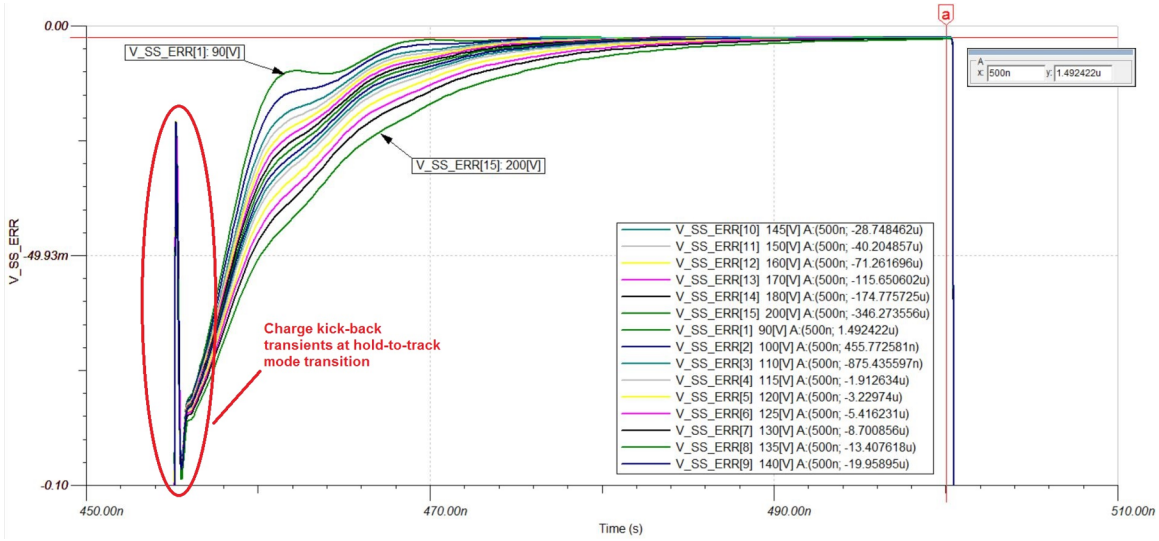


図 20. Parameter Stepping Simulation for Filter Resistors from 90 Ω to 200 Ω

Generally, there are three types of curves – one curve has overshoot, one curve is under-damped, and one curve is in-between the other two curves. Based on a visual inspection and the errors listed in the legend, look for the best curves from a settling perspective. Or, adjust the voltage scale to ±62 µV ,representing ±0.5 LSB of the ADS4142 ADC. As shown in 図 21, all curves from V_SS_ERR[1] through V_SS_ERR[11] settle to ±0.5 LSB in a given time period. Notice that the polarity of the settling error transitions from 1.492422 µV to –40.204857 µV. The idea is that some curve within this range will have an error near zero, for example, curve V_SS_ERR[2], with 100 Ω, settles to 455.77258 nV that is closest to the final value. However for this design, 130 Ω is used with a settling error of about 8.700856 µV, which is not far from the final value but well within ±0.5 LSB error limits. Now, the low-pass filter formed by 130 Ω and 33 pF reject more noise than the low-pass formed by 100 Ω and 33 pF. Therefore, with 130 Ω and 33 pF, the system bandwidth (–3 dB) is 37.12 MHz.

The RKB series resistor on the ADC inputs to damp-out ringing caused by package parasitic. Increasing this resistor also tends to reduce bandwidth peaking. However, increasing RKB increases signal attenuation, and the amplifier must drive a larger signal to fill the ADC input range. Select a kickback resistor (RKB1 and RKB2), based on experience and the ADC data sheet recommendations or both. The ADS4142 data sheet recommends a value between 5-Ω to 15-Ω in series with each input pin.

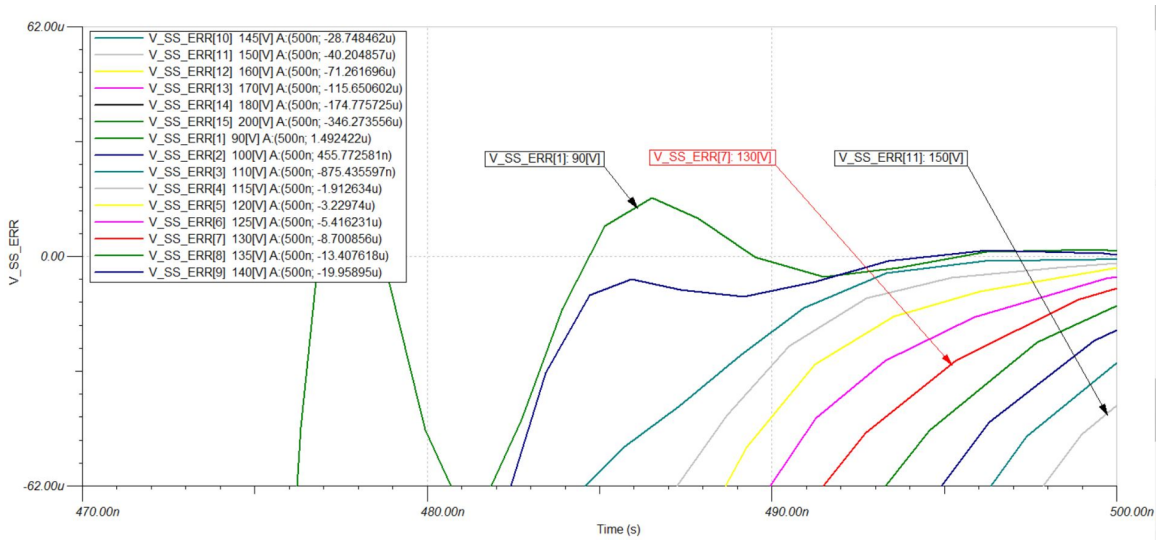


図 21. Parameter Stepping: Curves Settling Within ±0.5 LSB

3.4 Noise

Noise generated by the analog front-end electronics (AFE) must be minimized because it directly impacts dynamic range of the system. Noise in the AFE consists of wideband noise from driver amplifier circuitry, wideband noise from the ADC, and quantization noise from the ADC. The ac specifications of a stand-alone ADC like SNR and SINAD are usually tested with a sinusoidal input. Because imaging signals are not pure sine waves, ADC's ac specifications such as SNR and SINAD are not directly applicable to imaging systems. ADCs SNR or SINAD is tested with a sine-wave input, and includes the effects of distortion of the analog signal, converter distortion due to integral and differential nonlinearity (INL and DNL), quantization noise, and thermal noise. The distortion numbers are not of interest in imaging applications because image sensor's output signal is not sinusoidal in nature, and the frontend of the ADC samples the thermal image sensor's signal only during a relatively slow-moving portion of the waveform. Instead, SNR can be defined in a somewhat different manner, based on wideband noise. The wideband noise of an AFE can be measured by using a "fixed-input histogram" test. In an ideal system, a fixed input should produce a single output code. Noise in the system will produce a range of codes; from their random distribution, the RMS noise value can be statistically calculated. The RMS wideband noise can then be compared with imager noise, and the overall system SNR can be calculated. Noise will also be introduced by the amplifier circuitry, though this can be minimized by amplifier choice and circuit techniques.

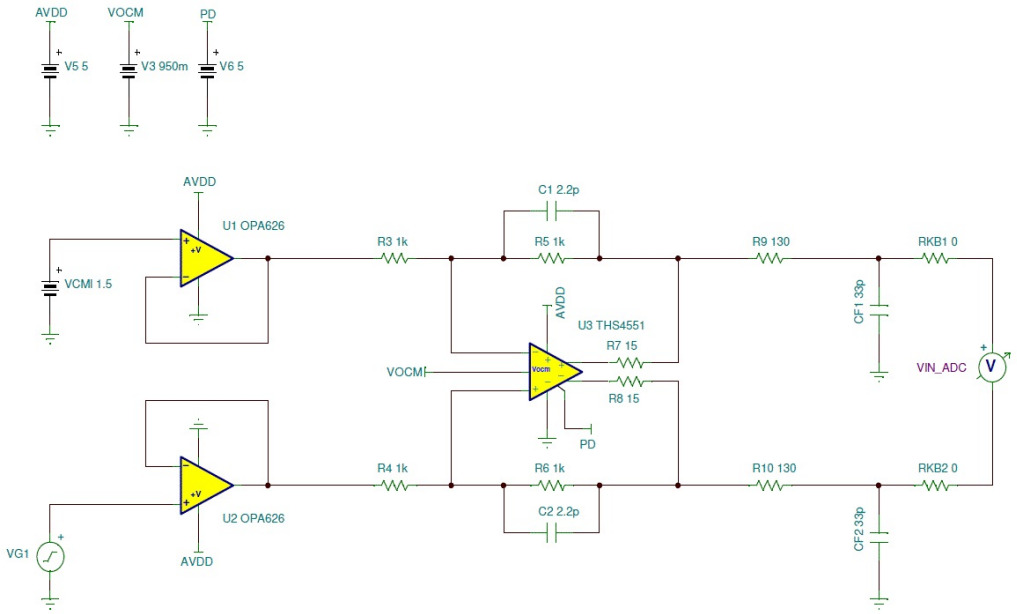


図 22. TINA Schematic for Noise Simulation

From TINA-TI simulation, the integrated output noise of the driver amplifier circuitry over the system bandwidth is around 73.38 μV_{RMS}. The amplitude of the noise is supposed to have a Gaussian distribution. Therefore, the peak-to-peak output noise is calculated in 式 12.

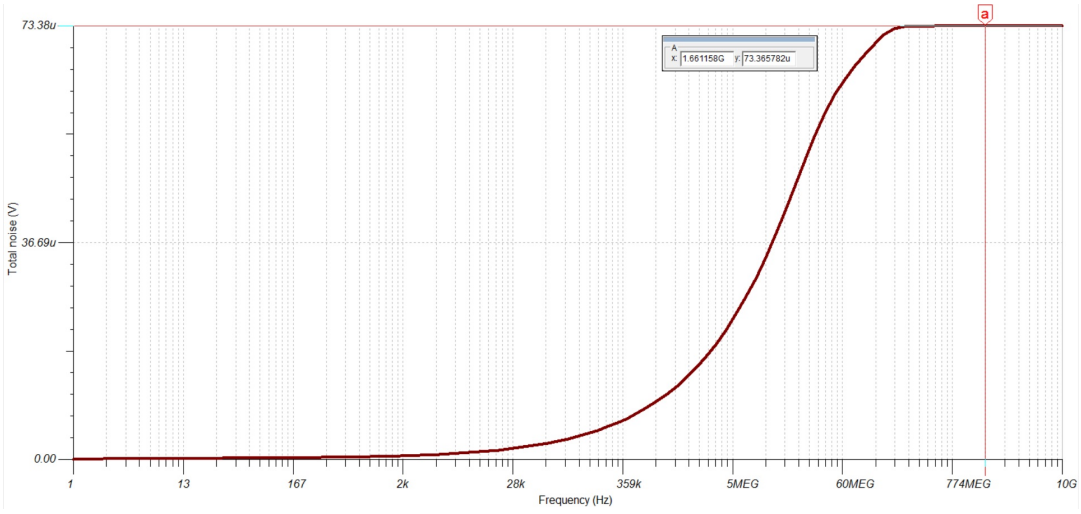


図 23. Total Output Noise of Front-End Amplifier

$$V_{Noise-AFE}(P-P) = 6.6 \times 73.38\ \mu V_{RMS} = 484.308\ \mu V_{PP} \quad (12)$$

Compare the output noise of the driver amplifier with 1 LSB (式 13) of the ADS4142 device, based on 12-bit ENOB and 2-V full-scale input range.

$$1\,LSB = \frac{2\,V}{2^{12}} = 488\ \mu V \quad (13)$$

The peak-to-peak output noise of the driver amplifier is comparable to the 1 LSB of the ADS4142 device with respect to 12-bit ENOB. Therefore, this driver amplifier circuitry seems to be a good choice from the noise perspective. However, the final decision must be made after testing the driver amplifier and ADC together.

4 Hardware Overview

図 24 shows the TIDA-01403 hardware and allows users to evaluate the performance of the TI Design system. All of the components such as ICs (high speed amplifier, fully differential amplifier, ADC, and LDOs), connectors, pin headers, and others are placed on the top side of the PCB. There are test points located on the PCB for most of the power nodes. The size of the board is 105.41 mm × 87.63 mm that was chosen for easy handling during the tests. However, the board size should be optimized as per mechanical constraints of the end product.

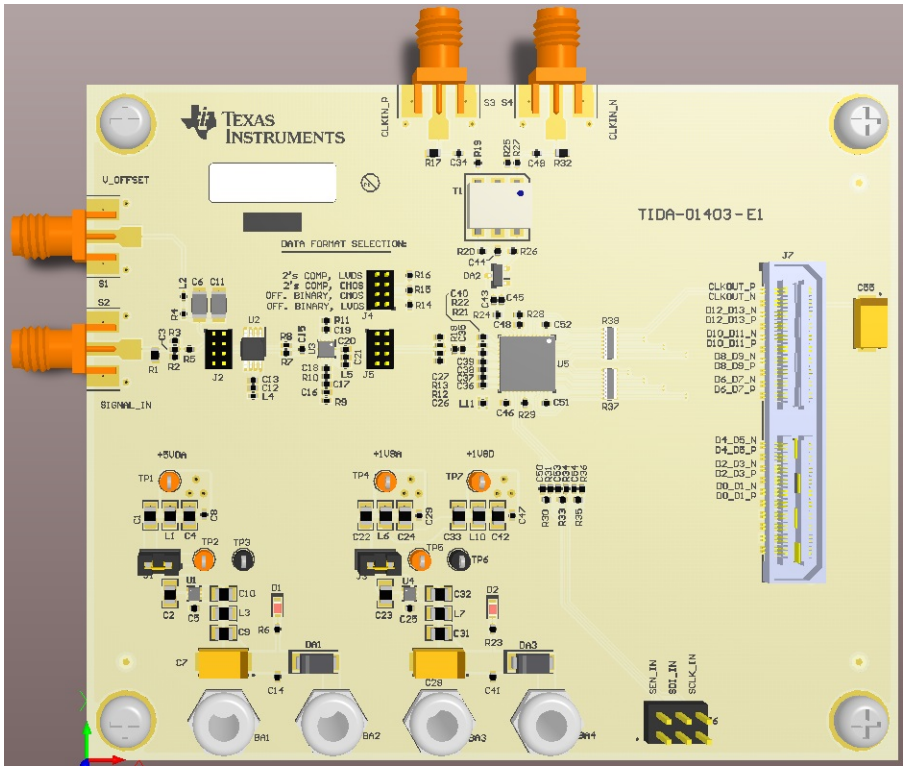


図 24. TIDA-01403 TI Design Hardware

TI Design hardware can be put in different configuration by changing jumper settings. 表 2 shows the function and setting of jumpers and connectors used in this reference design.

表 2. TIDA-01403 Connector and Jumper Details

CONNECTOR, JUMPER	FUNCTION, SETTINGS
S1	V_OFFSET: 2 V DC from lab power supply
S2	SIGNAL_IN: Single-ended 2-V_{PP} sinusoidal input signal from function generator
S3	CLKIN_P: Differential input sampling clock positive
S4	CLKIN_N: Differential input sampling clock negative
BA1 and BA3	Circuit Ground
BA2	External power supply input: 5.5 V Nominal; 6.5 V Max
BA4	External power supply input: 2.5 V Nominal; 6.5 V Max
J1	Connect or disconnect 5-V LDO output with the 5-V supply of the system
J2	For SNR, INL and DNL testing: • Jumper on J2-3 and J2-4 • Jumper on J2-5 and J2-6 For histogram testing • Jumper on J2-1 and J2-2 • Jumper on J2-5 and J2-6
J3	Connect or disconnect 1.8-V LDO output with the 1.8-V supply of the system
J4	ADC data output format selection: • Jumper on J4-1 and J4-2: Offset binary, LVDS • Jumper on J4-3 and J5-4: Offset binary, CMOS • Jumper on J4-5 and J4-6: 2's complement, CMOS • Jumper on J4-7 and J5-8: 2's complement, LVDS
J5	For normal operation: • Jumper on J5-3 and J5-4 • Jumper on J5-5 and J5-6 To disconnect amplifier stage and stand-alone ADC testing: • Jumper on J5-1 and J5-2 • Jumper on J5-7 and J5-8
J6	SPI interface to configure the internal registers of the ADC using GUI • J6-2: SEN • J6-4: SDI • J6-6: SCLK • J6-1, J6-3, J6-5: GND
J7	Interface to FPGA high speed data capture card

5 Test Setup

The test set-up for the TIDA-01403 is shown in 図 25. The test set-up requires either two signal generators that are externally locked through the 10-MHz reference or single function generator capable of providing synchronized clock and signal. The clock source is commonly synchronized with the signal generator of the input frequency to keep the clock and IF coherent for meaningful FFT analysis. A single-ended clock is supplied to the SMA connecter, S3, directly. This clock is converted to differential and AC coupled to the ADC by transformer coupling. The clock input must be from a clean, low-jitter source and is commonly filtered external to the board by a narrow bandpass filter. Depending on filter attenuation, the clock generator amplitude must be set to 10–13 dBm and the amplitude offset is not an issue due to the AC coupling of the clock input. The GUI automatically calculates the input frequency based on the FFT record length and the desired ADC sampling frequency. The function generator and lab power supplies are controlled by the GUI over the GPIB interface bus. The amplitude of input signal is adjusted until fundamental amplitude reaches approximately –1 dBFS.

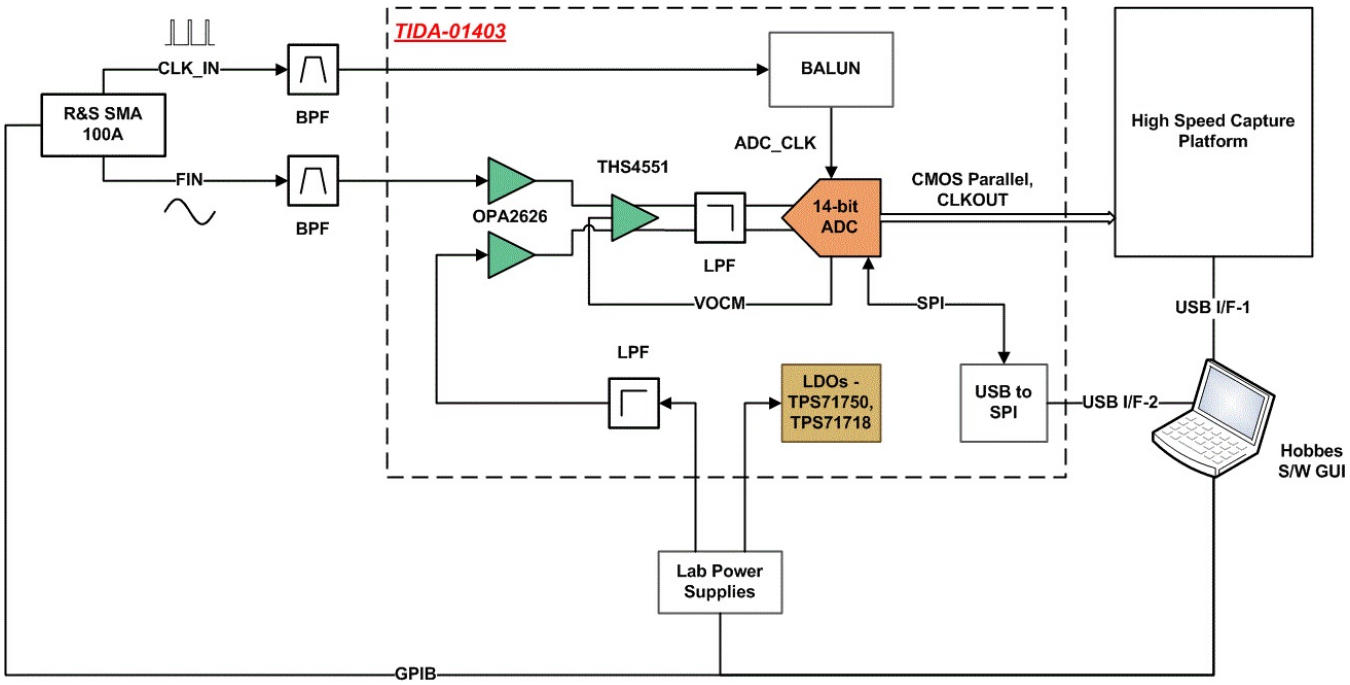


図 25. TIDA-01403 Test Setup

6 Test Results

The test data in the following sections were measured with the system at room temperature, unless otherwise noted.

All of the measurements in this section were measured with calibrated lab equipment.

6.1 Histogram Test

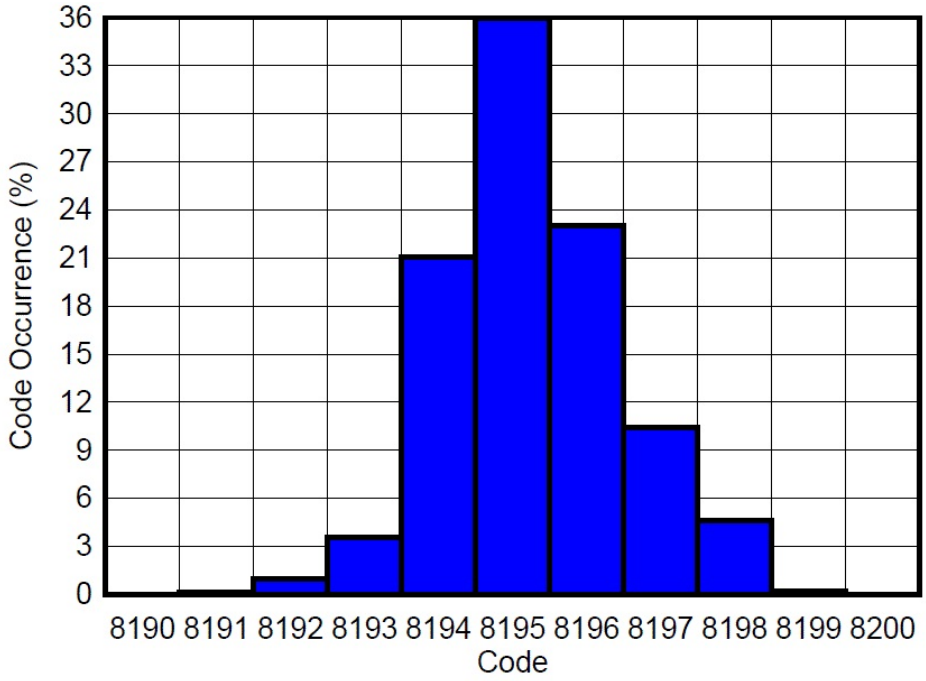


図 26. DC Input Histogram Test of ADC With Driver Amplifier

6.2 DNL and INL Test

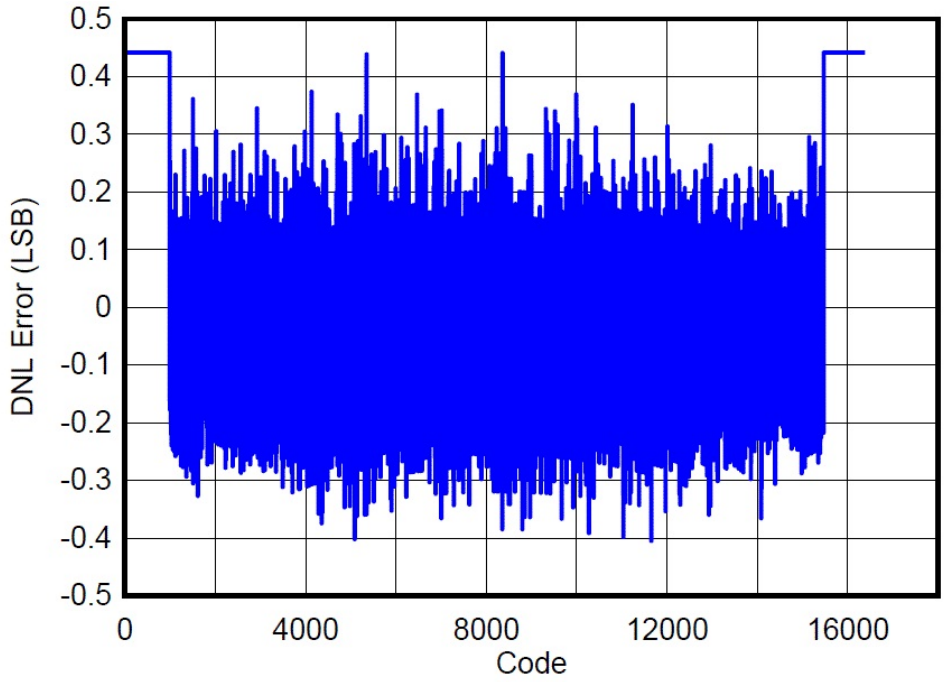


図 27. ADC DNL Test With Driver Amplifier

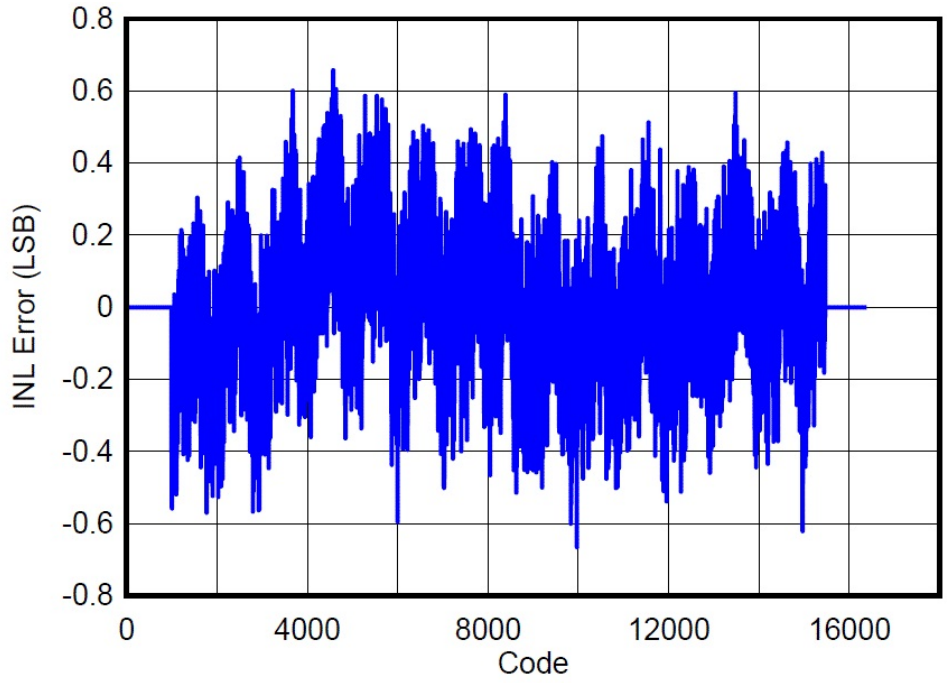


図 28. ADC INL Test With Driver Amplifier

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-01403.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01403.

7.3 PCB Layout Recommendations

7.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01403.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-01403.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01403.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01403.

8 Software Files

To download the software files, see the design files at TIDA-01403.

9 About the Author

Mike Wang is a field application engineer (FAE) at TI, where he has supported the video surveillance market for over three years, including sectors such as thermal imaging cameras, IP network cameras, video recorders, and so on. He received his master of science in mechantronic engineering at Zhejiang University in Hangzhou, Zhejiang.

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