# *TI Designs: TIDA-01587*
# *ブラシレスDCサーボ・ドライブ用の10.8V/30W、効率95%超、4.3cm²の電力段のリファレンス・デザイン*

## 概要

この15W、16mm×27mm電力段のリファレンス・デザインは、3～4セルのリチウムイオン・バッテリで動作するブラシレスDC (BLDC)モータを駆動し、その位置を制御します。この高効率ソリューションは、モータ内部への取り付けが容易で高精度モータ位置制御をサポートする超小型フォーム・ファクタで提供されます。また、このリファレンス・デザインは位置フィードバックによりモータの高速駆動が可能です。過電流と短絡に対する保護機能を備えており、オンボードMCUがUART接続を提供することから、任意の外部コントローラによる制御が可能です。

## リソース

| | |
|---|---|
| TIDA-01587 | デザイン・フォルダ |
| DRV8304 | プロダクト・フォルダ |
| CSD87502Q2 | プロダクト・フォルダ |
| MSP430FR5949 | プロダクト・フォルダ |
| TPS709 | プロダクト・フォルダ |
| TVS3300 | プロダクト・フォルダ |

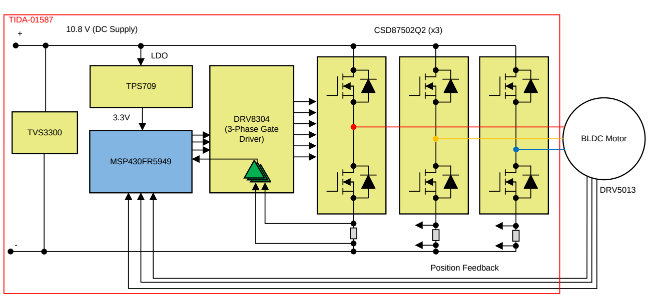
E2E™エキスパートに質問

## 特長

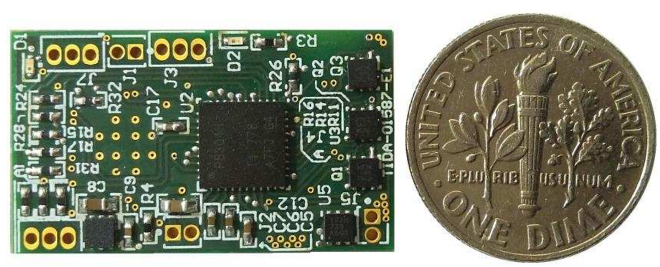
- BLDCサーボ・ドライブは6V～16.8Vの電圧範囲で動作(3～4セルのリチウムイオン・バッテリ)
- 連続2.5$A_{RMS}$、ピーク5Aのモータ巻線電流に対応
- 永久磁石モータの台形波および正弦波制御をサポート
- BLDCモータ向けデジタル・ホール・センサ・フィードバックによる閉ループ60°電気的位置制御
- アナログ・ホール・フィードバックを通じた正弦波励起による位置制御をサポート
- 16mm×27mmの超小型PCBフォーム・ファクタ
- ヒート・シンクなしで、95%を超える電力段効率
- 高効率の電力段、低消費電力のMCU、静止電流の低いLDOによりバッテリ駆動時間を延長
- 過電流、貫通電流、および低電圧保護
- UART有線通信をサポート
- 動作時周囲温度: －20℃～＋55℃

## アプリケーション

- ヒューマノイド(ヒト型ロボット)
- ロボット掃除機
- ロボット芝刈り機





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# 1 System Description

A humanoid robot is a type of service robot used in wide-end applications such as research applications where human access is risky, high-end toys used for teaching, dancing, and speaking, and more. Multiple motors are present in a typical humanoid depending upon the features and application requirement. The commonly used motors are brushed DC (BDC), brushless DC (BLDC), and sometimes stepper types. 図 1 shows the examples of motor drive locations in a typical humanoid. The high-end or high-power motors are typically present in the neck, legs, shoulders, and so on. Low-end or low-power motors are used in other locations such as elbows, knees, fingers, and so on. The electronic drive used in these motors has the following requirements:

- Must be small enough to fit with the motor
- Must support accurate position and torque control
- Must have the sufficient holding torque capability

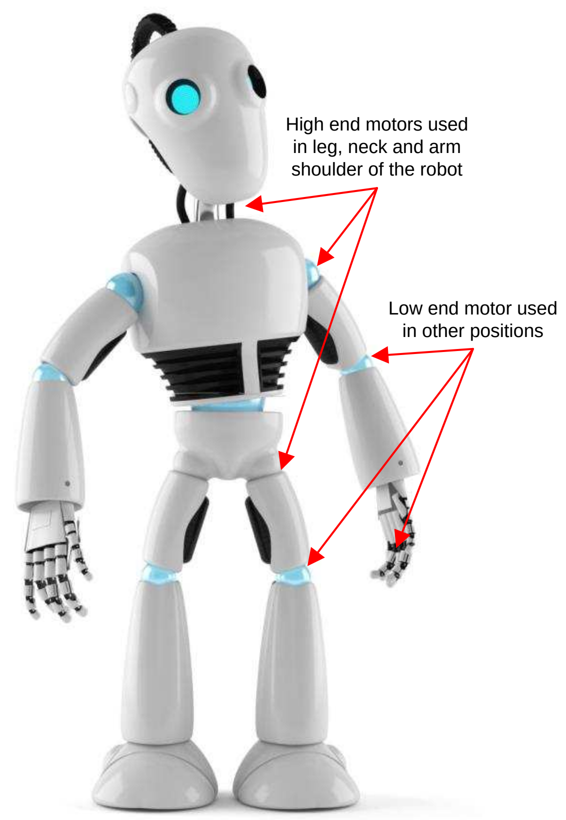


**図 1. Typical Humanoid—Motor Drive Locations**

Vacuum robots are another service robot widely used in consumer applications for cleaning. The motors used in vacuum robots have different requirements like high-speed rotation, high torque-slow speed operation, or position control depending on the functionality these motors support (for example, suction, wheel, side brush, position control of the robotic vision control motor, and so on). BDC, BLDC, or stepper motors are typically used. The electronic drives have similar requirements as said in the case of humanoids.


TIDUE42 翻訳版 — 最新の英語版資料 http://www-s.ti.com/sc/techlit/TIDUE42

This three-phase BLDC power stage reference design can support the position control in a humanoid or the motor control in a vacuum robot. The design demonstrates the BLDC motor servo drive power stage in a very small form factor using the highly-integrated three-phase gate driver DRV8304 featuring a high level of integration and protection, reducing the overall BOM to a large extend.

The very small form factor and higher efficiency is also achieved by using the CSD87502Q2 offering two independent 30-V N-channel MOSFET in a SON 2×2 mm plastic package, having a low drain-to-source on-resistance ($R_{DS(on)}$) of 27 mΩ. The TPS709 LDO features a low-quiescent current (< 1 μA) and generates the low-noise, stable, 3.3-V power supply for the MCU. The MSP430FR5949 runs the position control algorithm by taking the position feedback signals from the motor, and offers trapezoidal and sinusoidal motor control. The TVS3300 provide surge voltage protection on input voltage supply.

The test report evaluates the board power capability, efficiency, overcurrent protection, peak current capability, and the position control with sufficient hold-up torque.

## *1.1 Key System Specifications*

**表 1. Key System Specifications**

| PARAMETERS | SPECIFICATIONS |
|---|---|
| Input voltage | 10.8-V DC (6-V minimum to 16.8-V maximum) |
| Rated output power | 30 W |
| RMS winding current | 2.5 A |
| Peak winding current | 5 A |
| Inverter switching frequency | 20 kHz (adjustable from 5 kHz to 100 kHz) |
| Feedback signals | DC bus voltage, analog or digital position feedback, low-side inverter leg currents |
| Protections | Overcurrent, input undervoltage, over temperature, shoot-through |
| Cooling | Natural cooling only, no heat sink |
| Operating ambient | –20°C to +55°C |
| Board specification | 16 mm × 27 mm, 2-layer, 1-oz copper, 1.6-mm board thickness |
| Efficiency | > 95% |

# 2 System Overview

## 2.1 Block Diagram

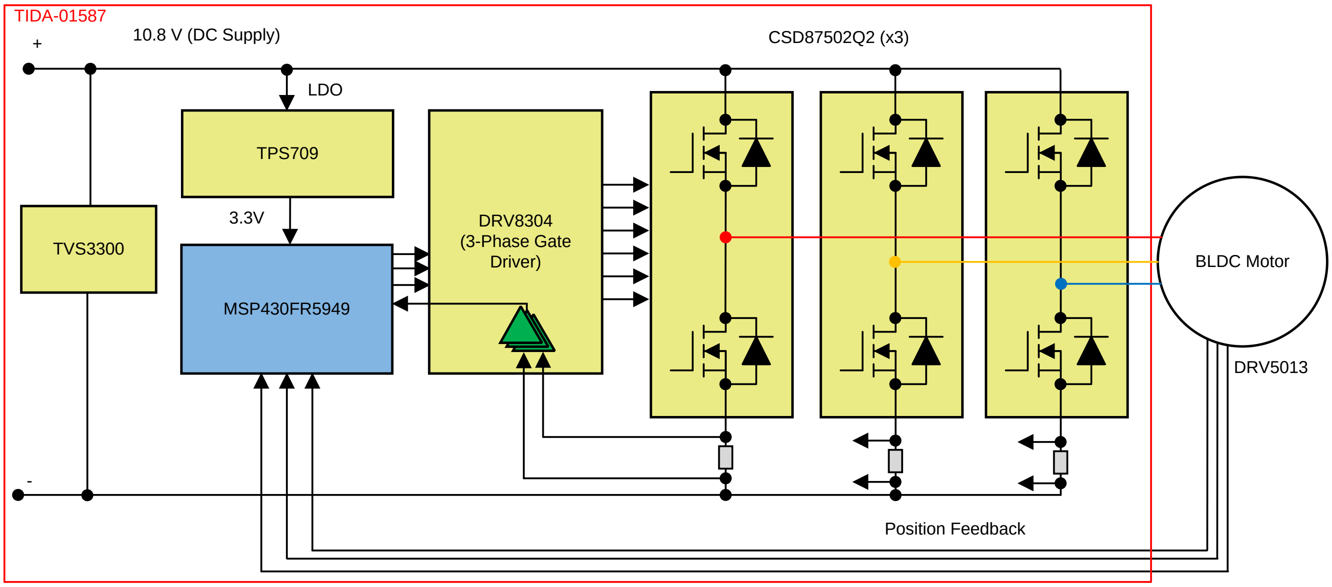




**図 2. TIDA-01587 Block Diagram**

## 2.2 Highlighted Products

### 2.2.1 DRV8304

The key requirements in selecting the gate driver are:

- Small form factor, three-phase gate driver with high level of integration and protection
- Support the operating voltage range with sufficient gate current
- Support the required minimum DC input voltage, still provides sufficient gate voltage for the external FET to operate at the minimum $R_{DS(on)}$
- Low power consumption

The reference design uses the three-phase gate driver DRV8304, which is specified for 6 V to 38 V, providing a maximum gate current of 150-mA source and 300-mA sink. The DRV8304 can support applications including field-oriented control (FOC), sinusoidal current control, and trapezoidal current control of BLDC motors. The DRV8304 device integrates three current-sense amplifiers (CSA) for sensing the phase currents of BLDC motors for optimum FOC and current-control system implementation. An AUTOCAL feature automatically calibrates the CSA offset error for accurate current sensing.

The DRV8304 device is based on smart gate-drive (SGD) architecture to eliminate the need of any external gate components (resistors and Zener diodes) while fully protecting the external FETs. The SGD architecture optimizes dead time to avoid any shoot-through conditions, provides flexibility in reducing electromagnetic interference (EMI) by gate slew-rate control and protects against any gate-short conditions. Strong pulldown current also prevent any dv/dt gate turnon. The gate driver provide overcurrent and short-circuit protection by MOSFET $V_{DS}$ monitoring.

### 2.2.2 CSD87502Q2

The key requirements in selecting the power stage MOSFETs are:

- Low $R_{DS(on)}$ and gate charge for high efficiency operation
- Small form factor
- Low thermal resistance and provision for heat dissipation to PCB

The reference design uses the CSD87502Q2, which is a 30-V, 27-mΩ N-channel device with dual independent MOSFETs in a SON 2×2-mm plastic package. The dual FETs feature a low $R_{DS(on)}$ that minimizes losses and offers low component count for space-constrained applications. The low junction-to-ambient thermal resistance with the help of thermal pads on the package allows easy heat dissipation.

### 2.2.3 MSP430FR5949

The MSP430™ ultra-low-power (ULP) FRAM platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power.

The MSP430 ULP FRAM portfolio consists of a diverse set of devices featuring FRAM, the ULP 16-bit MSP430 CPU, and intelligent peripherals targeted for various applications. The ULP architecture showcases seven low-power modes, optimized to achieve extended battery life in energy-challenged applications.

The device has a 16-bit RISC architecture supporting up to a 16-MHz clock. The device has five 16-bit timers with up to seven capture/compare registers each. The seven capture/compare registers helps to realize six PWM signals for three-phase sine control with a single time base. The device has 32-bit hardware multiplier and a 12-bit analog-to-digital converter (ADC) with internal reference and sample-and-hold and up to 16 external input channels. The enhanced serial communication allows easy communication with master controller in different service robots.

### 2.2.4 TPS709

The TPS70933 linear regulator is an ultra-low, quiescent current device designed for power-sensitive applications. The LDO can work up to a 30-V input voltage, which makes it ideal for up to six-cell Li-ion battery supply application. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes this LDO ideal for battery-powered, always-on systems that require very little idle-state power dissipation. This device has thermal-shutdown, current limit, and reverse-current protections for added safety. The TPS70933 linear regulator is available in WSON-6 and SOT-23-5 packages.

### 2.2.5 TVS3300

The TVS3300 is a transient voltage suppressor that provides robust protection for electronic circuits exposed to high transient voltage events. Unlike a traditional TVS diode, the TVS3300 precision clamp triggers at a lower breakdown voltage and regulates to maintain a flat clamping voltage throughout a transient overvoltage event. The lower clamping voltage combined with a low dynamic resistance enables a unique TVS protection solution that can lower the voltage a system is exposed during a surge event by up to 30% in unidirectional configuration and up to 20% in bidirectional configuration when compared to traditional TVS diodes.

The TVS3300 is a unidirectional precision surge protection clamp with a 33-V working voltage designed specifically to protect systems with mid-voltage rails in industrial, communication, and factory automation applications. The TVS3300 has a fast response time when surge current is applied so there is no overshoot voltage during clamping, making it ideal to replace traditional TVS and Zener diodes.

The TVS3300 is available in two small footprint packages which, when used in place of an industry standard SMB package, can reduce footprint by 94% (WCSP package) and 79% (SON package) for space constrained applications. Both package options robustly dissipate the surge power and provide up to 58% lower leakage current compared to traditional TVS diodes in SMA and SMB package.

## 2.3 System Design Theory

### 2.3.1 DC Voltage Input to the Board

The board gets the DC input voltage through the jumper J5 as shown in 図 3. The TVS3300 is a surge protection clamp provided at the input to protect the circuit from input voltage surges. The design is optimized for a three-cell Li-ion battery and can support up to four-cell applications, having a maximum voltage of 16.8 V.

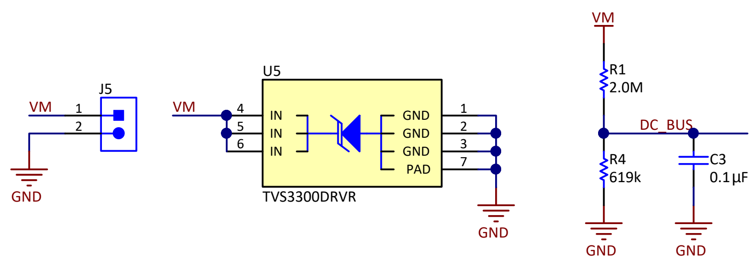




**図 3. Schematic of Battery Power Input Section**

The input supply voltage PVDD is scaled using the resistive divider network, which consists of R1, R4, and C3, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in 式 1.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(619\ \text{k}\Omega + 2000\ \text{k}\Omega)}{619\ \text{k}\Omega} = 3.3 \times \frac{(619\ \text{k}\Omega + 2000\ \text{k}\Omega)}{619\ \text{k}\Omega} = 13.96\ \text{V} \quad (1)$$

Considering a 10% headroom for this value, the maximum recommended voltage input to the system is 13.96 × 0.9 = 12.56 V. So for a power stage operating from three-cell Li-ion, having a maximum operating voltage of 12.6 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 6 V to 12.6 V.

### 2.3.2 Power Stage Design: Three-Phase Inverter

The three-phase inverter is realized using three dual MOSFET blocks CSD87502Q2, as shown in 図 4. Each CSD87502Q2 block consists of two independent 30-V, 27-mΩ N-channel MOSFETs in a SON 2×2-mm plastic package.

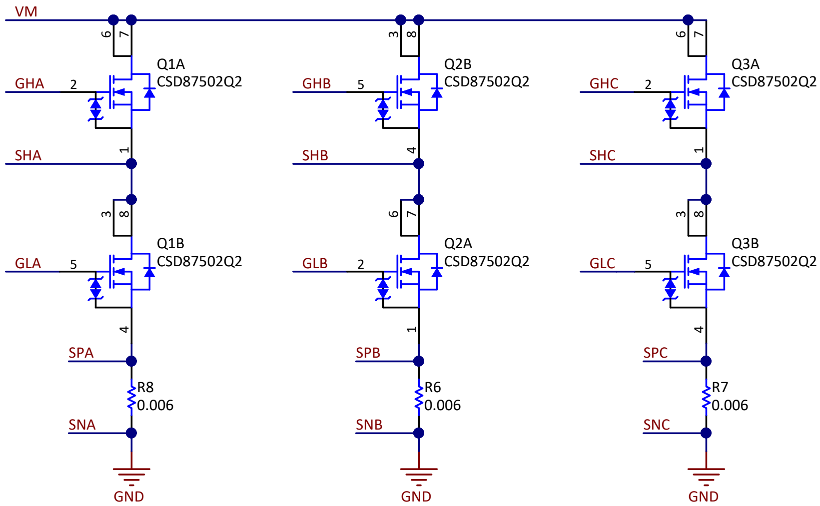




**図 4. Schematic of Three-Phase Inverter**

The resistors R6, R7, and R8 are used for inverter leg current sensing. The voltage across the sense resistor is fed to the MCU through the current shunt amplifiers in the DRV8304.

### 2.3.3 Selecting the Sense Resistor

The selection of sense resistor depends on different factors as follows:

- Power dissipation in the sense resistor
- Offset error voltage and gain of the current sense amplifier
- Peak current to be sensed

The sense resistors are designed to carry a continuous nominal RMS current of 2.5 A and a peak current of 5 A. A high sense resistance value increases the power loss in the resistors. A low sense resistor value increases the error due to input offset voltage of the current sense amplifier at high gain. If the current-sense amplifier is used without offset calibration, select the sense resistor value such that the sense voltage across the resistor is sufficiently higher than the op-amp input offset voltage to reduce the effect of the offset error. The TLV9061 has a maximum input offset error voltage of 1.5 mV. The reference design uses a 0.006-Ω sense resistor, and the power loss in sense resistor can be calculated using 式 2:

$$\text{Power loss in the resistor} = I_{RMS}{}^{2} \times R_{SENSE} = 2.5^{2} \times 0.006 = 0.0375\ \text{W} \tag{2}$$

At a 5-A peak current, using 式 2, the power loss in the resistor = 0.15 W.

### 2.3.4 Power Stage Design: Three-Phase Gate Driver

図 5 shows the schematic of the DRV8304 gate driver. C17 is the DVDD decoupling capacitor that must be placed close to DRV8304. C6 and C7 are the charge pump capacitors. These capacitors are selected to provide a stable charge pump voltage with minimum ripple. VM is the DC supply input; in this case, it is the battery voltage of 10.8 V. C1 and C4 are the bulk ceramic capacitor placed near the inverter bridge.

The gate drive circuit is designed, and the different resistors are selected to meet the specification as per 表 2.

**表 2. Design Specification of DRV8304 Gate Driver**

| PARAMETER | DEFAULT VALUE | CIRCUIT DESCRIPTION |
|---|---|---|
| MODE (PWM mode) | 6× PWM control mode | MODE pin tied to AGND |
| $I_{DRIVE}$ (gate source and sink current) | 15-mA source, 30-mA sink | IDRIVE pin tied to AGND |
| $V_{DS}$ (monitor reference voltage) | 0.15 V | VDS pin tied to AGND |
| GAIN (current sense amplifier gain) | 40 V/V | GAIN pin tied to 3.3 V (DVDD) |
| $V_{REF}$ | 3.3 V | Support bidirectional current sensing |
| CAL | Controllable through MCU | Amplifier calibration through MCU |

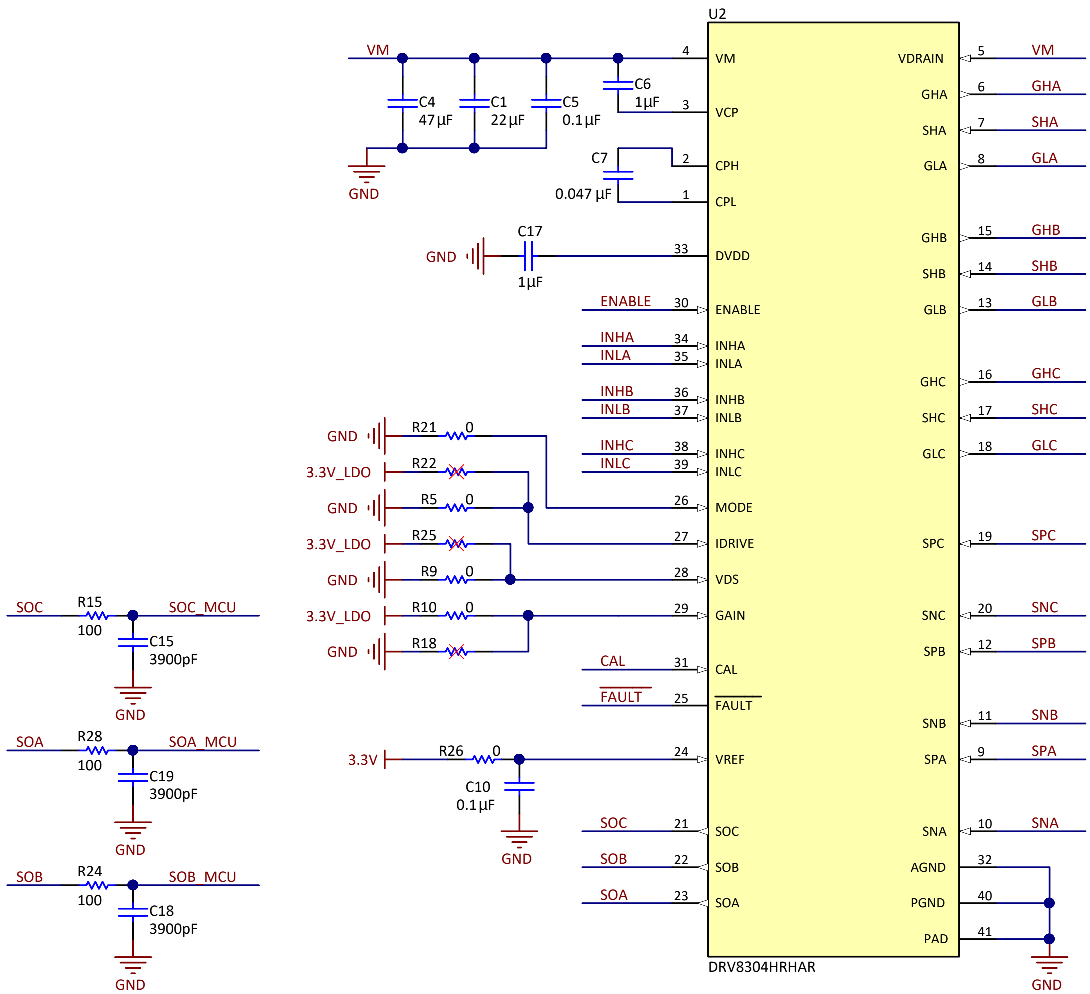

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**図 5. Schematic of DRV8304 Gate Driver**

### 2.3.5 Current Sense Amplifier

The SOx pin on the DRV8304 outputs an analog voltage equal to the voltage seen across the SPx and SNx pin multiplied by the gain setting (CSA_GAIN). The gain setting is adjustable between four different levels (5, 10, 20, and 40 V/V). The amplifier as shown in 図 6 can be used to monitor the current through the half-bridges and the current is approximately calculated using 式 3.

$$I_{SENSE} = \frac{\frac{V_{REF}}{2} - SO_X}{CSA\_GAIN \times R_{SENSE}} \quad (3)$$

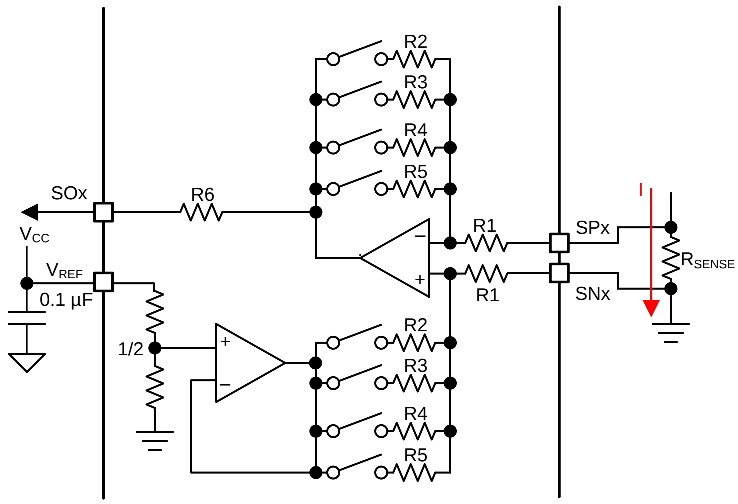


**図 6. DRV8304 Current Sense Amplifier**

The sense amplifier gains on the DRV8304 and sense resistor value are selected based on the target current range, $V_{REF}$, sense resistor power rating, and temperature. In bidirectional operation of the sense amplifier, the dynamic range at the output is approximately:

$$V_O = \left(V_{REF} - 0.25\ V\right) - \frac{V_{REF}}{2}$$

where

- $V_{REF}$ = 3.3 V (4)

The required current sense range for the reference design is from –5 A to +5 A. The DRV8304 has an SOx output linear range of 0.25 V to $V_{REF}$ – 0.25 V (from the $V_{LINEAR}$ specification). The differential range of the sense amplifier input is –0.3 V to +0.3 V ($V_{SP,DIF}$).

$$R_{SENSE} = \frac{1.4\ V}{A_V \times I_{SENSE}} \quad (5)$$

$$V_O = \left(3.3\ V - 0.25\ V\right) - \left(\frac{3.3\ V}{2}\right) = 1.4\ V$$

With $R_{SENSE}$ = 0.006 Ω and an amplifier gain of 40 V/V, using 式 5, the design allows a current sensing from –5.8 A to +5.8 A, which means 15% over rated from the required rated peak current of 5 A.

### 2.3.6 MSP430FR5949 MCU

図 7 shows the configuration of MSP430FR5949 MCU. The reference design uses 4.7-µF decoupling capacitors (C2, C12) at AVCC and DVCC pins. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency. The Timer B module of the MCU is used for PWM generation. The seven capture/compare registers helps to realize six PWM signals for three-phase sine control, with a single time base. The six PWM signals are generated at TB0.1 to TB0.6 pins. The digital Hall signals are connected to port 1 of the MCU. For an analog position signal interface, configure the pins as analog pins. The MCU is configured for sensing different analog signals like the inverter leg currents, DC bus voltage, position reference signals, and so on. The provision for UART communication is also provided.

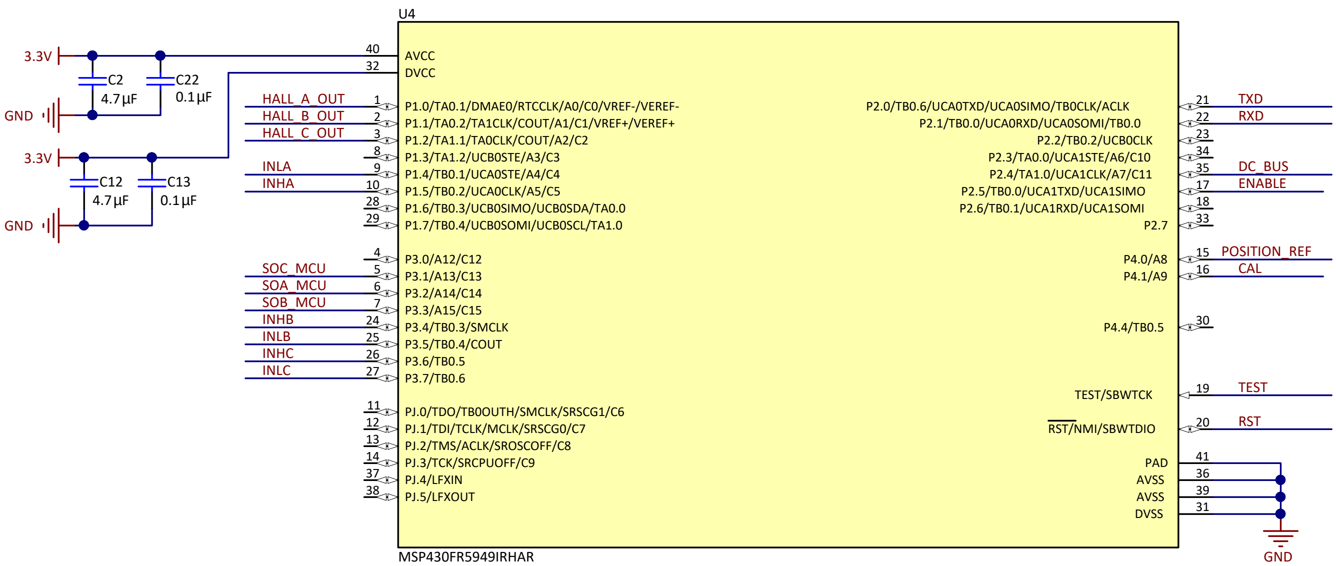




**図 7. Schematic of MSP430FR5949**

### 2.3.7 Motor Position Feedback

図 8 shows the position feedback interface from the motor to the reference design board. By default, the reference design is configured to sense digital Hall sensor output, which is connected to port 1 of MCU. The reference design can support analog position feedback also; in that case, connect the sensor output to same port pins and configure the pins as an analog input pin of the MCU ADC.

The position reference signal can be connected to J7 by connecting an external potentiometer (POT).

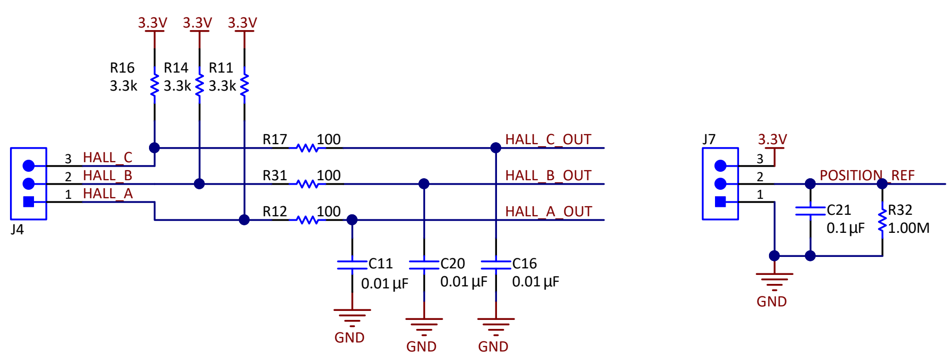




**図 8. Schematic of Position Feedback**

### 2.3.8 LDO

The reference design uses the ultra-low quiescent current, LDO linear regulator TPS70933 to generate the 3.3-V power supply for the MCU from the input voltage of 10.8 V. 図 9 shows the schematic of the LDO circuit.

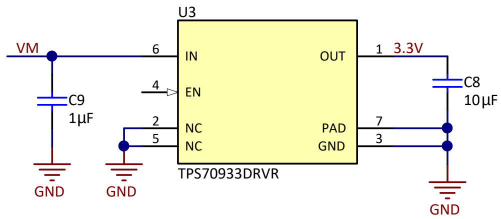




**図 9. Schematic of 3.3-V LDO**

The selection of LDO depends on the wide input voltage support (in this design, from 6 V to 16.8 V), the load current, and power dissipation. Power dissipation depends on input voltage and load conditions. Power dissipation ($P_{DISS}$) is equal to the product of the output current and the voltage drop across the output pass element, as given in 式 6.

$$P_{DISS} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \tag{6}$$

Assuming a nominal LDO load current of 20 mA, the power dissipation at $V_{IN}$ = 16.8 V can be calculated as:

$P_{DISS}$ = (16.8 – 3.3) × 0.02 = 0.27 W

表 3 shows the specifications of the LDOs used in this reference design. At lower input voltage, the power dissipation in the LDO reduces. This reference design assumes a maximum LDO output current of 30 mA when operating from a three-cell Li-ion battery.

**表 3. Specification of Buck Converter**

| PARAMETER | DESIGN SPECIFICATION |
|---|---|
| Input voltage | 6 V to 16.8 V (10.8-V nominal) |
| Output voltage | 3.3 V |
| Maximum output current | 30 mA (at 10.8-V input voltage) |

# 3 Hardware, Software, Testing Requirements, and Test Results

## 3.1 Required Hardware and Software

### 3.1.1 Hardware

#### 3.1.1.1 Connector Configuration of TIDA-01587

図 10 shows the connector configuration of this reference design, which features:

- Two-terminal input for power supply (J5): This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in 図 10.
- Three-terminal output for motor winding connection: The phase output connections for connecting to the BLDC motor winding marked as Phase A, Phase B, and Phase C as shown in 図 10.
- Three-pin connector J3: This connector is used for external UART communication interface. The RX and TX pins enable the communication with external master controller. The FAULT pin of this connector gives indication on FAULT signal from gate driver DRV8304.
- Two-pin connector J1: This is the programming connector for the MSP430FR5949 MCU, along with the 3.3-V lines at connector J2. The two-wire Spy-Bi-Wire protocol is used to program the MSP430FR5949. See the MSP430FR5949 development tools for programming options with an external JTAG interface.
- Three-pin connector J7: This connector interfaces the position reference from external potentiometer. A 20k POT can be used.
- Three-pin connector J4: This connector interfaces hall senor position signal from the motor.

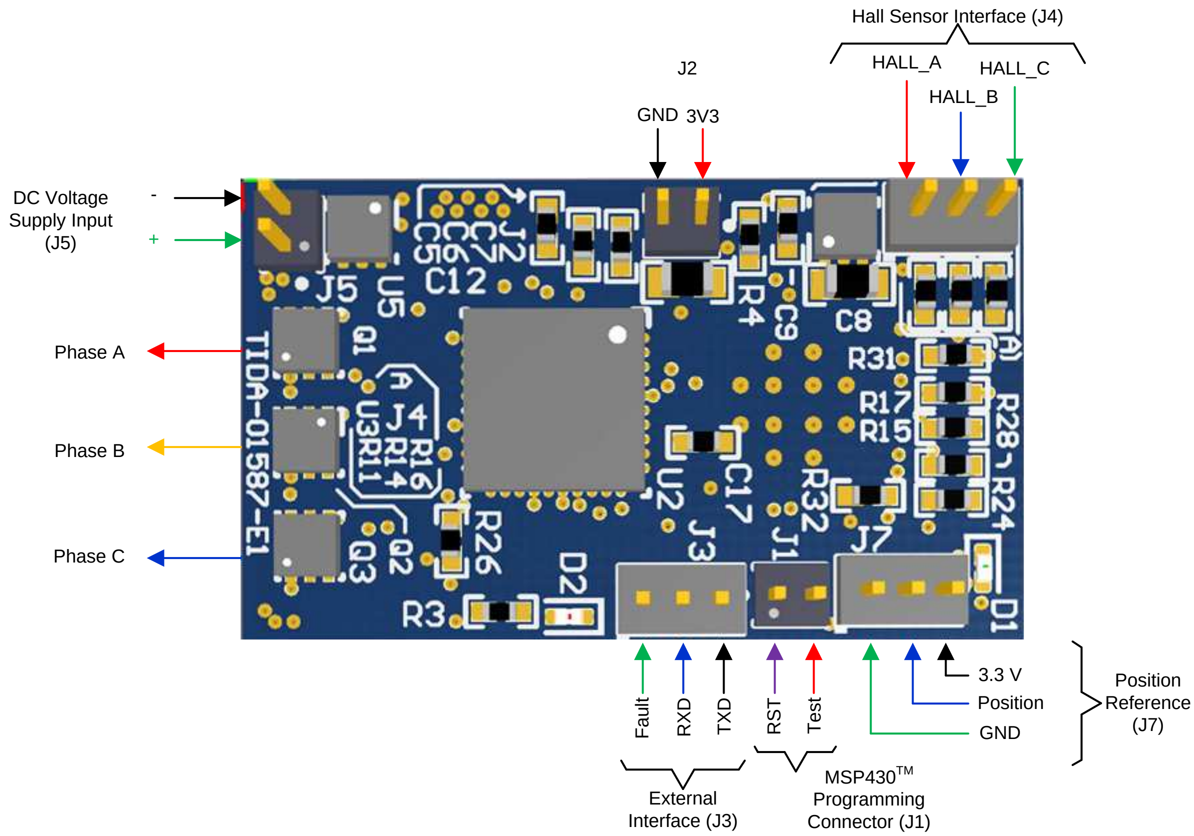


図 10. PCB Connectors

#### *3.1.1.2 Procedure for Board Bring-up and Testing*

Follow this procedure for board bring-up and testing:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of a 8-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU. Make sure that the configuration in the program is done as per 3.1.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the phase outputs from the board to the motor winding terminals.
5. Use a DC power supply with current limit protection and apply 8-V DC to the board. The motor starts rotating and stops at the position mentioned by the position reference.
6. To change direction, switch off the DC input, and correct the logic in the program and re-load the same in to the MCU.

### 3.1.2 Software

#### *3.1.2.1 High-Level Description of Application Firmware*

The reference design firmware offers the following features and user controllable parameters:

- 60° electrical position control using digital hall sensor position feedback
- BLDC motor speed control using trapezoidal control

表 4 lists the firmware system components.

**表 4. TIDA-01587 Firmware System Components**

| SYSTEM COMPONENT | DESCRIPTION |
|---|---|
| Development and emulation | Code Composer Studio™ (CCS) version 7 |
| Target controller | MSP430FR5949 |
| PWM frequency | 20-kHz PWM (default), programmable for higher and lower frequencies |
| Interrupts | Port 1 Interrupts enabled on P1.0, P1.1, and P1.2 corresponds to digital hall sensor interface |
| PWM generation—Timer configuration | PWMs: TB0.1–TB0.6 ; CLOCK = 16 MHz, PWM frequency set for 20 kHz |
| Position feedback—Hall sensor signals | P1.0 → HALL A<br>P1.1 → HALL B<br>P1.2 → HALL C |
| ADC channel assignment | A7 → DC bus voltage feedback<br>A8 → Position reference from potentiometer<br>A13 → Phase C inverter leg current<br>A14 → Phase A inverter leg current<br>A15 → Phase B inverter leg current |
| MCU digital inputs/output and communication | P2.5 → ENABLE signal for DRV8304<br>P2.0 → UART TXD<br>P2.1 → UART RXD<br>P4.1 → CAL pin of DRV8304 |

### *3.1.2.2 Customizing the Reference Code*

Select the main.c file. Parameters exist at the top of the file that can be optimized and are included as the configuration variables. The following section of code shows these parameters:

```
#define PWM_PERIOD 400 // PWM Frequency (Hz) = 16MHz / ((2*PWM_PERIOD) - 1)
#define DUTY_CYCLE 70 // Input Duty Cycle inversely relative to PWM_PERIOD
#define POLES 8     // Number of poles in motor
#define Gear_Ratio 1  // Gear ratio in the Motor
```

#### *3.1.2.2.1 PWM_PERIOD*

The PWM_PERIOD parameter sets the value in capture and compare register 0 of Timer_B0. The Timer_B0 is initialized to operate at a 16-MHz clock. Use 式 7 to calculate the PWM frequency. The TIMER_A0 PWM is configured in up-down mode.

$$\text{PWM Frequency}\left(\text{Hz}\right) = \frac{16\ \text{MHz}}{\left(\left(2 \times \text{PWM\_PERIOD}\right) - 1\right)} \tag{7}$$

For example, with PWM_PERIOD = 400, PWM frequency ≈ 20 kHz.

#### *3.1.2.2.2 DUTY_CYCLE*

Adjust this parameter to control the speed of the motor. This parameter is inversely related to PWM_PERIOD.

#### *3.1.2.2.3 POLES*

This parameter is the number of magnetic poles in the rotor of motor. The algorithm sets the 60° electrical position control using BLDC trapezoidal control, which means the resolution accuracy is 60° electrical.

The equivalent mechanical position resolution accuracy can be calculated from the number of magnetic poles in the rotor (p).

$$\text{Mechanical Angle}\left(\theta_m\right) = \frac{\text{Electrical Angle}\left(\theta_e\right)}{\left(\frac{p}{2}\right)} \tag{8}$$

For example, with p = 8, Mechanical resolution angle from motor = 15°. If the motor has a gear with 10:1 gear ratio, then:

$$\text{Equivalent mechanical position resolution} = \frac{\text{Mechanical resolution angle from motor}}{\text{Gear ratio}} = 1.5°$$

## 3.2 Testing and Results

### 3.2.1 Test Setup

The test is performed with a BLDC motor at 10.8-V DC with trapezoidal and sinusoidal control. 図 11 shows the test setup.

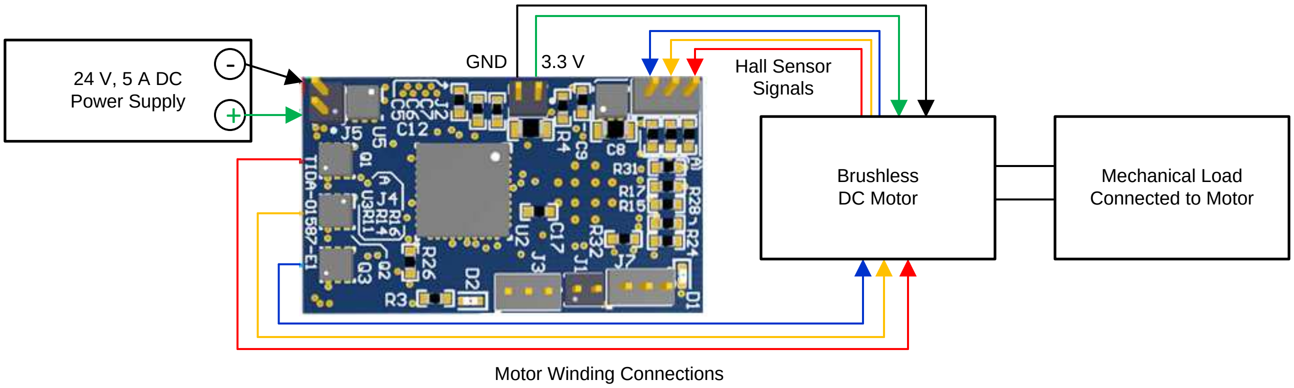




**図 11. Load Test Setup**

### 3.2.2 Test Results

#### *3.2.2.1 3.3-V Power Supply Generated by the LDO*

図 12 shows the 3.3 V generated from the LDO. The ripple in the 3.3-V rail is less than 15 mV.

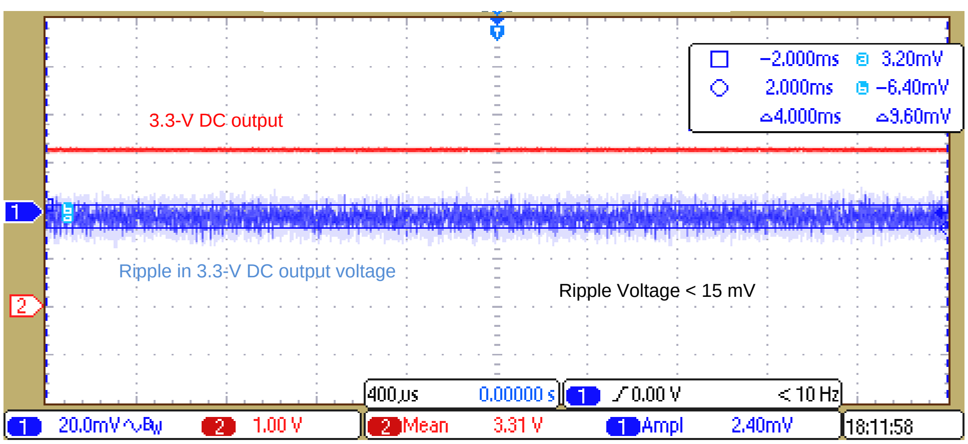


**図 12. 3.3 V Generated by TPS70933**

#### *3.2.2.2 DRV8304 Gate Driver Output Voltage*

図 13 shows the high-side and low-side gate drive output voltage of DRV8304 at a DC bus voltage of 10.8-V DC. The gate drive voltage is approximately 9.5 V, which means effective gate driving of standard MOSFETs. 図 14 shows the gate drive voltage of the DRV8304 at a lower DC bus voltage of 6 V. The gate drive output voltage is approximately 4.5 V. 図 15 shows the gate drive voltage of the DRV8304 at a higher DC bus voltage of 17 V. The gate drive output voltage is approximately 9.5 V.

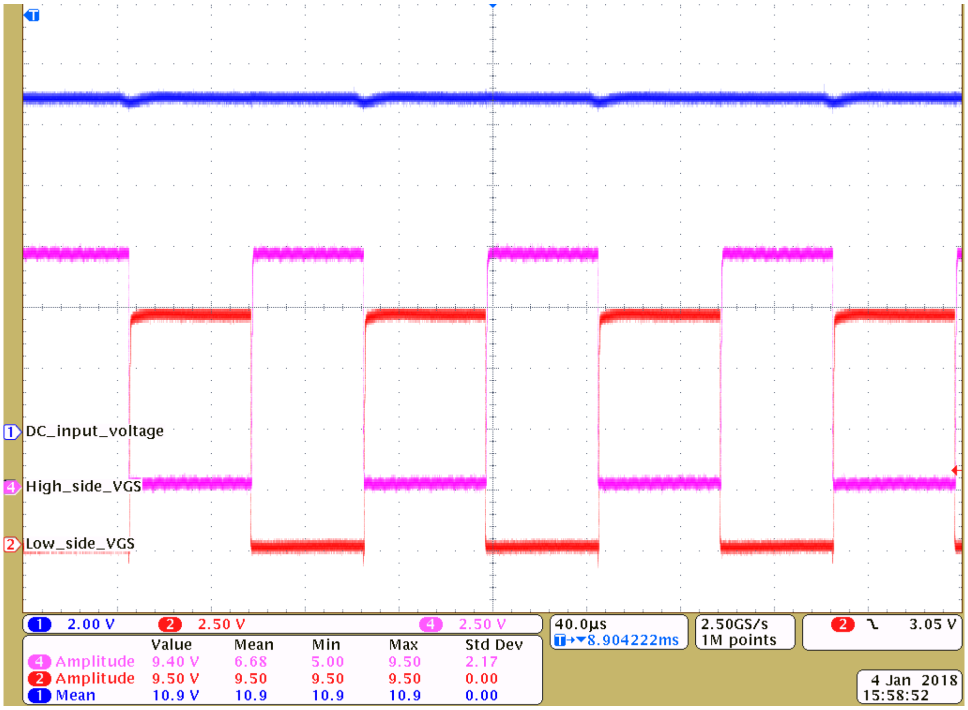


**図 13. Low-Side and High-Side Gate Drive Voltage at 10.8-V DC**


**図 14. Low-Side and High-Side Gate Drive Voltage at 6-V DC**

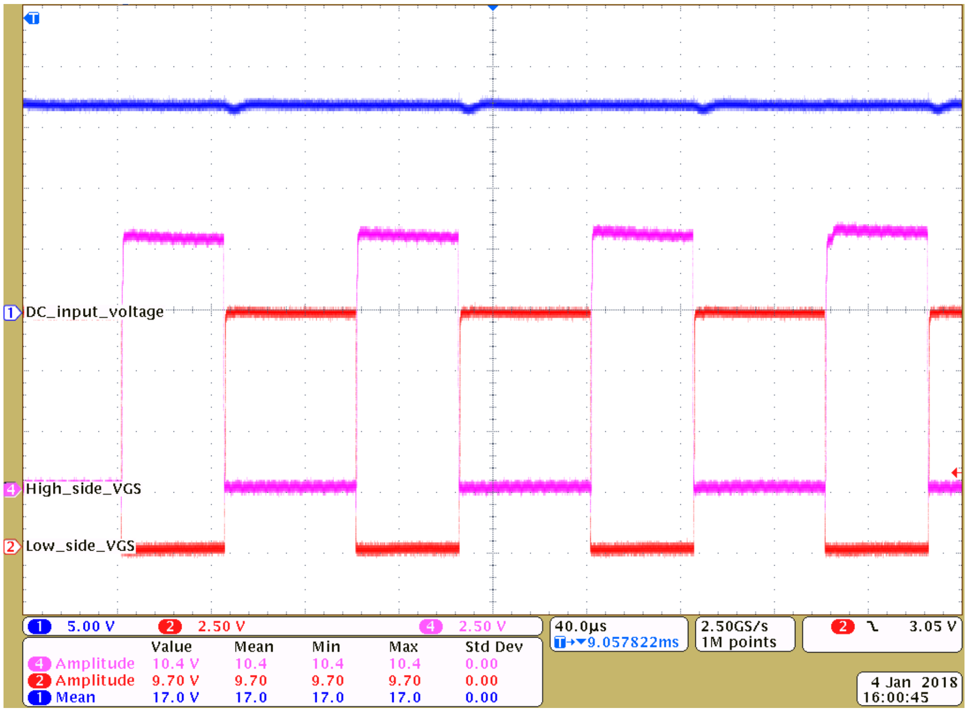


**図 15. Low-Side and High-Side Gate Drive Voltage at 17-V DC**

#### 3.2.2.3 Dead Time From DRV8304

The dead time ($t_{DEAD}$) is measured as the time between turning off one of the half bridge MOSFETs and turning on the other. The hardware version of DRV8304 inserts a fixed dead time of 120 ns. 図 16 and 図 17 shows the high-side and low-side gate source voltage from the DRV8304, which shows the dead time inserted by the DRV8304 at both the edges of the PWM.

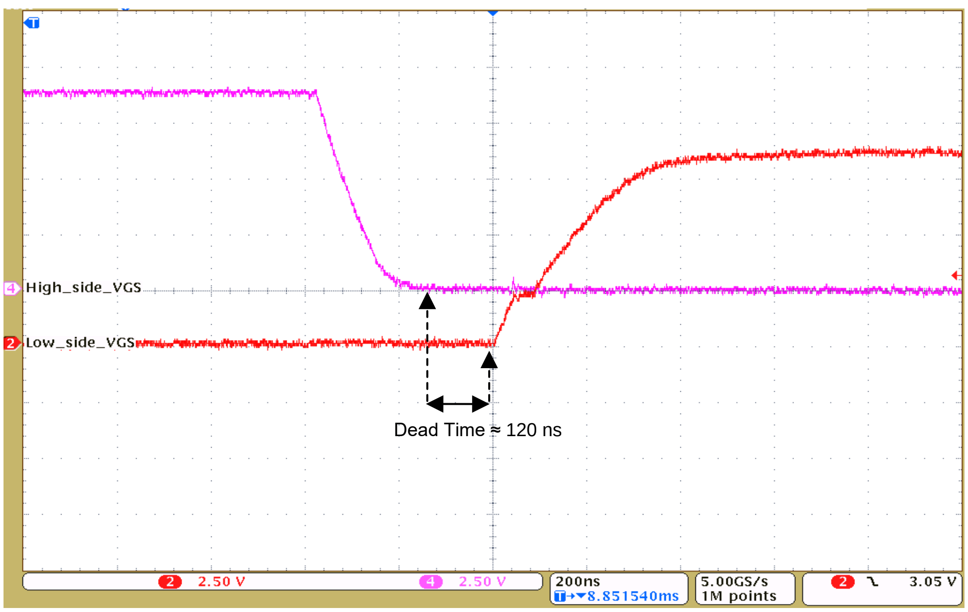


**図 16. Dead Time at Rising Edge of Low-Side $V_{GS}$**

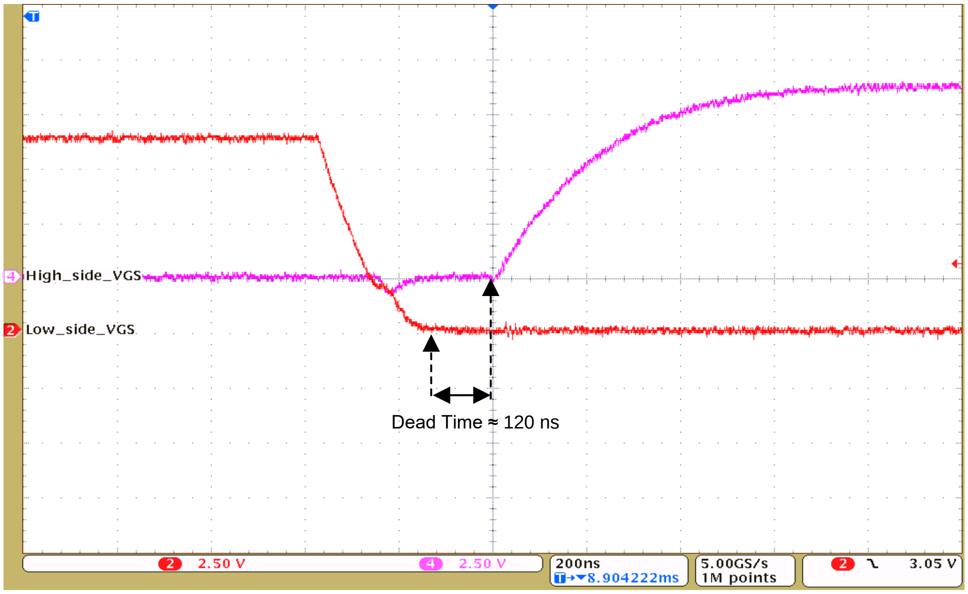


図 17. Dead Time at Trailing Edge of Low-Side $V_{GS}$

### 3.2.2.4 MOSFET Switching Waveforms

図 18 to 図 21 show the $V_{DS}$ and $V_{GS}$ waveforms of the low-side and high-side MOSFETs at a gate current of the DRV8304 ($I_{DRIVE}$) is set at a 15-mA source (the low gate charge of the CSD87502Q2 allows low source current) and a 30-mA sink current. Switching waveforms are clean without much overvoltage ringing due to the following:

- Small size CSD87502Q2 with two FETs in same package allows reduced PCB parasitic and hence reduces the phase node voltage ringing.
- The current controlled gate driver with slew rate control helps to optimize the switching.
- The $I_{DRIVE}$ and $T_{DRIVE}$ features of the gate driver helps to shape the gate current to optimize the switching.

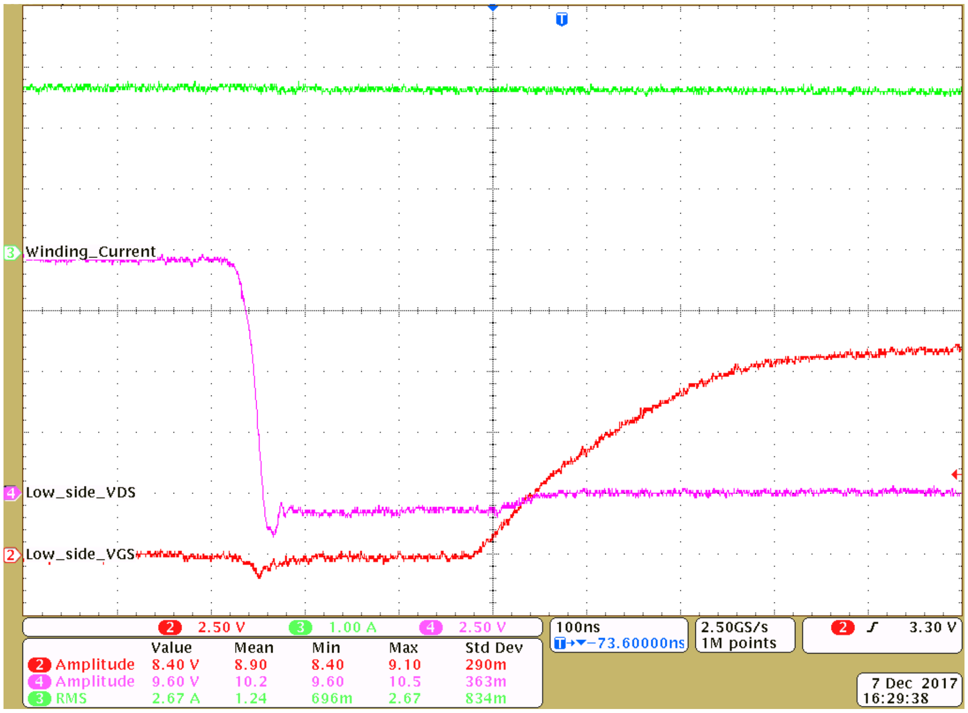


**図 18. Low-Side FET Turnon: Low-Side $V_{GS}$ and $V_{DS}$ at 2-A Winding Current**

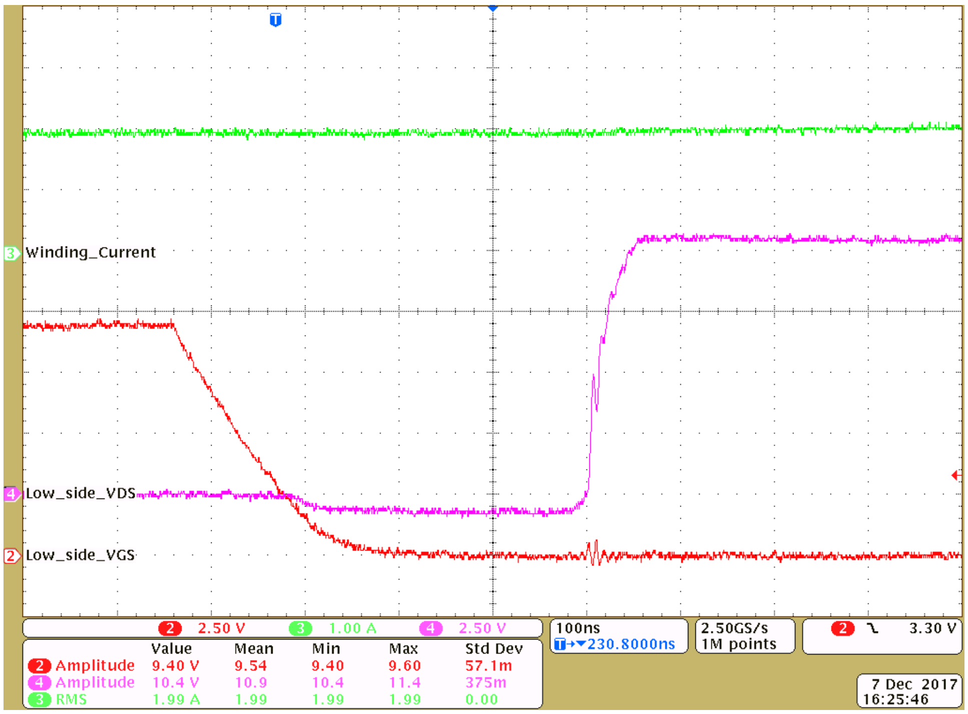


**図 19. Low-Side FET Turnoff: Low-Side $V_{GS}$ and $V_{DS}$ at 2-A Winding Current**

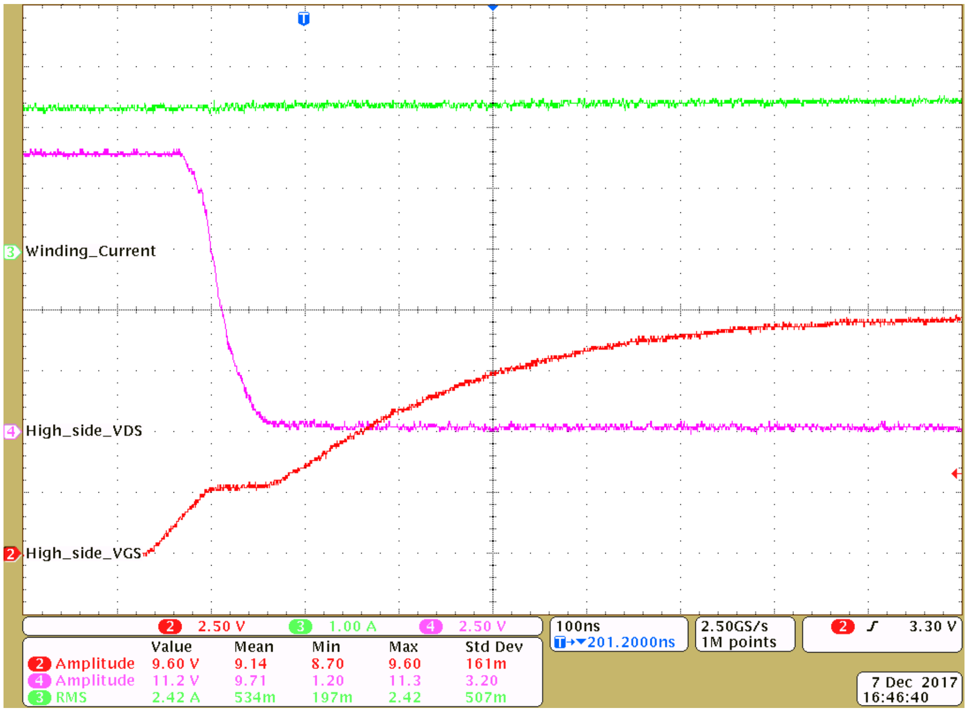


図 20. High-Side FET Turnon: High-Side $V_{GS}$ and $V_{DS}$ at 2-A Winding Current

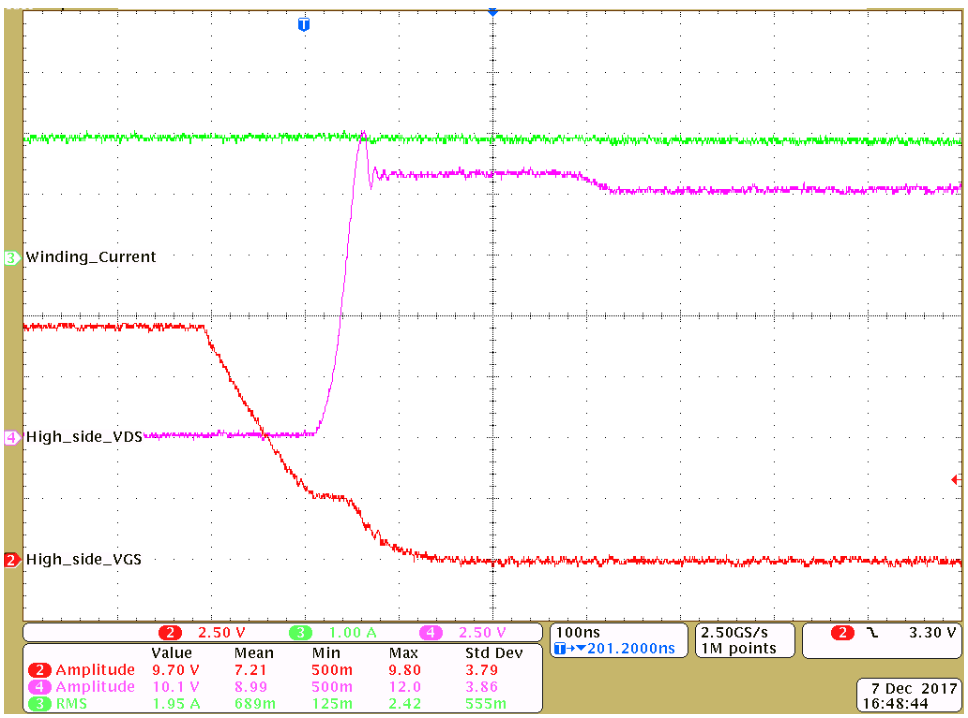


図 21. High-Side FET Turnoff: High-Side $V_{GS}$ and $V_{DS}$ at 2-A Winding Current

### *3.2.2.5 Load Test*

The load test is done with test setup as shown in 図 11. 表 5 lists the load test results. 図 22 shows the test results with trapezoidal control at 2.28-$A_{RMS}$ winding current and 100% duty cycle, and 図 23 shows the results thermal image of the board after 10 minutes of continuous running. The maximum temperature observed on the MOSFET is 81.4°C. 図 24 shows the test results with sinusoidal control at a 2.37-$A_{RMS}$ winding current, and 図 25 shows the thermal image of the board after 10 minutes of continuous running. The maximum temperature observed on the MOSFET is 85.9°C.

図 24 shows the test results with sinusoidal control at 2.5-A winding current.

**表 5. Load Test Results at 10.8-V DC**

| CONTROL METHOD | VDC (V) | IDC (A) | WINDING CURRENT (RMS) (A) | INPUT POWER (W) | MAXIMUM IC TEMPERATURE (°C) |
|---|---|---|---|---|---|
| Trapezoidal control | 10.8 | 2.70 | 2.28 | 29.16 | 81.4 |
| Sinusoidal control | 10.8 | 2.72 | 2.37 | 29.4 | 85.9 |

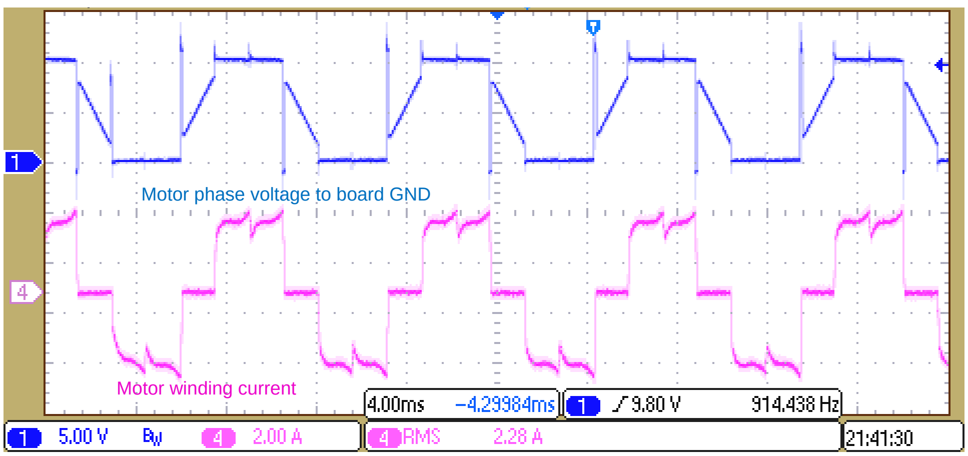


**図 22. Load Test Results With Trapezoidal Control at 2.28-$A_{RMS}$ Winding Current, 100% Duty Cycle**

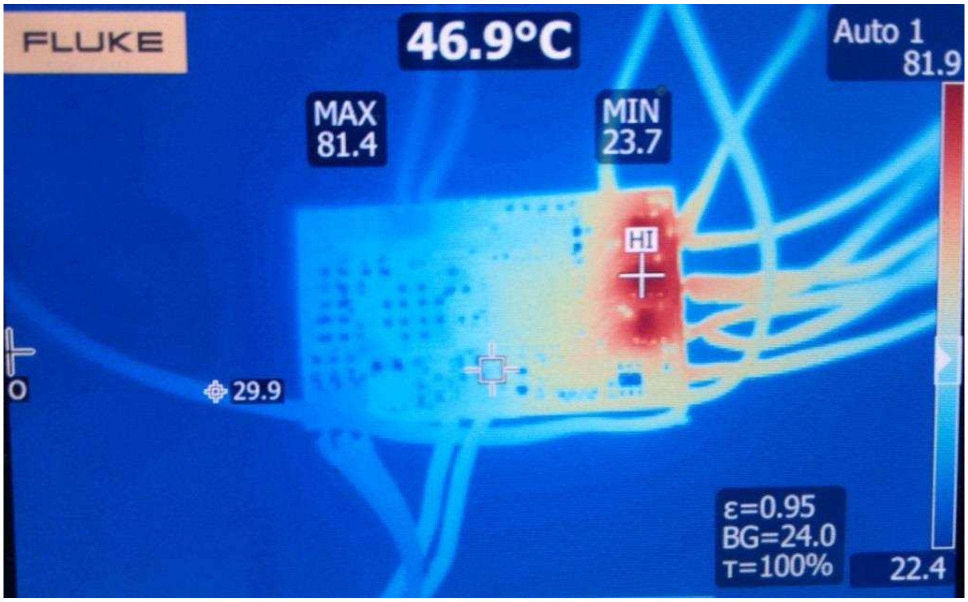


**図 23. Thermal Image of Board With Trapezoidal Control at 2.28-$A_{RMS}$ Winding Current, 100% Duty Cycle**

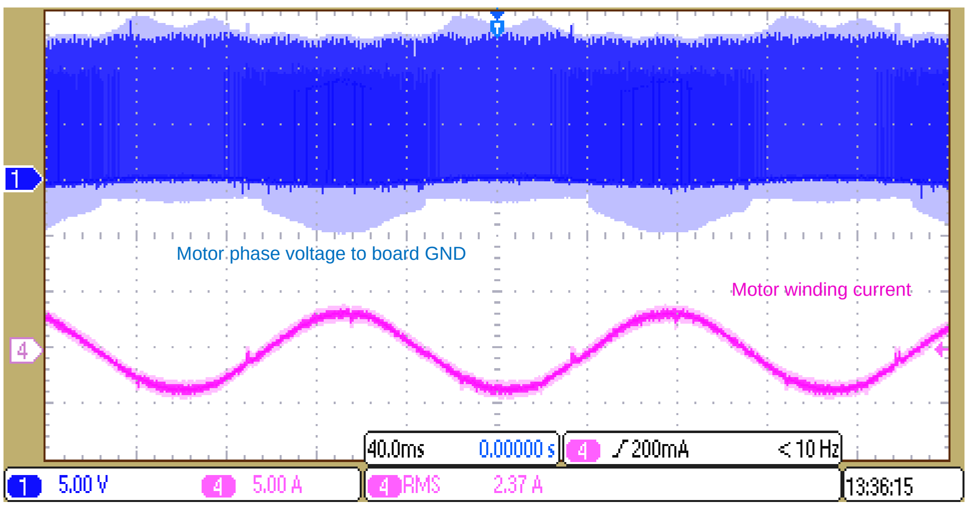


**図 24. Load Test Results With Sinusoidal Control at 2.37-$A_{RMS}$ Winding Current**

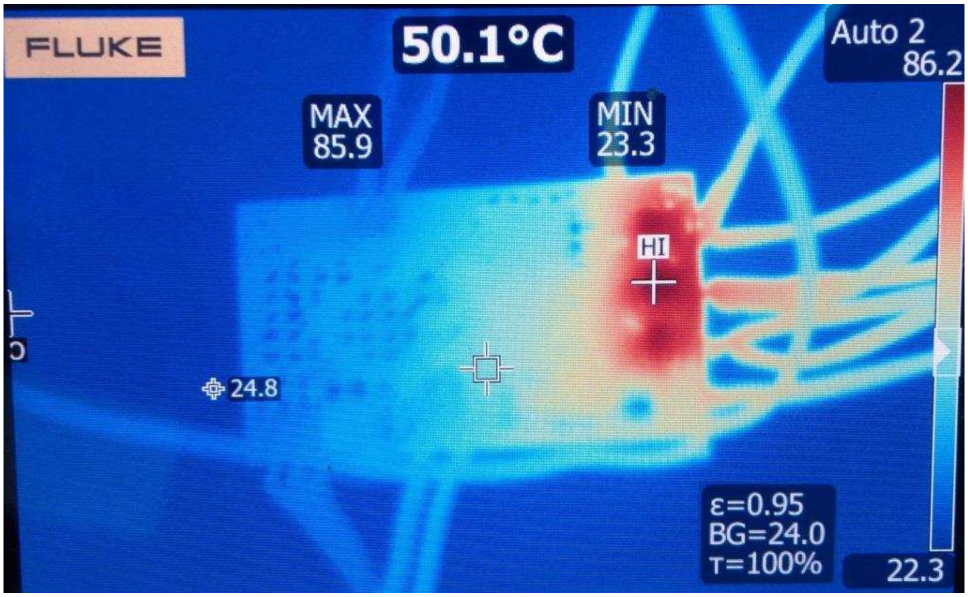


**図 25. Thermal Image of Board With Sinusoidal Control at 2.37-$A_{RMS}$ Winding Current**

#### 3.2.2.6 Power Stage Efficiency Test

The reference design board power stage efficiency is experimentally tested with a test setup as shown in 図 11. 表 6 lists the test results without heat sink at a 100% duty cycle. 表 7 lists the test results without heat sink at a 95% duty cycle.

**表 6. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and Without Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | INPUT DC POWER (W) | MOTOR WINDING RMS CURRENT (A) | BOARD OUTPUT POWER (W) | EFFICIENCY (%) |
|---|---|---|---|---|---|
| 10.63 | 0.859 | 9.13 | 0.792 | 8.93 | 97.73 |
| 10.81 | 1.031 | 11.15 | 0.932 | 10.89 | 97.66 |
| 10.78 | 1.207 | 13.02 | 1.074 | 12.70 | 97.56 |
| 10.75 | 1.411 | 15.17 | 1.239 | 14.78 | 97.44 |
| 10.91 | 1.678 | 18.31 | 1.460 | 17.79 | 97.13 |
| 10.87 | 1.965 | 21.35 | 1.698 | 20.65 | 96.73 |
| 10.80 | 2.378 | 25.67 | 2.039 | 24.70 | 96.21 |
| 10.73 | 2.785 | 29.87 | 2.362 | 28.62 | 95.80 |
| 10.69 | 2.989 | 31.95 | 2.507 | 30.51 | 95.51 |

**表 7. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow**

| INPUT DC VOLTAGE (V) | INPUT DC CURRENT (A) | INPUT DC POWER (W) | MOTOR WINDING RMS CURRENT (A) | BOARD OUTPUT POWER (W) | EFFICIENCY (%) |
|---|---|---|---|---|---|
| 10.91 | 0.667 | 7.27 | 0.661 | 7.02 | 96.47 |
| 10.87 | 0.886 | 9.63 | 0.845 | 9.28 | 96.41 |
| 10.83 | 1.156 | 12.52 | 1.070 | 12.03 | 96.13 |
| 10.78 | 1.448 | 15.61 | 1.325 | 14.96 | 95.85 |
| 10.90 | 1.813 | 19.76 | 1.634 | 18.85 | 95.36 |
| 10.81 | 2.191 | 23.69 | 1.959 | 22.48 | 94.88 |
| 10.77 | 2.490 | 26.81 | 2.215 | 25.35 | 94.53 |
| 10.69 | 3.002 | 32.10 | 2.657 | 30.21 | 94.12 |

図 26 shows the efficiency curve of these test conditions.

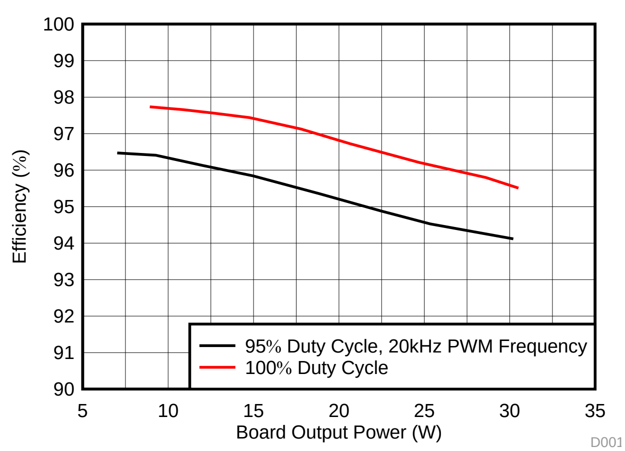


**図 26. Power Stage Efficiency versus Output Power**

The low $R_{DS(on)}$ of the CSD87502Q2 MOSFET power blocks along with clean MOSFET switching by the DRV8304 smart gate driver enable maximum three-phase inverter efficiency. The thermal pads on the MOSFET power blocks help to extract the heat to the PCB.

#### 3.2.2.7 Overcurrent Limit Results

The gate driver DRV8304 implement adjustable $V_{DS}$ monitors to detect overcurrent or short conditions on the external MOSFETs. The high-side $V_{DS}$ monitors measure the voltage between the VDRAIN and SHX pins. In configuration with three current shunt amplifiers, the low-side $V_{DS}$ monitors measure the voltage between the SHX and SPX pins.

When the voltage monitored is greater than the $V_{DS}$ trip point ($V_{DS,OCP}$) after the $V_{DS}$ deglitch time ($t_{DS,OCP}$) has expired, the DRV8304 detects an OCP condition and takes action according to the fault setting. In the hardware version of the DRV8304, the $V_{DS}$ monitor acts in automatic retry mode with a 4-ms retry time.

図 27 shows the $V_{DS}$ overcurrent action with the $V_{DS}$ reference voltage set to 0.15 V.

Assuming the junction temperature of 75°C, the $R_{DS(on)}$ at 75°C ≈ 34 mΩ (approximately 1.26 times the $R_{DS(on)}$ at 25°C, from the CSD87502Q2 data sheet).

where:

- $V_{DS}$ deglitch time ($t_{DS,OCP}$) = 4.5 µs
- Current limit threshold = $V_{DS}$ threshold / $R_{DS(on)}$ = 4.41 A

図 27 shows that the current is limited at 4.6 A. 図 28 shows the zoomed view where the PWM shuts off when the current hits the over current threshold and the fault is created. The fault resets after 4 ms.

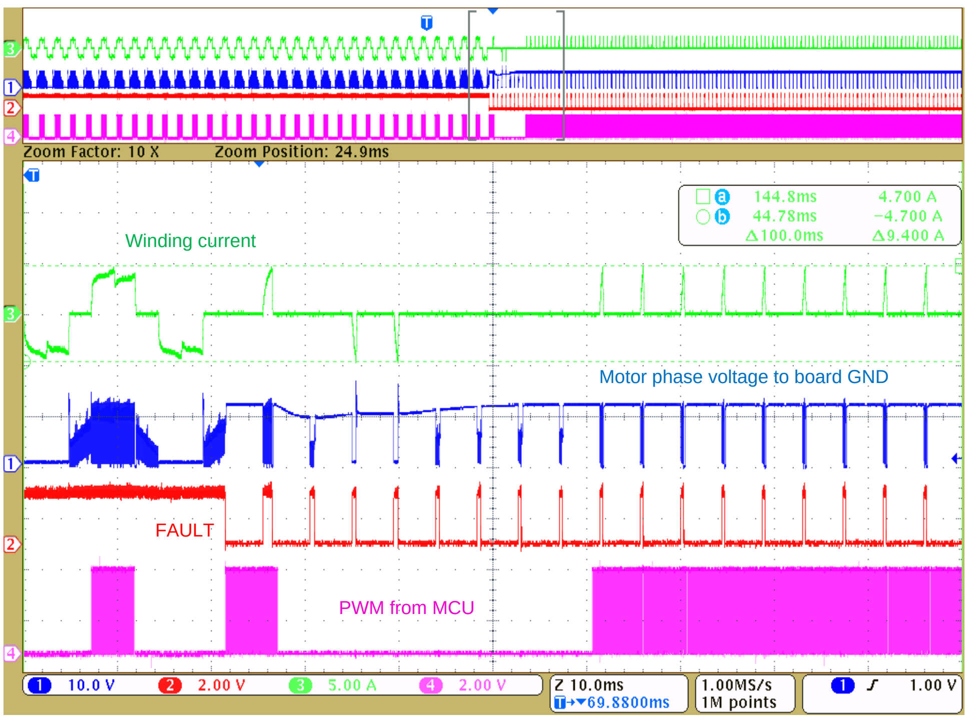


**図 27. Overcurrent Protection With MOSFET $V_{DS}$ Monitoring**

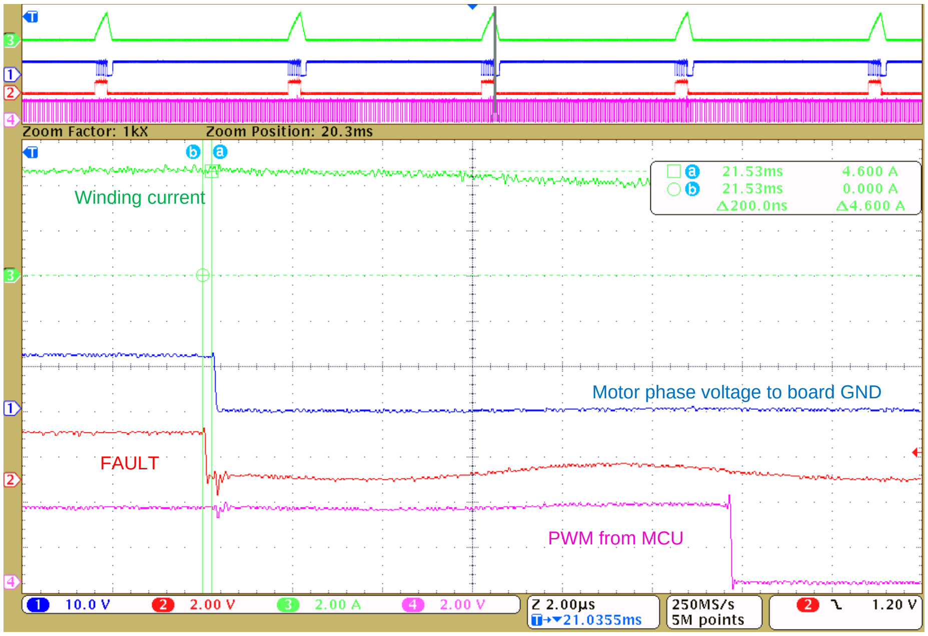


**図 28. Zoomed View of Overcurrent Protection With MOSFET $V_{DS}$ Monitoring**

### *3.2.2.8 BLDC Motor 60° Electrical Position Control With Trapezoidal Excitation*

Position control algorithm on the MSP430FR5949 is implemented using port interrupts capability of the MSP430 MCU. The testing is done on the BLDC motor that has three digital Hall position sensors.

図 29 and 図 30 show the position control test results with a BLDC motor having four pole pairs and no gear assembly. 図 29 shows the position control at 105° mechanical (420° electrical) with a holding torque equivalent to 2 A.

図 30 shows the test result with step change in mechanical position reference from 37.5° mechanical to 82.5° mechanical with a 1.5-A holding current.

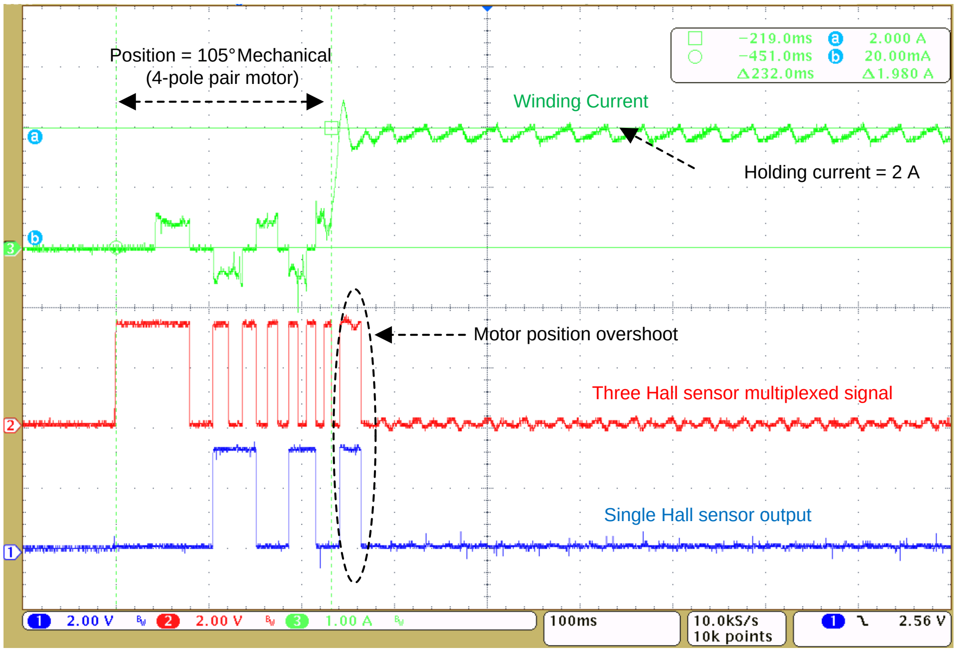


**図 29. Test Results for Position Control at 105° Mechanical**

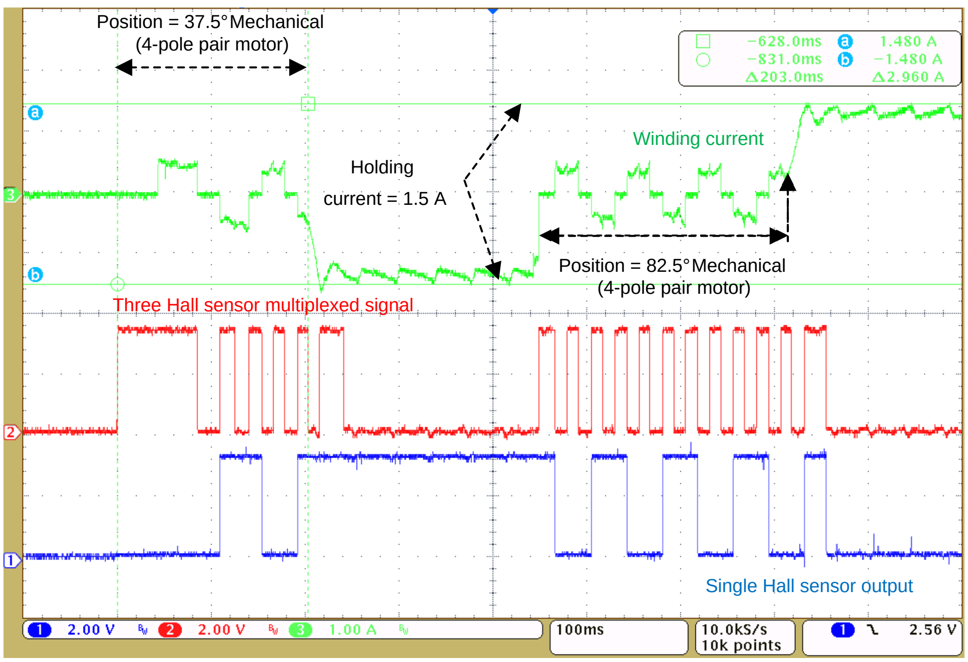


**図 30. Test Results for Position Control With a Step Change in Position Reference**

# 4 Design Files

## 4.1 Schematics

To download the schematics, see the design files at TIDA-01587.

## 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01587.

## 4.3 PCB Layout Recommendations

### 4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01587.

## 4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01587.

## 4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01587.

## 4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01587.

# 5 Software Files

To download the software files, see the design files at TIDA-01587.

# 6 Related Documentation

1. Texas Instruments, *Field Oriented Control (FOC) Made Easy for Brushless DC (BLDC) Motors Using TI Smart Gate Drivers Application Brief*
2. Texas Instruments, *DRV8304 38-V 3-Phase Smart Gate Driver Data Sheet*

## 6.1 商標

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# 7 Terminology

**BLDC—** Brushless DC

**ESD—** Electrostatic discharge

**MCU—** Microcontroller unit

**PWM—** Pulse width modulation

## 8 About the Authors

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