参考資料

デザイン・ガイド: TIDA-01505
回生ブレーキのテストをサポートする車載用 40V～1kV 入力フライバックのリファレンス・デザイン

概要

この車載補助回路用電源のリファレンス・デザインは、40V～1kVの広い入力電圧範囲から15V、4Aの出力を生成し、最大1.2kVの過渡電圧に対処できます。800Vバッテリ駆動ハイブリッド自動車(HEV)/電気自動車(EV)のトラクション・インバータ・システムに最適であり、最小入力電圧が40Vであることから、トラクション・モータの回生制動機能安全性試験にも対応しています。このリファレンス・デザインは、阻止電圧が高くゲート電荷が低い炭化ケイ素(SiC) MOSFETを実装しているため、スイッチング損失を低減できます。非絶縁型のレベル・シフタにより、フライバック・コントローラに組み込まれたSi MOSFETドライバからSiC MOSFETを駆動できます。基板には1次側レギュレーション(PSR)とフォトカプラ・フィードバックという2種類のフライバック・コンバータが搭載されているため、比較してさまざまなニーズに対応できます。トランスのデザインは強化絶縁型であり、車載用のAEC-Q200 Grade 1の認定に対応しています。

リソース

TIDA-01505	デザイン・フォルダ
UCC28C43-Q1	プロダクト・フォルダ
TL431-Q1	プロダクト・フォルダ

TI E2E™ Community

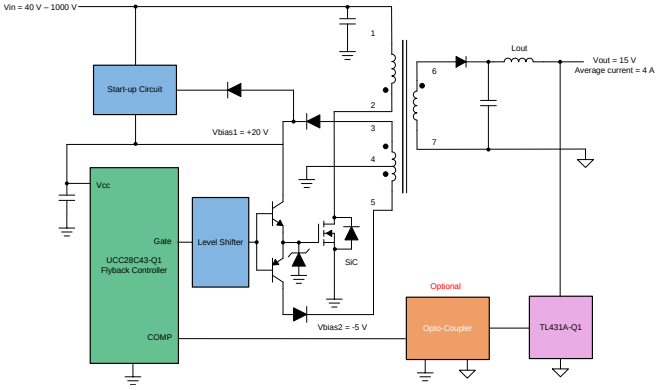
E2E™エキスパートに質問

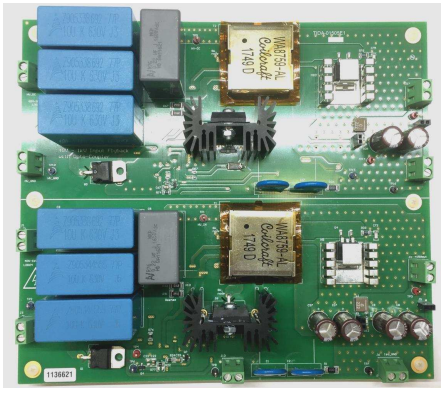
特長

- 40V～1kV 入力、15V 出力のフライバック補助電源として、最大 60W の電力を出力
- アクティブ・スタートアップ回路を使用してレギュレーション済みの 15V を供給し、スタンバイ消費電力を低減
- SiC MOSFET の高電圧対応能力を活用するために、より高い電圧/電力範囲に拡張可能
- 強化絶縁型で車載用グレード 1 認定済みのトランス (5.7kV High-Pot 試験により認定済み)
- PSR とフォトカプラ・フィードバックに対応した 2 種類のコンバータ派生製品を基板に搭載
- スイッチング周波数固定型のコントローラで、最大スイッチング周波数は 1MHz、デューティ・サイクルは 0%～96% の範囲

アプリケーション

- HEV/EV のトラクション・インバータ
- HEV/EV のオンボード充電器
- 電子制御ユニット
- HEV/EV の DC/DC コンバータ





1 System Description

At the time of this writing, the latest electric cars are experiencing dramatic technological changes in the power electronics area. The move toward 800-V technology has shown significant development among various car manufacturers. In infrastructure, raising the voltage to 800 will enable significantly reduced charging times and extend drive mileage. These developments also raise many design challenges, such as high-voltage safety and reliability, isolation requirements, trade-offs between cost and performance, and so forth.

This reference design is a 60-W power supply which enables an ultra-wide input range from a 40-V (minimum) to 1-kV (maximum) DC voltage targeted for use in 800-V battery systems. A primary feature of this design is that the converter can power up at the 40-V minimum input voltage, which allows support for the system safety test during the regenerative braking for traction inverters. This design is an auxiliary power supply solution that generates a 15-V output for the traction inverter subsystems. The design also implements reinforced isolation for safety enhancement. The single-ended, flyback topology has been chosen due to its low cost, high isolation rating, and design simplicity. Moreover, the design includes two onboard converter variants, with optocoupler and primary side regulation (PSR) for performance comparisons.

Carefully consider the following criteria to fulfill the design requirements:

- Voltage blocking capability of the switching device –

  Because of the high voltage, the Si MOSFET, which has a lower design margin for blocking voltage and high channel resistance, is not suitable. The design requires use of an SiC MOSFET with a higher blocking capability.
- Pulse-width modulated (PWM) switching duty cycle –

  Support for such an ultra-wide input voltage range requires a controller that is able to operate within the corresponding, wide PWM duty-cycle range.
- Active start-up circuit –

  The traditional, resistive start-up circuit causes high quiescent losses at high input voltage. This design implements an active start-up circuit for reduced leakage current.
- Noise coupling –

  The high-voltage input and fast switching of the SiC MOSFET leads to high dv/dt switching nodes, which generates a large amount of noise and antenna loops. The essential switching nodes must be kept small and away from quiet areas to reduce the noise coupling.
- Safety clearance –

  The distance between the high-voltage area at the primary side and low-voltage area at the secondary side must have enough clearance to comply with safety requirements. Reinforced isolations are normally imposed according to automotive safety requirements. The ground of the low-voltage side may be connected to a 12-V battery or vehicle chassis, which is touchable by the human body.
- Printed-circuit board (PCB) clearance and high-voltage components selection –

  The PCB clearance must be carefully designed to avoid electrical breakdown failure. Carefully select components that tolerate high voltages to properly handle the high-voltage stress.

図 1 shows a block diagram example of the 800-V battery-driven traction inverter system, which highlights the inverter stage, isolation, resolver, safety logics, current and voltage sensing. and so forth. This reference design is capable of powering up from a 40-V minimum input voltage for the purpose of enabling engineers to work safely and allow them to test the regenerative braking mechanism. Regenerative braking utilizes the same insulated-gate bipolar transistor (IGBT)-based traction inverter to force the power flow in the reverse direction from the motor and send the power back to the battery. The IGBTs are controlled in a different algorithm to regulate the DC output from AC. Regenerative braking technology funnels the energy created by the braking process back into the system in the form of charging the battery for further use. Typically, in a regenerative braking system, the energy loss from the braking process transfers to the generator from the rotating axel before transferring to the battery, thus saving energy.

Another TI Design, TIDA-01179, serves as the redundant supply, which is connected from the 12-V battery input to the TIDA-01505 output rail. As 図 1 shows, the isolated DC/DC (TIDA-01505) and the non-isolated DC/DC (TIDA-01179) are connected in an Oring configuration and provide the power to the downstream loads together. The TIDA-01179 includes a buck-boost converter and a buck converter. This device is a 30-W front-end power supply and supports the cold crank operations for the 12-V car battery. The device generates various power rails across the isolation barrier and supplies them to the circuits located at the high-voltage side.

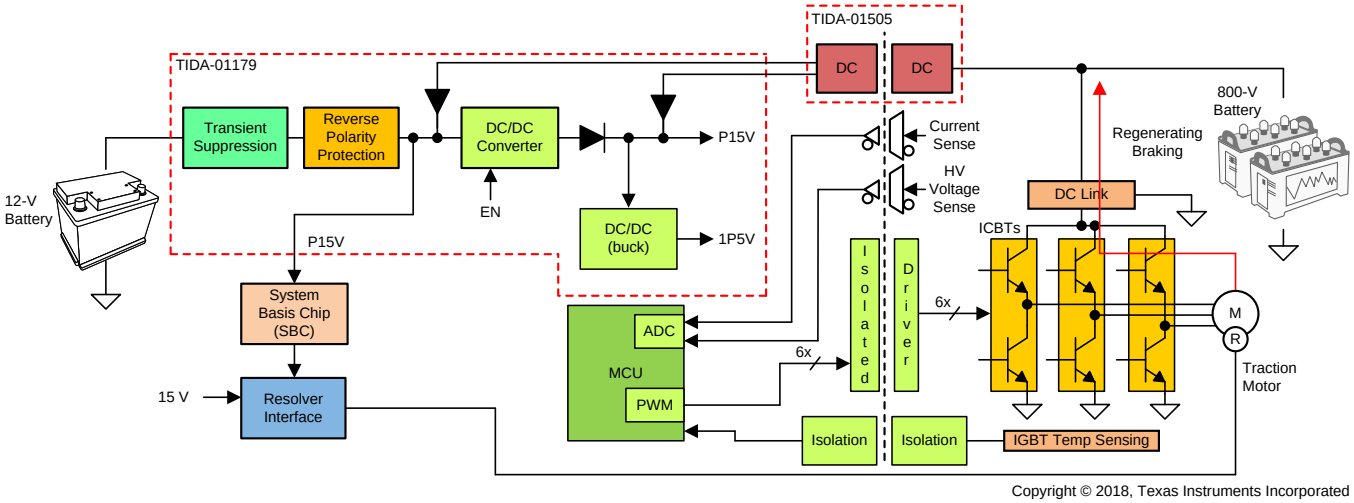


図 1. Block Diagram for 800-V Battery-Driven Inverter System and Implementation of TIDA-01505

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input	• 40-V to 1-kV ultra-wide input • 1.2-kV transient

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS
Output	• 15-V DC V_{OUT}, 4-A I_{OUT} DC continuous • 2-A maximum I_{OUT} for the variant of PSR at 40-V input, due to regulation degradation • Full power delivery starting from 100-V input voltage • Output power of 65 W max due to thermal constraints • Peak efficiency greater than 85% • Ripple less than 3% V_{OUT} at full load • Load step 50% to 100% with voltage deviation of less than 15% for the PSR flyback; voltage deviation of less than 5% for the flyback with optocoupler
Features	• Constant switching frequency type of controller operates at duty cycle range from 15% to 85% • SiC MOSFET application uses controller with Si MOSFET-integrated driver • Key components temperature rise: 40℃ maximum • Two design variants with comparable layout design • Automotive Grade 1-qualified transformer with reinforced isolation (tested at 5.7-kV high-pot test)

2 System Overview

2.1 Block Diagram

図 2 shows the system block diagram. The design consists of four main functional elements:

- The active start-up circuit replaces the pure, high MΩ resistors circuit to ensure fewer instances of power loss and a faster start-up time.
- The flyback controller operates at an ultra-wide duty cycle switching and drives the SiC MOSFET. Other benefits include a low part court and a single magnetic transformer for buck-boost conversion.
- The non-isolated level shifter converts the PWM switching signal from the integrated Si MOSFET driver to that of the SiC MOSFET. The requested driving voltages are +20 V and –5 V for turnon and turnoff, respectively.
- The optocoupler is optional in this design. The device closes the feedback loop and provides better regulation performance. This reference design includes two converter versions for the purposes of customer evaluation: one with an optocoupler and another with primary side regulation (PSR).

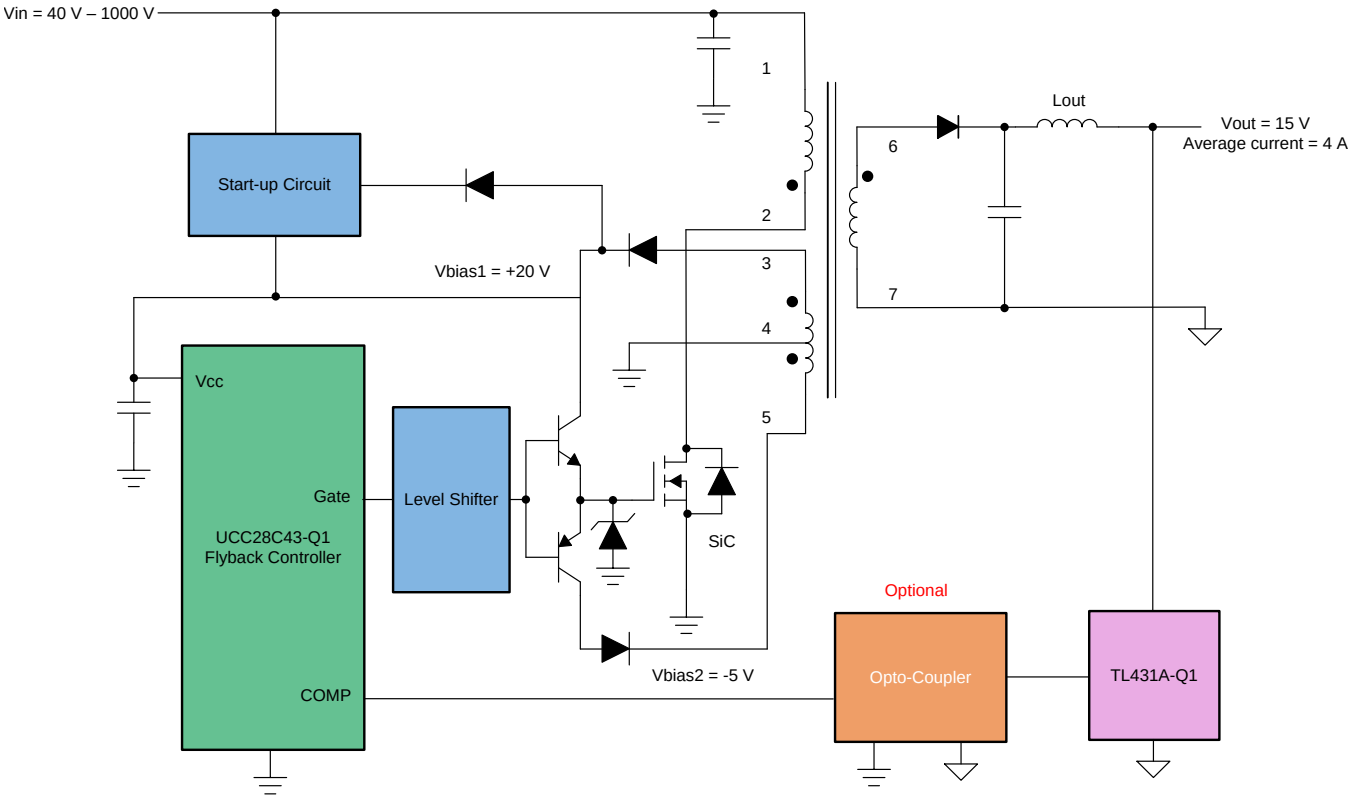


図 2. TIDA-01505 Block diagram

2.2 Highlighted Products

2.2.1 UCC28C43-Q1

The UCC28C43-Q1 is a high-performance, current-mode PWM controller. The BiCMOS design allows operation at high frequencies of at least 1 MHz that are not feasible in the predecessor bipolar devices. The low start-up current of 60 µA (typical) reduces the steady-state power dissipation in the start-up resistors and boosts the efficiency in battery-operated supplies. The BiCMOS internal reference of 2.5 V has an enhanced design and utilizes production trim to allow initial accuracy of ±1% at room temperature and ±2% over the full temperature range.

2.2.2 UCC28C42-Q1

The UCC28C42-Q1 is recommended as an alternative solution for the UCC28C43-Q1 due to the wider undervoltage lockout (UVLO) thresholds and higher turn-off voltage rating. The UCC28C42-Q1 belongs to the same device family of the UCC28C4x-Q1 as high-performance, current-mode PWM controllers. The 14.5-V turn-on and 9-V turn-off thresholds allow for more headroom on the VDD voltage before triggering UVLO which provides longer soft start times and requires less capacitance on the VDD pin. The 9-V turn-off also provides increased reliability of the SiC MOSFET over its lifetime. Drive voltages less than 8 V can cause the power device to operate in the saturation region, resulting in high conduction losses and heating.

The UCC28C4x-Q1 family devices implement AC-DC or DC-to-DC fixed-frequency current-mode control schemes with a minimum number of external components. Protection circuitry includes UVLO and current limiting. The oscillator contains a trimmed discharge current that enables accurate programming of the maximum duty cycle and dead time limit, making this device suitable for high-speed applications. Major differences between members of this series are the UVLO thresholds, acceptable ambient temperature range, and maximum duty cycle.

2.2.3 TL431A-Q1

The TL431-Q1 is a three-pin adjustable shunt regulator with a specified thermal stability over the applicable automotive temperature ranges. The TL431-Q1 can be used as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference. The TL431-Q1 consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, which allows this device to sink a maximum current of 100 mA.

2.3 System Design Theory

This reference design implements the single-end flyback topology with a single switch and transformer to achieve high power density over a wide range of operating conditions. The active start-up circuitry increases the steady-state efficiency. The use of a SiC MOSFET increases the input DC voltage range. The variant of including an optocoupler on the secondary side enables fast transient response and a higher loop bandwidth. The variant without an optocoupler avoids life-cycle degradation in a high-temperature, harsh automotive environment.

2.3.1 Switching Frequency

The switching frequency of the converter is chosen as 140 kHz, which is slightly below the conducted electromagnetic interference (EMI) frequency range. The internal oscillator uses a timing capacitor (C_{CT}) and a timing resistor (R_{RT}) to program the oscillator frequency and maximum duty cycle (as 図 3 shows). Program the operating frequency based on the curves specified in the data sheet, where the timing resistor can be found after selecting the timing capacitor. The best practice is to select a timing capacitor to have a flat temperature coefficient, typical of most COG- or NPO-type capacitors. Select values of 13k Ω and 1000 pF for R_{RT} and C_{CT}, respectively, to operate at a 140-kHz switching frequency.

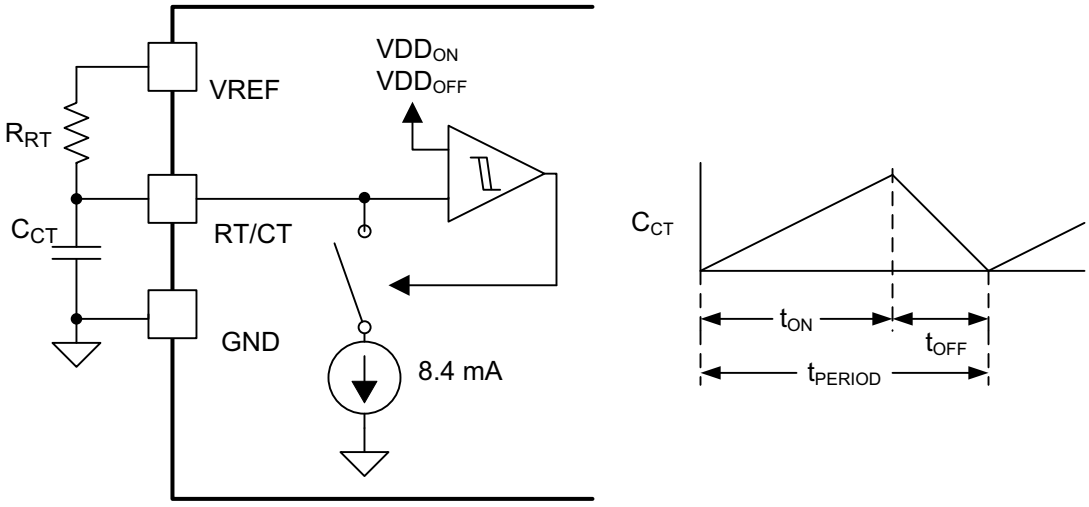


図 3. UCC28C43-Q1 Oscillator Circuit

2.3.2 Transformer Design

If ignoring the drop voltage across the switching MOSFET and output rectification diode, calculate the winding turns ratio as:

$$V_{IN\_min} \times T_{ON} = V_{OUT} \times T_{OFF} \times N_{PS} \quad (1)$$

where,

- V_{IN_min} is the minimum input voltage,
- T_{ON} is the switch-on time of the switching MOSFET,
- T_{OFF} is the OFF time of the switching MOSFET,
- N_{PS} is the turn ratio between the primary turns and secondary turns of the transformer.

The converter targets a full power delivery when the input voltage reaches 50 V; therefore, perform calculations with 50 V as the minimum input voltage. Considering

$$D = \frac{T_{ON}}{T_{OFF}} \quad (2)$$

is the duty cycle, and the maximum duty cycle is chosen as 85%. Therefore, calculate the turn ratio of the transformer primary winding to the secondary winding (N_{PS}) as:

$$N_{PS} = \frac{V_{IN\_min}}{V_{OUT}} \times \frac{D}{1-D} = 14.1 \quad (3)$$

N_{PS} is selected as 12. Therefore, calculate the actual duty cycle (D_{ON_act}) as:

$$D_{ON\_act} = \frac{(V_{OUT} + V_f) \times N_{PS}}{VIN\_min + (V_{OUT} + V_f) \times N_{PS}} = 0.8 \quad (4)$$

where,

- V_f is the forward drop voltage of the output rectification diode,
- V_{IN_min} is the minimum input voltage.

Calculate the turnoff time duty cycle of the MOSFET as:

$$D_{OFF\_act} = 1 - D_{ON\_act} = 0.2 \quad (5)$$

Calculate the average output current as:

$$I_{sec\_avg} = \frac{P_{OUT}}{V_{OUT}} = 4\ A \quad (6)$$

Calculate the average peak current (I_{sec_avgpk}) at the transformer secondary side as:

$$I_{sec\_avgpk} = \frac{I_{sec\_avg}}{D_{OFF\_act}} = \frac{4}{0.2} = 20\ A \quad (7)$$

Calculate the peak current at the transformer secondary side (I_{sec_pk}) as:

$$I_{sec\_pk} = \frac{2 \times I_{sec\_avgpk}}{2 - D_{OFF\_act}} = \frac{2 \times 20\ A}{2 - 0.2} = 22.3\ A \quad (8)$$

The average current flowing into the transformer secondary side is 4 A; therefore, calculate the RMS current at the transformer secondary side (I_{sec_rms}) as:

$$I_{sec\_rms} = I_{sec\_avgpk} \times \sqrt{D_{OFF\_act}} = 20\ A \times \sqrt{0.2} = 9\ A \quad (9)$$

Calculate the average peak current (I_{pri_avgpk}) at the transformer primary side as:

$$I_{pri\_avgpk} = \frac{I_{sec\_avgpk}}{N_{PS}} = \frac{20\ A}{12} = 1.7\ A \quad (10)$$

Calculate the peak current at the transformer primary side (I_{pri_pk}) as:

$$I_{pri\_pk} = \frac{I_{sec\_pk}}{N_{PS}} = \frac{22.3\,A}{12} = 1.86\,A \quad (11)$$

Calculate the RMS current at the transformer primary side (I_{pri_rms}) as:

$$I_{pri\_rms} = I_{pri\_avgpk} \times \sqrt{D_{ON\_act}} = 1.7\ A \times \sqrt{0.8} = 1.52\ A \quad (12)$$

The output voltage of the bias windings are V_{bias1} = 20 V and V_{bias2} = –5 V.

表 2 provides a summary of the previous calculations and specifications of the designed flyback transformer.

表 2. Flyback Transformer Specifications

PARAMETERS		SPECIFICATIONS
Qualification		AEC-Q200 Grade 1 qualified
Safety insulation		Reinforced, 5.7 kV for 1 minute
Power rating		60 W
Input voltage		40 V to 1 kV
Frequency		140 kHz
Maximum duty cycle		85%
Primary side inductance		1500 µH ± 10% at 140 KHz
Leakage inductance		< 1% of primary inductance
Output voltage		15 V at 4-A average current
Auxiliary winding output		20 V and 5 V at 35 mA
Turns ratio	Primary to secondary	12:1
	Primary to auxiliary 1 (20 V)	9.3:1
	Primary to auxiliary 2 (5 V)	36.4:1
Peak current	Primary	1.86 A
	Secondary	22.3 A
RMS current	Primary	1.52 A
	Secondary	9 A

TI recommends use of the automotive-grade AEC-Q200-qualified flyback transformer (WA8759-AL) from CoilCraft for this reference design. CoilCraft has specifically designed this part for TIDA-01505. Please contact CoilCraft for product details.

2.3.3 Current Sense Resistor

The controller implements the peak current-mode control scheme. The clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. Peak current-mode control determines the modulation of the switch. At the beginning of each switching cycle, the current in the primary begins to rise. This current develops a voltage across the sense resistor. This voltage is fed into the current-sense pin.

Calculate the current sense resistor as:

$$R_{sense} = \frac{CS_{th}}{1.2 \times I_{peak(pri)}} = \frac{1V}{1.2 \times 1.86\ A} = 0.45\ \Omega \quad (13)$$

Calculate the power rating of the resistor as:

$$P_{sense} = I_{pri\_rms}^{2} \times R_{sense} = 1.52^{2} \times 0.4\ \Omega = 0.93\ W \quad (14)$$

Select two 0.91-Ω, 1-W current sense resistors connected in parallel.

2.3.4 Input Capacitors

The input capacitor must supply the input current during the input voltage dip in the 800-V battery load transient conditions. Input capacitors are essential in limiting the ripple voltage at the input pin of UCC28C43-Q1 device while supplying most of the switch current during the MOSFET switch-on time.

Calculate the input capacitance as:

$$C_{IN} = \frac{I_{pri\_pk} \times D_{ON}}{F_{SW} \times \Delta V_{ripple}} = \frac{0.24\ A \times 0.71}{150\ k \times 80\ V \times 3\%} = 2.5\ \mu F \quad (15)$$

The input capacitor must be able to withstand 1.5-kV voltage ratings. This design uses five C1825X473KFRACTU 0.047-µF ceramic capacitors and B43501A6476M electrolytic capacitors (three in series, 22 µF, and 500 V).

Note the importance of checking the current sharing between the aluminum capacitor and the ceramic capacitor to avoid overheating. The equivalent series resistance (ESR) of an aluminum capacitor dominates its impedance, and the reluctance of a ceramic capacitor dominates its impedance. Therefore:

$$Z_{AL} = ESR_{AL} = 2.82\ \Omega \quad (16)$$

$$Z_{mlcc} = \frac{1}{2 \times \pi \times F_{SW} \times C_{mlcc}} = \frac{1}{2 \times 3.14 \times 150\ kHz \times 0.047\ \mu F} = 22\Omega \quad (17)$$

where,

- ESR_{AL} is the ESR of the input aluminum capacitor,
- C_{mlcc} is the capacitance of the total input ceramic capacitor.

The RMS input current is 0.52 A; therefore, calculate the currents flowing into each aluminum capacitor and the ceramic capacitor as:

$$I_{rms\_AL} = I_{pri\_rms} \times \frac{Z_{mlcc}}{Z_{AL} + Z_{mlcc}} = 0.52 \times \frac{22 \times \frac{1}{5}}{2.82\ \Omega \times 3 + 22\ \Omega \times \frac{1}{5}} = 0.18\ A \quad (18)$$

$$I_{rms\_mlcc} = I_{pri\_rms} \times \frac{Z_{AL}}{Z_{AL} + Z_{mlcc}} = 0.52 \times \frac{2.82\ \Omega \times 3}{2.82\ \Omega \times 3 + 22\ \Omega \times \frac{1}{5}} \times \frac{1}{5} = 0.068\ A \quad (19)$$

The input capacitors must be selected such that the withstand RMS current is higher than the calculated values. Select B43501A6476M as the aluminum capacitor because it has a 0.51-A withstand current at 85°C, per the data sheet.

2.3.5 Output Capacitor Selection

The output capacitance ensures that the converter has a small transient deviation to a step change of the load transient. Calculate the minimum required capacitance as such to maintain the output voltage drop less than 3% of the nominal voltage when the output current changes abruptly from the maximum to half (I_{step}):

$$I_{step} = \frac{I_{sec\_avg}}{2} = \frac{4\ A}{2} = 2\ A \quad (20)$$

$$V_{drop} = V_{OUT} \times 3\% = 15\ V \times 3\% = 0.45\ V \quad (21)$$

As with any back converter, the right-half-plane-zero (RHPZ) limits the bandwidth of the continuous current mode (CCM) flyback. Calculate the frequency of the RHPZ as:

$$L_S = \frac{L_{pri}}{\left(\frac{N_{pri}}{N_{sec}}\right)^2} = \frac{1.5\ mH}{\left(\frac{12}{1}\right)^2} = 10.4\ \mu H \tag{22}$$

$$f_{RHPZ} = \frac{V_{OUT} \times \left(1 - D_{max}\right)^2}{2 \times \pi \times L_S \times D_{MAX} \times I_{OUT}} = 2\ kHz \tag{23}$$

where,

- L_{pri} is the inductance of the transformer primary winding,
- L_S is the inductance of the transformer secondary winding.

Calculate the output impedance R_O as:

$$R_O = \frac{V_{OUT}}{I_{OUT}} = \frac{15\ V}{4\ A} = 3.75\ \Omega \tag{24}$$

The bandwidth of the system is estimated as 1/5 of the RHPZ:

$$f_{bandwidth} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 2\ kHz = 400\ Hz \tag{25}$$

For the result, calculate the output capacitance at the bandwidth frequency as:

$$C_{OUT\_min} = \frac{1}{2 \times \pi \times f_{bandwidth}} \times \frac{1}{\Delta V_{OUT} / \Delta I_{loadstep} - ESR_{OUT}}$$

$$C_{OUT\_min} = \frac{1}{2 \times 3.14 \times 400\ Hz} \times \frac{1}{15\ V \times 3\% / 2\ A - 0.028 / 3}$$

$$C_{OUT\_min} = 1845\ \mu F \tag{26}$$

This design uses four instances of 470-µF, 35-V rated capacitor EKZM350ELL471MJ16S, which are available from Chemi-Con. Eight instances of 10-µF, 35-V ceramic capacitors are selected in parallel with the aluminum capacitors.

2.3.6 Output Inductor Design

An output inductor is required to reduce the current ripple. The target is to reduce 20% current ripple when the input voltage reaches 100 V. Calculate the maximum current flowing through the diode as:

$$I_{sec\_max} = \left(I_{pri\_min} + I_{ripple}\right) \times \frac{N_{pri}}{N_{sec}} = \left(0.65\ A + 0.36\ A\right) \times 12 = 12.12\ A \tag{27}$$

Calculate the minimum current as 0.22 A at the 1-kV input. Calculate the output current without an inductor as:

$$\Delta i = 12.12\ A - 0.22\ A = 11.9\ A \tag{28}$$

Calculate the output average current as:

$$\Delta i = \frac{12.12\ A + 0.22\ A}{2} = 6.17\ A \tag{29}$$

Calculate the time interval during the switching-on period of the MOSFET as:

$$\Delta T = D \times \frac{1}{F_{SW}} = 71\% \times \frac{1}{140\ kHz} = 5.1\ \mu s \tag{30}$$

The inductance target is to reduce to 30% current ripple within 3% output voltage ripple; therefore, calculate the value as:

$$L_{OUT} = V_{RIPPLE} \times \frac{\Delta T}{\Delta i} = 15\ V \times 3\% \times \frac{5.1\,\mu s}{6.17\ A \times 20\%} = 1.85\ \mu H \quad (31)$$

2.3.7 Zener Clamping Snubber Design

When the MOSFET turns OFF, a high-voltage spike occurs at the drain (switch node) because of the leakage inductor of the main transformer and the parasitic capacitance in the circuit. The parasitic capacitance comprises three components: output capacitance of the MOSFET, junction capacitance of the output diode that reflects to the primary side, and parasitic capacitance of the transformer winding. As a result, implementation of the snubber circuit is very important to prevent avalanche breakdown and damage to the MOSFET.

This design implements a Zener clamp circuit, which consists of a diode and high-voltage Zener or transient voltage suppressor (TVS) diode, as 図 4 shows. The Zener diode effectively clips the voltage spike until the leakage energy completely dissipates in the Zener diode. The advantage of using this circuit is that it only clamps whenever the combined V_R and V_{spike} is greater than its breakdown voltage. At low line and lighter loads, where the spike is relatively low, the Zener may not clamp at all; therefore, there is no power dissipated in the clamp.

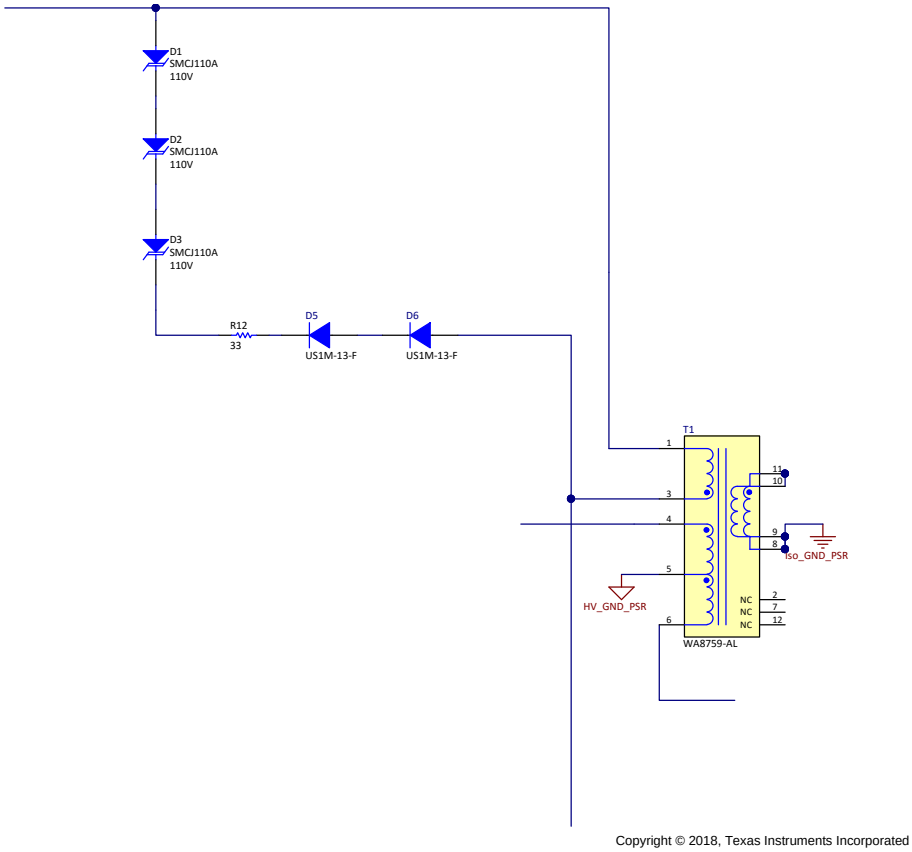


図 4. Zener Clamping Snubber Circuit

The general rule is to choose the Zener or TVS diode rating to be 1.2 times the reflected voltage:

$$V_{TVS} = 2 \times \frac{N_{pri}}{N_{sec}} \times V_{OUT} = 2 \times 12 \times 15\ V = 360\ V \quad (32)$$

Three TVS diodes, each with a clamping voltage of 110 V, are connected in series. The power rating of the TVS is estimated as 4% of the total maximum power:

$$P_{TVS} = 60\ W \times 4\% = 2.4\ W \quad (33)$$

Calculate the maximum duration of the spikes as:

$$T_{spike} = \frac{1}{140\ kHz} \times 85\% = 6\ \mu s \tag{34}$$

Per the data sheet of the selected TVS diode, the peak current it can tolerate is 6.2 A. A resistor must be placed in series with the TVS to limit the current. Calculate the minimum value as:

$$R_{clp} = \frac{V_{sn} - V_{TVS}}{I_{clp}} = \frac{450\ V - 330\ V}{6.2\ A} = 20\ \Omega \tag{35}$$

2.3.8 Active Start-Up Circuit

This reference design implements an active start-up circuit to reduce the standby power losses. This start-up circuit is used to replace a pure resistive start-up chain because it will constantly dissipate the power due to the high-voltage crossing it. 図 5 shows the implemented active start-up circuit.

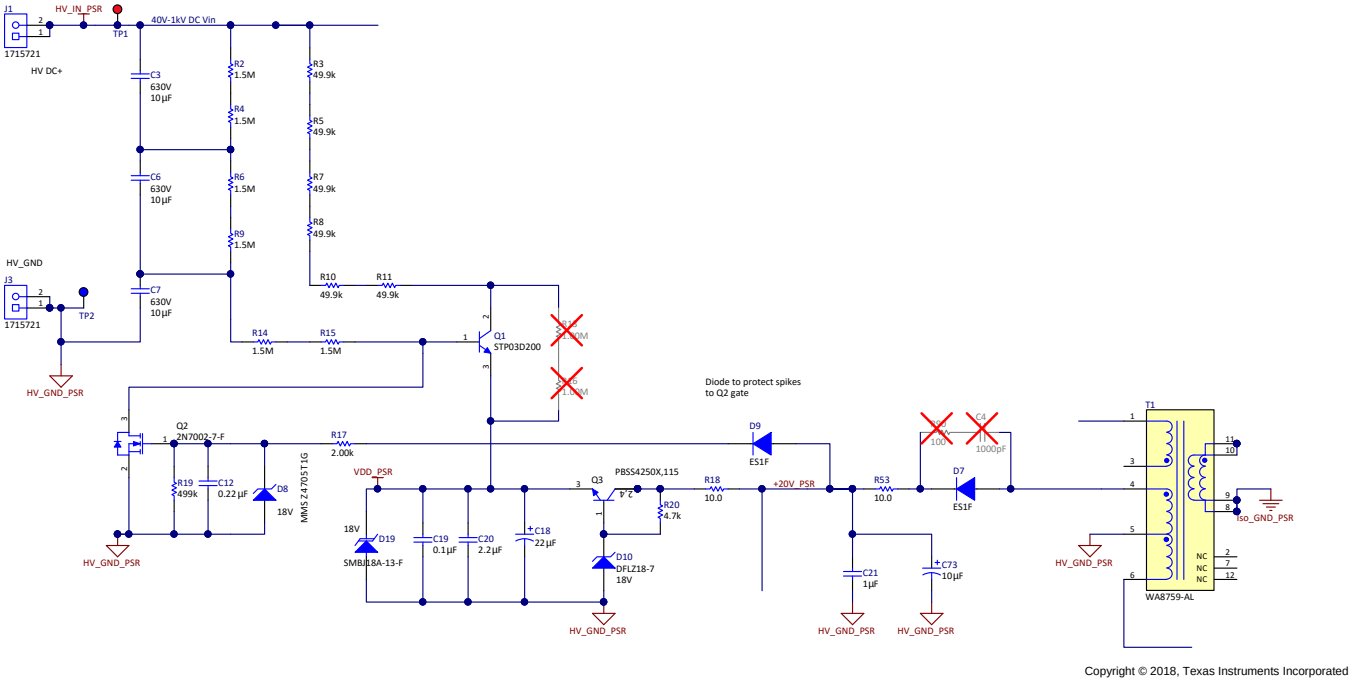


図 5. Active Start-Up Circuit

Calculate the start-up time of the converter as:

$$T_{start\_up} = C_{ss} \times \frac{dV_{COMP}}{I_{ss}} = 1\ \mu F \times \frac{2.5\ V - 0.7\ V}{1\ mA} = 1.8\ ms \tag{36}$$

where,

- C_{ss} is the soft-start capacitance,
- V_{comp} is the lower threshold of the oscillator,
- I_{ss} is the soft-start current.

The start-up voltage and turn-off voltage of the UCC28C43-Q1 is V_{UVLO_on} = 8.4 V and V_{UVLO_off} = 7.6 V, respectively.

The required capacitance on the VDD pin is at least ten times greater than the gate capacitance of the main switching field-effect transistor (FET). Assuming that a 22-µF capacitor is connected, calculate the minimum required start-up current as:

$$I_{start\_up} = \frac{C_{Vdd} \times V_{UVLO\_on}}{T_{start\_up}} = \frac{22\mu F \times 8.4V}{1.8\ mA} = 103\ \ mA \quad (37)$$

Therefore, calculate the total resistance for the fast start-up lane as:

$$R_{start\_fast} = \frac{V_{in\_min} - V_{UVLO\_off}}{I_{start\_up}} = 314 \quad \Omega \tag{38}$$

This design uses six instances of high-voltage resistors specified at 50 kΩ. Calculate the maximum collector current on Q1 as:

$$I_{CE\_Max} = \frac{V_{in\_max} - V_{UVLO\_off}}{R_{start\_fast}} = \frac{1\ kV - 7.6\ V}{300\ k\Omega} = 3.3 \quad mA \tag{39}$$

Calculate the power rating of the resistor as:

$$P_{start\_R} = I_{start}^{2} \times R_{start\_fast} = 0.55 \quad W \tag{40}$$

Select the 2-kV bipolar junction transistor (BJT) STP03D200 for the active start-up circuit. Assuming that the DC current gain is h_{FE} = 500, calculate the maximum total resistance at the slow lane as:

$$R_{start\_slow} \le h_{FE} \times R_{start\_fast} = 500 \times 300\ k\Omega = 150\ M\Omega \tag{41}$$

With this result, select six instances of 1.5MΩ high-voltage resistors. Calculate the power rating of the resistor as:

$$P_{start\_slow} = \left(\frac{V_{in\_max}}{R_{start\_slow}}\right)^2 \times R_{slow} = \left(\frac{1000\ V}{1.5\ M\Omega \times 6}\right)^2 \times 1.5\ M\Omega = 0.02\ W \tag{42}$$

2.3.9 Rectification Diodes

Three rectification diodes are in the circuit: The diode at the 20-V output bias winding D1, the diode at the 5-V output bias winding D2, and the secondary output rectification diode D3.

Calculate the blocking voltage rating for D1 from the reflected voltage plus the winding output voltage:

$$V_{bias\_min} = V_{ref} + V_{bias} = \frac{V_{in\_max}}{\frac{N_{pri}}{N\_bias}} + 20\ V = \frac{1000\ V}{\frac{1}{0.12}} + 20\ V = 140\ V \tag{43}$$

For enough head room, choose an ultra-fast recovery diode ES1F with a 300-V voltage rating. Select D2 to match.

Calculate the blocking voltage rating for D3 from the reflected voltage plus the winding output voltage:

$$V_{outdiode\_min} = V_{ref} + V_{OUT} = \frac{V_{in\_max}}{\frac{N_{pri}}{N_{sec}}} + 15\ V = \frac{1000\ V}{\frac{1}{0.086}} + 15\ V = 101\ V \tag{44}$$

2.3.10 Selection of MOSFETs

Calculate the required minimum breakdown voltage of the MOSFET as:

$$V = V_{inmax} + V_{sn} = 1kV + 360\ V = 1360\ V \tag{45}$$

Calculate V_{sn} as:

$$V_{sn} = 2 \times \frac{N_{pri}}{N_{sec}} \times V_{OUT} = 2 \times 12 \times 15\ V = 360\ V \tag{46}$$

where,

- V_{sn} is the reflected voltage from primary to secondary,
- V_{in_max} is the maximum input voltage.

Choose the SiC MOSFET with a 1.7-kV breakdown voltage. This reference design uses the Wolfspeed 1700-V SiC - C2M1000170D. Calculate the drain-to-source current of the MOSFET at the minimum input voltage:

$$I_D = \frac{P_{OUT}}{\eta \times V_{in\_min}} = \frac{60\ W}{0.85 \times 40} = 1.76\ A \quad (47)$$

Calculate the conduction losses of the MOSFET (P_{on}) as:

$$P_{on} = I_D{}^2 \times R_{dson} \times D_{on} = (0.7\ A)^2 \times 0.8\ \Omega \times 85\% = 2.1\ W \quad (48)$$

Calculate the switching losses of the SiC MOSFET from the data sheet. When the MOSFET is switching at 850-V drain-to-source voltage and 0.17-A drain-to-source current, then E_{on}= 15 µJ, and E_{off} = 9 µJ. Therefore, the switching losses are:

$$P_{SW1} = (E_{on} + E_{off}) \times F_{SW} = 24\ \mu J \times 140\ kHz = 3.36\ W \quad (49)$$

where,

- F_{SW} is the switching frequency.

2.3.11 Compensation Network

2.3.11.1 Slope Compensation

With current mode control, slope compensation is required to stabilize the overall loop with the duty cycles exceeding 50% (see *Modeling, Analysis and Compensation of the Current-Mode Converter*). Subharmonic instability can occur with duty cycles that may extend beyond 50%, where the rising primary-side inductor current slope may not match the falling secondary-side current slope. The subharmonic oscillation results in an increase in the output voltage ripple and may even limit the power-handling capability of the converter.

図 6 shows the implemented slope compensation circuit. The goal of slope compensation is to achieve an ideal quality coefficient (Q_P) equal to 1 at half of the switching frequency (see *Practical Considerations in Current Mode Power Supplies*). Calculate Q_P as:

$$Q_P = \frac{1}{\pi \times (M_C \times (1 - D) - 0.5)} \quad (50)$$

where,

- D is the primary-side switch duty cycle,
- M_C is the slope compensation factor.

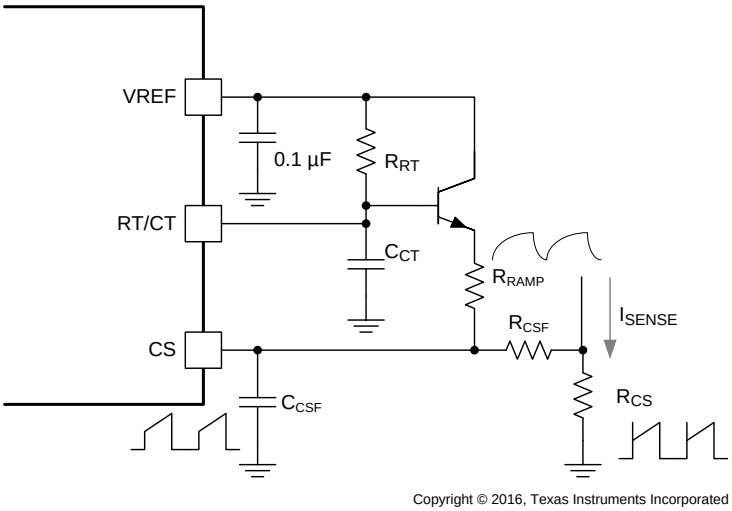


図 6. Slope Compensation Circuit of UCC28C43-Q1

M_C is defined as:

$$M_C = \frac{S_e}{S_n} + 1 \tag{51}$$

where,

- S_e is the compensation ramp slope,
- S_n is the inductor rising slope.

The optimal goal of the slope compensation is to achieve Q_P = 1. Calculate the ideal value of the slope compensation factor as:

$$M_{ideal} = \frac{\frac{1}{\pi + 0.5}}{1 - D_{max}} = \frac{\frac{1}{\pi + 0.5}}{1 - 82.5\%} = 4.67 \tag{52}$$

Therefore, the target of M_C is 4.67 when the duty cycle reaches its maximum value. Calculate the inductor rising slope (S_n) fed into the CS pin as:

$$S_n = \frac{V_{IN\_min} \times R_{CS}}{L_P} = \frac{40\ V \times 0.455}{1.5\ mH} = 0.012\ \frac{V}{\mu s} \tag{53}$$

Calculate the compensation slope (S_e) as:

$$S_e = (M_C - 1) \times S_n = (4.67 - 1) \times 0.012 = 44.53\ \frac{mV}{\mu S} \tag{54}$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF}. The C_{RAMP} is an AC-coupling capacitor that allows use of the oscillator voltage ramp without adding an offset to the current sense; select a value to approximate a high-frequency short circuit, such as 10 nF, as a starting point and make adjustments if required. The R_{RAMP} and R_{CSF} resistors form a voltage divider from the oscillator charge slope and this proportional ramp is injected into the CS pin to add slope compensation. Choose the value of R_{RAMP} to be much larger than the R_{RT} resistor so that it does not load down the internal oscillator and result in a frequency shift. Calculate the oscillator charge slope using the peak-to-peak voltage of the R_T / C_T sawtooth waveform (V_{OSCpp}) which is equal to 1.9 V, and the minimum ON time:

$$t_{on\_min} = \frac{D_{min}}{F_{SW}} = \frac{(1 - 82.5\%)}{140\ kHz} = 1.25\ \mu s \quad (55)$$

$$S_{OSC} = \frac{V_{OSCpp}}{t_{on\_min}} = \frac{1.9\ V}{1.25\ \mu s} = 1.52\ \frac{V}{\mu s} \quad (56)$$

R_{RAMP} and R_{CSF} must be able to meet the calculations from the following equations:

$$R_{CSF} = \frac{\frac{R_{RAMP}}{S_{OSC}}}{S_e - 1} = \frac{\frac{R_{RAMP}}{1520}}{44.53 - 1} = \frac{R_{RAMP}}{33.13} \quad (57)$$

$$S_e = \frac{\frac{S_{OSC}}{R_{RAMP}}}{R_{CSF} + 1} \quad (58)$$

Select R_{RAMP} and R_{CSF} as 9.1 kΩ and 2 kΩ, respectively.

2.3.11.2 Compensation Network of PSR Flyback

Achieve regulation of the PSR flyback by regulating the output voltage of the bias winding. Therefore, the coupling factor of the transformer is the key factor to minimize to increase the regulation accuracy. The bandwidth of the continuous-conduction-mode (CCM) flyback converter is limited to one-fifth of the RHPZ:

$$f_{BW} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 2\ kHz = 400\ Hz \quad (59)$$

Implement Type II compensation for the converter control loop. Calculate the power stage pole created by the load and output cap as:

$$f_{pole} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times 1960\ \mu F \times 3.75} = 21.65\ Hz \quad (60)$$

Calculate the high-frequency zero created by the ESR of the output cap as:

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} = \frac{1}{2 \times \pi \times 470\ \mu F \times 0.023} = 14.7\ kHz \quad (61)$$

Half of the switching frequency is 70 kHz, which is higher than f_{ESR}; therefore, set the compensator zero to the pole frequency of the power stage:

$$\frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times R_Z \times C_Z} = \frac{1}{2 \times \pi \times 1960\ \mu F \times 3.75} \quad (62)$$

Set the compensator pole to the ESR frequency of the output capacitor:

$$\frac{1}{2 \times \pi \times C_{OUT} \times ESR} = \frac{1}{2 \times \pi \times R_Z \times C_{pole}} = \frac{1}{2 \times \pi \times 470\ \mu F \times 0.023} \quad (63)$$

Consider the compensation gain to be 1; therefore, select R_Z to match the value of R_{fb1} 20.5 kΩ. Calculate the C_Z and C_{pole} as 350 nF and 530 pF, respectively.

2.3.11.3 Compensation Network of Flyback With Optocoupler

The design of the compensation loop involves selecting the appropriate components so that a stable system can be obtained over the entire operating range. The loop has three distinct portions: the TL431, the optocoupler, and the error amplifier.

The required compensation pole can be added to the primary-side error amplifier using R_{COMPp1} and C_{COMPp1}. This process is known as inner-loop compensation. The compensate pole at the inner loop is required at the frequency of the RHZP or the ESR zero, whichever is the lowest. When choosing R_{COMPp1} as 10 kΩ, the required value of C_{COMPp} is determined as:

$$C_{COMPp1} = 12 \times \pi \times f_{COMPz} \times R_{COMPp1}$$
$$C_{COMPp1} = 12 \times \pi \times 2\ \text{kHz} \times 10\ \text{k}\Omega$$
$$C_{COMPp1} = 7.9\ \text{nF} \quad (64)$$

where,

- f_{COMPz} is equal to the frequency of the RHPZ.

Select a 3.3-nF capacitor for C_{COMPp1}.

A good phase margin requires placing a compensator zero (f_{COMPz}) at the outer loop and at 1/10th the desired bandwidth:

$$f_{COMPz} = \frac{1}{10} \times f_{BW} = \frac{1}{10} \times 400\ \text{Hz} = 40\ \text{Hz} \quad (65)$$

図 7 shows the compensation network of the optocoupler, which mainly consists of the compensation zero capacitor C_{COMPz2} (C68), compensation zero resistor R_{COMPz2} (R70), and compensation pole capacitor C_{COMPp2} (C71).

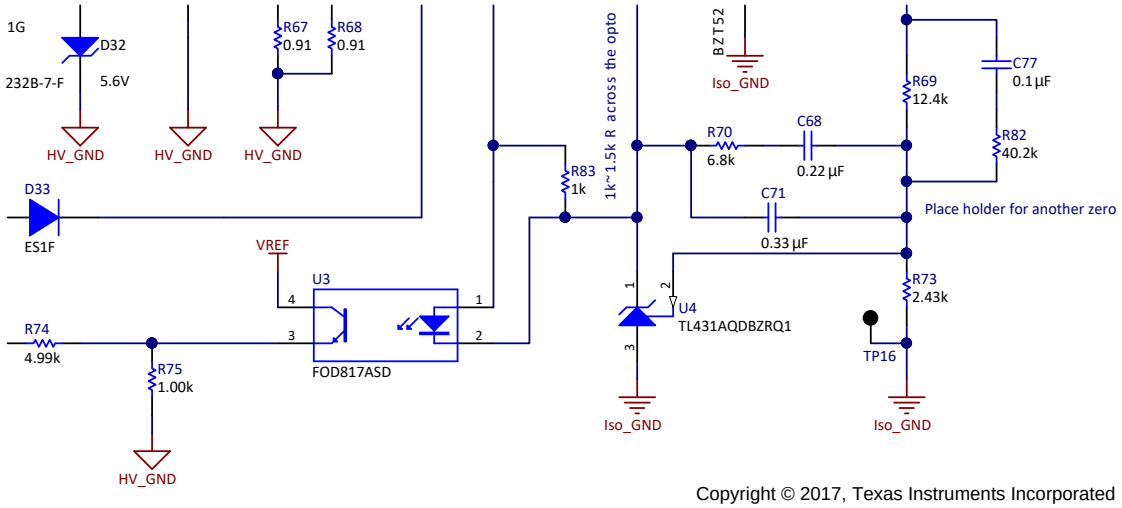


図 7. Compensation Network of Optocoupler

Place the compensation zero frequency a bit higher than the low-frequency pole. After setting C_{COMPz2} to 220 nF, calculate R_{COMPz2} as:

$$R_{COMPz2} = \frac{1}{2 \times \pi \times f_{COMPz} \times C_{COMPz2}} = \frac{1}{2 \times \pi \times 100\ \text{Hz} \times 220\ \text{nF}} = 7.2\ \text{k}\Omega \quad (66)$$

The most common practice is to set the compensation pole at the switching frequency or lower than the switching frequency to attenuate the high-frequency noise. Considering that the system contains a very-low frequency bandwidth, set the compensation pole frequency to less than twice that of the desired bandwidth. Select R_{COMPz} as 6.8 kΩ. The compensation pole is set at:

$$f_{pole} = \frac{1}{2 \times \pi \times C_{COMPp2} \times R_{COMPz2}} = \frac{1}{2 \times \pi \times 330\ \text{nF} \times 6.8\ \text{k}\Omega} = 70\ \text{Hz} \quad (67)$$

Select the current-limiting resistor R61 such that the forward current flowing into the optocoupler is below the saturation current (I_F). The saturation current is 4 mA according to the FOD817A data sheet. Therefore, calculate R61 as:

$$R_{61} \geq \frac{V_{OUT} - V_F}{I_F} = \frac{15\ V - 4\ V}{10\ mA} = 1.1 k\Omega \quad (68)$$

As a result, R61 is selected as 2 kΩ.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

図 8 and 図 9 show the PCB board image of this TIDA-01505 reference design from the top side and bottom side, respectively. Both of the two design variants—with optocoupler and PSR—are included on the board. The SiC MOSFET is mounted on the heat sink. Two connectors are placed for high-voltage positive and negative input, respectively. The other two connectors are placed for output positive and negative voltages, respectively.

The SiC MOSFET, high-voltage start-up bipolar transistor, and transformer are placed on the top side. The snubber circuit, UCC28C43-Q1 controller, and optocoupler are placed on the bottom side.

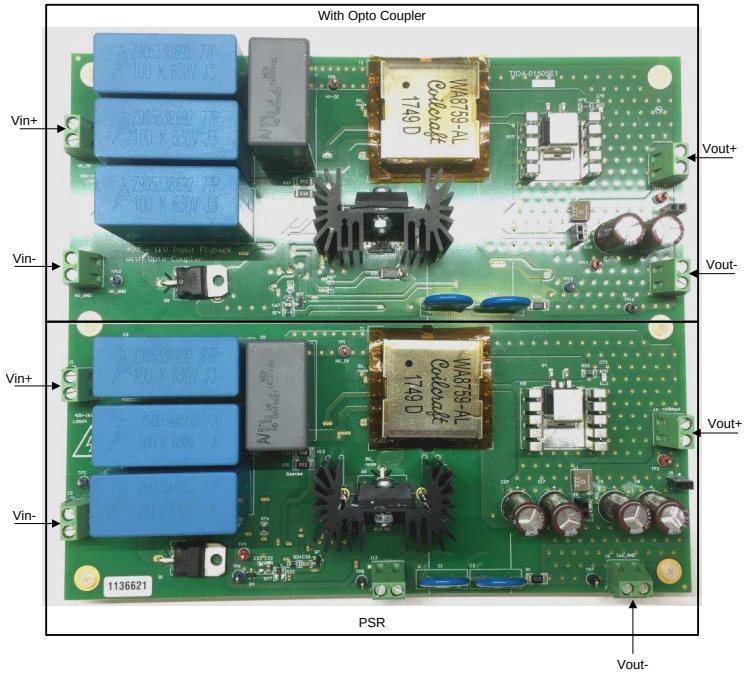


図 8. TIDA-01505 PCB Board Top Side

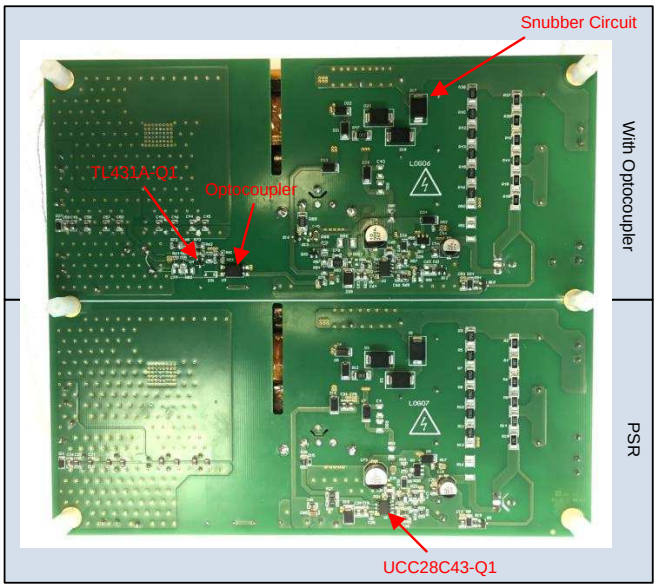


図 9. TIDA-01505 PCB Board Bottom Side

3.2 Testing and Results

3.2.1 Switching dv/dt of SiC MOSFET

図 10 shows the switching dv/dt of the SiC MOSFET during turn-on switching transient. As mentioned previously, the high dv/dt nodes must be kept small and away from quiet areas to reduce the noise coupling.

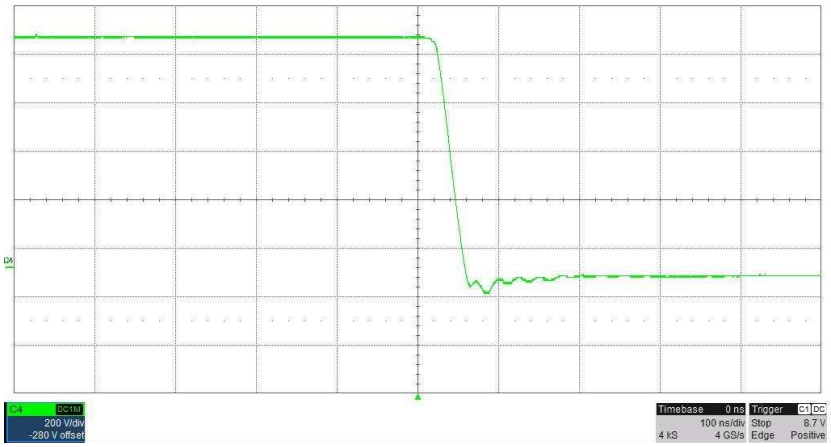


図 10. Switching dv/dt of SiC MOSFET During Turnon Transient (40-V/ns Average)

注: CH4: Drain-to-source voltage of the SiC MOSFET

3.2.2 Level Shifter Output

The level shifter is placed in between the Si FET driver and the SiC MOSFET to convert the PWM driving signals to +20-V and –5-V voltage levels for driving the SiC MOSFET. The level shifter is required to have the low propagation delay and fast driving slopes at both turnon and turnoff switching transients. The designer can also disconnect the level shifter from the circuit by removing the 0-Ω shunt resistors. 図 11 shows the PWM switching waveforms before and after the level shifter.

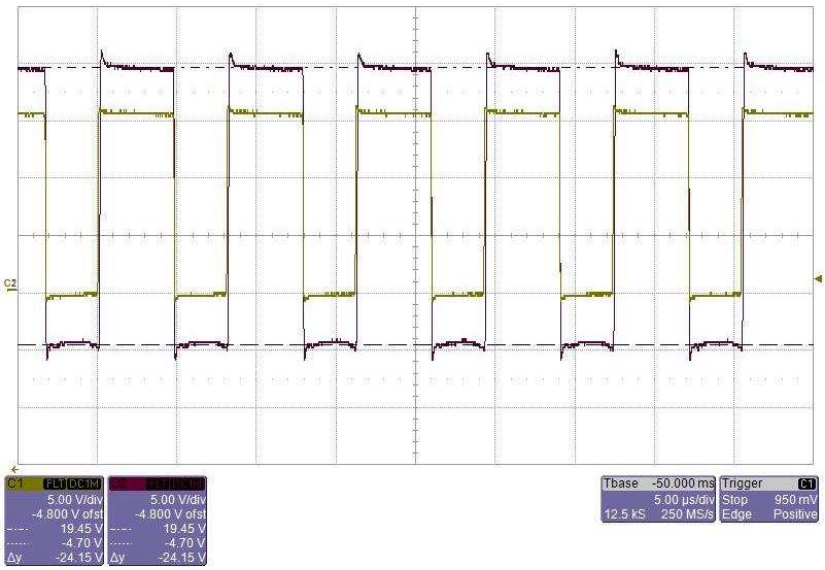


図 11. PWM Switching Waveforms Before and After Level Shifter

注: CH1: PWM signal generated from UCC28C43-Q1, CH2: PWM signal generated from the level shifter

図 12 shows the propagation delay of the level shifter rising slope. The waveform shows the generation of a 75.5-ns time delay.

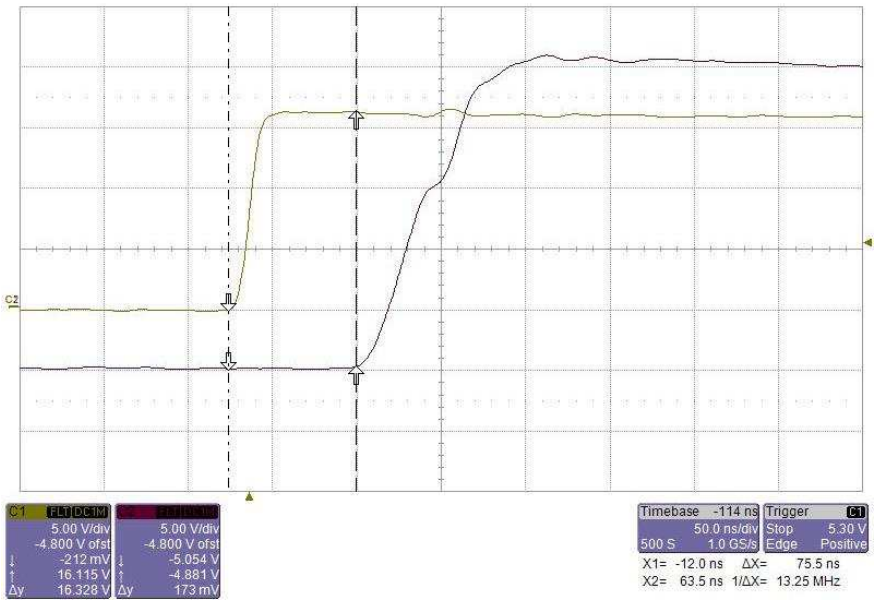


図 12. Propagation Delay of Rising Slope

注: From left to right – CH1: PWM signal generated from UCC28C43-Q1, CH2: PWM signal generated from the level shifter

図 13 shows the propagation delay of the level shifter falling slope. The waveform shows the generation of an 8.8-ns time delay.

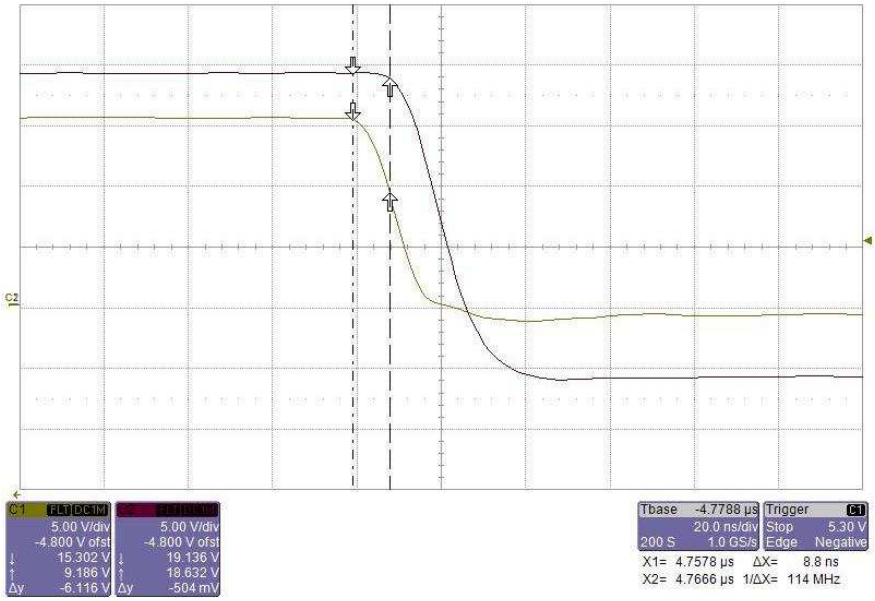


図 13. Propagation Delay of Falling Slope

注: From top to bottom – CH2: PWM signal generated from the level shifter, CH1: PWM signal generated from UCC28C43-Q1

3.2.3 Start-Up and Power Down

図 14 shows the start-up waveform of the converter. The duration is 450 µs. The waveform is measured at an 800-V input voltage.

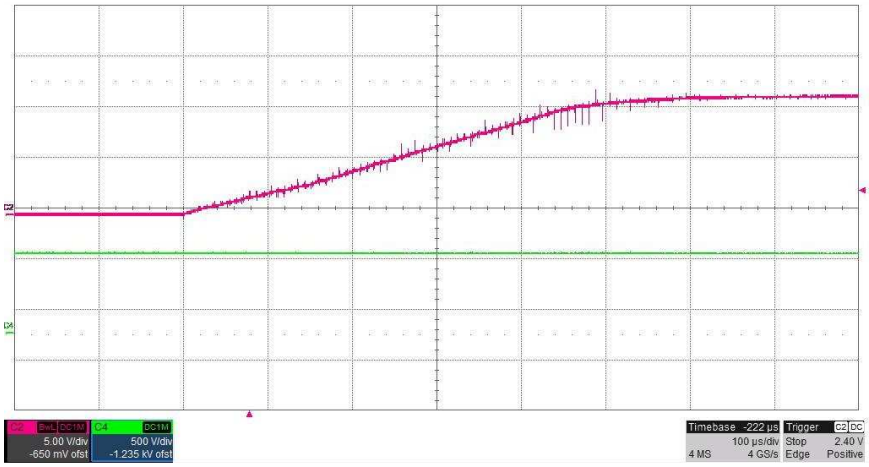


図 14. Start-Up Waveforms of TIDA-01505

注: From top to bottom – CH2: Output voltage, CH4: Input voltage

図 15 shows the power down of the converter, with an observed duration of approximately 50 ms. The power-down waveform is measured at an 800-V input voltage.

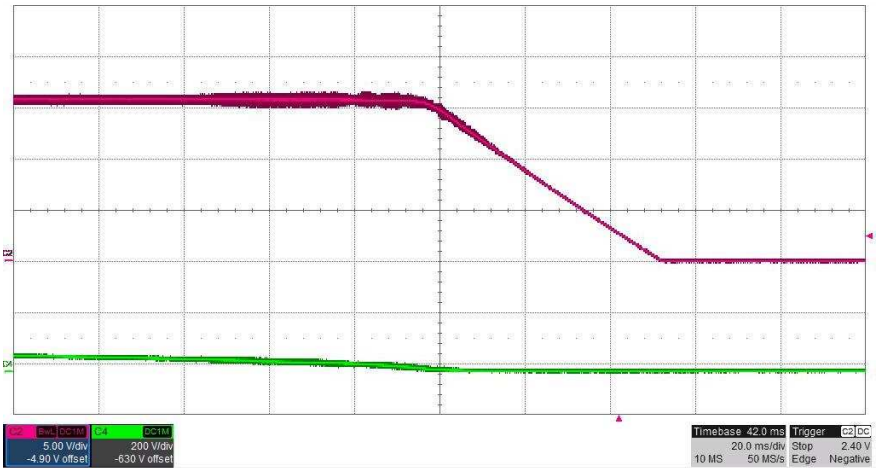


図 15. Power-Down Waveform of TIDA-01505

注: From top to bottom – CH2: Output voltage, CH4: Input voltage

3.2.4 Output Voltage Ripple

The output voltage ripple of the design is measured under light-load- and full-load conditions, respectively. A 600-V input voltage is applied. 図 16 and 図 17 show the waveforms. Note how less than 50-mV peak-to-peak ripple voltage is obtained at a 4-A full load.

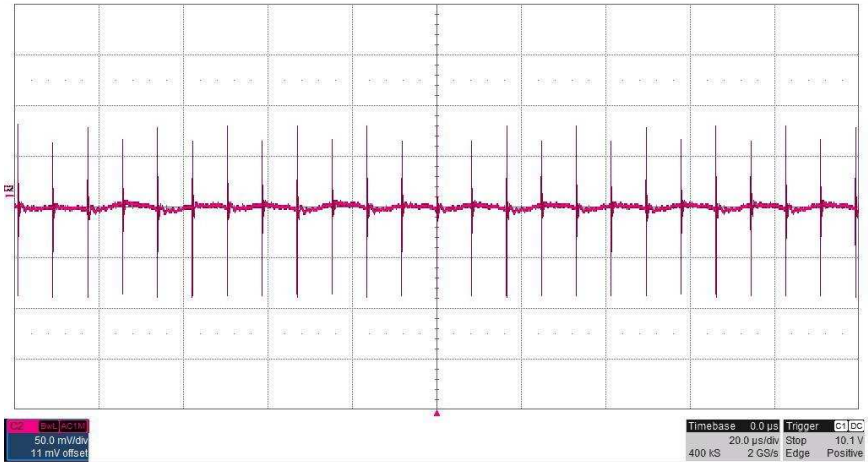


図 16. Output Voltage Ripple of TIDA-01505 Under V_{IN} = 600 V and 0.2-A Load (With Optocoupler)

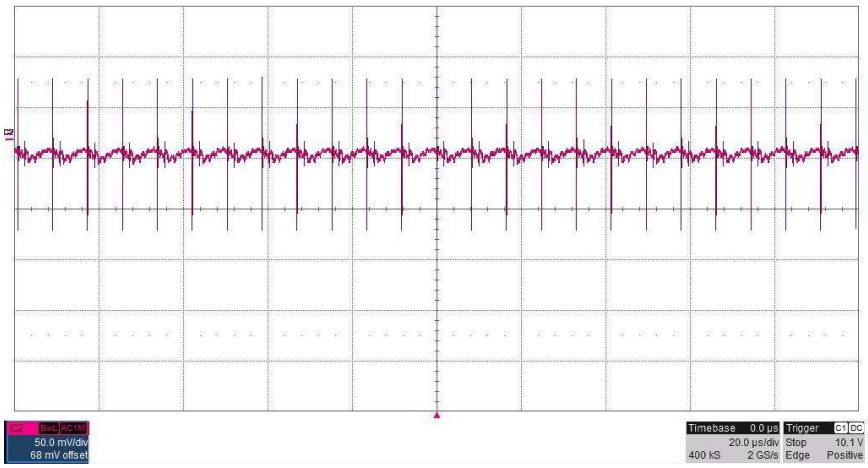


図 17. Output Voltage Ripple of TIDA-01505 Under V_{IN} = 600 V and I_{OUT} = 4 A (With Optocoupler)

3.2.5 Switch Node Waveforms

The gate drive and the switch node voltage waveforms of the converter are measured under various input voltage and load conditions. Both of the design variants with and without optocoupler (PSR) are tested.

3.2.5.1 With 40-V Input

図 18 through 図 21 show the switch node and gate drive waveforms under the 40-V input.

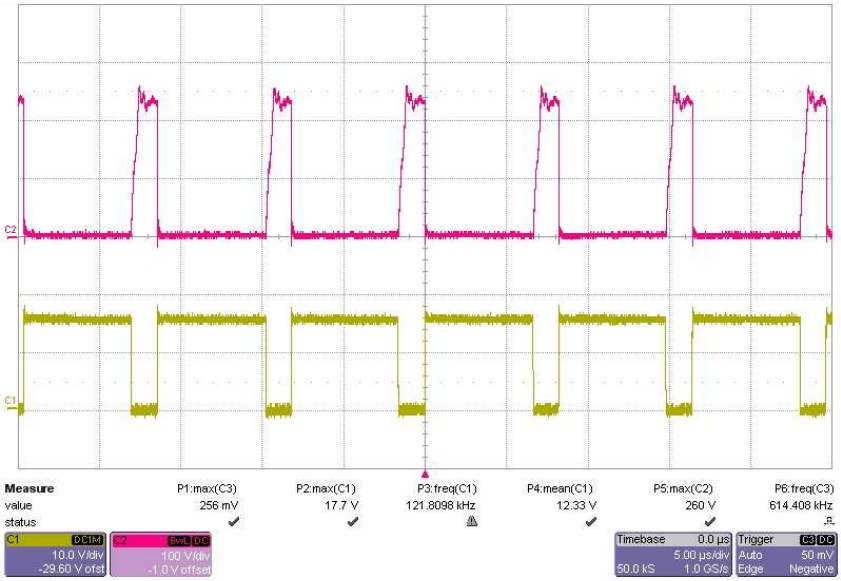


図 18. Switch Node and Gate Drive Waveforms Under V_{IN} = 40 V and No Load (With Optocoupler)

注: From top to bottom – CH2: Switch node voltage, CH1: PWM switching from the controller

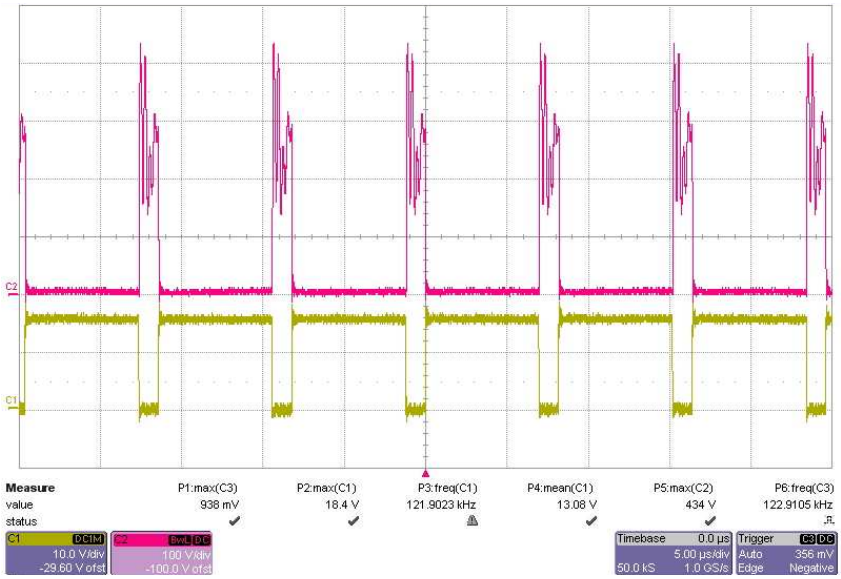


図 19. Switch Node and Gate Drive Waveforms Under V_{IN} = 40 V, I_{OUT} = 3 A (With Optocoupler)

注: From top to bottom – CH2: Switch node voltage, CH1: PWM switching from the controller

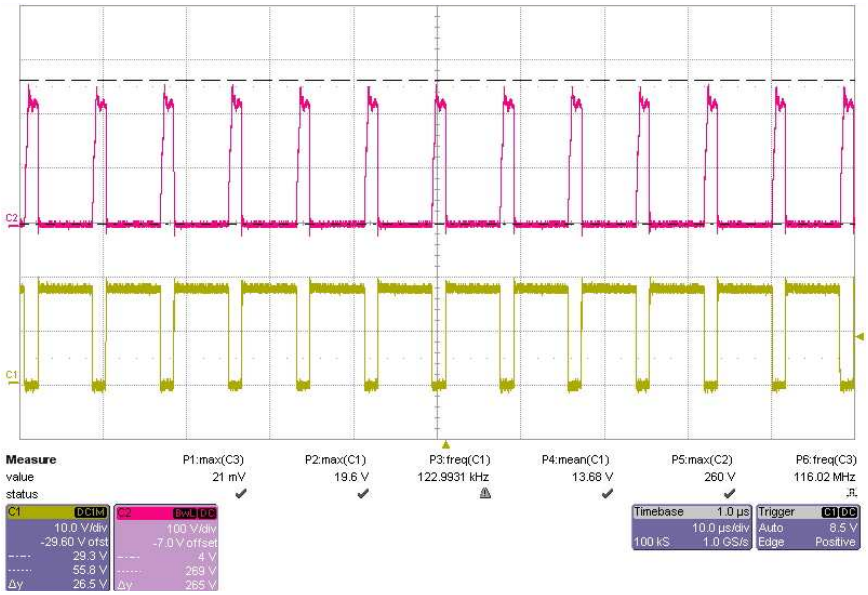


図 20. Switch Node and Gate Drive Waveforms Under V_{IN} = 40 V and No Load (PSR)

注: From top to bottom – CH2: Switch node voltage, CH1: PWM switching from the controller

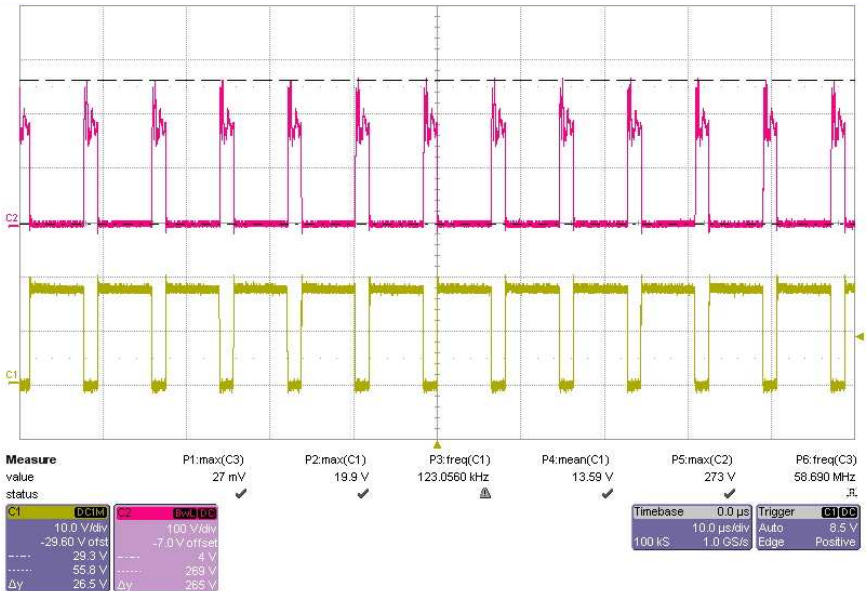


図 21. Switch Node and Gate Drive Waveforms Under V_{IN} = 40 V and I_{OUT} = 1.5 A (PSR)

注: From top to bottom – CH2: Switch node voltage, CH1: PWM switching from the controller

3.2.5.2 With 200-V Input

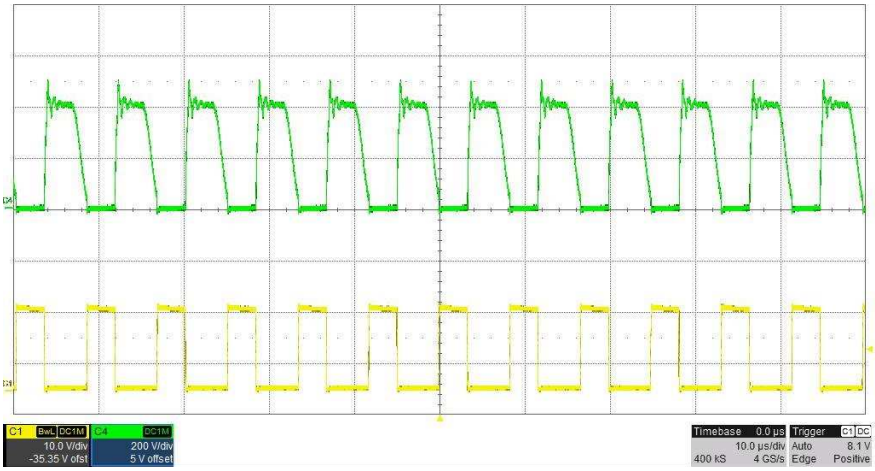


図 22. Switch Node and Gate Drive Waveforms Under V_{IN} = 200 V and I_{OUT} = 3.5 A (With Optocoupler)

注: From top to bottom – CH4: Switch node voltage,CH1: PWM switching from the controller

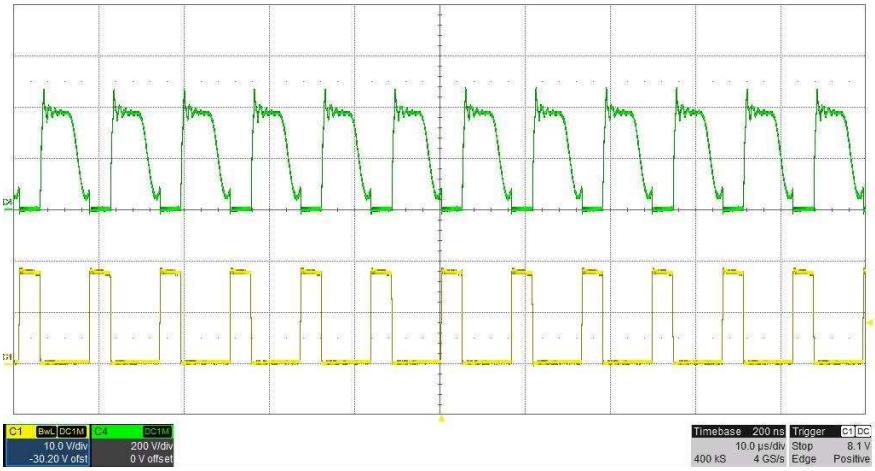


図 23. Switch Node and Gate Drive Waveforms Under V_{IN} = 200 V and I_{OUT} = 3.5 A (PSR)

注: From top to bottom – CH4: Switch node voltage,CH1: PWM switching from the controller

3.2.5.3 With 400-V Input

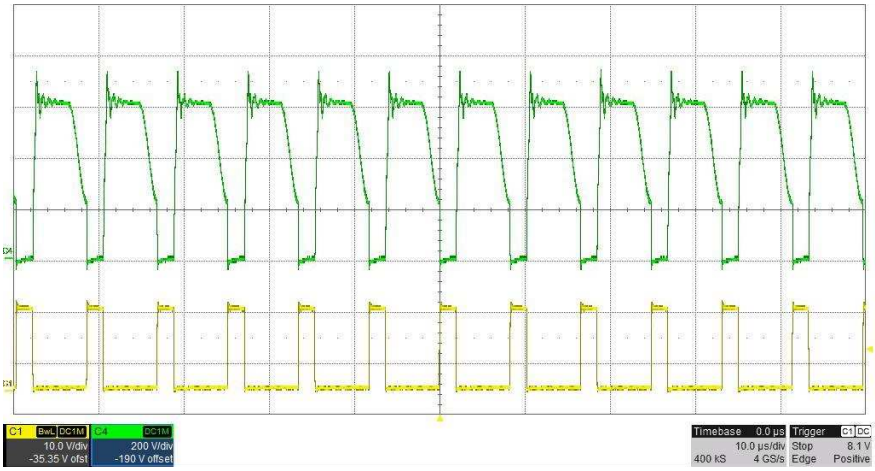


図 24. Switch Node and Gate Drive Waveforms Under V_{IN} = 400 V and I_{OUT} = 4 A (With Optocoupler)

注: From top to bottom – CH4: Switch node voltage, CH1: PWM switching from the controller

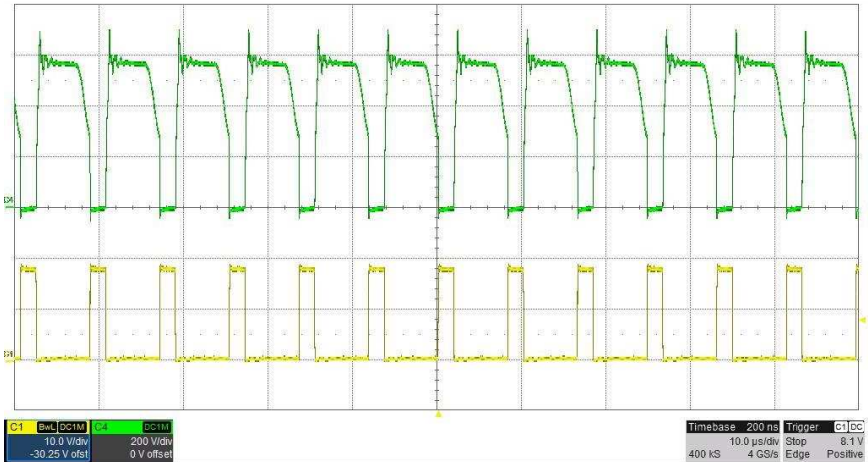


図 25. Switch Node and Gate Drive Waveforms Under V_{IN} = 400 V and I_{OUT} = 4 A (PSR)

注: From top to bottom – CH4: Switch node voltage, CH1: PWM switching from the controller

3.2.5.4 Higher Than 400-V Input

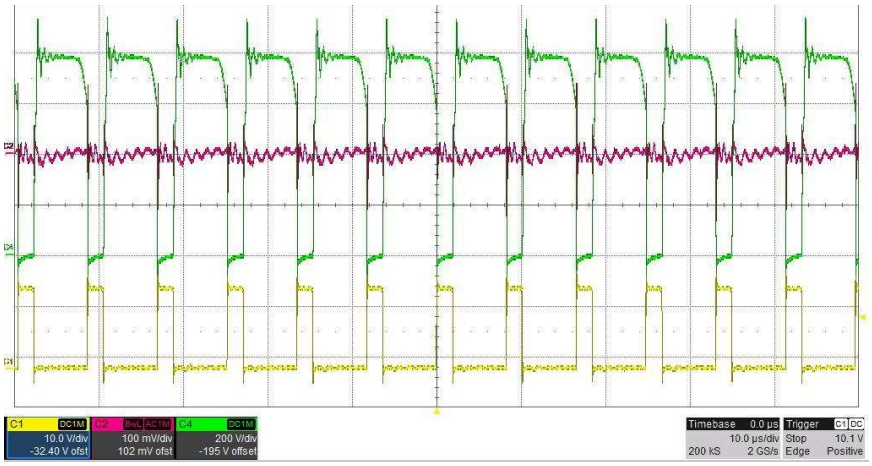


図 26. Switch Node and Gate Drive Waveforms Under V_{IN} = 600 V and I_{OUT} = 4 A (With Optocoupler)

注: From top to bottom – CH4: Switch node voltage, CH2: Output voltage ripple, CH1: PWM switching from the controller

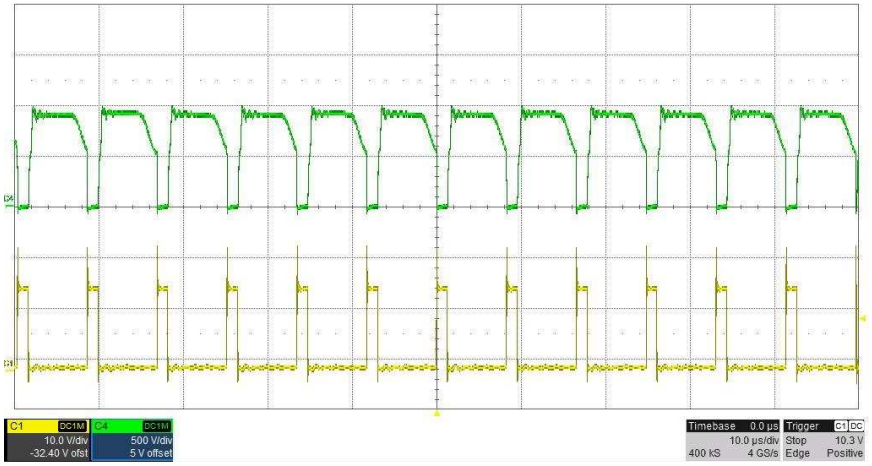


図 27. Switch Node and Gate Drive Waveforms Under V_{IN} = 800 V and I_{OUT} = 4 A (With Optocoupler)

注: From top to bottom – CH4: Switch node voltage, CH1: PWM switching from the controller

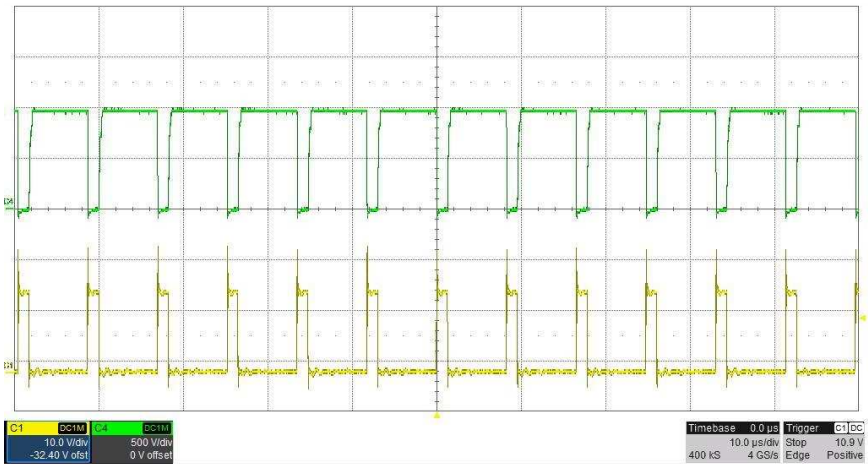


図 28. Switch Node and Gate Drive Waveforms Under V_{IN} = 1000 V and I_{OUT} = 4 A (With Optocoupler)

注: From top to bottom – CH4: Switch node voltage, CH1: PWM switching from the controller
The switch node waveform becomes flat at the top because the voltage probe is saturated.

3.2.6 Efficiency

The efficiency of the design is measured under conditions of various input voltages. 図 29 shows the measurement setup. Two precision digital multimeters are placed at the input for measuring the input voltage and input current, respectively. The input voltage is measured through a resistive voltage divider. The input current is measured at the input ground terminal to avoid the high CM voltage stress. Another multimeter is placed at the output for measuring the output voltage. The output current is indirectly measured by the voltage drop from a precision shunt resistor.

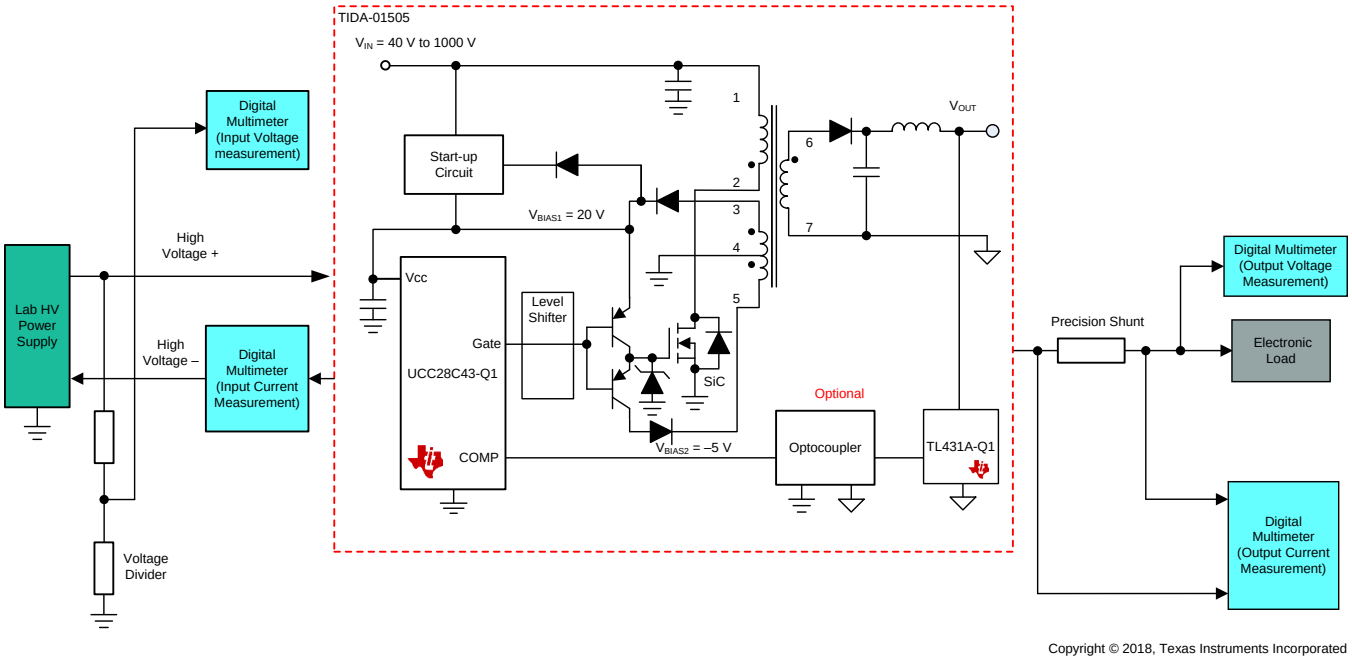


図 29. Experiment Setup for Measuring Efficiency of TIDA-01505

図 30 shows the measured efficiency of the design with the optocoupler version. Note that the peak efficiency of 85% is achieved at a 400-V input voltage and 2-A load.

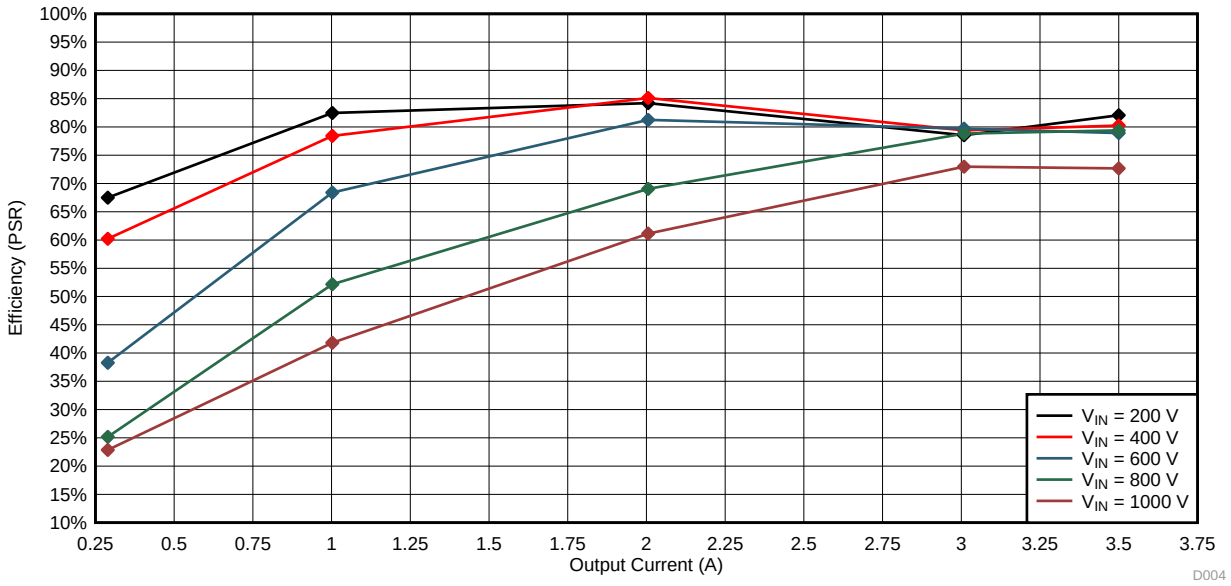


図 30. Measured Efficiency of Optocoupler Flyback in TIDA-01505

図 31 shows the measured efficiency of the design without the optocoupler version. Note that the peak efficiency of 86% is achieved at a 200-V input voltage and 1-A load.

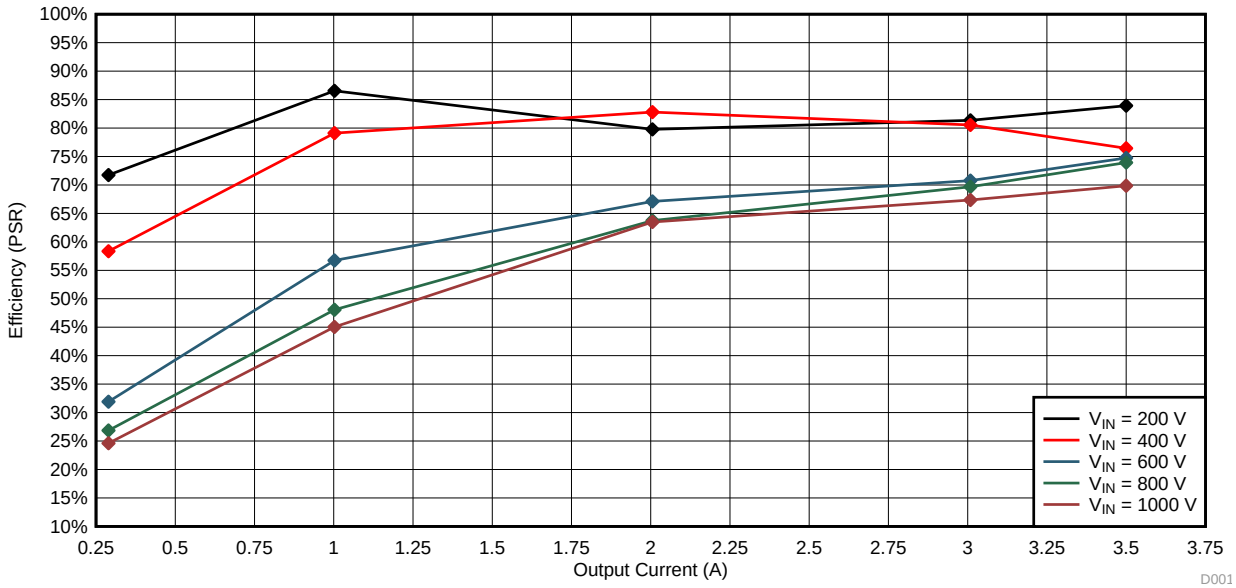


図 31. Measured Efficiency of PSR Flyback in TIDA-01505

3.2.7 Load Regulation

Load regulation measurements show the % deviation from the nominal output voltage as a function of output current. The experiment setup is the same as that of the efficiency measurement (see 図 29). 図 32 and 図 33 show the measured results of the PSR flyback and optocoupler flyback variants, respectively.

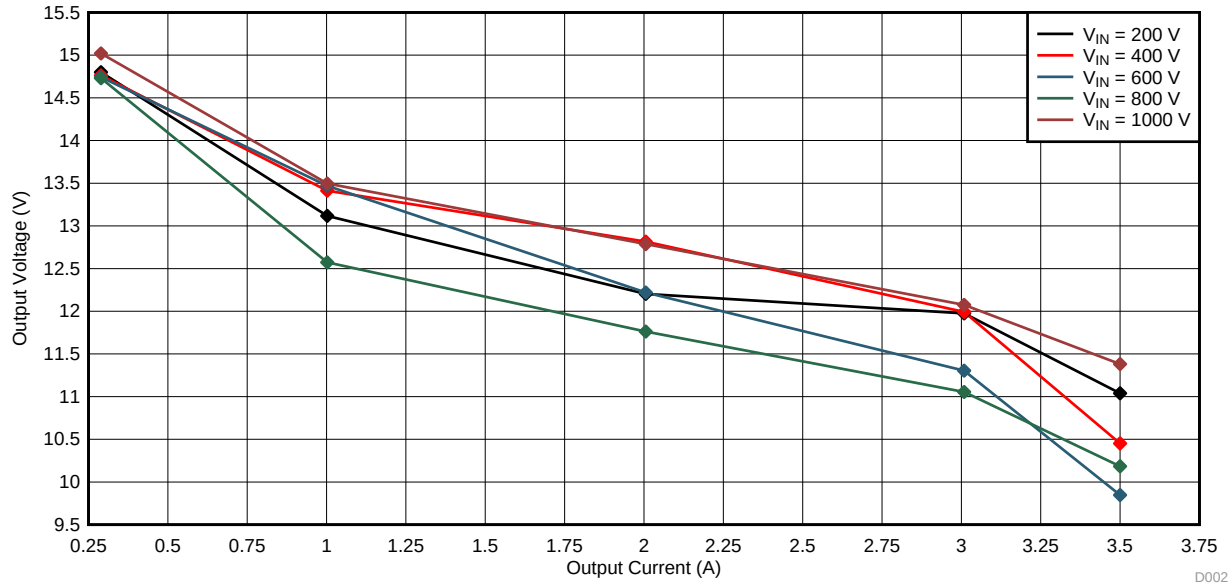


図 32. Load Regulation of PSR Flyback in TIDA-01505

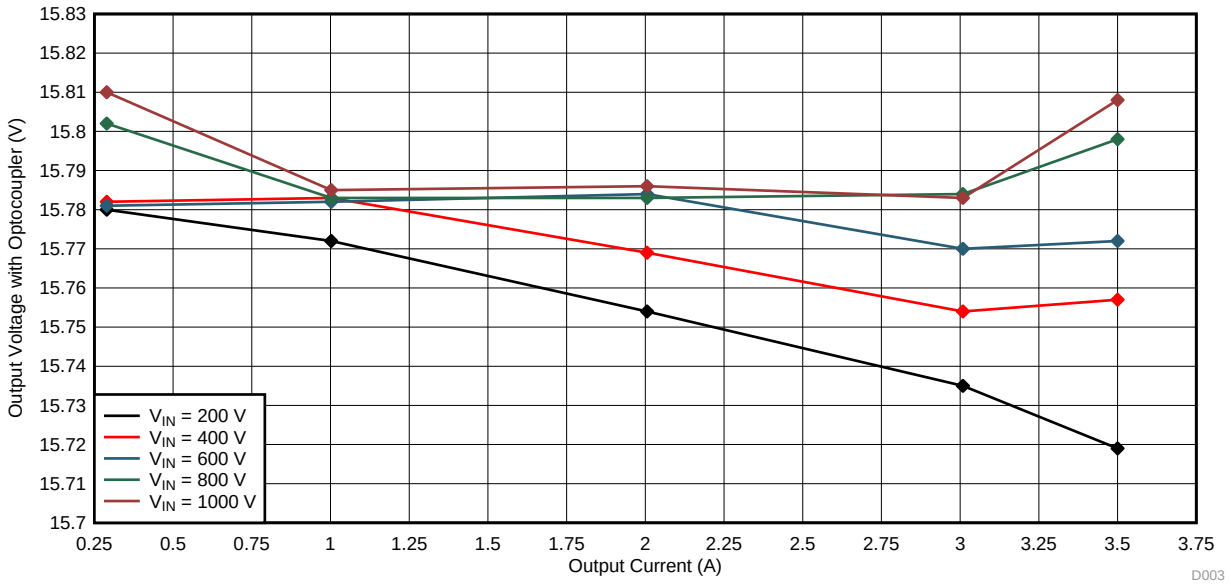


図 33. Load Regulation of Flyback With Optocoupler in TIDA-01505

3.2.8 Control Loop Frequency Response

The control loop frequency response represents the stability of the power supply system. The loop frequency response of the design is measured under various loads and input voltages, respectively. The worst condition occurs when the converter runs under the minimum input voltage and a full load.

3.2.8.1 PSR Flyback

This subsection shows the control loop response of the design version without an optocoupler. 図 34 shows the plot when the input is 40 V and the load is 100 mA. Note that a 100° phase margin is achieved.

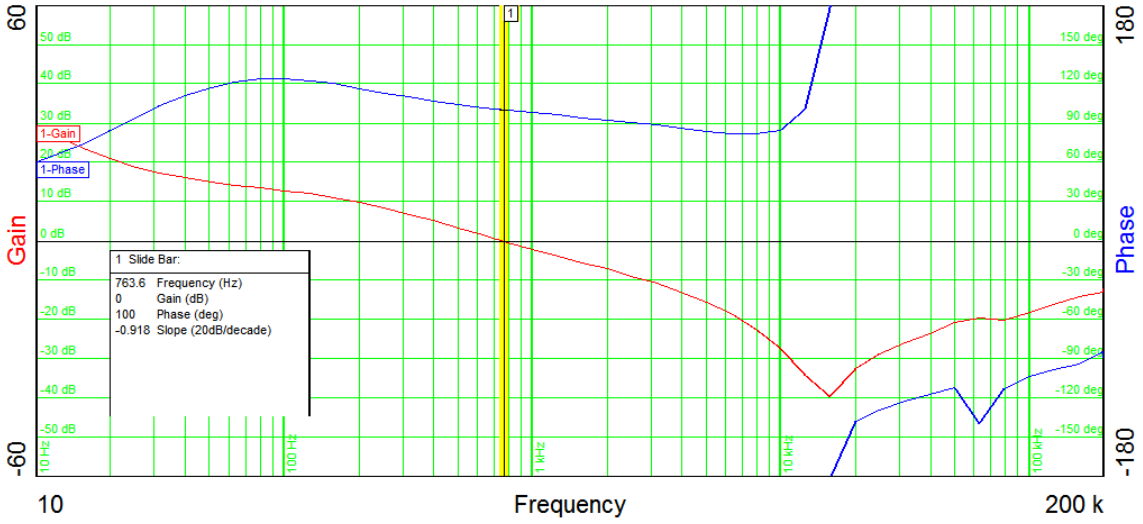


図 34. Loop Frequency Response With V_{IN} = 40 V and 0.10A Load (Without Optocoupler)

図 35 shows the plot when the input is 40 V at a 1.5-A load. Note that a 94° phase margin is achieved.

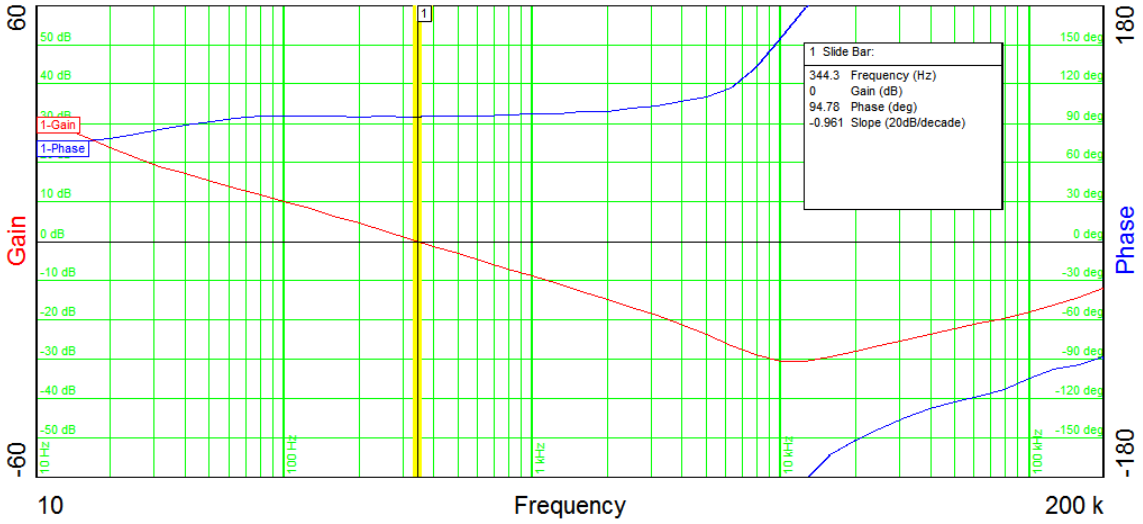


図 35. Loop Frequency Response With V_{IN} = 40 V and 1.5-A Load (Without Optocoupler)

図 36 shows the plot when the input is 120 V at a 0.1-A load. Note that a 84° phase margin is achieved.

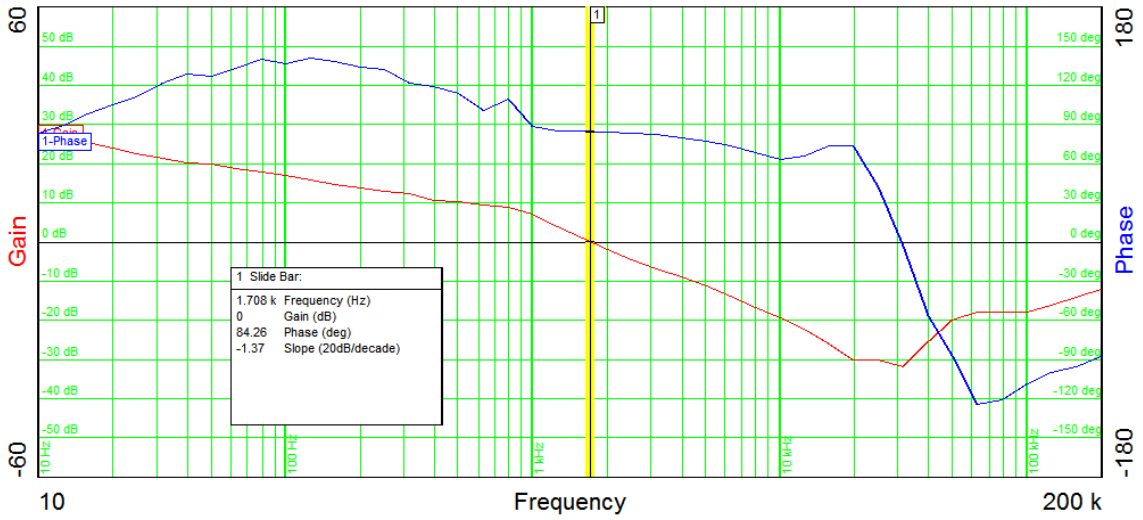


図 36. Loop Frequency Response With V_{IN} = 120 V and 0.1-A Load (Without Optocoupler)

図 37 shows the plot when the input is 120 V at a 2-A load. Note that a 94° phase margin is achieved.

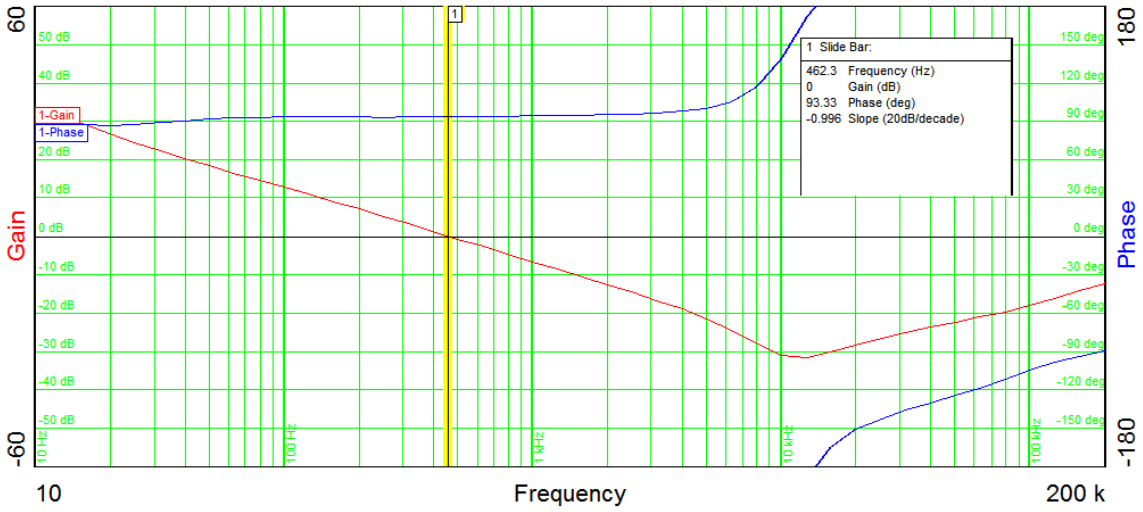


図 37. Loop Frequency Response With V_{IN} = 120 V and 2-A Load (Without Optocoupler)

3.2.8.2 Flyback With Optocoupler

This subsection shows the control loop response of the design version with an optocoupler. 図 38 shows the plot when the input is 40 V at a 0.1-A load. Note that a 82° phase margin is achieved.

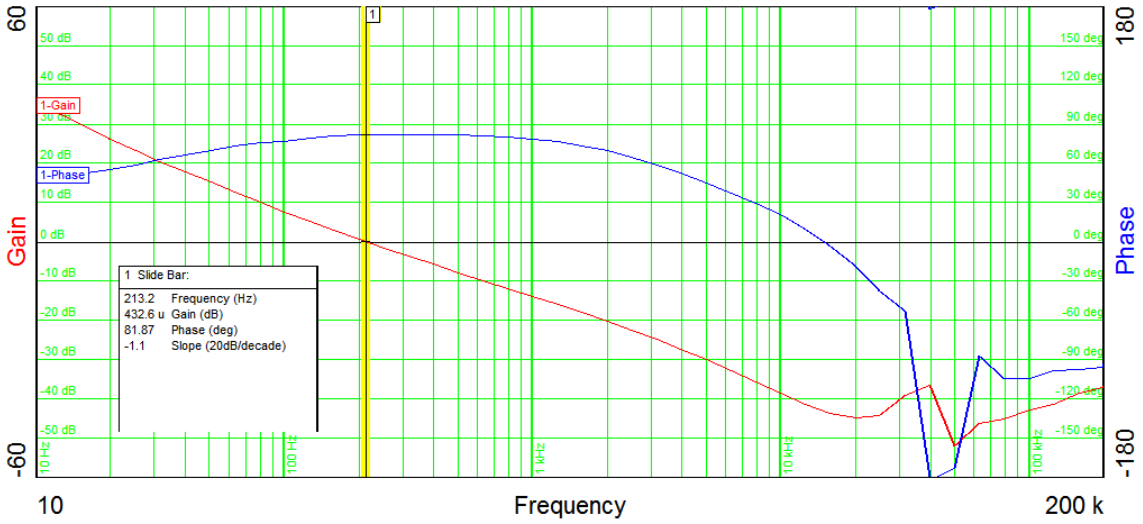


図 38. Loop Frequency Response With V_{IN} = 40 V and 0.1-A Load (With Optocoupler)

図 39 shows the plot when the input is 40 V at a 2.7-A load. Note that a 77° phase margin is achieved.

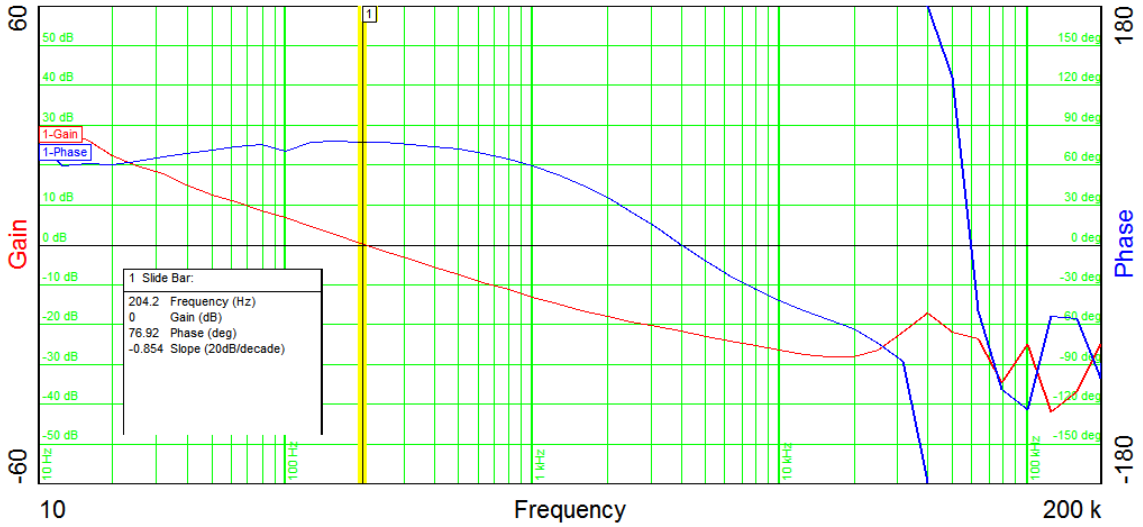


図 39. Loop Frequency Response With V_{IN} = 40 V and 2.7-A Load (With Optocoupler)

図 40 shows the plot when the input is 120 V at a 0.1-A load. Note that a 89° phase margin is achieved.

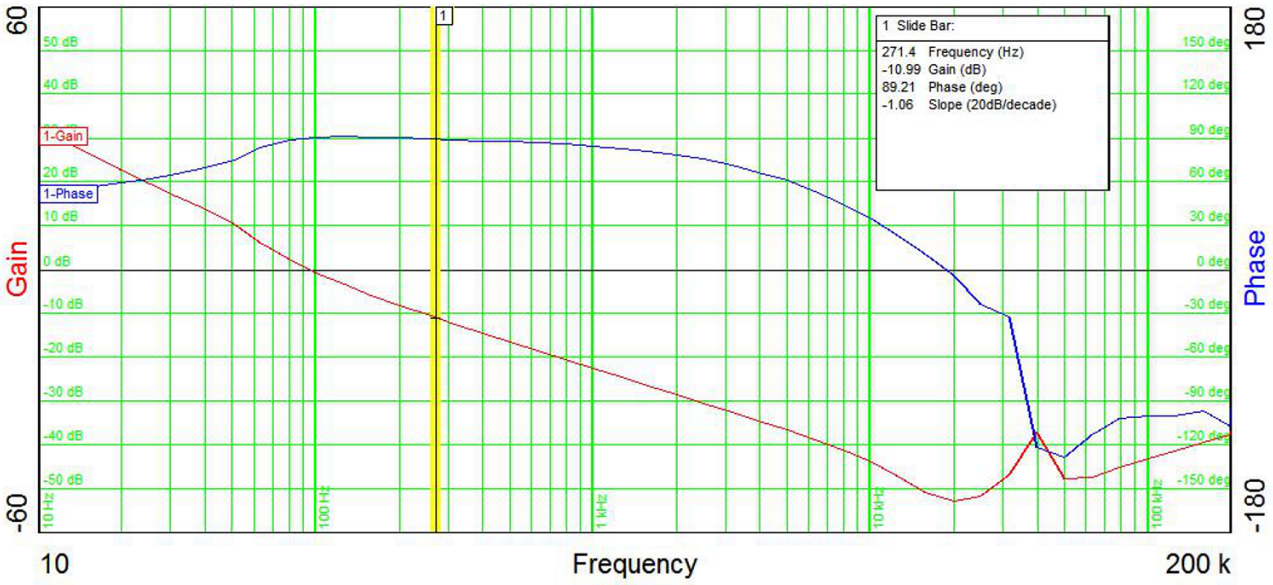


図 40. Loop Frequency Response With V_{IN} = 120 V and 0.1-A Load (With Optocoupler)

図 41 shows the plot when the input is 120 V at a 4-A load. Note that a 82° phase margin is achieved.

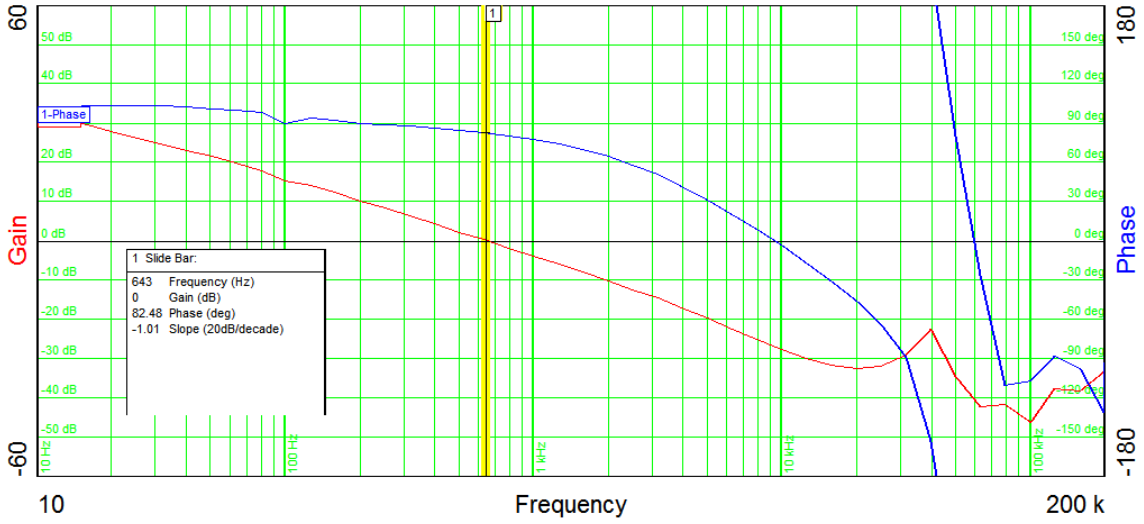


図 41. Loop Frequency Response With V_{IN} = 120 V and 4-A Load (With Optocoupler)

3.2.9 Load Transient Response

A load transient response presents how well a power supply copes with the changes in the load current demand. 図 42 and 図 43 show the load transient response of two converter variants in the reference design, respectively. A 800-V input voltage is applied. The load is switching from 1 A to 4 A with a period of 100 ms and a 50% duty cycle.

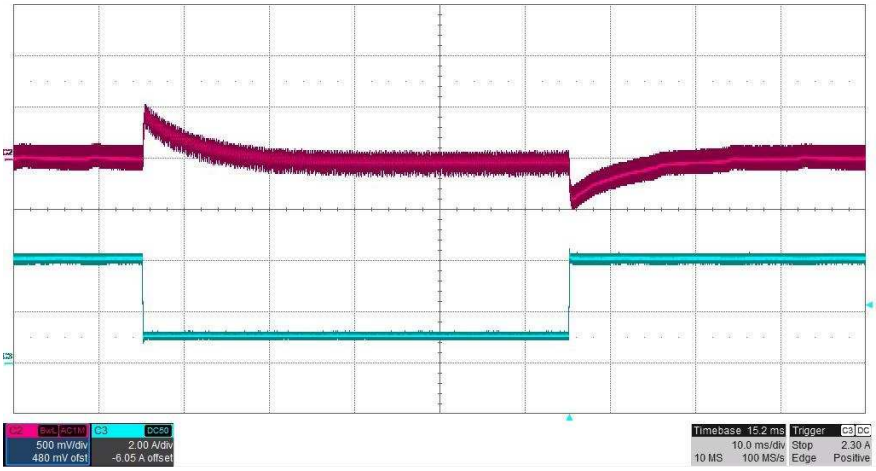


図 42. Load Transient Response of Flyback With Optocoupler Under V_{IN} = 800 V and I_{OUT} Switching Between 1 A and 4 A

注: (From top to bottom – CH2: Output voltage ripple, CH3: Load current)

図 43 shows the load transient response of the PSR Flyback converter when the input voltage is 800 V. The load is switching from 1 A to 4 A with a period of 100 ms and a 50% duty cycle.

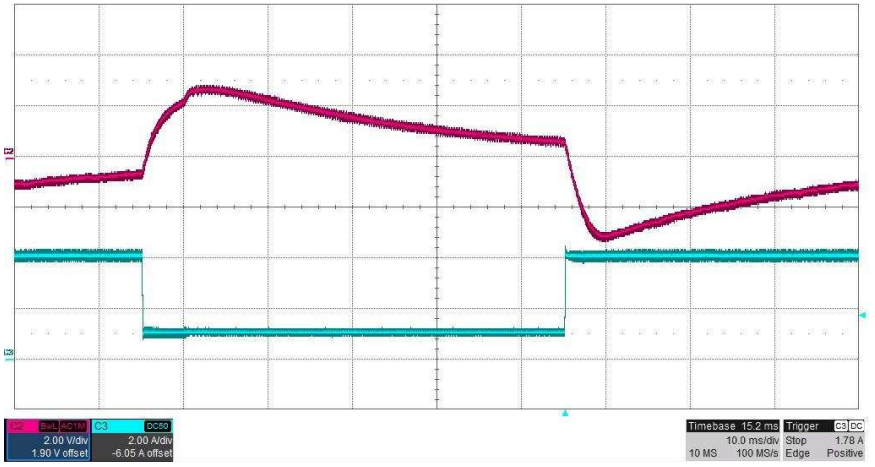


図 43. Load Transient Response of PSR Flyback Under V_{IN} = 800 V and I_{OUT} Switching Between 1 A and 4 A

注: (From top to bottom – CH2: Output voltage ripple, CH3: Load current)

3.2.10 Thermal Images

The thermal image of the design board is measured under a 600-V input voltage and full-load conditions. The circuit runs at the room temperature for 15 minutes. The converter is loaded with 4 A and the output power is 60 W. 図 44 shows the temperature of the transformer surface, PCB traces, heat sink of the secondary diode (D25), and the SiC MOSFET. The transformer area appears to have the highest temperature. The PCB traces, which are located next to the transformer, also appear to retain heat. The diode at the output and the SiC MOSFET are kept under cool temperature.

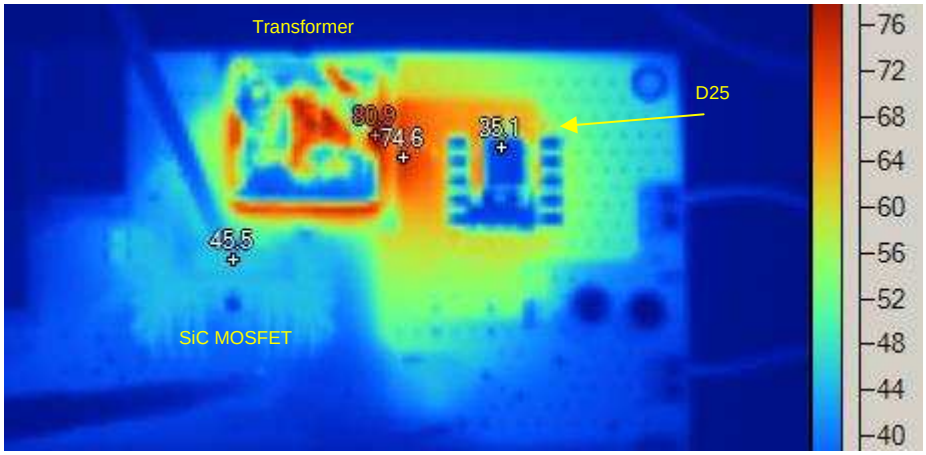


図 44. Thermal Image of Board Top Side

注: Measured at V_{IN} = 600 V, P_{OUT} = 60 W running for 20 minutes at room temperature

図 45 shows the temperature of the transformer winding. The peak temperature of the transformer winding reaches 113.4°C.

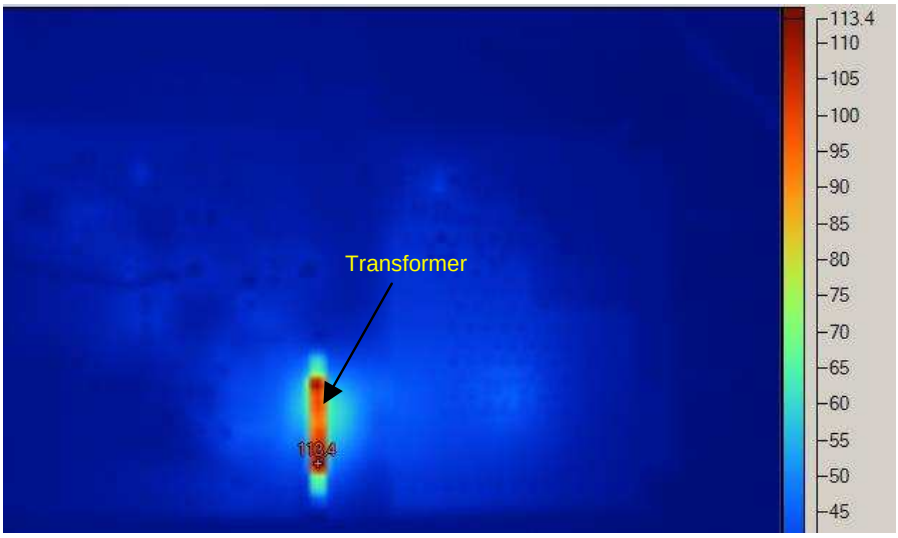


図 45. Thermal Image of Power Transformer

注: Measured at V_{IN} = 600 V, P_{OUT} = 60 W running for 20 minutes at room temperature

図 46 shows the temperature of the device ICs. The peak temperature is kept below 40°C.

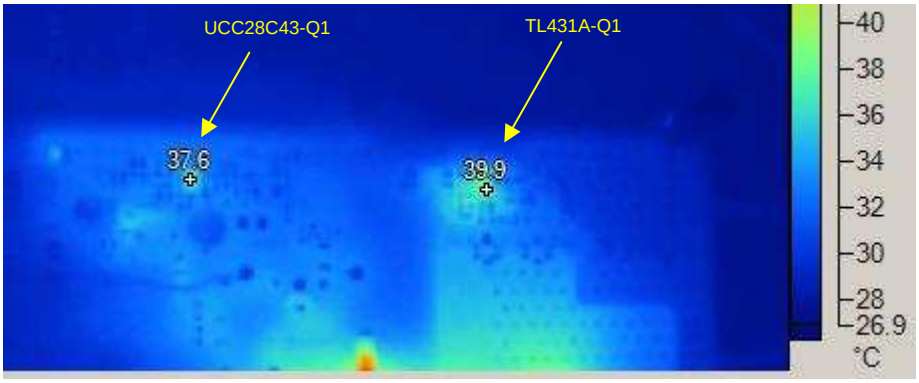


図 46. Thermal Image of Device ICs UCC28C43-Q1 and TL431A-Q1

注: Measured at V_{IN} = 600 V, P_{OUT} = 60 W running for 20 minutes at room temperature

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01505.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01505.

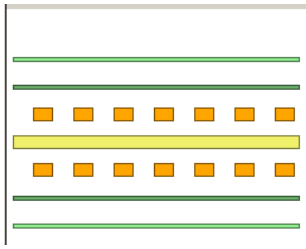
4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01505.

4.3.2 Layout Guidelines

This reference design implements a two-layer PCB. 図 47 shows the board material, copper thickness, and the dielectric distance in between.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Co Ex
Top Overlay	Overlay							
Top Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	Core	59.2	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

図 47. Layer Stack of TIDA-01505

図 48 shows the component placement for the main current-flowing loop. The input film capacitor, SiC MOSFET, and current sense resistors are placed as close as possible to the transformer T1 to minimize the loop.

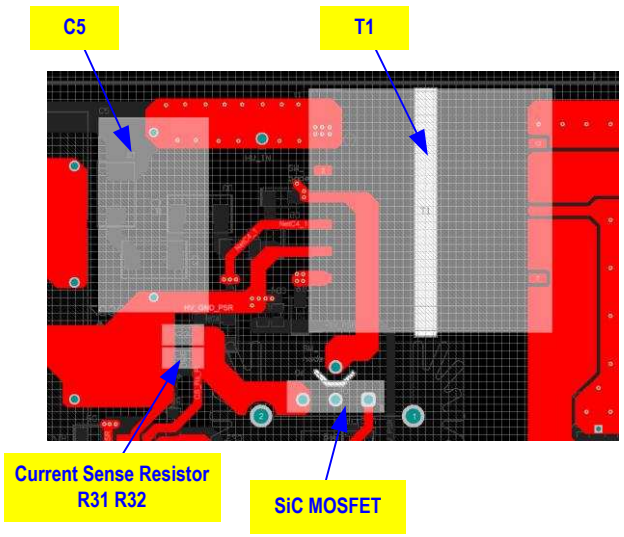


図 48. Component Placement of Main Current Flowing Loop

図 49 shows the component placement of the gate drive loop, which includes the storage capacitor C28, UCC28C43-Q1, gate resistors, SiC MOSFET, and current sense resistors. The PCB traces for current sensing are kept close and identical to minimize the differential noise crosstalks.

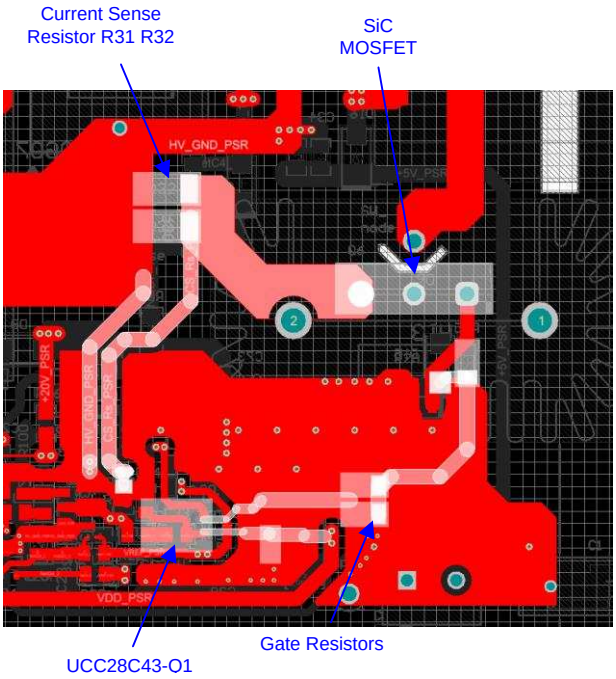


図 49. Component Placement of Gate Drive Loop

図 50 shows the component placement of the active start-up circuit. This circuit consists of the high-ohmic- and low-ohmic resistive lanes, and the two lanes are placed in parallel connecting the high-voltage side to the low-voltage side.

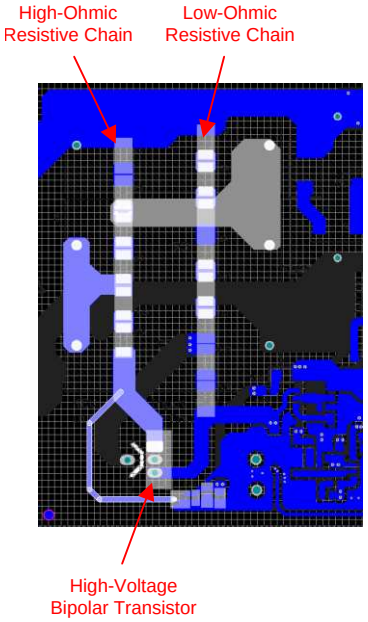


図 50. Component Placement of Active Start-Up Circuit

図 51 shows the component placement of the snubber network. This network is connected close between the transformer output and DC bus+ to minimize the current-flowing loop.

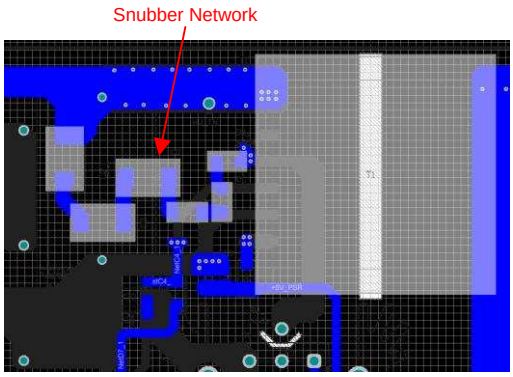


図 51. Component Placement of Snubber Network

図 52 shows the placement of components surrounding the UCC28C43-Q1 controller. The components are placed as close as possible to the IC to avoid any noise coupling. For more guidelines, see the section regarding layout guidelines in the UCC28C43-Q1 data sheet: *UCC28C4x-Q1 Automotive BiCMOS Low-Power Current-Mode PWM Controllers*.

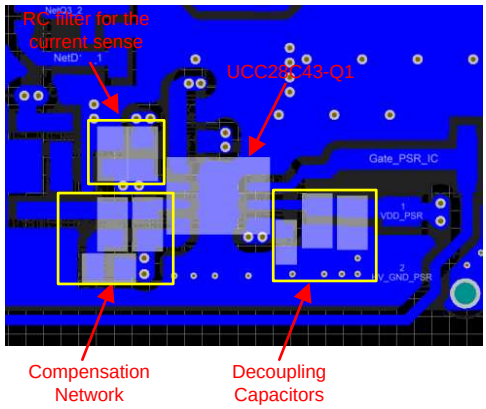


図 52. Component Placement Surrounding UCC28C43-Q1 Controller

4.4 Altium Project

To download the Altium project files, see the design files at

To download the bill of materials (BOM), see the design files at TIDA-01505.

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4.5 Gerber Files

To download the Gerber files, see the design files at

To download the bill of materials (BOM), see the design files at TIDA-01505.

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4.6 Assembly Drawings

To download the assembly drawings, see the design files at

To download the bill of materials (BOM), see the design files at TIDA-01505.

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5 Related Documentation

1. Texas Instruments, *Automotive Wide V_{IN} Front-End Power Reference Design With Cold Crank Operation and Transient Protections*
2. Texas Instruments, *MODELING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER*
3. Texas Instruments, *PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES*

5.1 商標

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6 Terminology

AEC— Automotive Electronics Council

AFE— Analog front end

BOM— Bill of materials

CISPR— International Special Committee on Radio Interference

CM— Common mode

CCM— Continuous conduction mode

DCM— Discontinuous conduction mode

DM— Differential mode

EMC— Electromagnetic compatibility

EMI— Electromagnetic interference

ESR— Equivalent series resistance

EV— Electric vehicle

HEV— Hybrid electric vehicle

MOSFET— Metal-oxide-semiconductor field-effect transistor

OEM— Original equipment manufacturer

PCB— Printed-circuit board

PE— Protective earth

PSR— Primary side regulation

RMS— Root mean square

UVLO— Undervoltage lockout

7 About the Author

XUN GONG is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the automotive segment in HEV/EV Power Train applications. Xun brings to this role expertise in the field of IGBT and SiC (Silicon Carbide) power transistors, Motor drive applications, non-isolated and isolated DC-DC converters up t 6.6 kilowatt. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the 1st prize papers of the Academic Journal *IEEE Transactions on Power Electronics* of 2014.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (February 2019) から **Revision B** に変更 **Page**

- UCC28C42-Q1 to *Highlighted Products* 追加 6
- 式 37 変更..... 15
- 式 38 変更..... 16
- 式 39 変更..... 16
- 式 40 変更..... 16

2018年2月発行のものから更新 **Page**

- ドキュメントのタイトルを「*回生ブレーキの安全性テストをサポートする車載用 40V～1kV 入力フライバックのリファレンス・デザイン*」から「*回生ブレーキのテストをサポートする車載用 40V～1kV 入力フライバックのリファレンス・デザイン*」に 変更 1
- ブロック図の画像 変更 1
- 基板の画像 変更 1
- the TIDA-01505 PCB board top side image 変更 22

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