参考資料

TI Designs: TIDA-01081
マシン・ビジョン用のLEDライティング制御のリファレンス・デザイン

概要

このLEDライティング制御のリファレンス・デザインでは、複数の大電力発光ダイオード(LED)ストリングを駆動および制御するための独自手法を紹介します。このリファレンス・デザインは、産業用マシン・ビジョン・システムを対象としており、他の産業用または車載用ライティング・アプリケーションにも適しています。このデザインにより、ユーザーはLEDの電流とタイミングをプログラムし、LEDを安全にオーバードライブして輝度を増すことができます。このデザインは自律的に動作できますが、トリガで起動したり、絶縁インターフェイス経由でトリガを生成したりもできます。内部回路ブロックは広い入力電圧範囲、プログラム可能な入力電流、および入力電力制御をサポートし、逆極性、過電圧、過熱保護も行います。

リソース

デザイン・フォルダ

TIDA-01081

プロダクト・フォルダ

TPS92515HV	TPS92561	TPS26602	LM5165
DAC082S085	REF3025	INA169	DAC7311
MSP430F5172	ISOW7842	LP5907	TPS22810
TPS7A4101	UCC27511	TLV3201	TMP116
SN74LVC1G175	SN74LVC1G02	CSD18543Q3A	CSD15380F3
SN74LVC1G17	SN74LVC1G14	TPD1E10B06	

TI E2E™ Community

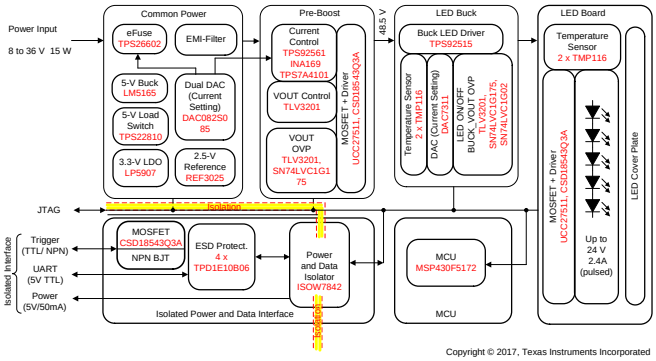
E2E™エキスパートに質問

特長

- 最大24VのLEDストリング電圧
- 複数のパラメータをプログラム可能:
  - LED電流: 200mA～2.4A
  - LEDモード: 連続または200ns～4.9sのパルス
  - LEDパルスの繰り返し: 0.2Hz～10kHz
  - トリガ遅延時間: トリガ入力について10µs
  - マルチ・パルス時間、および電流ブラケット処理によりAEBおよびHDRイメージングをサポート
- デュアル電力段のカスケード:
  - プリブースト: 広い8V～36V、15Wのシステム入力、適応型インダクタ電流制限付き
  - バック: 高速インダクタ電流ランプ処理
- 絶縁されたトリガおよびUARTインターフェイス
  - 絶縁された5V、50mA出力
  - シンキングNPN-およびTTLトリガINおよびOUT
- eFuse: 逆極性保護、適応型過電流制限、および入力電力制限
- 包括的なシステムの監視および保護
  - オンボードの温度センサおよび電圧監視機能
  - 超高速の出力過電圧保護
- EEPROMに最大256ビットのユーザー・データを保存

アプリケーション

- マシン・ビジョンおよびロジスティクス
  - ライティングおよび照明ソリューション
  - カメラ
  - コード・リーダー
  - バーコード・スキャナ
- 産業用ライティング
- 車載照明



1 System Description

CAUTION:

Do not leave this reference design powered when unattended.

HOT SURFACE:

Contact may cause burns. Do not touch. Take the proper precautions when operating.

LED Safety Guidelines

CAUTION

Retinal blue light or thermal hazard = 400-nm to 780-nm wavelength.

The high-power LEDs used and controlled in this reference design are in excess of the LED Exempt Risk Group. The viewer-related risk is dependent upon how the user installs and uses this reference design.

LEDs contained on this board are Risk Group 2, and reduce to Risk Group 1 at a distance > 0.5 m. To minimize risk of eye injury, never stare at operating LEDs as may be harmful to the eyes.

WARNING

To minimize risk of eye injury, do not remove LED cover plate.

Intense light sources have a high secondary blinding effect. A temporary reduction in visual acuity and afterimages can occur, leading to irritation, annoyance, visual impairment, and even accidents—depending on the situation.

Always consider the use of light filtering and darkening protective eye wear and be fully aware of surrounding laboratory type setups when viewing intense light sources to minimize or eliminate such risks to avoid accidents related to temporary blindness.

This reference design is designed with the requirements of machine vision applications for factory automation and logistics in mind. Machine vision has proven itself as a key technology, addressing the needs of automated manufacturing, including inspection, identification, quality control and logistics. The illumination solution and lighting control of machine vision systems play a major role to meet the challenging requirements of modern imaging solutions regarding increased production speed and effectiveness. The illumination and lighting control applications can be found as separate end equipment, but can be also found as integrated parts of cameras, code readers, or barcode scanners.

These applications have common requirements such as:

- Using high-power LEDs as a source of light
- Programmable LED current as a direct measure of light brightness, including a safe overdriving of the LEDs during pulsed operation with short LED ON-times
- Precise timing control, including autonomous and synchronized (externally triggered) operation with short trigger delay time

- Continuous ON as well as pulsed operation of the LEDs
- Support of LED ON-times down to the µs range to avoid or reduce motion blurs (this includes ultra-fast ramping up or down of the LED current)
- Pulse repetition frequencies up to 1 kHz or above to support the frame rate requirements of high-speed imaging
- Wide supply input voltage range, supporting standard 24-V power sources as found in industrial applications, but also other standard voltages like 12 V or 15 V

This reference design for LED lighting control reflects the market trend of using high-power LEDs as the light source. The design demonstrates how to drive those LEDs with a programmable constant current up to 2.4 A provided by a dedicated buck LED driver. A strobe repetition frequency (frame rate) of up to 10 kHz and a configurable pulse width down to 200 ns match the requirements of light sources needed for high-speed imaging. A digital-to-analog converter (DAC) is used to set the output current of the *LED buck*. The output voltage of the LED buck and the temperature of the buck LED driver as well as the buck inductor are supervised to protect against overvoltage and overtemperature. Each of the used temperature sensors offer 64 bits of user programmable EEPROM, which allows the user to save and read data for board identification, configuration, parameter sets, or other purposes.

A *pre-boost* converter enables operation over an 8-V to 36-V input voltage range. This wide input voltage range ensures that this reference design can use 12-V, 15-V, or 24-V power supplies as input power source. The pre-boost provides a regulated 48.5-V output, serving as the input for the downstream LED buck. The output of the pre-boost is supervised by a dedicated overvoltage protection (OVP) circuitry.

The pre-boost is equipped with an adaptive average input current limit and an energy storing bank of output capacitors. Those two features together avoid overloading of the input power source of the reference design while enabling a much higher instantaneous power level to drive the LEDs. The adaptive average input current limit of the pre-boost results in an 8-W to 10-W input power limit while the LEDs are driven with a peak pulse power of up to 40 W in the exemplary case of this reference design.

The *common power* block of the design uses an eFuse as a second level of a smart input current and input power limit. The input current limit of the reference design can be a selectable fixed value or to be adaptive to the output voltage of the input power source. The adaptive option limits the reference design's input power to a range of 12 W to 15 W, which avoids the need for oversized power supplies. The common power block contains further a 5-V buck and load switch, a 3.3-V LDO, and a 2.5-V reference, providing the needed point-of-load rails as well as their sequencing. The dual DAC of the common power block controls the adaptive current limit of the eFuse and of the pre-boost.

The reference design uses an exemplary string of five white high-power LEDs on a separate *LED board* for the purpose of demonstrating the feature set of the design. The need for ultra-fast ON- and OFF-switching of the LEDs is addressed by separate MOSFETs and their driver circuits on the LED board.

The *MCU* block of the reference design controls the ON- and OFF-timing of the LEDs and the value of the LED current. This flexible control allows the user to set up this reference design to generate single pulses as well as multiple pulses (burst) with an identical pulse width or with a progressively rising pulse width. The reference design can also demonstrate how a sequence of pulses with changing intensity can be generated. The latter two features are a pre-requisite to enable automatic exposure bracketing (AEB) and high dynamic range (HDR) imaging.

The MCU block interfaces furthermore with the eFuse and pre-boost, controls the sequencing of the 5-V rails, and monitors important system voltages and currents as well as the temperature data and content of the total 256 bits of general purpose EEPROM provided by the four temperature sensors.

The reference design features an *isolated power and data interface* to enable trouble-free communication with a notebook or PC and triggering from external sources. The isolated UART interface supports configuration, monitoring and control of the design through a simple terminal software. The isolated interface provides furthermore an isolated 5-V rail, which can be loaded with up to 50 mA.

Besides its use in machine vision and logistics applications, the different blocks of this reference designs can also be adapted and modified for usage in industrial and automotive lighting applications.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
POWER INPUT		
Input voltage	8 V to 36 V	—
eFuse current limit	Selectable: 500 mA , 770 mA, 1 A Adaptive to provided input voltage to limit input power to 15 W for input voltage of 8 V to 36 V	2.4.1.5
LED OUTPUT		
LED string voltage	Up to 24 V	2.4.1.1
Average LED current (brightness control)	200 mA to 2.4 A Programmable in steps of 50 mA	
Pulse width	200 ns to 4.9 s; programmable	3.1.2.1
Pulse rise- and fall-time	< 40 to 100 ns; depends on LED current	
Maximum duty cycle	1% to 100%; programmable; depends on LED current	
Pulse repetition frequency (frame rate)	0.2 Hz to 10 kHz; programmable	
ISOLATED TRIGGER INTERFACE		
Isolated power output	5 V / 50 mA	2.4.1.6
Isolated trigger input	Trigger delay time: 10 µs Inverting TTL-IN Non-inverting NPN-Sourcing-IN (pullup resistor)	
Isolated trigger output	Delay time: –6.5 µs Non-inverting TTL-OUT Inverting NPN-Sinking-OUT (open drain output)	
Isolated UART	TTL-IN (RXD) TTL-OUT (TXD)	
MODES OF OPERATION		
Continuous		For combinations and limitations, see 3.1.2.3
Pulsed		
Externally triggered		
Standalone (internally triggered)		
Switched		
Multi-pulsed		
Automatic exposure bracketing (AEB)		

2 System Overview

2.1 Block Diagram

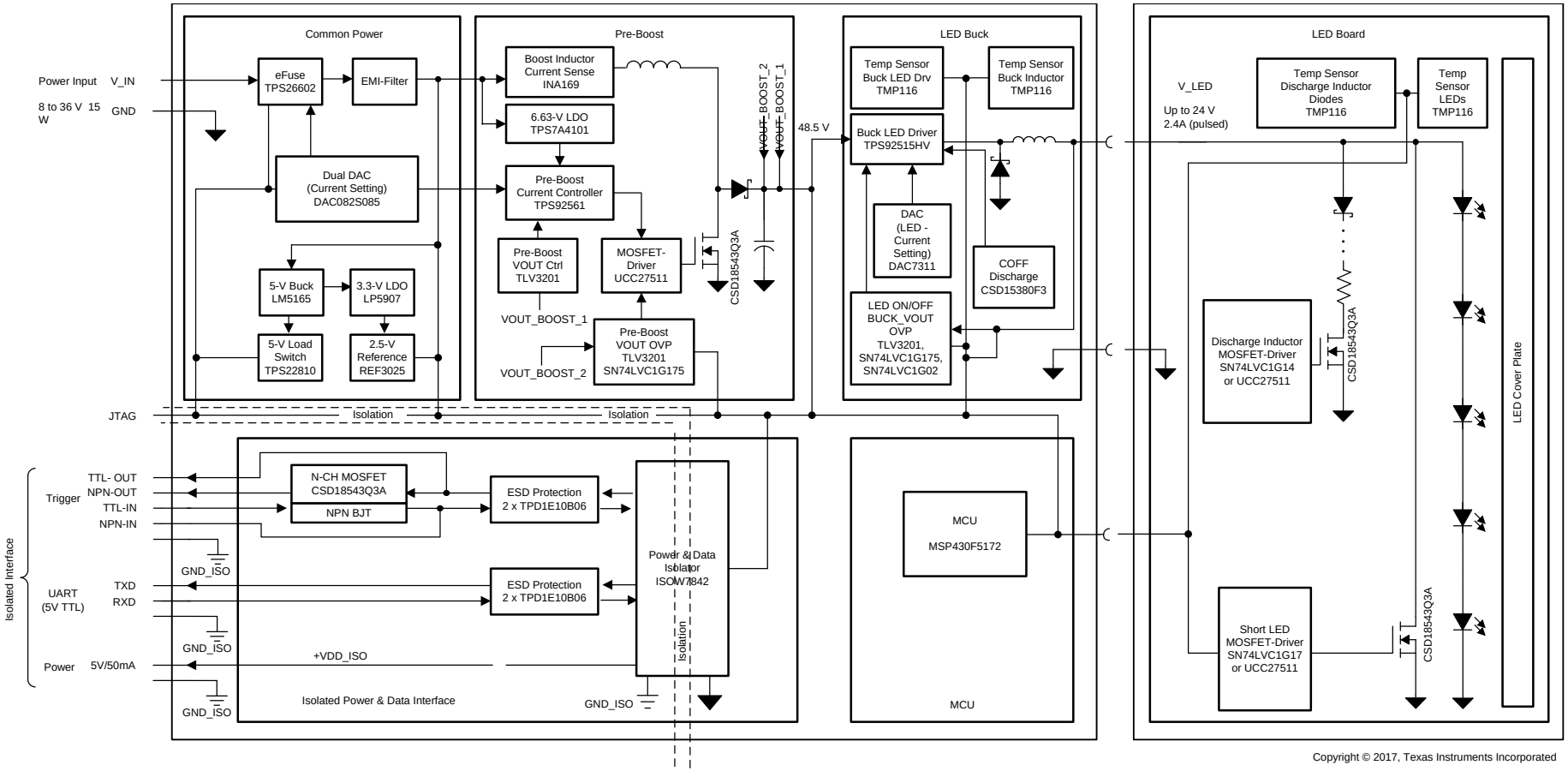


図 1. TIDA-01081 Block Diagram

2.2 Highlighted Products

2.2.1 TPS92515HV

The TPS92515HV is a compact, monolithic switching regulator integrating a low resistance N-Channel MOSFET. The device is intended for high-brightness LED lighting applications where efficiency, high bandwidth, PWM, analog dimming, and small size are important. The regulator operates using a constant off-time, peak current control. After an off-time based on the output voltage, an on-time begins. The on-time ends once the inductor peak current threshold is reached. The TPS92515HV can be configured to maintain a constant peak-to-peak ripple during the ON and OFF periods of a shunt FET dimming cycle. This constant peak-to-peak ripple is ideal for maintaining a linear response across the entire shunt FET dimming range. Steady-state accuracy is aided by the inclusion of a low-offset, high-side comparator. LED current can be modulated using either analog or PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, inherent LED open operation, and a wide operating temperature range with thermal shutdown. The TPS92515HV offers a high input voltage range of up to 65 V. The device is available in a thermally enhanced 10-pin HVSSOP package.

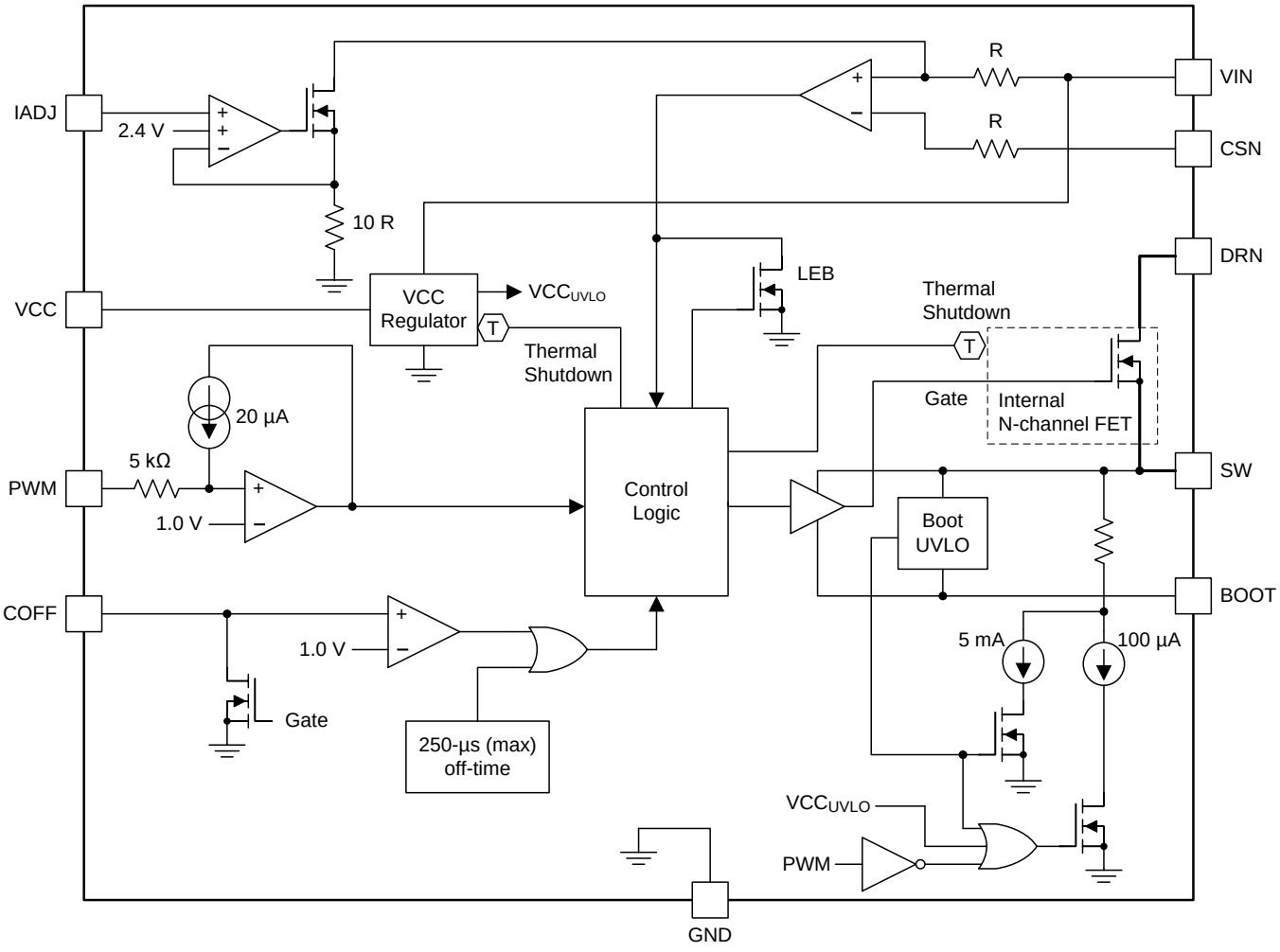


図 2. Functional Block Diagram of TPS92515HV

2.2.2 TPS92561

The TPS92561 device is a boost controller for LED lighting applications using high-voltage, low-current LEDs. A boost converter approach to lighting applications allows the creation of the smallest volume converter possible and enables high efficiencies beyond 90%. The device incorporates a current sense comparator with a fixed offset enabling a simple hysteretic control scheme free of the loop compensation issues typically associated with a boost converter. The integrated OVP and VCC regulator further simplify the design procedure and reduce external component count.

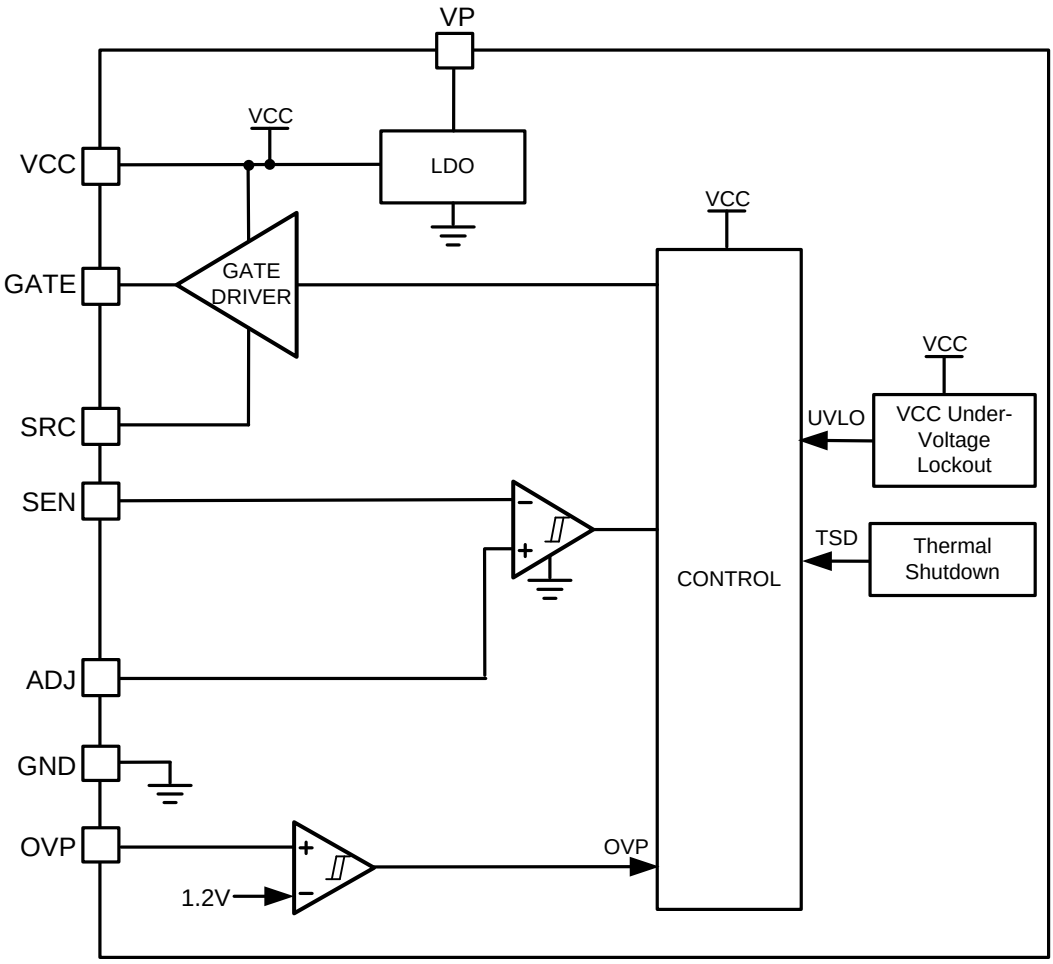


図 3. Functional Block Diagram of TPS92561

2.2.3 TPS26602

The TPS26602 device is a compact and feature rich high-voltage eFuse with a full suite of protection features. The wide supply input range of 4.2 V to 55 V allows the device to control many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. Integrated back-to-back FETs provide a reverse current blocking feature, making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source, and device protections are provided with many adjustable features including overcurrent, output slew rate, and overvoltage and undervoltage thresholds. The internal robust protection control blocks along with the high-voltage rating of the TPS26602 help simplify the system designs for surge protection. A shutdown pin provides external control for enabling and disabling the internal FETs as well as placing the device in a low-current shutdown mode. To monitor system status and downstream load control, the device provides fault and precise current monitor output. The MODE pin allows flexibility to configure the device between the three current-limiting fault responses (circuit breaker, latch off, and auto-retry modes). The devices are available in a 5-mm × 4.4-mm 16-pin HTSSOP as well as 5-mm × 4-mm 24-pin VQFN package and are specified over a –40°C to +125°C temperature range.

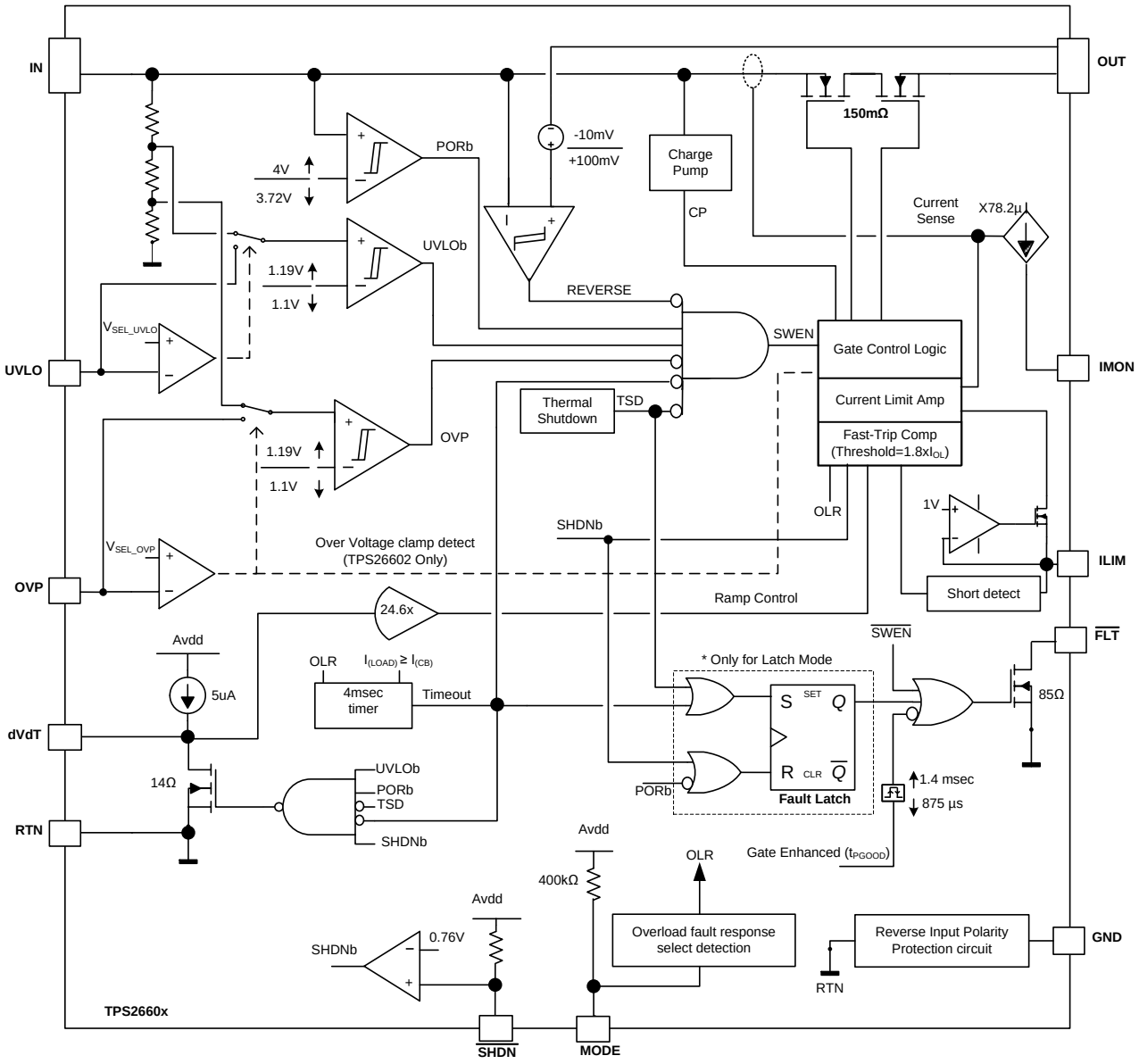


図 4. Functional Block Diagram of TPS2660x

2.2.4 LM5165

The LM5165 device is a compact, easy-to-use, 3-V to 65-V, ultra-low I_Q synchronous buck converter with high efficiency over wide input voltage and load current ranges. With integrated high-side and low-side power MOSFETs, up to 150 mA of output current can be delivered at fixed output voltages of 3.3 V or 5 V or at an adjustable output. The converter is designed to simplify implementation while providing options to optimize the performance for the target application. Pulse frequency modulation (PFM) mode is selected for optimal light-load efficiency or constant on-time (COT) control for nearly constant operating frequency. Both control schemes do not require loop compensation while providing excellent line and load transient response and short PWM on-time for large step-down conversion ratios. The high-side P-channel MOSFET can operate at a 100% duty cycle for lowest dropout voltage and does not require a bootstrap capacitor for the gate drive. Also, the current limit setpoint is adjustable to optimize the inductor selection for a particular output current requirement. Selectable and adjustable start-up timing options include minimum delay (no soft start), internally fixed (900 µs), and externally programmable soft start using a capacitor. An open-drain PGOOD indicator can be used for sequencing, fault reporting, and output voltage monitoring. The LM5165 buck converter is available in a 10-pin, 3-mm × 3-mm, thermally-enhanced VSON-10 package with a 0.5-mm pin pitch.

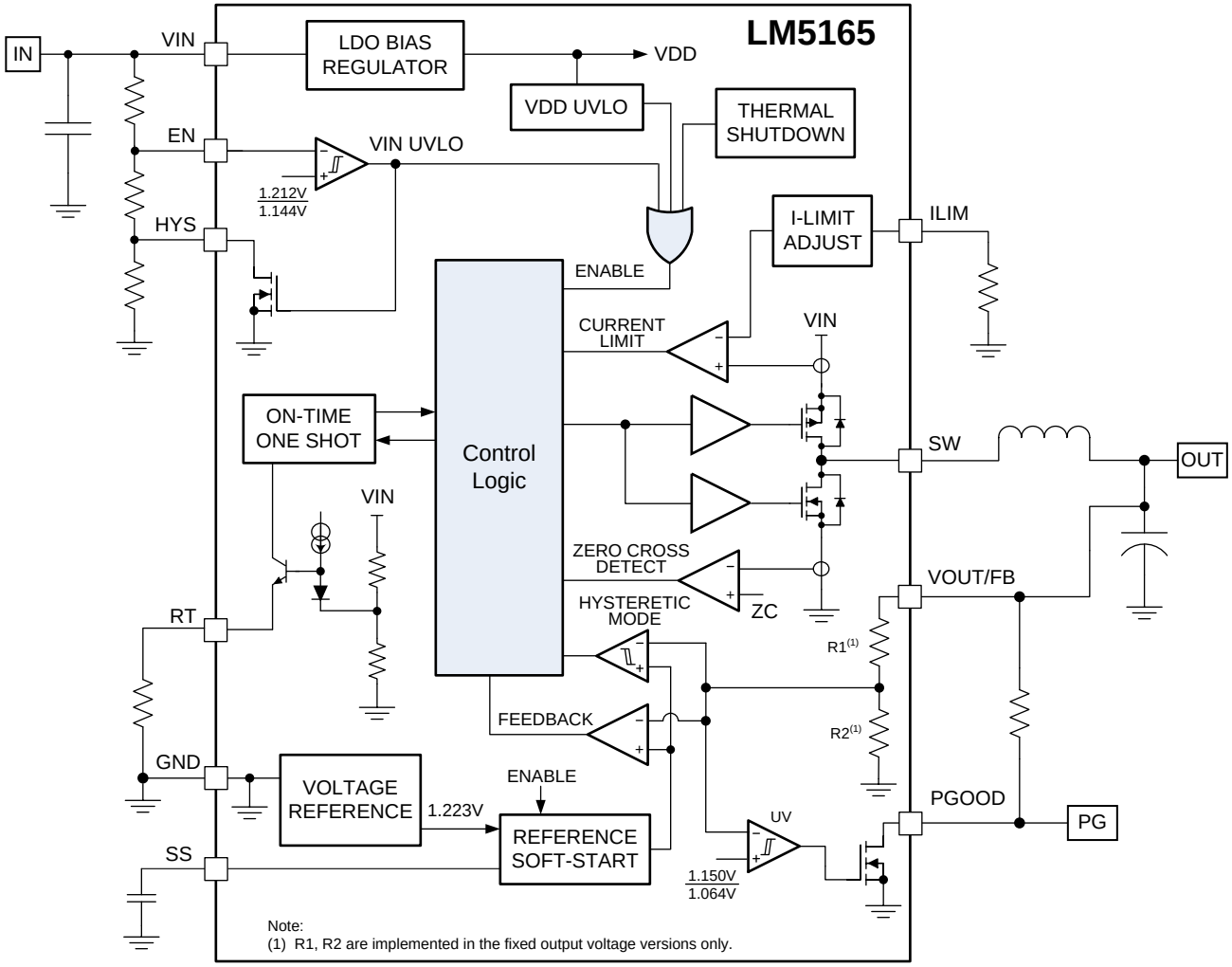


図 5. Functional Block Diagram of LM5165

2.2.5 DAC082S085

The DAC082S085 device is a full-featured, general-purpose, dual, 8-bit, voltage-output DAC that can operate from a single 2.7-V to 5.5-V supply and consume 0.6 mW at 3 V and 1.6 mW at 5 V. The DAC082S085 is packaged in 10-pin SON and VSSOP packages. The 10-pin WSON package makes the DAC082S085 the smallest dual DAC in its class. The on-chip output amplifier allows rail-to-rail output swing, and the three-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25-MHz clock rates at supply voltages in the 2.7-V to 3.6-V range. The serial interface is compatible with standard SPI™, QSPI™, MICROWIRE, and DSP interfaces.

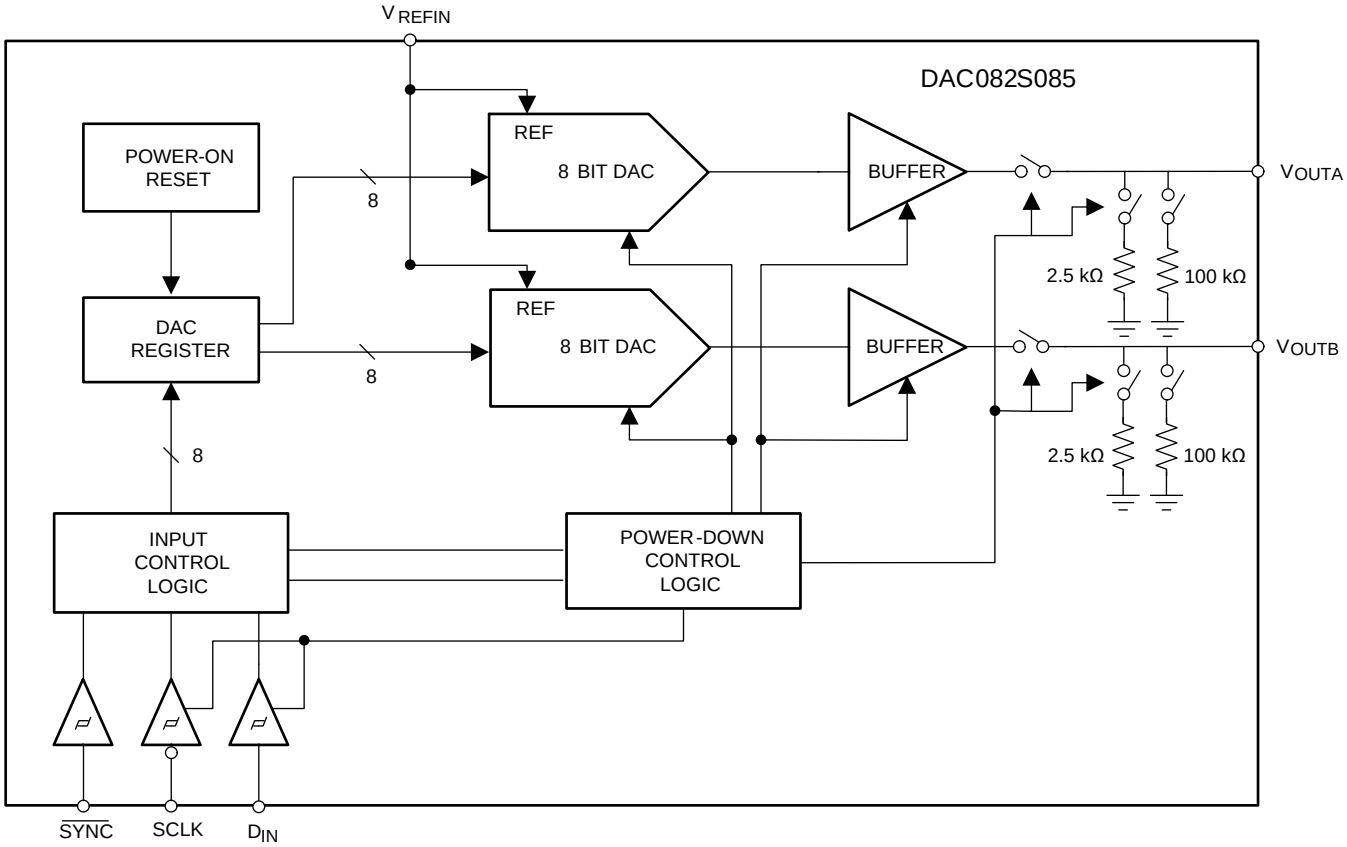


図 6. Functional Block Diagram of DAC082S085

2.2.6 REF3025

The REF3025 is a precision, low-power, low dropout voltage reference available in a tiny SOT-23-3 package. The REF3025 offers excellent temperature drift and initial accuracy while operating at a quiescent current of 42 µA (typical). The low power consumption and the relatively high precision make the REF3025 very attractive for loop-powered industrial applications such as pressure and temperature transmitter applications. The REF3025 is easy to use in intrinsically safe and explosion-proof applications because it does not require a load capacitor to be stable. The REF3025 is specified over the extended industrial temperature range of –40°C to +125°C. The REF3025 operates with supplies within 1 mV of output voltage under zero-load conditions. The low dropout along with small size and low power consumption make The REF3025 ideal for portable and battery-powered applications.

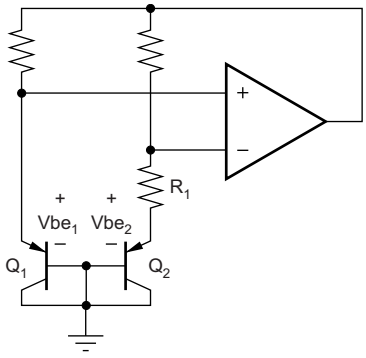


図 7. Functional Block Diagram of REF3025

2.2.7 INA169

The INA169 is a high-side, unipolar, current shunt monitor. Its wide input common-mode voltage range, high speed, low quiescent current, and tiny SOT-23 packaging enable use in a variety of applications. Input common-mode and power supply voltages are independent and can range from 2.7 V to 60 V for the INA169. The quiescent current of the device is only 60 µA, which permits connecting the power supply to either side of the current measurement shunt with minimal error. The device converts a differential input voltage to a current output. This current is converted back to a voltage with an external load resistor that sets any gain from 1 to over 100. Although designed for current shunt measurement, the circuit invites creative applications in measurement and level shifting. The INA169 is available in a 5-pin SOT-23 package. The INA169 is specified from –40°C to +85°C.

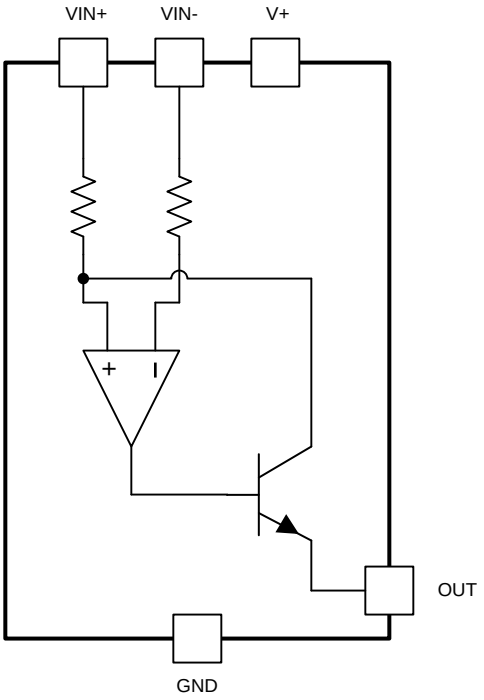


図 8. Functional Block Diagram of INA169

2.2.8 DAC7311

The DAC7311 (12-bit) device is a low-power, single-channel, voltage output DAC. The low power consumption of this device in normal operation (0.55 mW at 5 V, reducing to 2.5 µW in power-down mode) makes it ideally suited for portable, battery-operated applications. This DAC is monotonic by design, provides excellent linearity, and minimizes undesired code-to-code transient voltages while offering an easy upgrade path within a pin-compatible family. This device uses a versatile, three-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces. The DAC7311 uses an external power supply as a reference voltage to set the output range. The device incorporates a power-on reset (POR) circuit that ensures the DAC output powers up at 0 V and remains there until a valid write to the device occurs. The DAC7311 contains a power-down feature, accessed over the serial interface, that reduces current consumption of the device to 0.1 µA at 2.0 V in power-down mode. This device is pin-compatible with the DAC8311 and DAC8411, offering an easy upgrade path from 8-, 10-, and 12-bit resolution to 14- and 16-bit. The DAC7311 is available in a small, 6-pin, SC70 (SOT) package. This package offers a flexible, pin- and function-compatible, drop-in solution within the family over an extended temperature range of –40°C to +125°C.

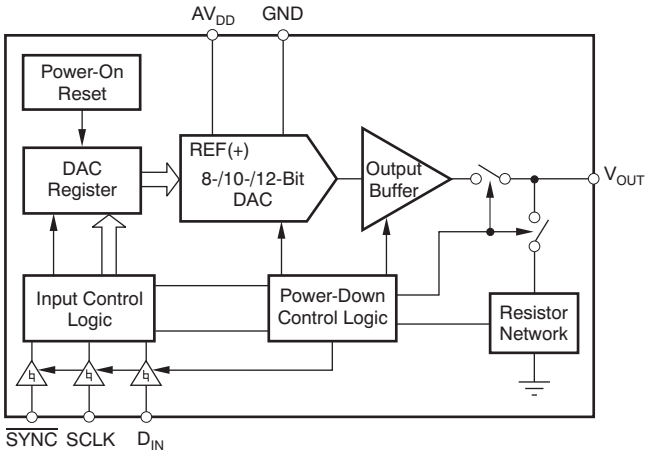


図 9. Functional Block Diagram of DAC7311

2.2.9 MSP430F5172

The TI MSP family of ultra-low-power microcontrollers (MCUs) consists of several devices featuring different sets of peripherals targeted for various applications. Combined with five low-power modes, the architecture is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs. The MSP430F5172 MCUs include two 16-bit high-resolution timers, two USCIs (USCI_A0 and USCI_B0), a 32-bit hardware multiplier, a high-performance 10-bit analog-to-digital converter (ADC), an on-chip comparator, a 3-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins. Typical applications for this device includes analog and digital sensor systems, LED lighting, digital power supplies, motor controls, remote controls, thermostats, digital timers, and handheld meters.

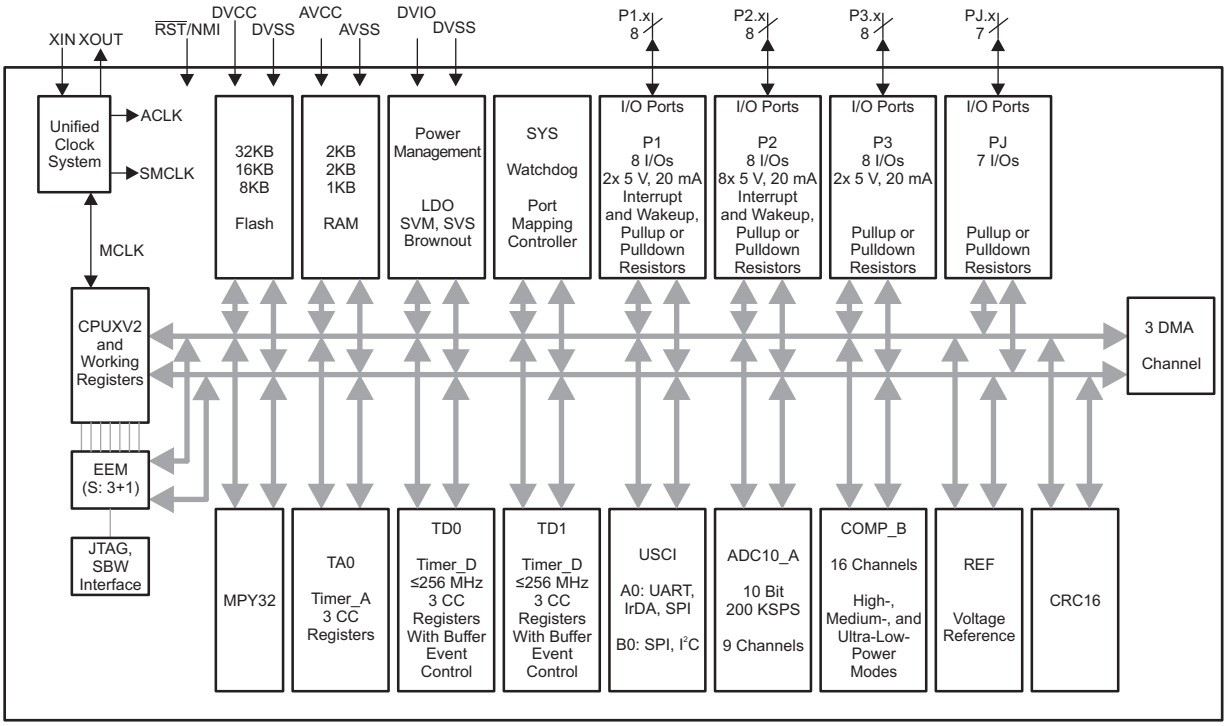


図 10. Functional Block Diagram of MSP430F5172

2.2.10 ISOW7842

The ISOW7842 is a high-performance, quad-channel reinforced digital isolator with an integrated high-efficiency power converter. The integrated DC/DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore, this device eliminates the need for a separate isolated power supply in space-constrained isolated designs. The ISOW7842 device provides high electromagnetic immunity (EMI) and low emissions while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. Various configurations of forward and reverse channels are available. If the input signal is lost, the default output is high for the ISOW7842 and low for the devices with the F suffix. This device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISOW7842 device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The high-efficiency of the power converter allows operation at a higher ambient temperature. The ISOW7842 device is available in a 16-pin SOIC wide-body (SOIC-WB) DWE package.

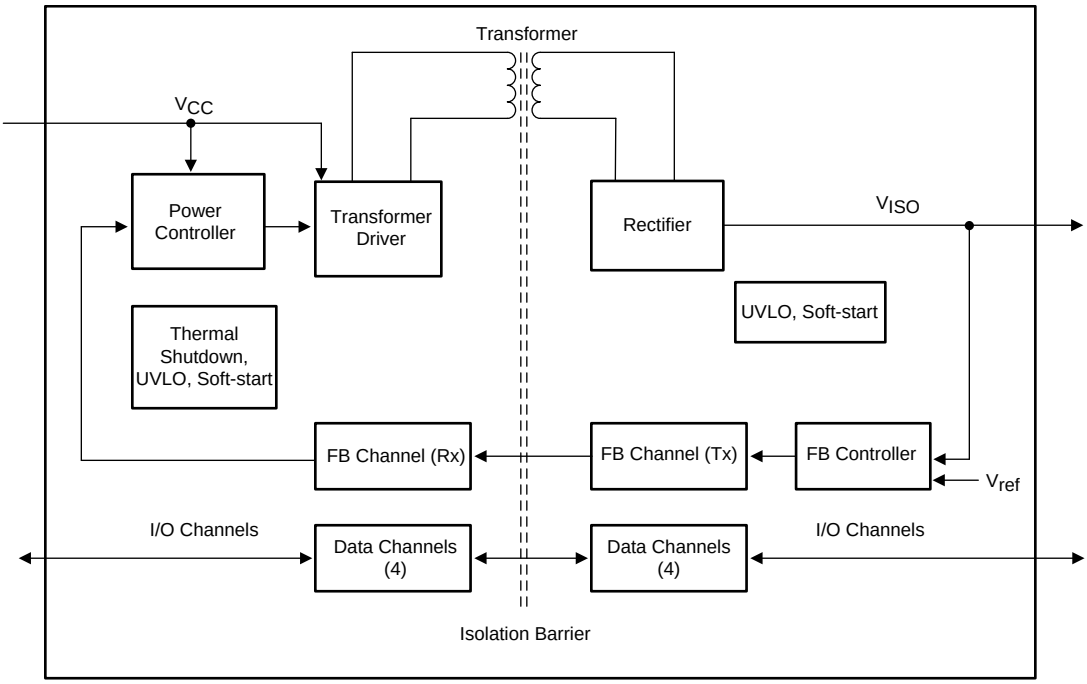


図 11. Functional Block Diagram of ISOW784x

2.2.11 LP5907

The LP5907 is a low-noise LDO that can supply up to a 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement. The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor (no separate noise bypass capacitor is required). This device is available with fixed output voltages from 1.2 V to 4.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

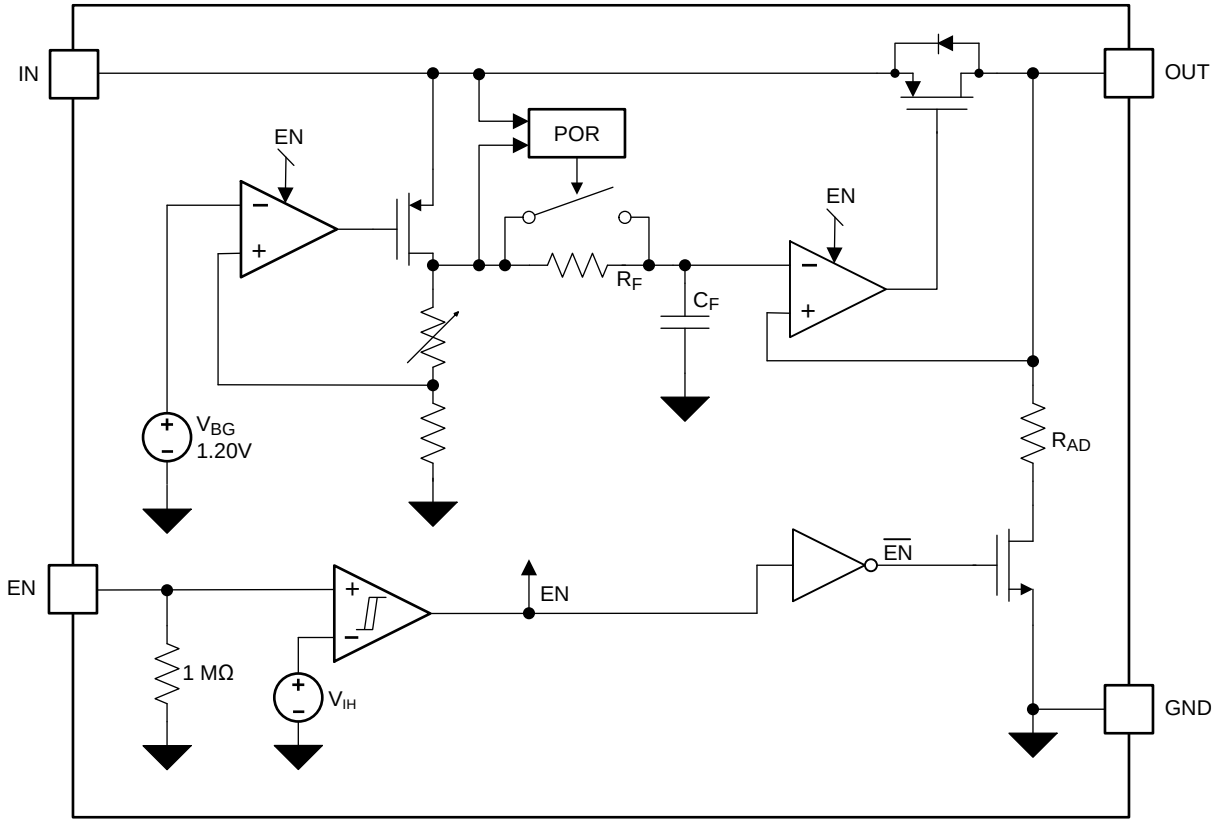


図 12. Functional Block Diagram of LP5907

2.2.12 TPS22810

The TPS22810 is a single-channel load switch with a configurable rise time and with an integrated quick output discharge (QOD). In addition, the device features thermal shutdown to protect the device against high junction temperature. Because of this, the safe operating area of the device is inherently ensured. The device contains an N-channel MOSFET that can operate over an input voltage range of 2.7 V to 18 V. A SOT23-5 (DBV) package can support a maximum current of 2 A. A WSON (DRV) package can support a maximum current of 3 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals. The configurable rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. UVLO is used to turn off the device if the V_{IN} voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged by being supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device to allow design flexibility for power down. The TPS22810 is available in a leaded, SOT-23 package (DBV), which allows to visually inspect solder joints as well as a WSON package (DRV). The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

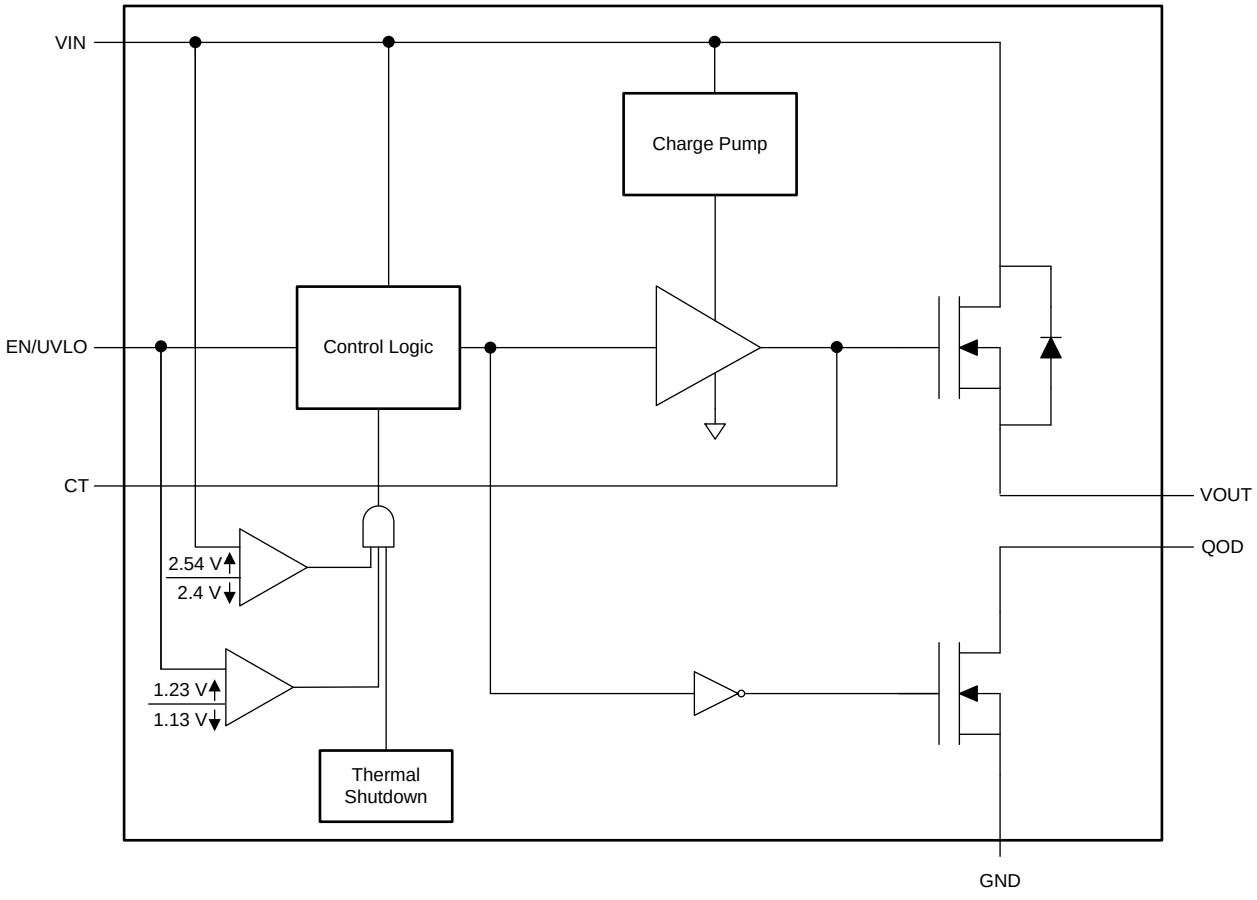


図 13. Functional Block Diagram of TPS22810

2.2.13 TPS7A4101

The TPS7A4101 device is a very high-voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8) and is able to withstand continuous DC or transient input voltages of up to 50 V. The TPS7A4101 is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (over temperature and tolerance). Thus, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A4101 offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode. The TPS7A4101 has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 packages has an operating temperature range of T_J = –40°C to +125°C. In addition, the TPS7A4101 is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only can the device supply a well-regulated voltage rail, but it can also withstand and maintain regulation during very high and fast voltage transients. These features translate to a simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications.

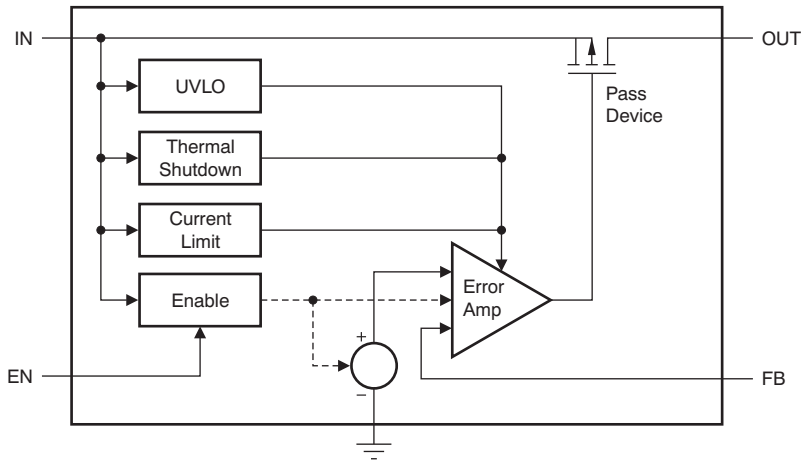


図 14. Functional Block Diagram of TPS7A4101

2.2.14 UCC27511

The UCC27511 device is a single-channel, high-speed, low-side gate driver that can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC27511 is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 13 ns. The UCC27511 features a dual-input design, which offers flexibility of implementing both inverting (IN– pin) and non-inverting (IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For safety purposes, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when input pins are in floating condition. Hence the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation. The input pin threshold of the UCC27511 device is based on TTL and CMOS-compatible low-voltage logic, which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity. The UCC27511 provides a 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turnon effect. The UCC27511 device also features a unique split output configuration where the gate drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins, respectively, and easily control the switching slew rates. The UCC27511 device is designed to operate over a wide VDD range of 4.5 V to 18 V and a wide temperature range of –40°C to +140°C. The internal UVLO circuitry on the VDD pin holds output low outside the VDD operating range.

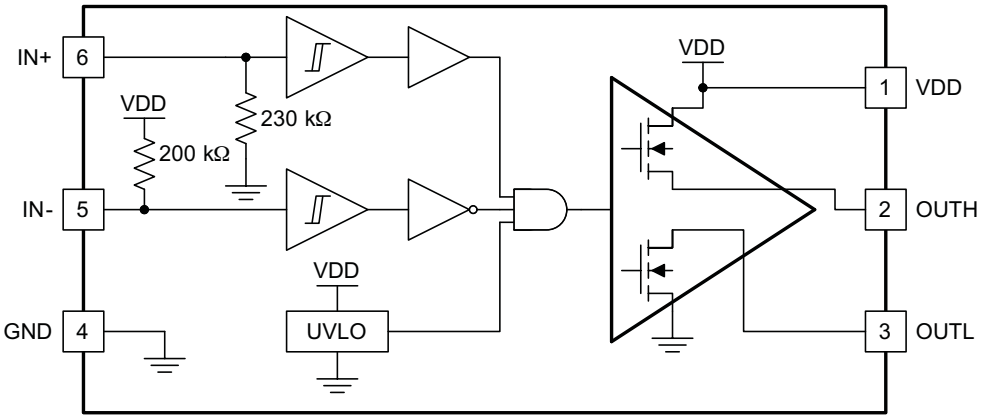


図 15. Functional Block Diagram of UCC27511

2.2.15 TLV3201

The TLV3201 is a single-channel comparator that offers the ultimate combination of high speed (40 ns) and low-power consumption (40 µA), all in an extremely small package with features such as rail-to-rail inputs, low offset voltage (1 mV), and large output drive current. The device is also very easy to implement in a wide variety of applications where response time is critical. The TLV3201 comparator is available with push-pull outputs. The TLV3201 is available in 5-pin SOT-23 and 5-pin SC70 packages. This devices is specified to operate across the expanded industrial temperature range of –40°C to +125°C.

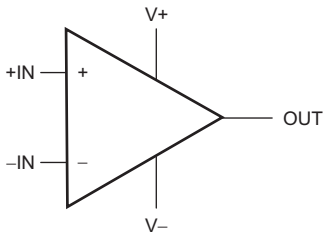


図 16. Functional Block Diagram of TLV3201

2.2.16 TMP116

The TMP116 (TMP116, TMP116N) is a family of low-power, high-precision temperature sensors with integrated EEPROM memory. The TMP116 provides a 16-bit temperature result with a resolution of 0.0078°C and an accuracy of up to ±0.2°C with no calibration. The TMP116 is I^2C- and SMBus-interface compatible, has programmable alert functionality, and can support up to four devices on a single bus. In addition to providing power savings, the TMP116 consumes minimal current that minimizes self-heating and improves measurement accuracy. The TMP116 operates from 1.9 V to 5.5 V and typically consumes 3.5 µA. Across the device operating temperature range of –55°C to +125°C, the TMP116 exceeds the accuracy of a class A RTD, while consuming less than one fifth of the typical excitation current for a PT100 RTD. The TMP116 is easier to use than RTDs, eliminating the need for calibration, external circuitry, matched traces, and Kelvin connections. The TMP116 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO and IEC 17025 accredited standards.

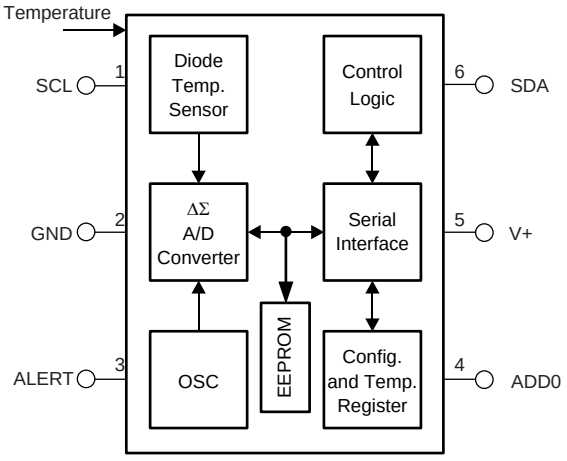


図 17. Functional Block Diagram of TMP116

2.2.17 SN74LVC1G175

This single D-type flip-flop is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC1G175 device has an asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is high, data from the input pin (D) is transferred to the output pin (Q) on the rising edge of the clock (CLK). When $\overline{CLR}$ is low, Q is forced into the low state, regardless of the clock edge or data on D. NanoFree™ package technology is a major breakthrough in device packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

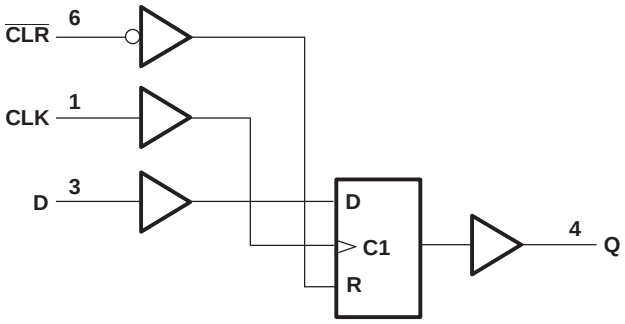


図 18. Functional Block Diagram of SN74LVC1G175

表 2. Function Table of SN74LVC1G175

INPUTS			OUTPUT Q
$\overline{CLR}$	CLK	D	
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_0
L	X	X	L

2.2.18 SN74LVC1G02

This single, two-input, positive-NOR gate is designed for a 1.65-V to 5.5-V VCC operation. The SN74LVC1G02 performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \times \overline{B}$ in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad VCC operating range. The SN74LVC1G02 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 × 0.8 mm.

図 19. Functional Block Diagram of SN74LVC1G02

表 3. Function Table of SN74LVC1G02

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

2.2.19 SN74LVC1G17

This single Schmitt trigger buffer is designed for a 1.65-V to 5.5-V VCC operation. The SN74LVC1G17 device contains one buffer and performs the Boolean function Y = A. The CMOS device has high output drive while maintaining low static power dissipation over a broad VCC operating range. The SN74LVC1G17 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

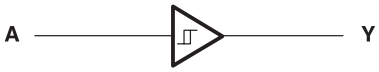


図 20. Functional Block Diagram of SN74LVC1G17

表 4. Function Table of SN74LVC1G17

INPUT A	OUTPUT Y
H	H
L	L

2.2.20 SN74LVC1G14

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC1G14 device contains one inverter and performs the Boolean function Y = $\overline{A}$. The device functions as an independent inverter, but because of Schmitt action, it may have different input threshold levels for positive-going (VT+) and negative-going (VT–) signals. NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

図 21. Functional Block Diagram of SN74LVC1G14 for Different Packages

2.2.21 CSD18543Q3A

This 60-V, 8.1-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

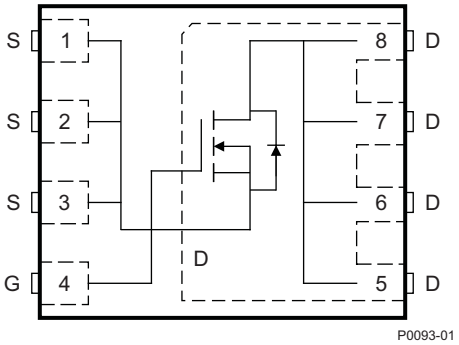


図 22. Top View of CSD18543Q3A

表 5. Product Summary of CSD18543Q3A

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-source voltage	60		V
Q_g	Gate charge total (10 V)	11.1		nC
Q_{gd}	Gate charge gate-to-drain	1.7		nC
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V	12.0	mΩ
		V_{GS} = 10 V	8.1	
$V_{GS(th)}$	Threshold voltage	2.0		V

2.2.22 CSD15380F3

This 20-V, 990-mΩ, N-channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. Ultra-low capacitance improves switching speeds. When used in data line applications, the low capacitance minimizes noise coupling. This technology is capable of replacing standard small-signal MOSFETs while providing a substantial reduction in footprint size.

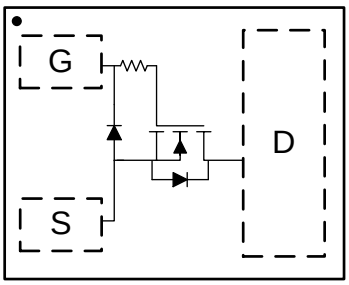


図 23. Top View of CSD15380F3

表 6. Product Summary of CSD15380F3

T_A = 25°C		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-source voltage	20	V
Q_g	Gate charge total (4.5 V)	0.216	nC
Q_{gd}	Gate charge gate-to-drain	0.027	nC

表 6. Product Summary of CSD15380F3 (continued)

T_A = 25°C		TYPICAL VALUE		UNIT
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V	2220	mΩ
		V_{GS} = 4.5 V	1170	mΩ
		V_{GS} = 8 V	990	mΩ
$V_{GS(th)}$	Threshold voltage	1.1		V

2.2.23 TPD1E10B06

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications.

Typical applications of this ESD protection product are circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is good for the protection of the end equipment like ebooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

図 24. Functional Block Diagram of TPD1E10B06

2.3 Design Considerations

Driving high-power LEDs with pulses of high current in a fast and accurate manner is known to be a design challenge. Designers are commonly confronted with limitations based on the basic laws of physics, component ratings, and environmental conditions.

This reference design provides an example on how to address some of these challenges in the hardware and software design. For more details, consult outside literature.

2.4 System Design Theory

2.4.1 Hardware

2.4.1.1 LED Buck

The LED buck is the core hardware block that directly influences the electrical characteristics of driving the LEDs. A switching regulator is selected to drive the string of five LEDs with a constant current of up to 2.4 A. Using this switching regulator has the clear advantage of less power dissipation compared to any linear regulator approach. This holds especially true when considering the huge variation in the LED string voltage over forward current, temperature, and binned forward voltage groups.

However, using a switching regulator introduces other burdens for the design, for example noise, ripple, complexity, and ability to fulfill the demanding dynamic requirements.

The buck topology is selected because it is the only topology out of the standard non-isolated topologies (buck, boost, inverting buck-boost, SEPIC) that ensures a continuous current flow through the load (LEDs) on its output, even without the need for an energy storing output capacitor. The buck topology eases furthermore the accurate control of its load (LEDs) current because this load current equals the inductor current of the buck.

表 7 lists the challenges for the practical design of the specific LED buck.

表 7. Challenges of LED Buck Design and Measures to Address Them

FEATURE	MEASURES TO ADDRESS DESIRED FEATURES				ADDITIONAL OR ALTERNATIVE MEASURES
	L	COUT	FS	VIN	
ILED: support short ON-times		↓	↑		
ILED: short rise, fall, or trigger delay times	↓	↓		↑	Start converter into shorted output, actively discharge inductor for switching LEDs off
ILED: low ripple	↑	↑	↑	↓	
Efficiency: high			↓	↓	
Minimum ON-time limit of buck converter, do not violate	↑		↓	↓	

A dedicated buck LED driver, TPS92515HV [1] , is chosen due to its integrated switching FET and its used constant off-time, peak-current control as shown in 図 25. The principle of this special mode is based on two states dictating the high-side FET control. The switch turns on and stays on until the programmed peak current $I_{L\text{-}Peak}$ is reached. The peak current is controlled by monitoring the voltage across the sense resistor, R_{SENSE}. When the voltage drop is higher than the programmed threshold (V_{IADJ}/10), the peak current is reached, and the switch is turned OFF, which initiates the OFF-time period t_{OFF}. The OFF-time is derived from the output voltage V_{LED} to create a quasi-constant inductor ripple $\Delta I_{L\text{-}PP}$.

式 1 gives the ideal values for the average inductor current, I_{Lave}, and for the average LED current I_{LEDave}. 式 1 is valid for positive integer numbers of switching periods only. Non-integer numbers of switching periods lead to a deviation from the ideal values. The resulting error is negligible for large numbers of switching periods (when the switching frequency of the buck LED driver >> 1/LED_on_time) and for I_{Lave} >> $\Delta I_{L\text{-}PP}$.

$$I_{Lave} = I_{LEDave} = \frac{\frac{V_{IADJ}}{10}}{R_{SENSE}} - \left(\frac{\Delta I_{L-PP}}{2}\right) \quad (1)$$

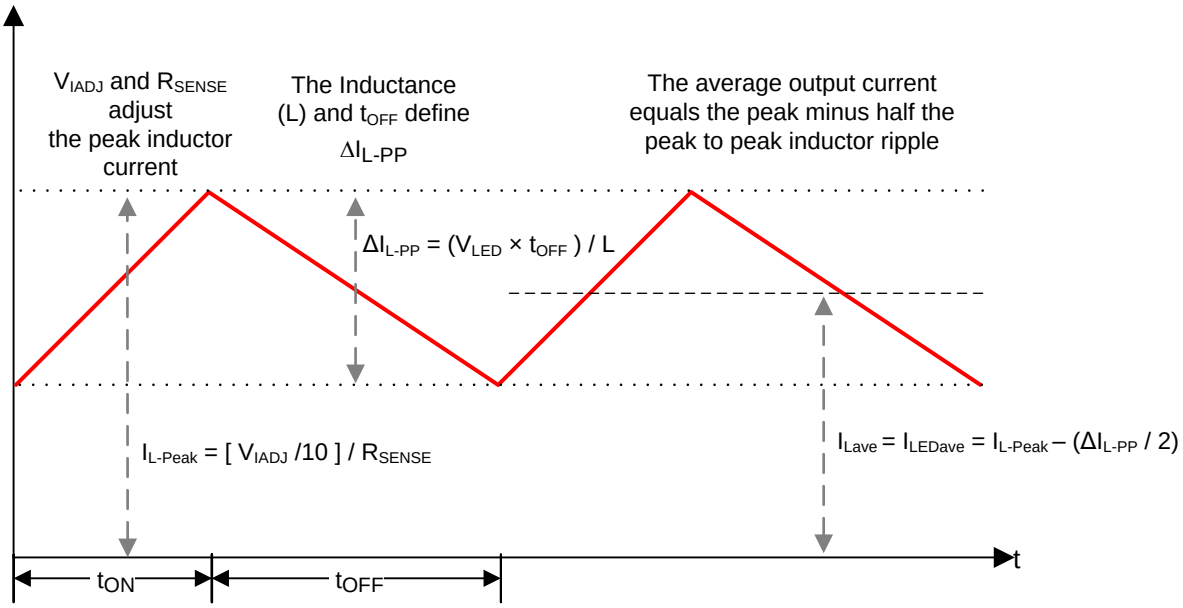


図 25. Principle of Hysteretic Operation: Constant Off-Time, Peak-Current Control

Furthermore, the TPS92515HV offers the advantage of a dedicated PWM dimming input to switch the buck instantaneously ON and OFF without the delay or soft-start phases found in other DC/DC converters and LED drivers.

The TPS92515HV provides additionally a specific IADJ input for setting the I_{L-Peak} threshold by an analog voltage V_{IADJ} applied to that input pin. This feature enables the control of the average inductor current I_{Lave} and therefore also the control of the average LED current I_{LED}.

Although the hysteretic operation of the TPS92515HV allows a high control bandwidth, this reference design cannot fulfill the fast rise and fall time requirements for the LED current given in 表 1 based on the hysteretic operation alone. The buck inductor and its physical property of slowing down any change in current flow through the inductor is the reason for it. This challenge can be addressed in theory by reducing the inductor value or increasing the voltage V_L applied across the inductor. The former measure can be in conflict with the minimum on-time limits of the TPS92515HV as well as with the desired low ripple of the LED current.

This reference design uses an innovative approach to optimize V_L and to achieve finally the required short timing requirements. 図 26 shows the basic approach for the circuit as well as the path where the inductor current flows during the different states of operation.

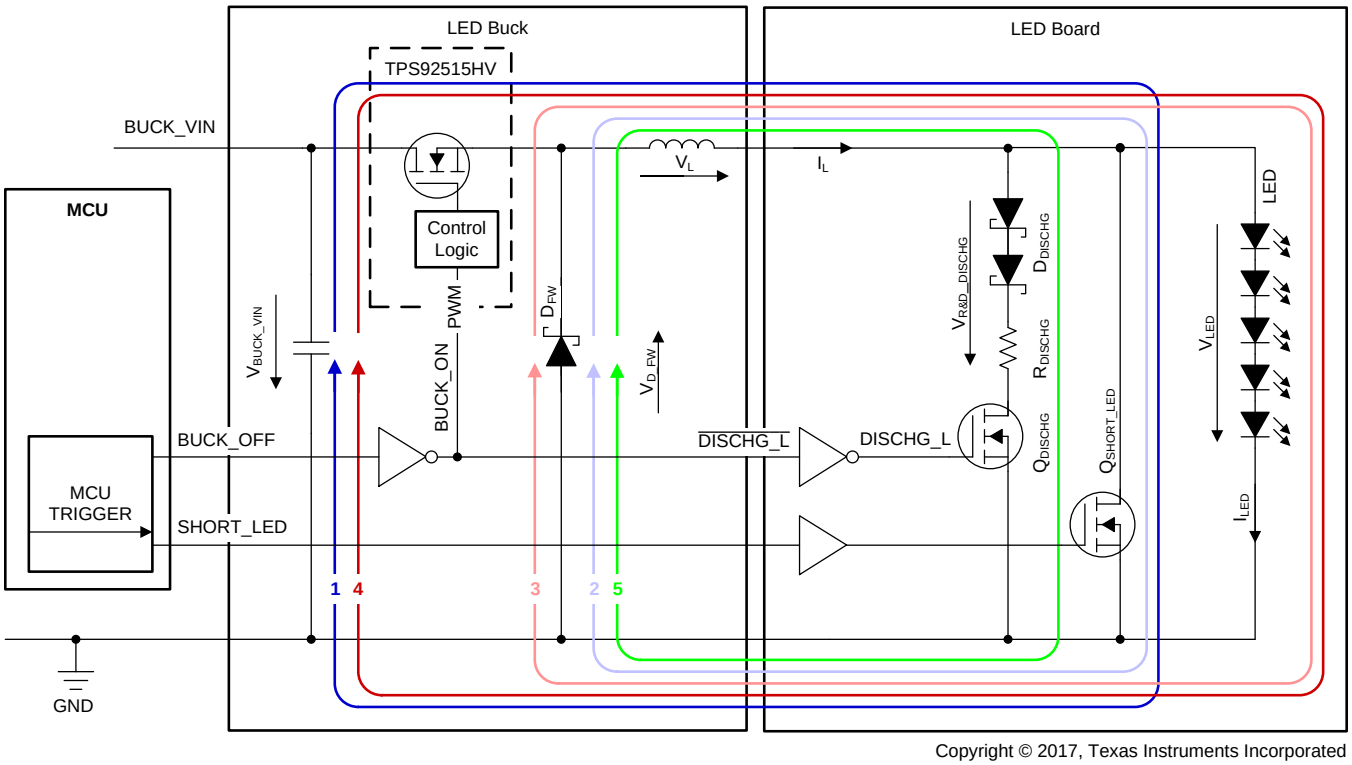


図 26. Basic Schematic of LED Buck and LED Board

The basic circuit diagram is furthermore supplemented by the respective timing diagram provided in 図 27. This timing diagram shows the most important details of the signals that control the timing of the LED buck as well as of the switches (MOSFETs) on the LED board. 図 27 also illustrates the ideal waveforms for the inductor current of the LED buck and for the LED current I_{LED}.

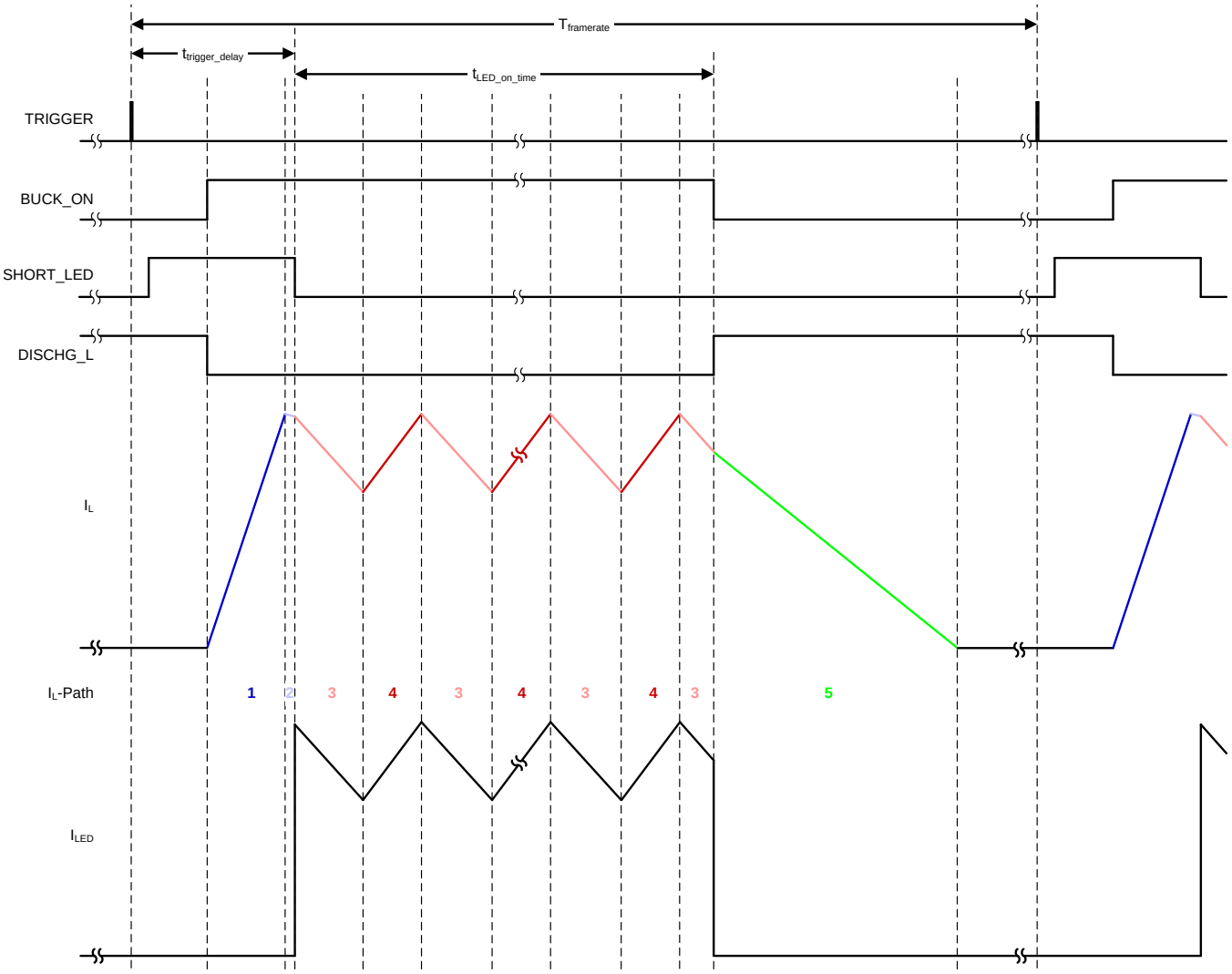


図 27. Timing Diagram of LED Buck and LED Board

表 8 provides further specifics of the control and timing. This table not only describes each of the different states shown in the timing diagram, but also provides the ideal value for the voltage V_L applied across the inductor during each of the states. The larger the value of V_L, the faster the current through the inductor can change.

表 8. Detailed Description of LED Buck and LED Board Control and Timing

STATE	DESCRIPTION	V_L
Trigger	Interrupt, caused externally by isolated trigger input or internally by timer	
1	Start of the buck LED driver (TPS92515HV) and precharge of its inductor to the $I_{L\text{-}Peak}$ corresponding to the configured "I LED" (see 表 9). Start of this state is initiated by MCU (BUCK_ON is going high and DISCHG_L is going low and is based on the desired $t_{trigger\_delay}$ (10 µs), the estimated precharge time (duration of state 1), and the time margin factored in (state 2). Output of buck is shorted by Q_{SHORT_LED} to maximize V_L and to minimize the time needed for state 1. End of state 1 is controlled by buck LED driver (TPS92515HV) when $I_{L\text{-}Peak}$ threshold is hit.	V_{BUCK_VIN} (2)
2	Time margin with freewheeling of I_L (using Schottky diode D_{FW}) to factor in tolerances in precharging (state 1). State 2 starts automatically as soon as the buck LED driver stops state 1. Output of buck is still shorted by Q_{SHORT_LED} to minimize V_L and to minimize the drop in I_L.	$-V_{D\_FW}$ (3)
3 and 4	$t_{LED\_on\_time}$ is when the output of the buck is not longer shortened by Q_{SHORT_LED} and I_L flows through the LEDs (as I_{LED}). Waveform and switching frequency of I_{LED} are completely controlled by buck LED driver (TPS92515HV). Start of first falling slope of I_{LED} is initiated by MCU control (SHORT_LED signal going low). First falling slope of I_{LED} starts almost at the configured $I_{L\text{-}Peak}$ level due to the short time margin (state 2) and the minimized drop of I_L during state 2. The MCU controls the end of $t_{LED\_on\_time}$ determined by the configured "On Time" parameter (see 表 9). As a result, the current flow through the LEDs can stop anytime during state 3 or state 4, leading to non-integer number of switching periods and causing a deviation of the resulting I_{LEDave} from the ideal value calculated by 式 1.	Down-Slope (State 3): $-\left(V_{LED} + V_{D\_FW}\right)$ (4) Up-Slope (State 4): $V_{BUCK\_VIN} - V_{LED}$ (5)
5	Inductor discharge state: to start any LED pulse (flash) from a know state of the circuit and to ensure that minimum ON-time limit of the buck LED driver (TPS92515HV) is not violated. The MCU stops operation of buck LED driver by driving the BUCK_ON signal to go low and the DISCHG_L signal to go high. The latter one switches Q_{DISCHG} on and steers I_L away from the LEDs towards the path through D_{DISCHG} and R_{DISCHG}. To be fast and effective the following condition needs to be fulfilled. $V_{LED} >> V_{R\&D\_DISCHG} >> 0\ V$ (6) This approach significantly increases the voltage across the inductor V_L and decreases the time needed to completely discharge the inductor when compared to the standard freewheeling with the LEDs simply shortened as in state 2. A fast inductor discharge reduces the average power dissipation in the freewheeling diode and inductor compared to a pure shunt-FET dimming implementation.	$-\left(V_{R\&D\_DISCHG} + V_{D\_FW}\right)$ (7)

2.4.1.1.1 Specific Implementation of LED Buck

A maximized voltage V_L across the inductor is needed to obtain a fast change of the inductor current I_L. According to 表 8, a maximized input voltage for state 1 is required to meet the trigger delay time specification of 10 µs, especially for the maximum LED current I_{LEDave} of 2.4 A. The high-voltage version of TPS92515HV is therefore selected, offering a maximum V_{IN} of 65 V compared to its standard (non-HV) version with only a 42-V input voltage capability.

図 28 shows the specific implementation of the TPS92515HV in this reference design.

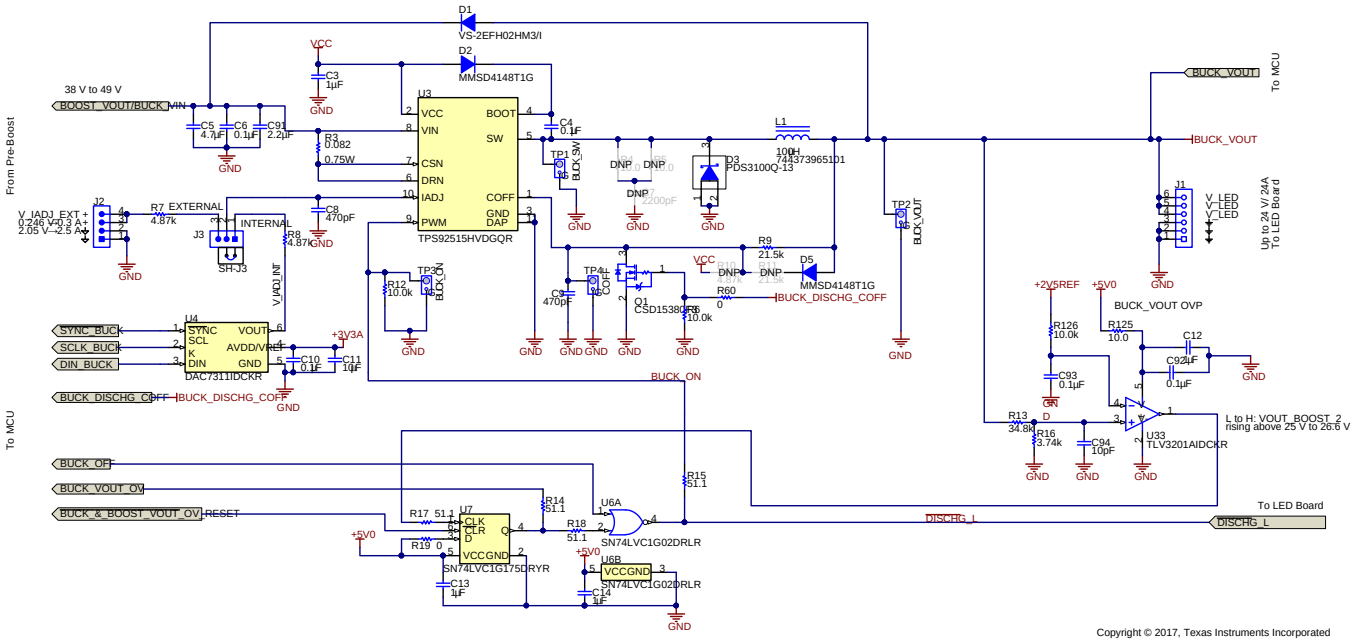


図 28. LED Buck With IADJ-DAC and OVP

The input voltage of the LED buck (BUCK_VIN) is provided by the pre-boost (BOOST_VOUT). The LED buck can operate over a nominal input voltage range (BUCK_VIN) from 38 V to 49 V. C5, C6, and C91 serve as bypass capacitors and need to be placed as close as possible to their respective pins of U3. The peak inductor current of L1 can be configured either by an external analog voltage (V_IADJ_EXT) applied to header J2 or by an internal voltage (V_IADJ_INT) provided by the DAC U4. DAC U4 is controlled from the MCU. The jumper setting on header J3 selects whether the internal or external voltage is used. R7 and C8 or R8 and C8 form a low-pass filter and lead to a RC time constant of roughly 2.5 µs.

The switch node of the LED buck can be probed on test point TP1 by using a modified oscilloscope probe. The reference design contains numerous of such test points for all the different circuit blocks to simplify the evaluation of the board. 図 30 shows three of the four test points assigned to the LED buck. To modify the probe, remove the probe tip cover. In addition, the ground lead and alligator clip must be replaced by a ground spring as shown in 図 29. The small ground spring reduces significantly the noise, which can couple otherwise into the long ground lead of a standard probe configuration.

図 29. Probe With Long Ground Lead and Alligator Clip vs Probe With Ground Spring

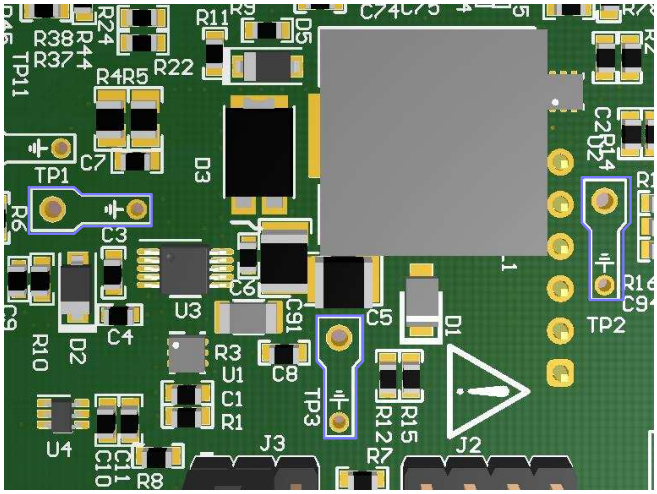


図 30. Dedicated Test Points (Blue) to Simplify Board Evaluation

R4, R5, and C7 are placeholders for a snubber network on the switch node of the LED buck. The type and value of snubber components must be adapted to the circuit of a specific design in case a snubber is needed. Testing the reference design (see 3.2.3) shows a very clean switching waveform on TP1, which makes a snubber unnecessary.

The buck inductor L1 is selected carefully. This inductor influences the accuracy of the output current of the buck and therefore also the current through the LEDs as outlined in *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability* . The selected inductor is rated for 2.6 A, which is sufficient for the peak inductor current of 2.5 A in this reference design. Beside this, the saturation characteristic plays an important role. The inductance of inductors falls usually more or less rapidly in close proximity to the given rated current; however, the selected power inductor from Würth Elektronik shines with a inductance drop of only 20% at 5.2 A given as the saturation current.

R9 and C9 are other components influencing the ripple current of the inductor and LED (states 3 shown in 図 27). The peak-to-peak ripple current based on those components and on the 100 µH chosen for L1 is roughly 200 mA, resulting in an switching frequency in the range of 600 kHz to 900 kHz. The switching frequency of the LED buck increases when the voltage of the LED string and the input voltage applied to the LED buck increase; however, the switching frequency decreases when the LED current increases.

The LED buck of this reference design uses a very specific approach for protecting the buck circuit as well as the voltage sensitive components on the LED board (MOSFETs Q3 and Q4) against overvoltage. Overvoltage events can be caused by a sudden interruption of the current flow of the buck inductor. Reasons for such interruptions are, for example, the disconnection of the LED board from the rest of the circuit or LED open failures.

To address such cases, diode D1 is implemented to clamp any voltage on the output of the LED buck to the safe level of the input voltage (BUCK_VIN). In addition, an overvoltage detection circuit based on the comparator U33, the D-Flip-Flop U7, and the NOR-gate U6 is implemented. A detected overvoltage event causes a low-to-high transition on the comparator's output, leading to a positive edge on the clock input of the D-Flip-Flop. As a result, the High signal from the input pin of the D-Flip-Flop (D) is transferred to its output pin (Q), which drives the output of the NOR-gate U6 low. The NOR-gate's output provides the BUCK_ON signal for the PWM input of the buck LED driver U3. The BUCK_ON signal is low due to the overvoltage event and switches the buck LED driver U3 off. This state is latched by the D-Flip-Flop.

The overvoltage event is also detected by the MCU through the BUCK_VOUT_OV signal, which is generated by the D-Flip-Flop. The terminal software shows "Buck OVP fault" when an overvoltage event for the buck is detected. To return to a normal system state, the user needs to acknowledge the "Buck OVP fault" by "Reset OV" in the terminal software window. The "Reset OV" forces the MCU to reset the D-Flip-Flop by applying the $\overline{\text{BUCK\_\&\_BOOST\_VOUT\_OV\_RESET}}$ signal to the $\overline{\text{CLR}}$ input of the D-Flip-Flop.

This reference design demonstrates a dedicated solution for overtemperature protection. The temperature of the buck converter (U3) and of the buck inductor (L1) are supervised by two separate temperature sensors, U1 and U2. The temperature sensors communicate through the I^2C bus with the MCU to enable configuration, readout of the sensed temperature data and alerting of overtemperature (see 2.4.2.3). The measured temperatures are shown in the terminal software in the status output zone under "Temp:", "TPS92515", and "Inductor".

The buck inductor is not connected to ground. The thermal pad of the temperature sensor is therefore electrically not connected to the inductor, nor is it from a thermal perspective optimal coupled to it. The latter one holds true for the thermal connection of the temperature sensor sensing the temperature of the TPS92515HV as well. This can lead to severe differences between the actual temperature of the components and the temperatures sensed and shown by the temperature sensors.

Therefore, the user must verify the temperature of those components under operating conditions by own temperature measurements. Do not leave the reference design powered when unattended.

Each of the two TMP116 temperature sensors offer 64 bits of user programmable EEPROM as a unique and helpful feature. This feature enables the user to save and read data for board identification, configuration, parameter sets, or other purposes. Using this EEPROM is supported by the terminal software's parameters "EEPROM" and "Data" as listed in 表 9.

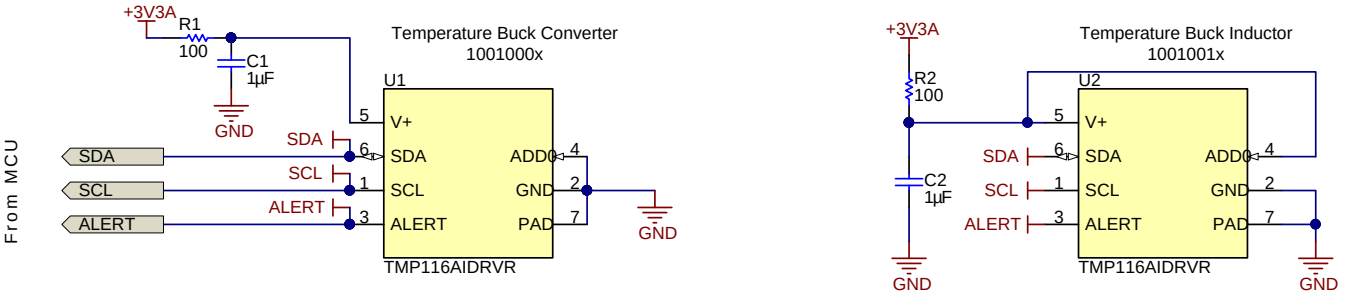


図 31. Temperature Sensors of LED Buck

2.4.1.2 LED Board

This reference design has a dedicated board (LED board) assigned to the five high-power LEDs: D9, D11, D14, D15, and D16. For demonstration purposes, this reference design uses OSLON™ Black Flat LEDs[11]. These LEDs are specified in their data sheet for forward currents up to 1.5 A and provide even graphs for currents down to 300 mA (down to 50 mA with increased tolerances). The data sheet gives even data for the permissible pulse handling capability up to peak pulses of 2.5 A.

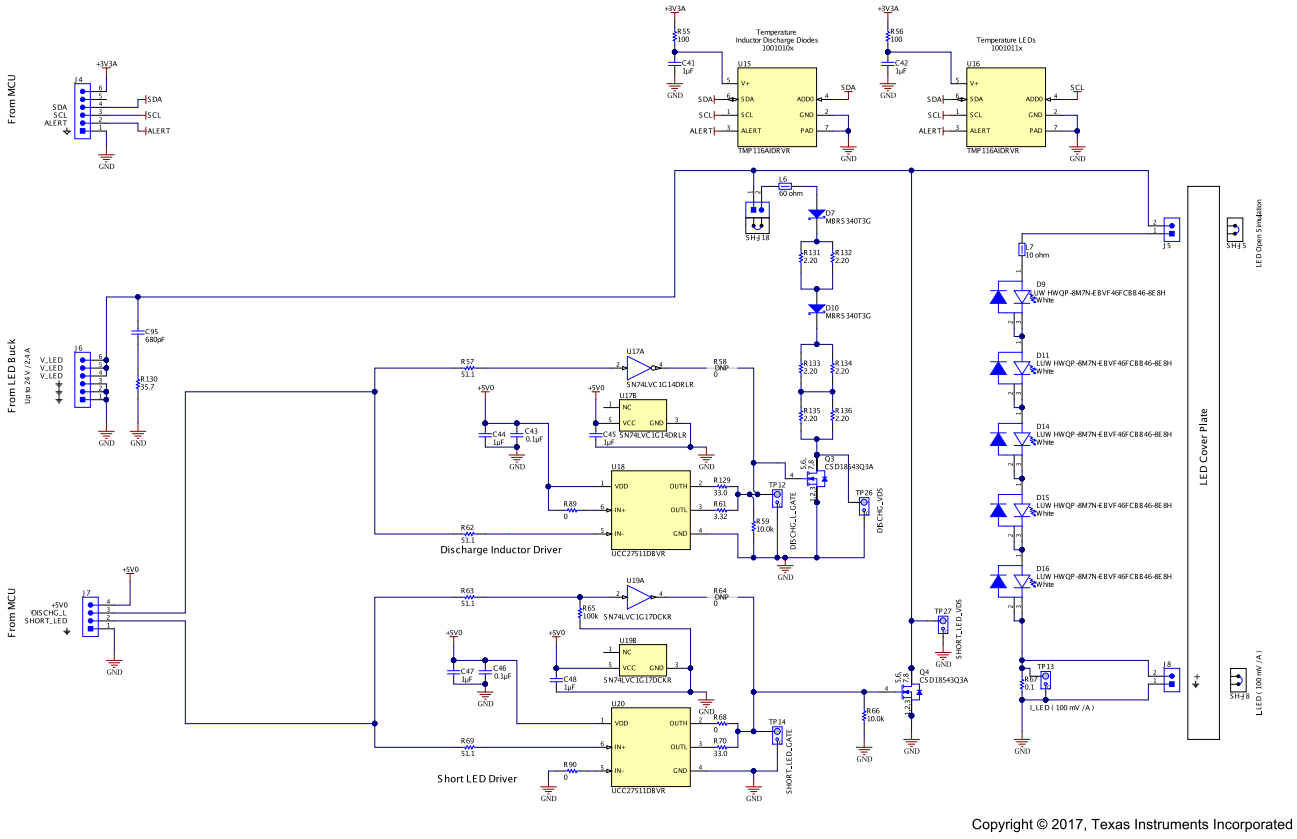


図 32. Schematic of LED Board

The target of this reference design is to demonstrate that the LED string can be turned on and off very fast with rise and fall times in the 40- to 100-ns range. To achieve this target specification, the two MOSFETs Q4 and Q3 are located in close proximity to the LEDs to steer the current flow.

Q4 acts as Q_{SHORT_LED}-FET (see 図 26 and 図 27). This FET shorts the LEDs and therefore the output of the LED buck during the precharge of L1 (state 1) and the first freewheeling of L1 (state 2). When this FET is switched off, the inductor current IL is steered immediately through the five LEDs, switching them on instantaneously.

Q3 acts as Q_{DISCHG}-FET, which is activated to switch the LEDs off. Q3 provides an parallel path (D7, D10, R131 to R136, and L6, Q3) to the LED string. The voltage drop across this parallel path (at the same current as the LED current) is much lower than the forward voltage of the LED string. This is why the LED current is instantaneously steered away from the LEDs towards this parallel path. This parallel path accelerates the discharging of the buck inductor L1 to shorten the time and as a result reduce the losses

during which the inductor's freewheeling current flows through the DC resistance of the inductor L1 as well as through the freewheeling diode D3 of the LED buck. The reduced losses reduces the heating of those components (especially at high LED currents). L1 and D3 needs to be placed in close proximity to U3 from an EMI point of view. Those three components together form a thermal hotspot if accelerated discharging L1 is not implemented.

The losses and heating of the LED board are increased. In a real system, it is likely that the LED board is designed with a dedicated thermal board design in mind so that the additional losses can be managed better on the LED board.

The time needed to switch the LEDs on and off depends on the switching speed of the FETs Q3 and Q4. Dedicated MOSFET drivers (U18 and U20) provide the needed gate drive current for a fast switching of the FETs. Separate outputs (OUTH and OUTL) on those drivers allow a separate fine tuning for the speed with which the MOSFETs are switched on and off. The separate IN+ and IN– pins of this driver (UCC27511) enables its configuration as an inverting or non-inverting MOSFET driver. This kind of flexibility is used in this reference design as well.

図 32 shows a simplified approach for how to drive the MOSFETs alternative but is not tested in this reference design. The shown single-gate Schmitt triggers (U17 inverting, U19 non-inverting) have a reasonable output drive capability and might be sufficient for driving MOSFET. To evaluate, populate R58 and R64 and remove R129, R61, R68 and R70.

The ferrite beads L6 and L7 and the snubber R130/C95 are used to improve EMI; however, these parts slow down the speed of switching the LEDs on and off. This speed is critical when using the design for ultra-short LED pulses of less than 1 µs.

The LED board uses the two TMP116 temperature sensors similarly to the LED buck (see 2.4.2.3) to sense the temperature of the LEDs (U16) as well as of the components of the discharge path (U15). U16 is placed close to the LED D16 while U15 is placed near R131, R132, and D10. The sensed temperatures are shown in the terminal software in the status output zone under "Temp:", "LED", and "Diodes". The "Diodes" value represents the sensed temperature of the respective resistors R131 and R132 and diode D10. The two temperature sensors do not only sense the temperatures but provide also an alert in case of overtemperature conditions (≥ 70°C).

The LEDs and the components of the discharge path are electrically floating and are not connected to ground. The thermal pad of the temperature sensors is therefore electrically not connected to the LED or the components of the discharge path, nor is it from a thermal perspective optimal coupled to them. This can lead to severe differences between the actual temperature of the components and the temperatures sensed and shown by the temperature sensors.

Therefore, the user must verify the temperature of those components under operating conditions by own temperature measurements. Do not leave the reference design powered when unattended.

Each of the two TMP116 sensors offer 64 bits of user programmable EEPROM as already outlined for the temperature sensors of the LED buck.

2.4.1.3 Pre-Boost

The pre-boost has the following manifold purposes in this reference design:

- Boost the 8-V to 36-V input voltage (V_IN on J19) of the reference design to the 48.5-V level needed by the downstream LED buck
- Separate the large discontinuous input ripple current of the LED buck from the input of this reference

design by converting it into the more continuous input current ripple of the pre-boost.

- Provide an average input current limit, which adapts to the reference designs input voltage (V_IN on J19). The adaptable input current limits of the pre-boost leads to a quasi-constant input power limit of 8 W to 10 W, which is independent of the V_IN applied on J19.
- Implement the average input current limit of the pre-boost in a quasi-lossless manner. The pre-boost operates always with this average input current limit as long as the pre-boost is active. This is in contrast to the reference design's higher input current limit provided by the eFuse U27. The eFuse limits the current by controlling the ON-resistance of the internal pass FET. There is therefore an increase of losses and power dissipation in the eFuse as soon as the eFuse enters the current limit region.
- Energy storage in the pre-boost output capacitors enables the LED buck to generate LED pulses with higher peak power (up to 40 W and more) than the 8-W to 10-W input power limit of the pre-boost.

2.4.1.3.1 Specific Implementation of Pre-Boost

The core of the pre-boost implementation is the pre-boost current controller, U10. The TPS92561 [2] is selected as a control device for this purpose due to its pure and simple hysteretic operation as shown in 図 33. Two thresholds are formed as a result from a voltage applied on the ADJ-pin of U10 and from an internally superimposed ±30 mV to this ADJ voltage. These thresholds determine the control of the ON- and OFF-times, t_{ON} and t_{OFF}. The comparator-based operation principle takes complete care of the inductor and input-current control of the pre-boost without any control loop involved. The hysteretic approach also avoids the delays, bandwidth limitations, and loop stability issues commonly found in standard loop-controlled boost topologies.

This reference design uses a modified implementation of the TPS92561 device. The left schematic shown in 図 33 represents the standard usage of the TPS92561 while the right schematic illustrates the specific implementation of the device to enable its operation in this reference design. The main difference is the current sensing scheme and the ground connection of the load.

The standard implementation does not allow a direct ground connection of the load (string of LEDs). Instead, the LEDs must be connected to ground through a low-side current sense resistor to enable the inductor and input current to be sensed even during the OFF-time of the boost's MOSFET (state 2, t_{OFF}). The sensing of the inductor current during t_{ON} *and* t_{OFF} is a prerequisite for equating the input current I_{IN} with the inductor current I_L.

The specific case of this more complex reference design requires a common ground usable for the complete system, ranging from the system's power input (J19) over the eFuse, pre-boost, MCU, and LED buck to the output LED string. To achieve this common ground connectivity, the low-side current sensing of the standard configuration is replaced by a high-side current sensing of the inductor current. The input current waveform is almost identical for both use cases. The modified implementation requires just that the R_{SENSE} term in the equations given in 図 33 are corrected by the resulting gain of the high-side current sensing.

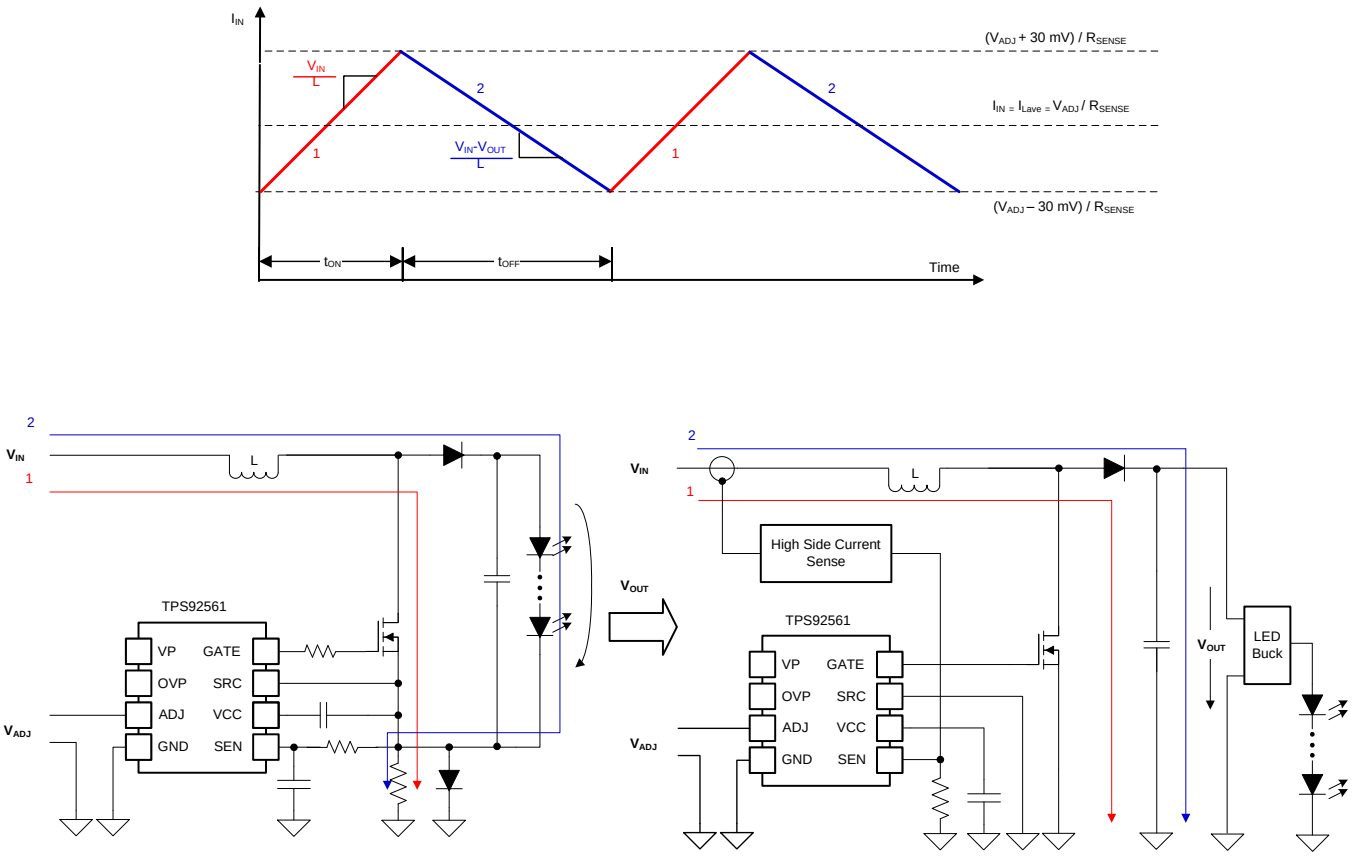


図 33. Pre-Boost Operation—Standard vs Modified Implementation and Input Current Waveform

A dedicated high-side current shunt monitor (INA169) is used in the real schematic of the pre-boost to implement the high-side current sensing of the boost inductor's current (see 図 34).

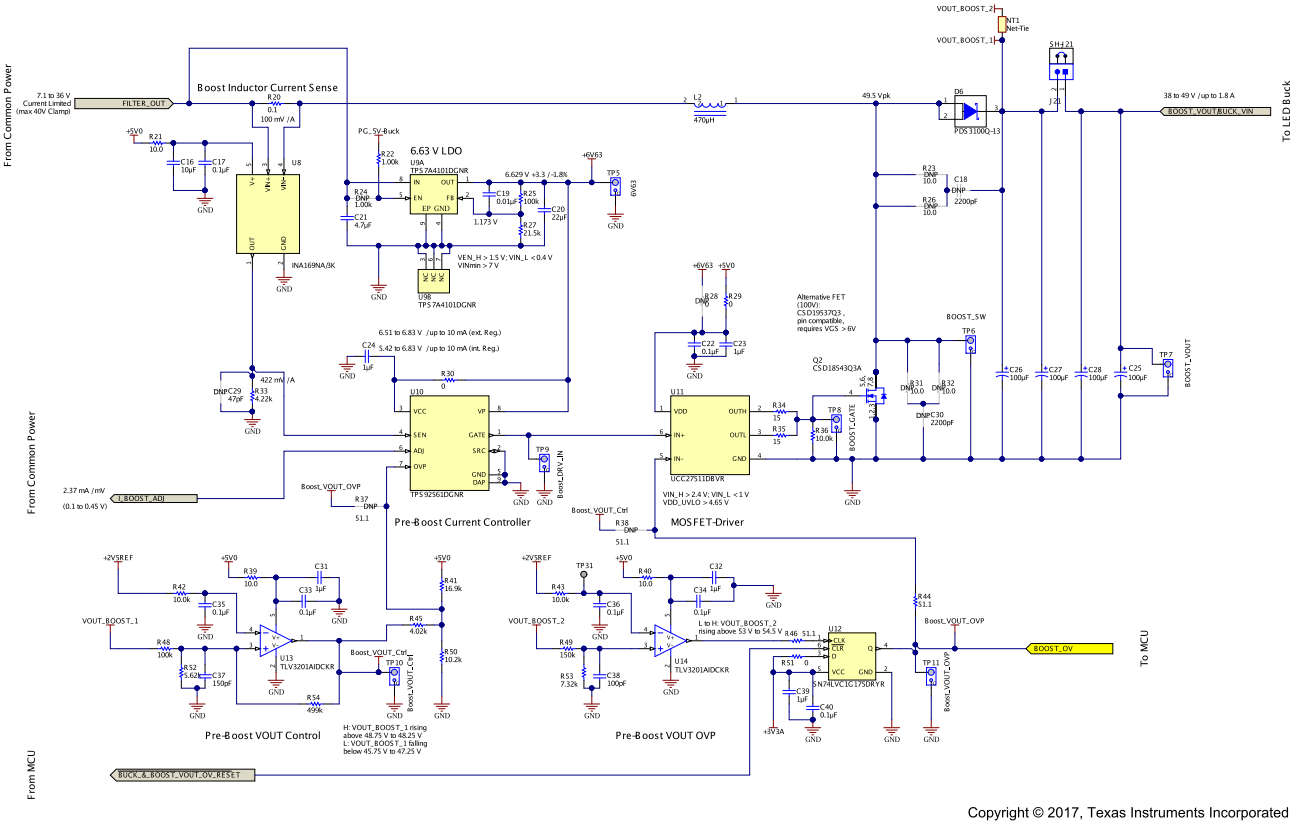


図 34. Schematic of Pre-Boost

R20 serves as current sense resistor, providing a voltage (V_{R20}) of 100 mV/A. The INA169 (U8) offers a differential input for sensing this voltage and converts the sensed voltage V_{R20} into a current I_{OUT_U8} (see 式 8) flowing through R33 to ground (GND). gm is the transconductance of U8 and has a value of 1000 µA/V.

$$I_{OUT\_U8} = g_m \times V_{R20} = 1000\frac{\mu A}{V} \times 100\frac{mV}{A} \times I_{L2} = 100 \times 10^{-6} \times I_{L2} \quad (8)$$

R33 is converting I_{OUT_U8} into a ground referred voltage V_{R33} (as shown in 式 9), which is perfectly suited to be used as sense voltage V_{SEN_U10} for the boost controller U10.

$$V_{SEN\_U10} = V_{R33} = I_{OUT\_U8} \times R33 = 100 \times 10^{-6} \times I_{L2} \times 4.22\ k\Omega = 422\frac{mV}{A} \times I_{L2} \quad (9)$$

U10 compares internally the sense voltage (V_{SEN_U10}) applied to its SEN pin with the voltage V_{ADJ_U10} applied to its ADJ pin. V_{ADJ_U10} serves for setting the average boost inductor current limit I_{L2_limave}, which equals the average input current limit of the pre-boost $I_{IN\_Pre\text{-}Boost\_limave}$. V_{ADJ_U10} to get a specific desired current limit can be calculated according to 式 10.

$$V_{ADJ\_U10} = V_{SEN\_U10} = 422\frac{mV}{A} \times I_{L2\_limave} = 422\frac{mV}{A} \times I_{IN\_Pre\text{-}Boost\_limave} \quad (10)$$

The current limit for an specific V_{ADJ_U10} applied to the ADJ pin of U10 can be calculated by 式 11.

$$I_{L2\_limave} = I_{IN\_Pre\text{-}Boost\_limave} = \frac{V_{ADJ\_U10}}{422\frac{mV}{A}} = 2.37\frac{A}{V} \times V_{ADJ\_U10} \quad (11)$$

In this reference design, the V_{ADJ_U10} is provided by the channel B of the dual DAC U28, which is part of the common power block. The provided V_{ADJ_U10} is adapted (see also 2.4.2.9) to the input voltage applied to J19 of this reference design to achieve the desired constant input power limit of 8 to 10 W for the pre-boost.

U10 is powered by a separate LDO U9, generating a 6.63-V rail instead of using the internal 8.35-V LDO of U10. The output (VCC) of this internal 8.35-V LDO is shorted to its power input pin VP. This LDO (TPS7A4101 [6]) has a maximum input voltage of 50 V (recommended) and an absolute maximum rating of 55 V. This high input voltage capability gives an additional margin compared to a 42-V or 45-V maximum input voltage capability of the TPS92561—especially when system input voltage transients like surges are considered. The external LDO U9 ensures a stable operation even for very low input voltages of the pre-boost down to 7.1 V. Such input conditions can be expected at the lowest system input voltage (8 V) and largest voltage drop across the eFuse and the EMI filter at maximum load.

Due to its low dropout voltage (< 290 mV) and the ability to adjust the output voltage to 6.63 V, a much more stable output voltage can be expected over the full input voltage range (down to 7.1 V) when using this external TPS7A41 compared to the internal 8.35-V LDO of U10. The separate LDO also offers an ENABLE pin, which supports a sequenced start-up of the different voltage rails of the system. For this reference design, the 6.63-V LDO (and with it the pre-boost) is enabled by the power-good signal of the 5-V buck (PG_5V-Buck).

An additional delay is introduced by the MOSFET driver U11. The output of U11 is held low by the internal UVLO of U11, which supervises the supply voltage on the VDD pin of the MOSFET driver. U11 is powered by the +5V0 rail, which is not powered up when the system starts. This +5V0 rail is controlled by the MCU and comes up later during the system start-up.

This sequenced approach ensures that the eFuse can smoothly charge all the capacitors of the eFuse, the EMI filter, and the pre-boost without being disturbed by the larger start-up and operation current of the pre-boost.

The TPS92561 is designed to control current, but the device does not have an internal loop to regulate output voltage. The output voltage is usually determined and clamped by the forward voltage of the LED string when the TPS92561 is used in its standard configuration of driving LEDs directly (shown in the left schematic of 図 33). The device in this standard configuration has an OVP with a ±7% threshold tolerance, which steps in when the LEDs are disconnected or when the LEDs fail to open.

The target for this reference design is to use the pre-boost not only for controlling the inductor and input current, but also for generating a regulated output voltage of 48.5 V. This 48.5-V level is high enough to charge the buck inductor L1 quickly, but also low enough (staying below 50V) to evaluate it in laboratories with more severe electrical safety concerns. In addition, a backup circuit is needed for OVP in case the nominal 48.5 V is not controlled. During this failure, the voltage must stay below the maximum VDS rating of 60 V for the boost MOSFET Q2.

Those requirements can not be fulfilled with the features of the TPS92561. Two independent comparators have been added therefore to add the Pre-Boost VOUT Control as well as the Pre-Boost VOUT OVP. Both comparators sense the pre-boost's output voltage VOUT_BOOST_1 and VOUT_BOOST_2 directly on the cathode of the boost diode. From that point on, both circuits use two separate PCB traces and voltage dividers R48,R52 and R49,R53 to feed the inputs of the two comparators. The pre-boost uses the same type of 40-ns fast microPOWER comparators (TLV3201 [4]) as had already been used for the OVP of the LED buck.

The comparator U13 used to control the output voltage is configured as a Schmitt trigger by adding a positive feedback using R54. U13 stops the TPS92561 from switching when VOUT_BOOST_1 rises above 48.25 V to 48.75 V and restarts the switching when VOUT_BOOST_1 falls below 47.25 V to 45.75 V. U13 is using the OVP pin of U10 for that purpose.

To implement an OVP function independently from the VOUT control of the boost, a separate path for stopping the switching is needed. This separate path is established by using the OVP circuit based on comparator U14 to enable or disable the driver U11 of the MOSFET Q2. U14 is acting as a pure comparator; no external hysteresis is added. The threshold for its switching is between 53 V and 54.4 V. U14 does not control the FET driver directly, but triggers the D-Flip-Flop U12 instead. A detected overvoltage event causes U12 to latch, notifies the MCU by the BOOST_OV signal, and the latched Flip-Flop disables the MOSFET driver U11. The terminal software shows "Boost OVP fault". The user must acknowledge the "Boost OVP fault" by "Reset OV" to return to a normal system state. The "Reset OV" forces the MCU to reset the D-Flip-Flop by applying the $\overline{\text{BUCK\_\&\_BOOST\_VOUT\_OV\_RESET}}$ signal to the CLR input of the D-Flip-Flop.

2.4.1.4 MCU

For control and monitoring, this reference design uses the MSP430F5172. This MCU observes the supply voltage, the LED voltage, the boost voltage, and the current reported by the eFuse. These values are used not only for switching off in case of exceeding programmed limits, but also for controlling the settings of the boost regulator and the eFuse current limit.

Temperatures are monitored using four TMP116 I^2C sensors. Two sensors are placed on the main board: one next to the buck regulator, the other one at the inductor of the buck regulator. On the LED board, two more sensors are placed: one monitors the temperature of the LEDs, and the other one monitors the discharge diodes. Each sensor is programmed by the MCU to assert an alert pin to signal the MCU of an overtemperature. For more details about the monitoring, see 3.1.2.2.

The MCU controls the boost current as well as the eFuse current limit automatically, depending on the input voltage through a dual-channel DAC. This DAC is connected through an SPI to the MCU. For more information on this function, see 2.4.2.9.

For the user, the most important function of the MCU is controlling the LED flashes and providing the user interface. The flash timings are controlled with a time resolution of up to 5 ns using timer D of the MSP430F5172. The compare outputs of the MCU are connected to the buck regulator, the short FET to control the system, and to the Coff capacitor of the buck regulator. For more information on generating flash, see 2.4.2.1.To understand the configuration, see the source code provided in the product folder of this reference design.

The MCU also provides the entire user interface. This interface is stored and controlled by the MSP430F5172 and is accessible by using the UART and any terminal program on the user's PC. No special software is necessary. For more information on the software for the interface, see 2.4.2.4. The source code is also helpful for understanding the operation.

The MCU can be programmed using an MSP-FET over the JTAG interface J13. The MSP430™ can be programmed by setting J11 to 2-3 and shorting J12.

The power supply of the MSP430 is decoupled by 10 Ω and 10 µF || 100 nF on each supply pin. Because the MSP430F5172 has two voltage rails, one operating at 5 V, it is important to respect the proper power-up sequence. The 5 V has to rise after the 3.3-V supply. This rise is achieved by switching on the 5 V with a load switch controlled by the MSP430 itself.

2.4.1.5 Common Power

The *common power* block of the design provides additional protection, system management, and system support functions as well as the following features:

- eFuse for reverse input protection, inrush current-limited soft start, three selectable current limits or an adaptive input current limit for constant input power clamp (12 W to 15 W), basic input OVP
- Basic surge protection
- EMI filter for conducted noise
- Dual DAC to provide the control voltage for the adaptive current limit of the eFuse and the pre-boost
- 5-V buck to generate the main supply rail used either directly by system components or by feeding the additional 3.3-V LDO and 5-V load switch
- 2.5-V reference to provide a highly precise 2.5-V rail used for all system functions that need high accuracy

2.4.1.5.1 Specific Implementation of Common Power Block

The header J19 is used as the power input connector, targeted to be powered from an external power supply providing a supply voltage from 8 V to 36 V. The power supply must have at least a 15-W output power to use the electrical power of this reference design to its full extent. The 8-V minimum supply voltage must be ensured even under full power consumption of the reference design.

The TPS26602 [7] is selected as eFuse U27 and has an UVLO function for supervising the supply voltage provided by the external power supply. The eFuse starts powering up the system for input voltages larger than 7.6 V (typical) and stops and shuts down the system as soon as the input voltage drops below 7 V. Input voltages that exceed a level of 38 V (typical) are clamped to this level as a basic protection against short overvoltage events.

The eFuse can operate with input voltages up to 55 V and protects against reverse input voltages of up to –55 V. The TPS26602 has an absolute maximum input voltage rating of ±60 V and can withstand ±70 V for transients up to 10 ms.

The internal reverse input voltage protection makes the usually used reverse protection diodes unnecessary.

An additional level of protection, especially against surges, is provided by the used TVS and Schottky diodes D18, D17 and D19 and D20. The TVS diodes are targeted to clamp a ±1-kV surge pulse (8 / 20 µs), which is coupled by a coupling network of 40 Ω / 0.5 µF to a save voltage level below ±60 V.

Diodes D22, D23, and D24 and resistors R97, R100, R128, and R108 protect the sensitive system components (MCU, dual DAC, and the eFuse itself) from reverse input polarity. This added protection is recommended because the external circuit of the TPS26602 differs in the proposed implementation of this reference design from the standard configuration. The major difference is the adaptive current limit setting and the connections of the eFuse to the MCU.

The inrush current-limited soft start is programmed by the C73 connected to the DVDT pin of U27. This capacitor determines the slew rate with which the output of the eFuse rises up. Without this controlled soft start, a huge peak current would flow to charge at once all the capacitors connected in one or the other way to the OUT pin of the eFuse. These capacitors range from the capacitors of the EMI filter over the input capacitor of the 5-V buck to the output capacitor bank of the pre-boost.

The eFuse provides a programmable current limit. This limit is usually implemented by connecting a resistor from the ILIM pin of the eFuse to the RTN pin of the TPS26602. In this case, The eFuse's output current limit I_{CL} can be calculated using 式 12.

$$I_{CL} = \frac{12000}{R_{ILIM}} \quad (12)$$

In this reference design, R_{ILIM} is one of the three resistors (R101, R103, and R104) to finally get a selectable current limit depending on the jumper setting on header J20. The resistor values can be adapted to other needed current limit values as long as the specified and recommended operating conditions for the system components are not being violated.

The very unique feature of this reference design is its adaptive current limit, which adapts the current limit to the input voltage of the system in a way that a 12-W to 15-W input power limit is achieved. The value for the current limit to be set is provided by the MCU and used by channel A of the dual-DAC U28 to generate an adequate voltage to which R128 and R108 are connected. With R106 and the output of the DAC, those two resistors form together a network that is connected to the ILIM pin of the DAC when the jumper SH-J20 is placed on pins 7 and 8 of the header J20. This network then replaces the single resistor that is usually connected from the ILIM pin of the eFuse to its RTN pin.

The output of the eFuse feeds the EMI filter. A power design seminar topic [10] serves as a guideline for the design of the EMI filter.

The system start continues by starting the 5-V buck as soon as the voltage on Filter_OUT exceeds the 6.75-V UVLO level of U31. An LM5165 converter is used as a simple and robust low-power switching regulator that operates in COT mode and uses a ripple injection network R115, C83, and C85 for reducing the output voltage ripple on the generated 5V-BUCK_OUT. This generated 5-V rail feeds the input of a 3.3-V LDO as well as the input of a 5-V load switch. The 3.3-V LDO is enabled by the Power Good signal of the 5-V buck. The 5-V load switch is enabled by the 5V-LS_ON signal generated by the MCU. This power-up sequencing is implemented to fulfill the sequencing requirements of the MCU and to ensure a smooth power-up of the eFuse and of the complete system.

The precision 2.5-V reference U30 is fed from the 3.3V-LDO. The generated reference voltage is used as reference for the internal DAC of the MCU, as reference for the three comparators used for OVP of the LED buck and pre-boost, and for the output voltage control of the pre-boost.

2.4.1.6 Isolated Power and Data Interface

All external control inputs and outputs are isolated from the internal supply voltages and from the 8-V to 36-V supply voltage on the power input J19. Therefore, an ISOW7842 is used as it not only provides data isolation but also isolated power. By default, the isolated voltage is set to 5 V, but can be changed by setting J17 from 1-2 to 2-3 to get 3.3 V. *When changing this voltage, the levels of the UART interface also change and the correct FTDI cable or other interface must be used.* The isolated voltage can be loaded with up to 50 mA and can be accessed by the user on J14.

For reducing ripple caused by the ISOW7842 on the main 5-V rail, it is recommended to use a CRC π-filter using 10 µF and 1 Ω.

The isolated UART is brought out at J16 and uses the standard pinout for FTDI USB UART cables. The isolated UART interface and the NPN-In and TTL-Out signals of the isolated trigger interface are ESD protected by using TPD1E10B06 TVS (U23 to U26) diodes.

The trigger input and output is implemented to provide a TTL and NPN input and output. The trigger NPN input is directly connected to the ISOW7842 with a pullup resistor and ESD protection diode. The TTL input uses an additional NPN BJT providing the same functionality. The system is designed to always have a delay of 10 µs from trigger input to the LED flash.

The trigger output is designed in a similar manner, providing a TTL output with ESD protection, and a NPN output realized by a CSD18543Q3A N-Channel MOSFET. The delay between trigger output and start of the LED flash is set to –6.5 µs.

2.4.2 Software

This reference design includes software running on the MSP430F5172 to configure, monitor, and control the LED flash. There are four temperature sensors on the board that are monitored and cause a power off in case of overtemperature. Also, the most important voltages are monitored and displayed. The input voltage is used for configuring the eFuse as well as the boost regulator according to the maximum allowed input power. A simple terminal is provided to configure the design and to display measurements.

2.4.2.1 Flash Generation

To generate a single flash with fast rise and fall time, the software controls the buck regulator as well as the short FET with the timings as shown in 図 35. When the flash sequence gets triggered, the MSP430 turns on the short FET and the buck regulator. After a given time, depending on the selected LED current, the short FET is released.

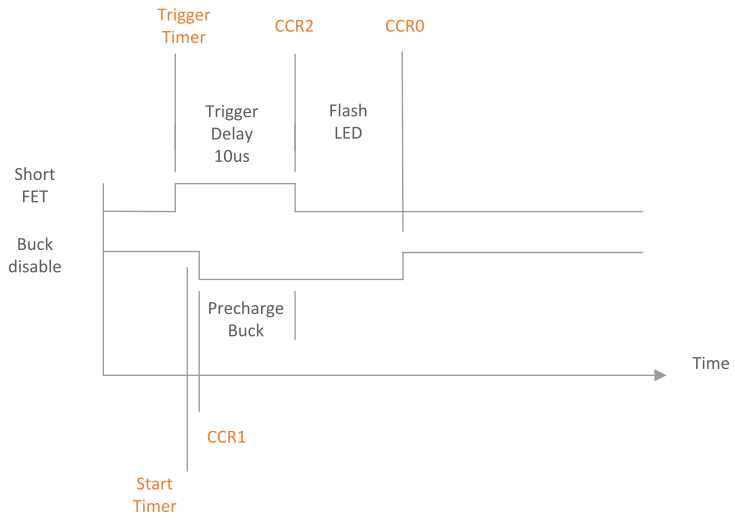


図 35. Timing of Buck Regulator and Short FET

To control this sequence, timer D of the MSP430F5172 is used. This timer offers a resolution of up to 4 ns for the compare outputs because it has an internal clock generation of 256 MHz.

To generate this timing, the control of the necessary pins is handed over to the compare outputs of the timer module. The buck regulator is controlled by CCR1, and the short FET is controlled by he CCR2. Because the buck regulator control is active low, the compare control register (CCTL1) is configured to "Reset" at match and "Set" at the end of the sequence (configured by CCR0). The short FET is active high and only has be turned on during the buck precharge time. As a result the CCTL2 is configured to "Reset", and the output is manually set at the beginning of the sequence.

To maintain the same time from triggering and the actual flash independent from the selected current (and the buck precharge time), the start of the buck is delayed and does not start immediately after triggering. 図 36 shows the software flow for configuring the timer to handle this sequence. The CCR0 indicates the end of the sequence on the hardware side by turning off the buck regulator and on the software side by causing an IRQ. The ISR then disables the timer (otherwise, the sequence would start again) and configuring the GPIOs back to software control. To this time, an offset can be added to compensate delays and rise times caused by the hardware.

In this reference design, the trigger delay time is set to 10 µs. This delay can be changed depending on the requirements, but must be long enough to charge the inductor of the buck regulator to the desired current.

図 36. Configuration of Timer D

2.4.2.2 ADC Operation

In this reference design, the ADC measures the 3.3-V supply of the MSP430 as well as the input voltage (EFUSE_VIN) and current (EFUSE_IMON), LED voltage, and boost output voltage. The 3.3 V is monitored to turn on the 5-V supply (+5V0) after the 3.3 V is stable to have a proper power-on sequence.

図 37 shows the four external channels connected to the internal ADC channels next to each other (A0 to A3). This connection enables the possibility to read the channels as sequence without interaction of the CPU.

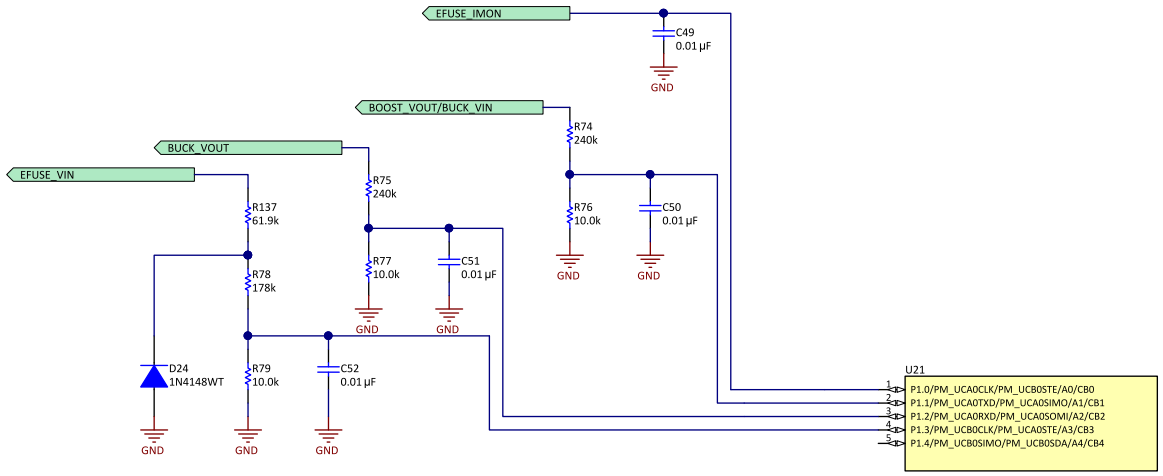


図 37. ADC Usage on MSP430

To reduce the CPU usage on the ADC operations further, DMA is used to transfer the conversation results to the main memory. The sample rate of the ADC is controlled by using a timer output for controlling the sample and hold input.

By this, it is possible to get new ADC values to the memory with a limited data rate and without interaction of the CPU. The main loop can use these values and update the voltage and current reading on the console when the values change.

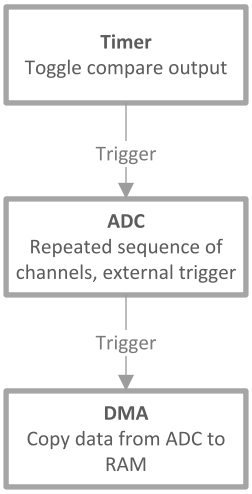


図 38. ADC Operation Optimized for Low CPU Load

2.4.2.3 Temperature Sensing

図 1 shows the four TMP116 temperature sensors. Each sensor has a unique address on the I^2C bus with which it can be configured and conversation results can be read.

The I^2C bus is configured to run at the maximum allowed data rate of the TMP116 of 400 kHz to keep the time of each operation as short as possible. Each TMP116 is configured to indicate overtemperature by pulling the "Alert" output low. This output is checked before every LED flash and disables the flash if the allowed temperature of 70ºC is exceeded.

When the display of measurements is enabled, one of the four sensors is checked each update cycle. When temperature changes, the updated value is printed to the console.

The thermal pad of the temperature sensors is, from a thermal perspective, not optimal coupled respective thermal sensitive components. This can lead to severe differences between the actual temperature of the components and the temperatures sensed and shown by the temperature sensors.

Therefore, the user must verify the temperature of those components under operating conditions by own temperature measurements. Do not leave the reference design powered when unattended.

2.4.2.4 VT100 Terminal

The user interface uses a standard UART with 115200 Baud that can be connected using a USB-UART cable to any PC. The MSP430 software makes use of the VT100 [1] control sequences for formatting the output. With this, it is possible to implement a simple user interface without the need of special software on the PC. Only a simple serial terminal program is needed.

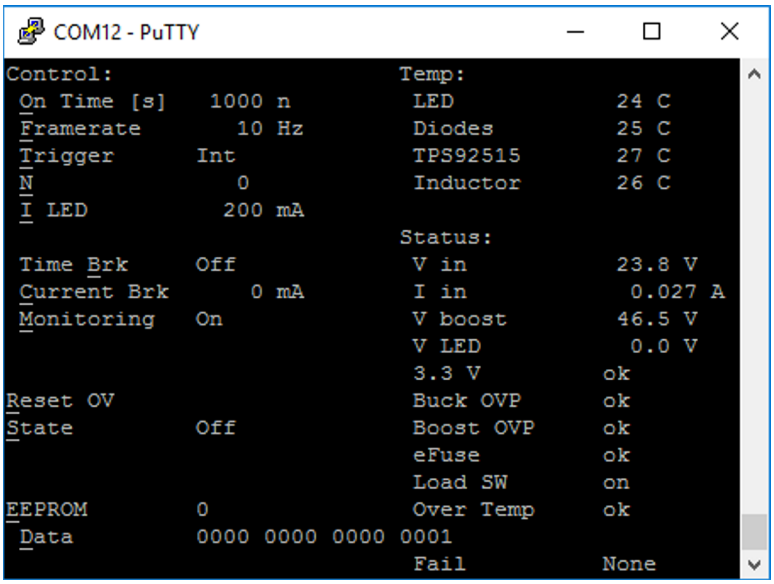


図 39. Terminal

図 39 shows the output of the terminal. The screen is basically divided in two zones: the left half for control and the right one for status output. Entering the underlined character jumps to the corresponding entry and allows the user to change the value. For more information, see 3.1.2.

To keep the flash jitter low, it is important to have no interrupts that can occur in parallel. UART transmission is either done by sending and waiting for the busy flag or it is synchronized to the timer IRQ that occurs every 100 µs.

To generate this menu, an array consisting of the structure describing these entries is created. For each value that can be displayed, a separate variable must be instantiated. The menu initialization routine iterates to this array and prints every entry to the specified position. Whenever a value is changed, only the field containing this value has to be updated.

```
struct menu_struct{
  const char *text;     /** Title of entry */
  const int startx;     /** x position */
  const int starty;     /** y position */
  char *value;          /** pointer to char array storing displayed value */
};
const struct menu_struct menu[]={
  {"Control:", 0, 1, ""},
  {" "UNDERLINECHAR("O")"n Time [s]", 0, 2, ontime_value},
  ...
};
```

(1) http://ascii-table.com/ansi-escape-sequences-vt-100.php

2.4.2.5 External Triggering

To react on an external event as fast as possible, the external trigger is handled by configuring the corresponding pin to cause an IRQ on the falling edge. Other IRQs must be avoided in this mode, as it happens that the external interrupt occurs during another IRQ is serviced and the pin interrupt has to wait.

To avoid this, the timer IRQ is reconfigured and the internal timing is derived from the external event. If no external event occurs within 5 seconds, a timeout occurs and the timer ISR causes the main loop to run.

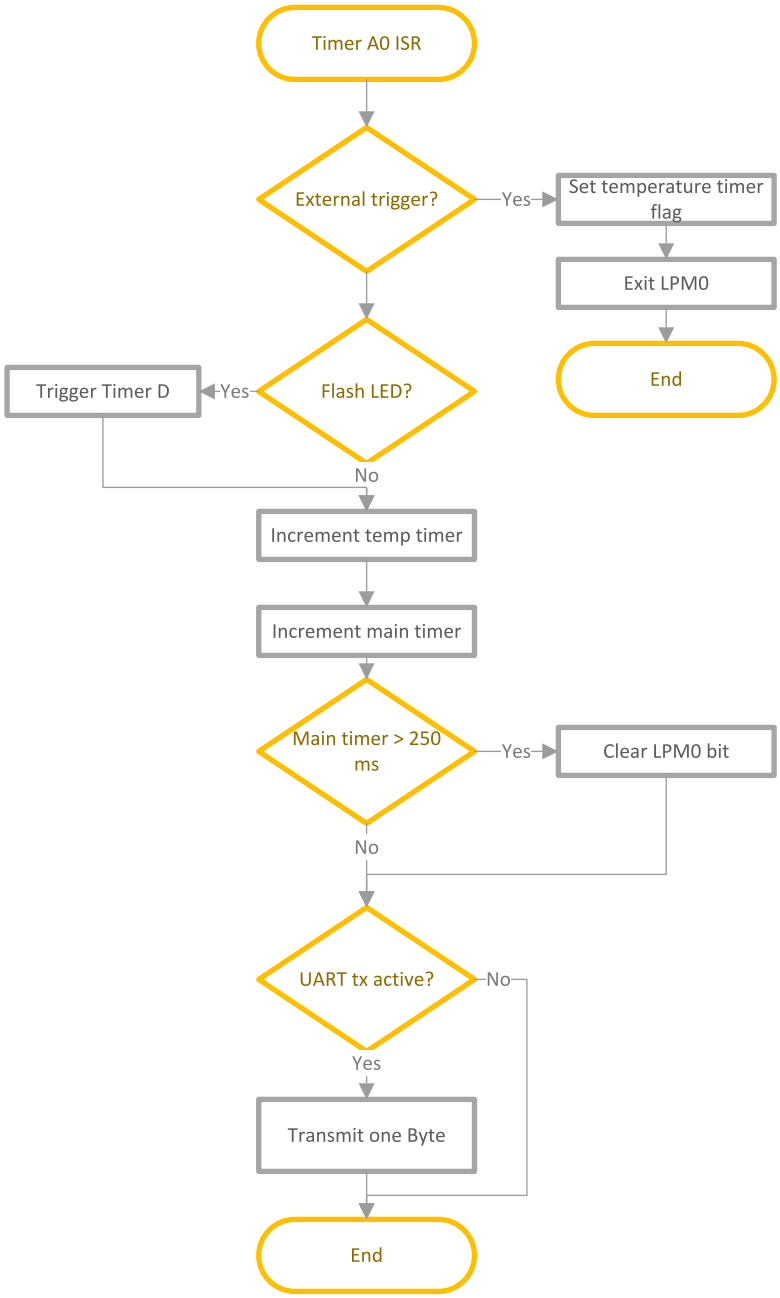


図 40. Timer ISR

Normally, the timer A occurs every 100 µs and controls the internal timing for sampling temperatures and LED flashing. Additionally, the UART sending is handled here. If an external trigger is selected, this ISR is called only when no external event occurred within the last 5 seconds.

To achieve a constant delay of 10 µs from trigger input to flash, the software has a time of less that 2 µs before the buck regulator has to be turned on. As soon as the ISR is entered, only a few flags are checked before starting the timer sequence described in 図 36. After starting the timer, enough time is left until the flash pulse. In this time, the software checks if temperature is okay, if the "on" flag is set, and if the number of pulses is already reached. If any of these conditions are a reason to stop, the timer is turned off and the sequence is canceled before the LED is turned on.

2.4.2.6 Main Program

The main function initializes every necessary peripheral and then only has to check for new temperature and voltage measurements and update the values on the user interface if monitoring is enabled. Whenever anything is entered using the interface, the new data must be checked and applied.

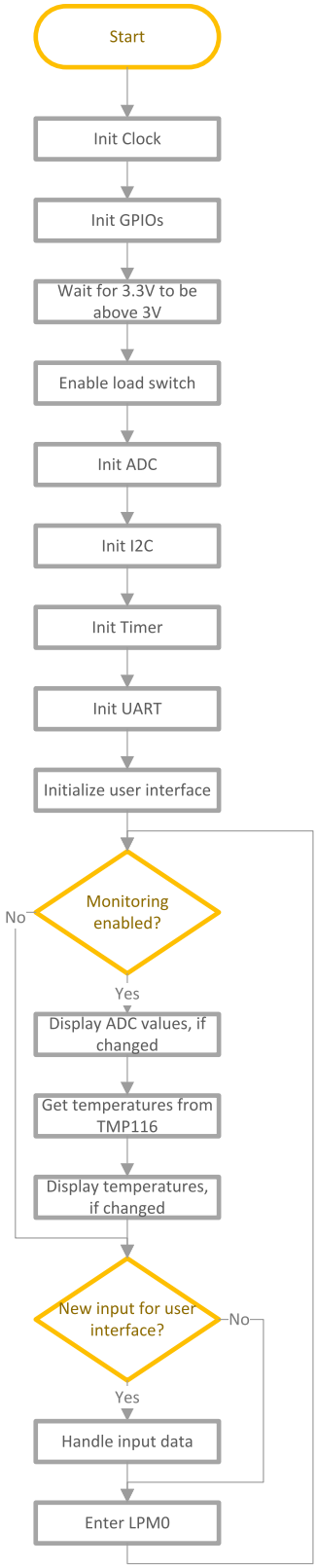


図 41. Main Program Flow

2.4.2.7 Jitter Reduction

When reacting on the trigger signal of a camera, precise timing of the flash is mandatory. Especially when flash time is below 1 µs, a jitter in the range of 1µs is too much. Whenever a system has to handle several IRQs that are not synchronized to each other, it happens that one IRQ occurs while another is handled.

図 42 shows what is happening in this case. The MSP430 is LPM0; MCLK is high when the timer IRQ occurs. Now it is a fixed time of about 1 µs until the timer ISR is handled. During the timer ISR, a port IRQ is triggered (FGEN Start). The MSP430 continues to execute the timer ISR and then change to the port ISR. As a result, the time from IRQ to handle the ISR is about 2 µs. Depending on when during the timer ISR this happens, a different time is needed until the port ISR is executed. This scenario must be avoided to have precise timing.

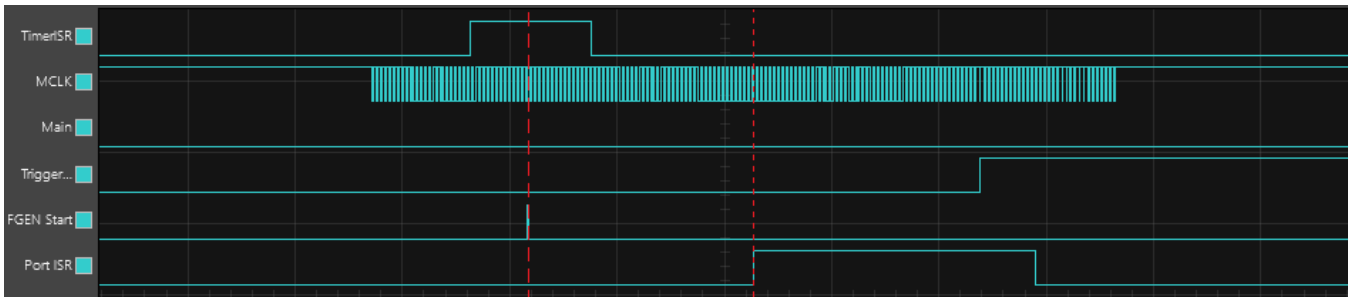


図 42. Jitter on External IRQ Caused by Timer (1 µs/div)

Whenever an exact timing is needed, the MSP430 must always be woken from LPM0 into the ISR.

2.4.2.8 Flash Time Bracketing

To implement flash time bracketing, the flash time values are stored in a lookup table as multiplication factors. This table is organized as a two-dimensional array of float values.

```
static const float flash_bracket_time[][5] = {
  {0.707, 0.841, 1, 1.189, 1.414},
  {0.630, 0.794, 1, 1.260, 1.587},
  {0.500, 0.707, 1, 1.414, 2.000},
  {0.250, 0.500, 1, 2.000, 4.000},
  {0.063, 0.250, 1, 4.000, 16.00}
};
```

Each bracketing value that is entered (0.25, 0.33, 0.5, 1.0, 2.0) is internally translated to an index of 1–5 and used as one index for the bracketing table. The other index is the number of the current flash pulse. When bracketing is selected, before each pulse, the on-time is calculated from the entered on-time and the multiplication factor and the timer is configured accordingly.

2.4.2.9 eFuse and Pre-Boost Current Setting

When J20 is set to position 7–8, the MSP430 must set the current limit depending on the input voltage. Channel A of the DAC082S085 is connected to the eFuse, which is designed to allow a current range of 0.28 A up to 1.43 A. The corresponding DAC value for each voltage is stored in a lookup table and applied when the voltage changes.

Channel B of the DAC is responsible for setting the average input current of the pre-boost regulator. To not exceed the current limit of the eFuse, the input current of the pre-boost is also set depending on the input voltage and is slightly lower than the current limit of the eFuse.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

図 43 shows the general hardware setup for this reference design.

Connect the power input connector J19 of this reference design to an isolated power supply with an output voltage capability in the range of 8 V to 36 V and an output power capability of at least 15 W. Connect the isolated UART interface (J16) of this reference design through a USB FTDI cable (TTL-232R-5V) with the USB port of a PC or notebook.

For the sequence to make these connections, start the terminal application, and switch on the power supply, see 3.1.2.

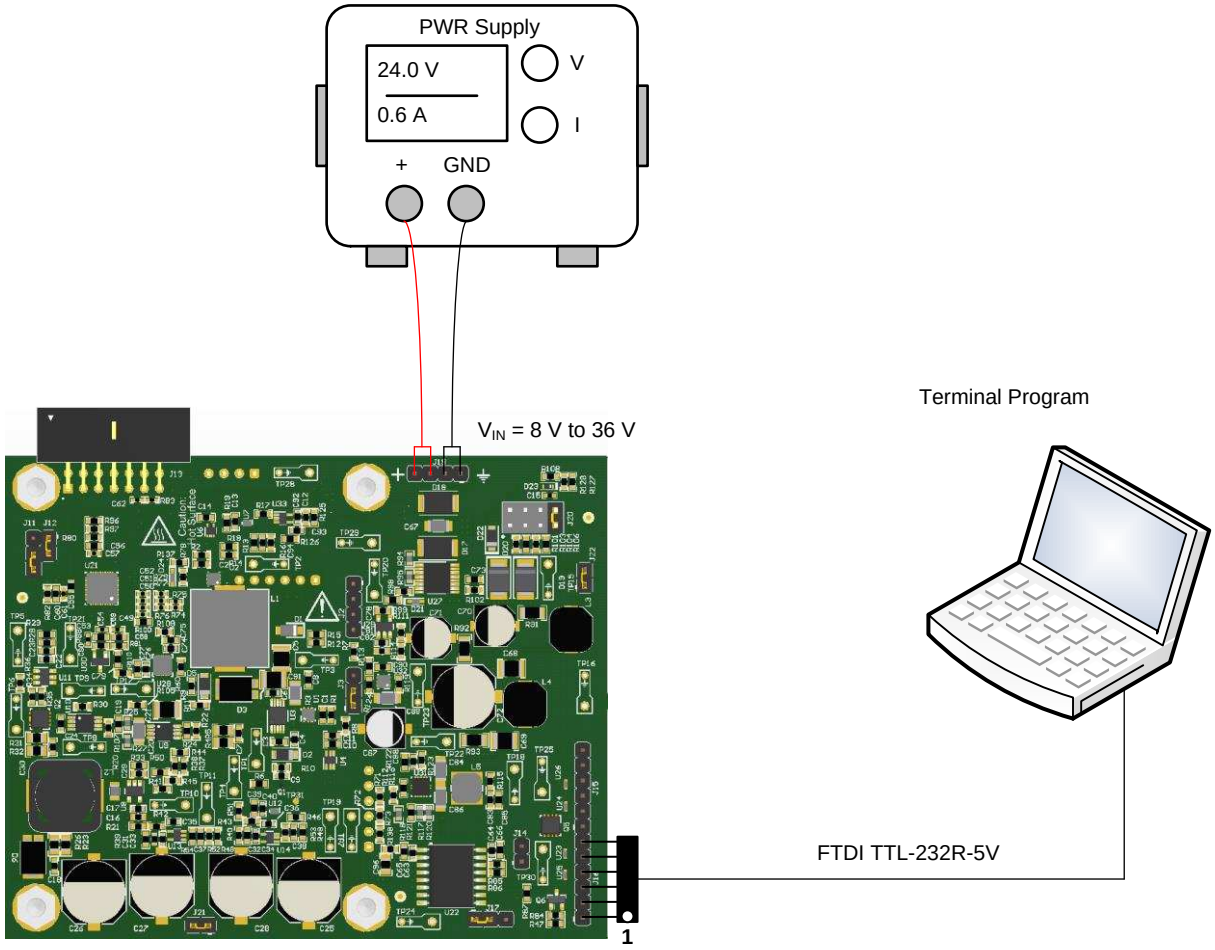


図 43. General Hardware Setup

3.1.2 Software

To get started with the design, connect the USB FTDI cable to a PC. If the driver is not found automatically, download from FTDI.

The cable gets enumerated as a serial port; the address is found in the device manager. Use a preferred serial terminal application (such as PuTTY or Tera Term) to connect to this port using a baud rate of 115200 baud.

First connect the cable to a PC, start the terminal application, and then power on the reference design. The MSP430 on the design sends some control commands at startup to setup the terminal.

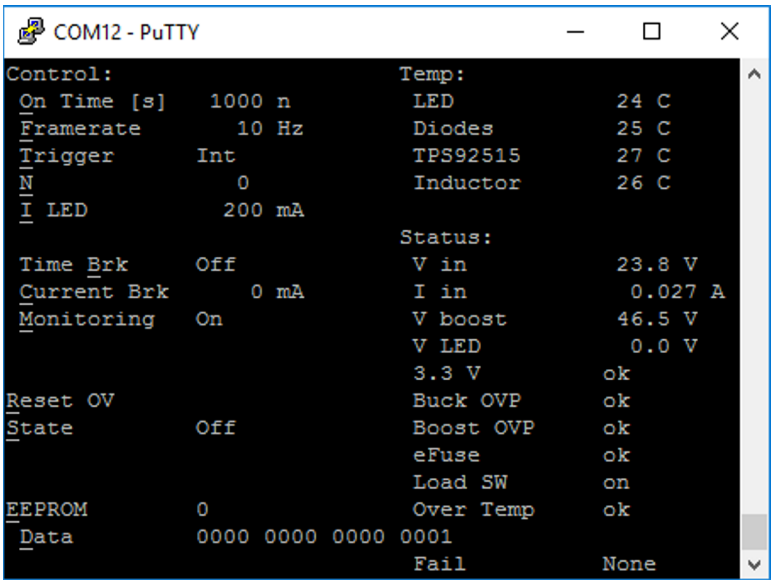


図 44. Terminal After Startup

When the MSP430 powers up and the 3.3 V are stable, the galvanic isolated UART gets turned on and the terminal is initialized and displays data as seen in 図 44.

After startup, the default settings are loaded (1 µs on-time, a frame rate of 10 Hz, a LED current of 200 mA, and internally triggered). By entering 's', the LEDs start flashing with the given parameters and "State Off" changes to "State On".

3.1.2.1 Changing Settings

Each parameter on the left side of the terminal screen can be changed by entering the underlined character. For example, to change the on-time, press 'o' and enter a time followed by the symbol representing the desired prefix ('n' for nanoseconds; 'u' for microseconds; 'm' for milliseconds). This entry overwrites the currently used value as seen in 図 45. There must not be a space between the entered number and the symbol representing the prefix.

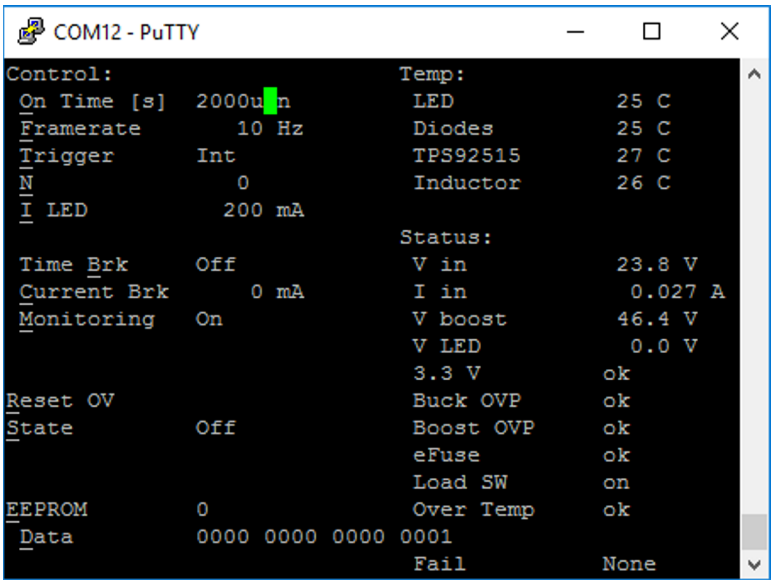


図 45. Changing Values

The input is parsed and shown after pressing enter. The terminal now shows the entered value.

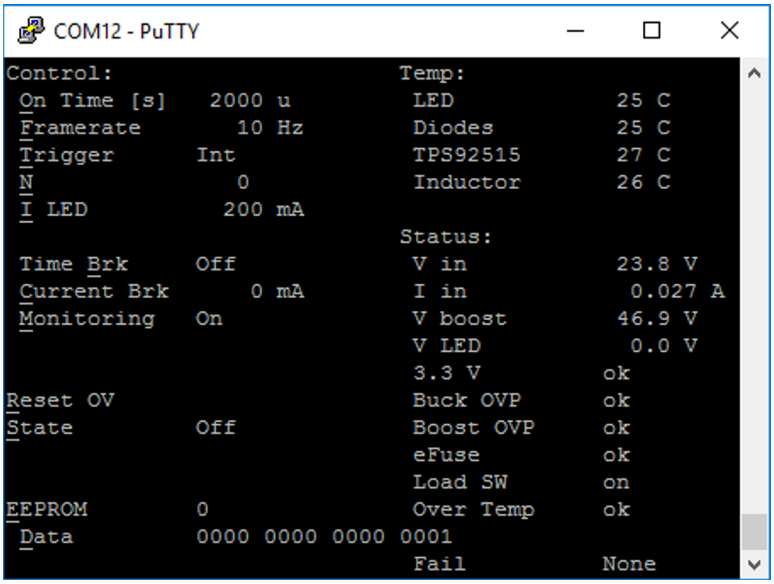


図 46. Accepted Value

It is *not* possible to enter floating point values except for the frame rate. Entering a symbol for the prefix is *only* possible for the "On Time" field.

表 9 lists the limitations of the parameter input mask.

表 9. Parameter Overview

PARAMETER	EXPLANATION	POSSIBLE VALUES
On Time	LED on time	200n to 4900m ('n','u','m' as symbols representing the prefix; No space between number and exponent; Do not enter 's' for seconds)
Frame Rate	Repetition rate of internal trigger	0 to 10000 (no unit; 0 = continuously on; changes to next rate that is possible with 100-µs timer); values between 0.2 and 9.9 can be entered with one digit behind the decimal delimiter ('.')
Trigger	Internal or external trigger	Toggles between "Int" and "Ext"
N	Number of flashes	0 to 32767 (0 = continuous flashing)
I LED	LED current	200 to 2400 (without mA or A, no floating point)
Time Brk	Flash time bracketing	Changes between "Off", "0.25", "0.33", "0.5", "1.0", "2.0", representing 1/4, 1/3, 1/2, 1 and 2 "stop increments" as used in photography when AEB is done by shutter speed steps (see 2.4.2.8 for the multiplication values)
Current Brk	Current bracketing	Increment the current after each flash by this step; only used when a number of flashes is specified
Monitoring	Print voltages and temperature to terminal	Toggles between "On" and "Off"
Reset OV	Resets OVP	N/A
State	Operation state	Toggles between "On" (LED Flashing) and "Off"
EEPROM	Selects TMP116 EEPROM	0 to 3 (0 = U1; 1 = U2; 2 = U15; 3 = U16)
Data	Displays EEPROM data	Enter the data to be written in hexadecimal and 16 bit chunks, as displayed

3.1.2.2 Status Information

The right side of the terminal screen gives information about the status of the reference design, including temperatures, voltages, current, and some flags. 図 47 shows the measurement points for the different displayed values.

The temperatures are measured at four different points, where the majority of the heat is generated: the LEDs, the discharge path (diodes and resistors), the buck inductor, and the buck regulator TPS92515HV. At those points, a TMP116 is placed and connected to the MSP430 using an I^2C bus. The TMP116 is programmed to generate an overtemperature event by pulling the ALERT signal low. Even when the measurements are disabled and no values are retrieved and displayed, the reference design still turns off the LEDs if a temperature of 70°C is exceeded. Additionally, this flag is displayed in the terminal window.

The displayed input voltage is measured at the input of the reference design (J19, EFUSE_VIN). Input current is measured by the eFuse and provided as an analog signal that is connected to the MSP430. The output voltage of the pre-boost regulator can be measured at TP7. The same voltage is monitored in hardware with a comparator and a flip flop to latch overvoltage events and disable the boost regulator. This flag is displayed in the terminal window. The same applies for the buck regulator (TP2).The voltage is monitored in the hardware and triggers a flip flop, disabling the TPS92515HV.

Additional displayed flags are:

- The eFuse status flag: The fault output of the TPS26602(for more information, see *TPS2660x 60-V, 2-A Industrial eFuse With Integrated Reverse Input Polarity Protection*)
- 3.3 V of the MSP430: The supply voltage of the MSP430 can be fed to the ADC and monitored. This voltage is used to switch on the load switch powering the 5 V part of the circuit after the 3.3 V are stable and above 3 V.

- Load switch status: Gives an information if the load switch is turned on. The terminal can only be displayed if the load switch is on, as the 5 V after the load switch power the ISOW7842 that is used for the isolated UART.
- Failure information: When the design switches off, this can have different reasons: overtemperature, undervoltage of the boost voltage, or a fault signaled by the eFuse. This is reported to show why it has turned off. This fault is reset by switching the LED on again (toggling State from Off to On).

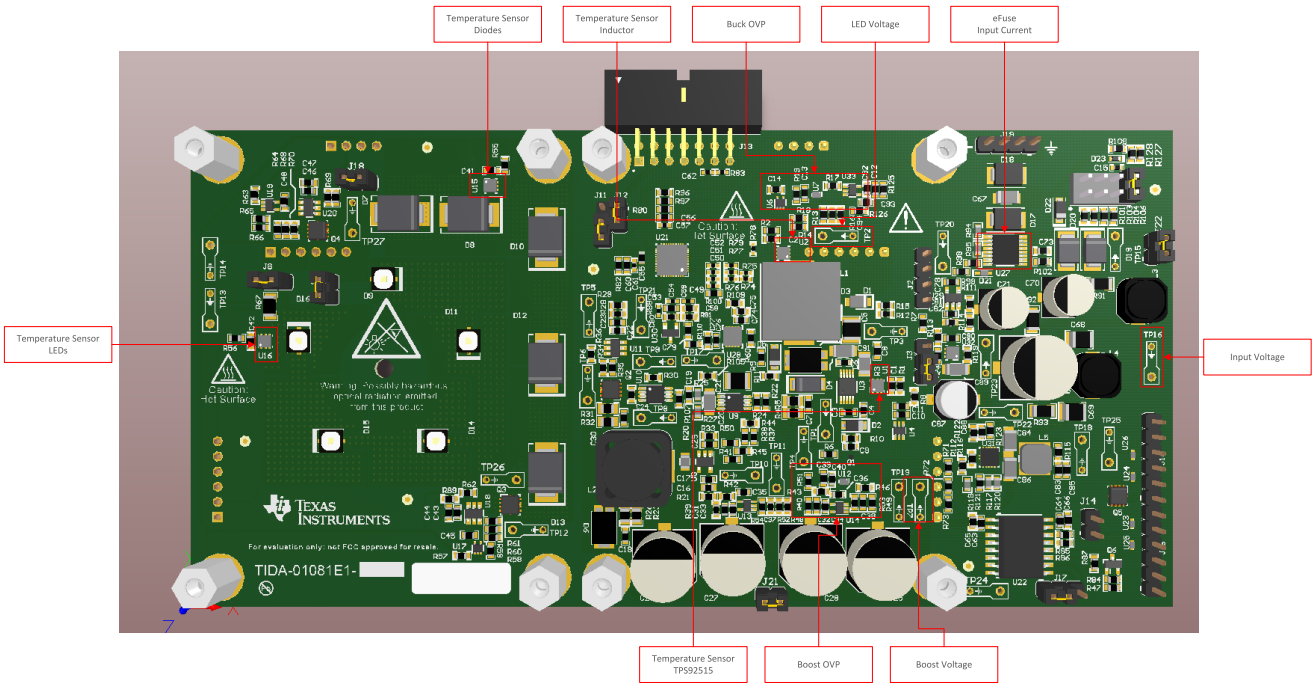


図 47. Status Information Measurement Points

3.1.2.3 Operation Modes

表 10. Operation Modes

MODE	DESCRIPTION
Continuous	When the frame rate is set to 0 Hz, continuous mode is active. The LEDs are turned on continuously with a set current up to 500 mA. Can be triggered externally (Trigger set to "Ext") or turned on from terminal.
Pulsed	The frame rate has to be set to any other value than 0 to enable pulsed mode. The pulse width ("On time") can be set, as well as the current. The number of pulses ("N") has to be set, entering 0 will allow infinite number of pulses. This mode has to be combined with internal or external trigger.
Externally triggered	To provide an external trigger signal, set trigger to Ext. Depending on the frame rate value (0 = Continuous, else = Pulsed) the LED will turn on or flash the preset time every edge of the trigger signal. Changing the trigger is only possible when State is set to off.
Standalone (internally triggered)	For internal triggering, the trigger has to be set to Int and a frame rate with any value above 0. This will cause LED flashes with a repetition frequency set as frame rate. Changing the trigger is only possible when "State" is set to off.
Switched	To enter switched mode, set the frame rate to 0 Hz and the trigger source to Ext. The reference design will now switch on and off depending on the level of the trigger input.
Multi-pulsed	To flash only a given number of pulses, set "N" to the number of desired pulses. 0 will lead to infinite pulses. This parameter is used with internal and external trigger.

表 10. Operation Modes (continued)

MODE	DESCRIPTION
AEB	To enable exposure bracketing set "Bracketing" to any value. This will flash five pulses with different flash time based on the entered "On Time". See 2.4.2.8 for the resulting times. These pulses can be triggered internally or externally. Also it is possible to vary the current of each LED flash by setting Current Brk and the number of flashes to the desired value.

In all modes, it is necessary to set the State to On; otherwise, it will not flash. Some values are changed after entering due to hardware limitations, such as timing constrains or power requirements, that exceed the design power. It is possible to enter configurations that exceed limitations that cause malfunctions or damage the design. Be careful when entering or changing configurations and parameters.

3.2 Testing and Results

3.2.1 Operation Modes

3.2.1.1 Automatic Exposure Bracketing (AEB)

This reference design and the related terminal software are able to demonstrate LED brightness bracketing (implemented by current bracketing, see 図 48) as well as time bracketing (see 図 49) as prerequisites needed for AEB.

- Channel 3: TP13—I_LED measured as voltage (100 mV / A) across the current sense resistor R67
- Channel 4: TP2—BUCK_VOUT (represents the LED voltage)

The LED current changes in the shown current bracketing example from 200 mA to 2400 mA in equal increments of 550 mA. The LED voltage is almost independent from the LED current as a result of the nonlinear VF versus IF characteristic of the LEDs D9, D11, D14, D15, and D16.

The time bracketing example has a fixed LED setting of 1000 mA. The 400-µs on-time is valid for the centered pulse in case of the time bracketing. The on-time of the LED pulses varies according to the "Time Brk" setting of "0.5" stop increments with the sequence 0.500, 0.707, 1, 1.414, and 2.000 of multiplication factors referred to the centered pulse width.

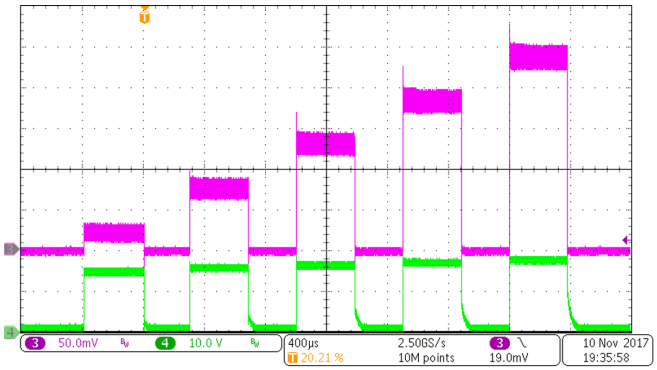


図 48. Current Bracketing: On Time = 400 µs, Frame Rate = 1428 Hz, N = 5, I LED = 200 mA, Current Brk = 550 mA, 5 Steps From 200 mA to 2.4 A in 4 Increments of 550 mA

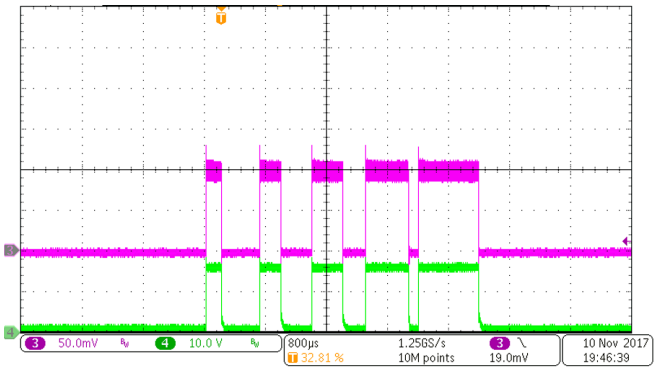


図 49. Time Bracketing: On Time = 400 µs, Frame Rate = 1428 Hz, N = 5, I_{LED} = 1000 mA, Time Brk = 0.5

3.2.2 External Triggering

This reference design uses the falling edge on TP24 (non-isolated Trigger_In, channel 1) to trigger a flash (pulse) of the LEDs. The external trigger signal generated by a pulse generator is applied to the isolated NPN-IN (pin 4) of the isolated trigger interface (J15, channel 2). The LED current is probed on TP13 (100-mΩ current sense resistor on the LED board) and assigned to channel 3. Channel 4 shows the isolated trigger output signal probed on the isolated TTL-OUT (pin 2 of J15).

The test verified the targeted 10-µs trigger delay time between the falling edges of the trigger input signals and the rising edge of the LED current 図 50. The "delay"time to trigger external systems by means of the isolated trigger output of this reference design is –6.5 µs (time between the rising edge of the Trigger_Out and the start of the LED pulse).

図 51 shows that the propagation delay caused by the digital isolator (U22) is matching its datasheet specification and is with only 14 ns negligible for to use in this reference design.

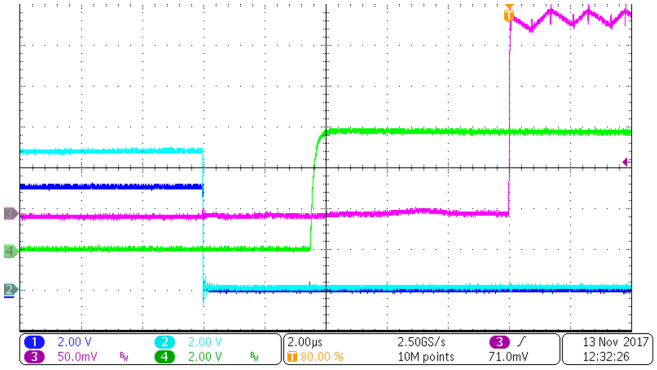


図 50. Trigger Delay of 10 µs Fixed

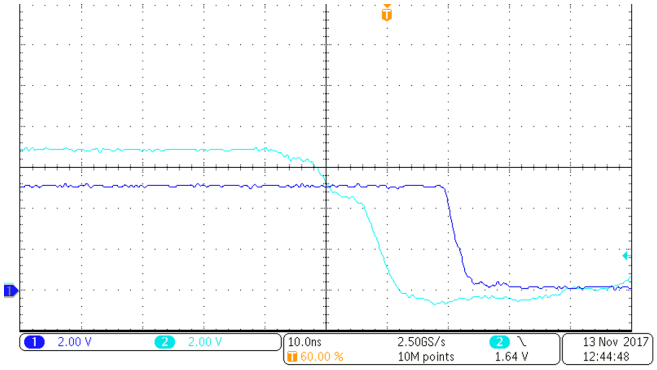


図 51. ISOW7842 Propagation Delay of 14 ns

3.2.3 LED Buck

The LED buck is evaluated "stand-alone" with a resistive load instead of the LED board. The following test conditions and test setup are used:

- Test without the LED board
- Firmware modified: the temperature sensors U15 and U16 from the missing LED board must not cause a fault, BOOST_VOUT/BUCK_VIN undervoltage fault disabled
- J19-pin 3 powered by external 15V (ground on J19, pin 2) to ensure that the board's complete control electronic (MCU, isolated power and data interface, and so on) is powered under normal operating conditions
- Jumper J21 removed to disconnect the LED buck from the pre-boost. Pre-boost is running in no-load condition, just with C26 and C27 as its output capacitor. Pre-boost VOUT control senses VOUT_BOOST on the remaining C26 or C27 and works therefore as expected—supervised with scope probe on J21-pin 2 referred to ground of the board. C28 and C25 act as bulk bypass capacitors for the LED buck converter.
- Buck_VIN is powered from external power supply, connected through an ammeter (to measure the buck's input current) to J21-pin 1 (ground on J19-pin 1). BUCK_VIN is sensed on J21-pin 1, also referred to J19-pin 1.
- USBport of the PC or notebook connected through an FTDI cable to the isolated UART interface header J16, continuous mode selected in terminal (frame rate setting "0") to switch the buck on all the time.
- Jumper SH-J3 is placed on pin 2 and 3 of header J3 to enable external V_IADJ. V_IADJ_EXT fed into J2-pin 4; ground is connected to J2 pin 2.
- Scope probe connected to the buck's switch node TP1 (BUCK_SW) to supervise correct switching of buck without spikes.
- 1-µF, 100-V X7R in parallel to 330 pF and 100µF / >50-V aluminum electrolytic capacitor connected to J1-pins 3 and 4.To avoid that, AC voltage and AC current are seen by the voltmeters and ammeter measuring the output voltage and output current of the buck.
- Power resistor decade connected to J1-pins 2 and 5, ammeter for measurement of BUCK_IOUT inserted into the wire connected to J1-pin 5. Current probe on the wire connected to J1-pin 2 to verify that AC part of current does not flow through the power resistor decade and ammeter. The

oscilloscope channel to which the current probe is connected to is set to its highest sensitivity and AC coupling. Voltmeter for measuring BUCK_VOUT connected to J1-pins 1 and 6.

The input voltage (BUCK_VIN) of the buck had been varied between 38 V and 48 V. The performance of the buck is evaluated at two different output voltages (BUCK_VOUT) of 13 V and 17 V to emulate the variations of forward voltage of the LED board. The load current was stepped in 300-mA increments from 200 mA up to 2.6 A for the characteristics of switching frequency FSW versus IOUT (図 53) and for Efficiency versus IOUT (図 54.

Similarly, the external V_IADJ_EXT voltage is stepped up from 250 mV to 2.25 V in increments of 250 mV to evaluate the BUCK IOUT versus BUCK V_IADJ_EXT characteristic presented in 図 52.

A performance comparison of an initial test conducted with the LED Board connected versus the previously described test with a resistive load is provided in 図 55. VOUT is measured on J18-pin 1, referred to J8-pin 1 of the LED board. IOUT is measured across J8 (100-mV, 1-A voltage drop across R67). The results of the test are similar—the differences are based on the non-linear VF/IF characteristic of the LEDs and on the missing bypass path for the AC part contained on VOUT and IOUT (the bypass capacitors 100 µF ∥ 1 µF ∥ 330 pF had not been used for this initial test with the LED board).

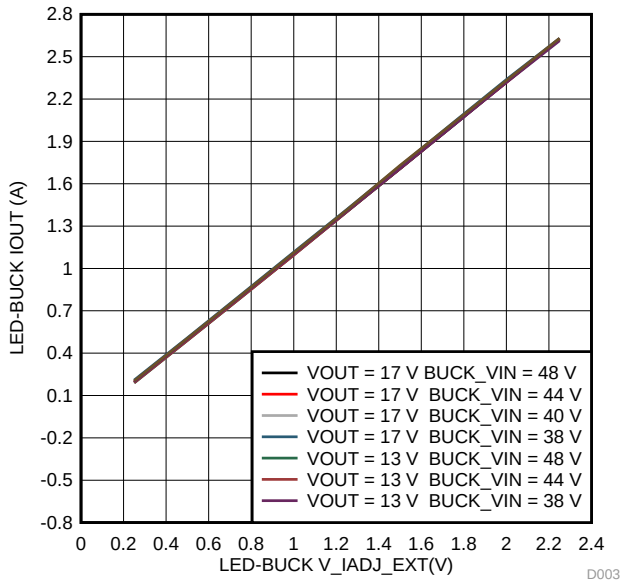


図 52. IOUT vs V_IADJ_EXT

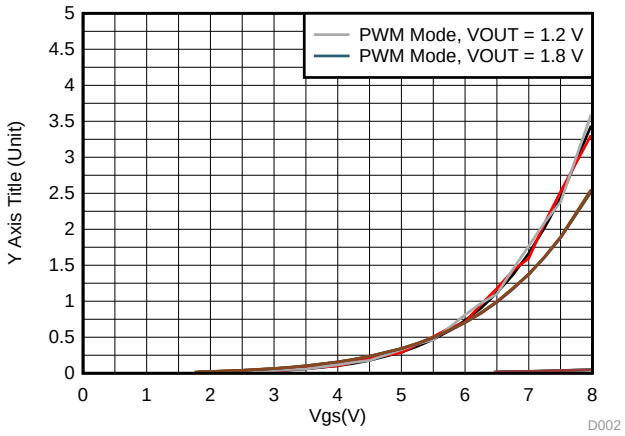


図 53. Switching Frequency vs IOUT

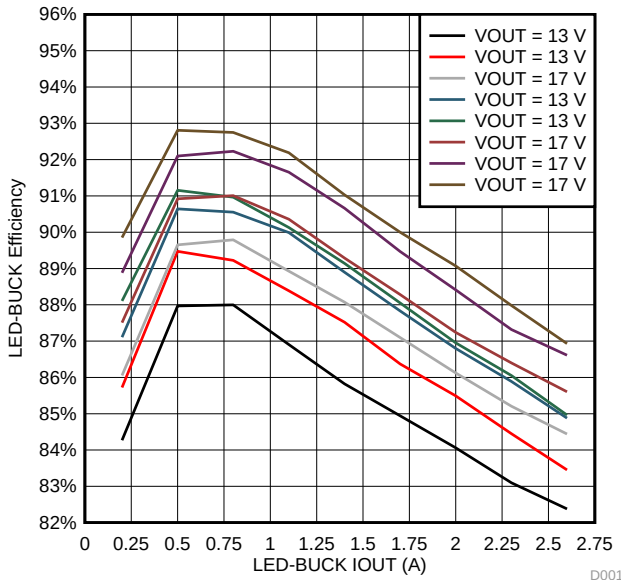


図 54. Efficiency vs IOUT

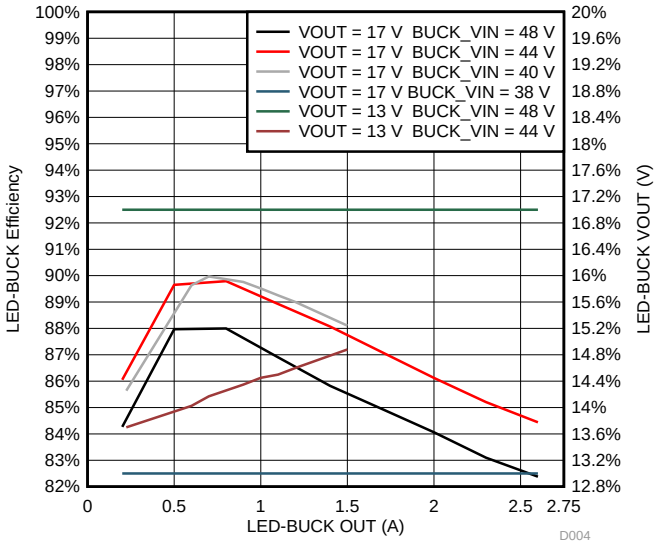


図 55. LED Efficiency and VOUT_vs_IOUT: Comparing Test With LED Board vs Resistive Load

The waveform on the switch node of the LED buck are evaluated in standard configuration and with parameter control through the terminal running on a notebook. The reference design is powered by a 15-V source connected to J19.The switch node waveform is probed on TP1 (BUCK_SW) for LED currents of 200 mA an 2.4 A. The results are shown in 図 57 and 図 56. Channel 1 represents the switch node, and Channel 3 shows the LED current waveform probed on TP13 (I_LED) measured as voltage (100 mV/A) across the current sense resistor R67.

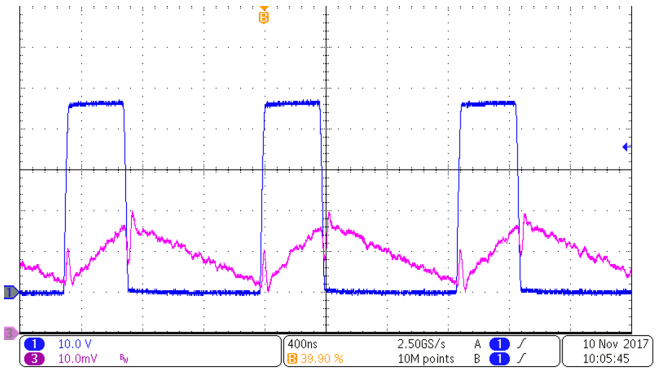


図 56. Buck Switch Node at 200 mA of LED Current

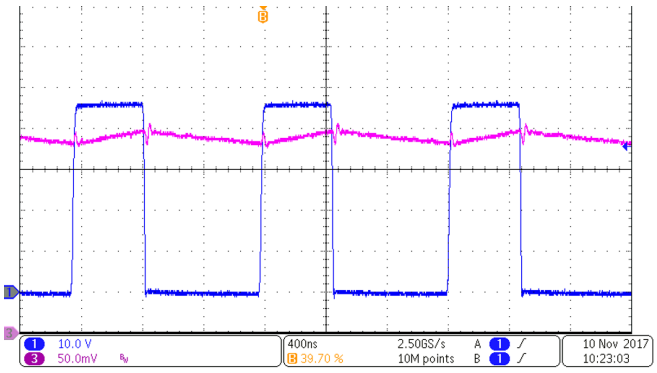


図 57. Buck Switch Node at 2400 mA of LED Current

To evaluate the OVP of the LED buck, use the same test setup to evaluate the switch node. The probes are connected as follows:

- Channel 1: TP1—switch node (BUCK_SW)
- Channel 2: TP3—BUCK_ON signal
- Channel 3: TP13—I_LED measured as voltage (100 mV/A) across the current sense resistor R67
- Channel 4: TP2—BUCK_VOUT

The reference design is configured for an LED on-time of 450 µs, a frame rate of 1000 Hz and an I_LED of 500 mA. The following figures show a sequence of three LED pulses; the end of second and the first LED ON pulse is during normal operation completely controlled by the BUCK_ON signal. This sequence happened in 図 60 during the OFF-time of the buck converters (BUCK_SW is roughly on ground potential, freewheeling of inductor L1, decreasing I_LED). 図 61 shows this similarly for the ON-time of the buck. When BUCK_SW is roughly at BUCK_VIN potential, U3's high-side switch is ON, increasing I_LED. Both figures have in common that first the BUCK_ON signal goes intentionally low, and after that the I_LED and BUCK_VOUT fall to zero.

The opposite happens during an overvoltage event. First the I_LED is interrupted and goes suddenly to zero. BUCK_VOUT ramps up immediately and is then clamped by D1 to the BUCK_VIN potential. Overvoltage is detected, causing the BUCK_ON signal to be forced low even before the configured LED ON-time had been elapsed.

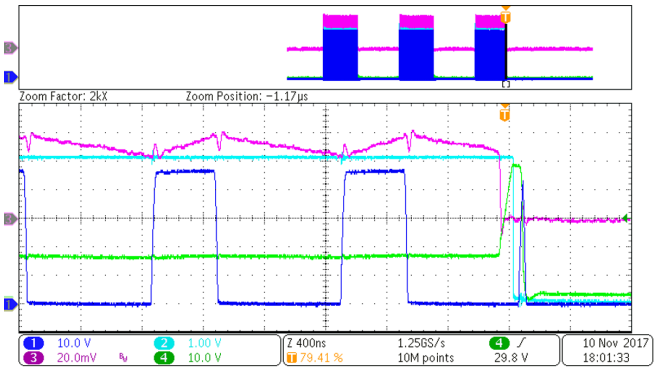


図 58. LED Buck OVP—Third LED Pulse Stopped After Overvoltage Caused by Removing SH-J5

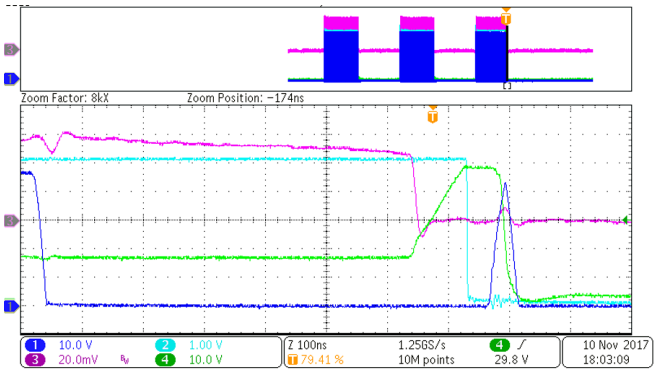


図 59. LED Buck OVP—Zoomed-in View (100 ns/div) of 図 58

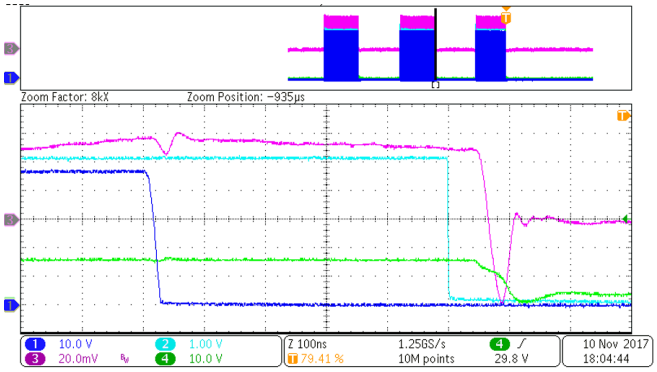


図 60. LED Buck Normal Operation Control Through BUCK_ON Signal, LED ON/OFF—Transition During t_{OFF}

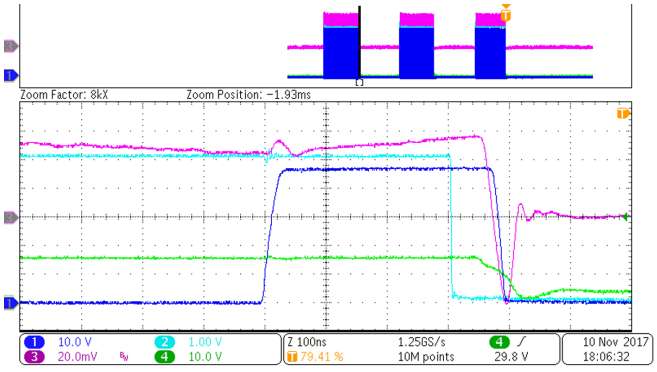


図 61. LED Buck Normal Operation Control Through BUCK_ON Signal, LED ON/OFF—Transition During t_{ON}

3.2.4 Pre-Boost

The switch node of the pre-boost is probed on TP6 to test different output resistors for the MOSFET driver U11. Initially, the resistor values as shown in 図 62 and 図 63 are used. There is a slight ringing during the falling edge of the switch node (transition to the ON-state of the FET) of the MOSFET. This ringing is completely gone after increasing the values of the resistors as shown in 図 64 and 図 65. The latter resistor values have therefore been used for the final build. The testing is done with 8 V applied to J19 and a resistive load on pin 2 of header J19.

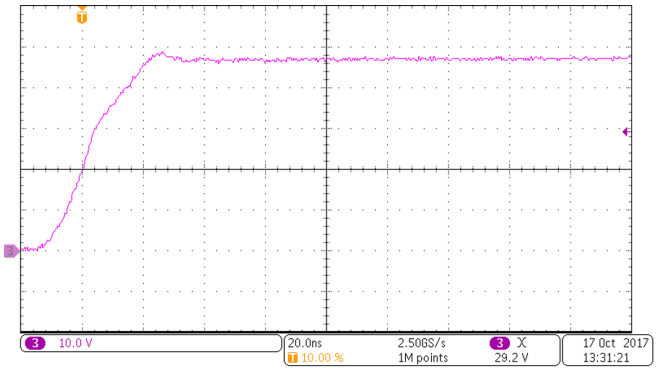


図 62. Pre-Boost Switch Node, Rising, R34 = 0 Ω, R35 = 3.32 Ω

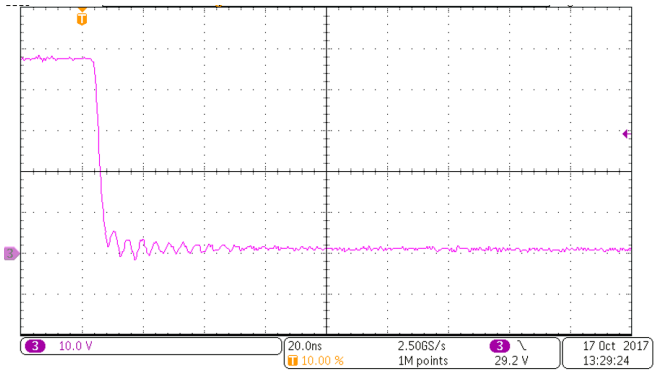


図 63. Pre-Boost Switch Node, Falling, R34 = 0 Ω, R35 = 3.32 Ω

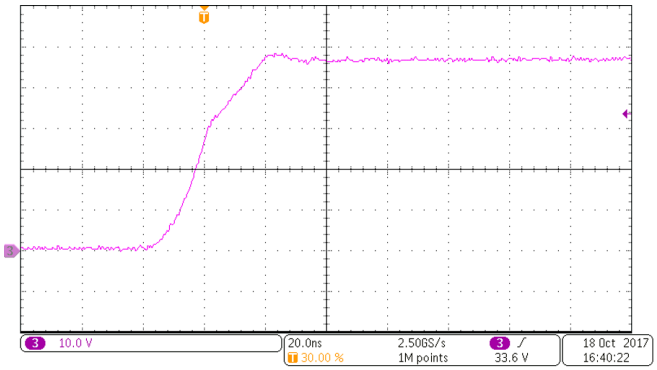


図 64. Pre-Boost Switch Node, Rising, R34 = 15 Ω, R35 = 15 Ω

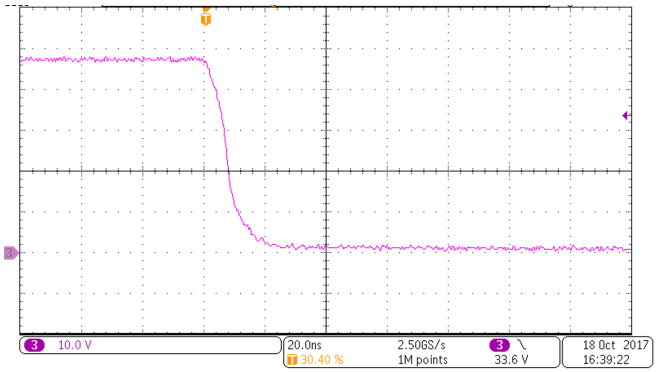


図 65. Pre-Boost Switch Node, Falling, R34 = 15 Ω, R35 = 15 Ω

3.2.5 Common Power Block

3.2.5.1 System Power Up

The waveforms during hot-plug of the systems power input is monitored and are shown in the following figures. The test is conducted with 35 V of input voltage. The sharp positive and negative spike shown at the beginning of the input current waveform (channel 4 in 図 66) is the inrush current for charging C67, a 1-µF MLCC capacitor. All other capacitors are at this moment still disconnected by the eFuse. The charging of all the other capacitors (in total more than 500 µF in capacitance) starts with the rising of the input current to roughly 100 mA and the rising of the voltage on channel 1 (FILTER_OUT). The charging is very smoothly and well controlled by the eFuse.

The additional rising and peaking of the input current is related to the start of the 5-V buck (channel 2) and the start of the 3.3-V LDO (channel 1 in 図 67), which is enabled by the PG_5V-Buck signal (TP19). The next rise in input current is a 330-mA constant current pulse, which is slightly longer than 40 ms. This pulse is the initial start of the pre-boost and it is clearly showing its constant input current control. The next much shorter input current pulse with almost the same current value is the first re-charging of the pre-boost's output capacitors by pre-boost.

The load switch U32 is enabled by the MCU. The output of U32 (+5V0) and the isolated 5-V rail (both shown in 図 67) come up simultaneously because the isolated DC/DC of the digital isolator U22 is powered by the output of the load switch.

The +5V0 rail also powers the MOSFET-Driver U11 of the pre-boost, delaying any switching and current consumption of the pre-boost during the system power-up.

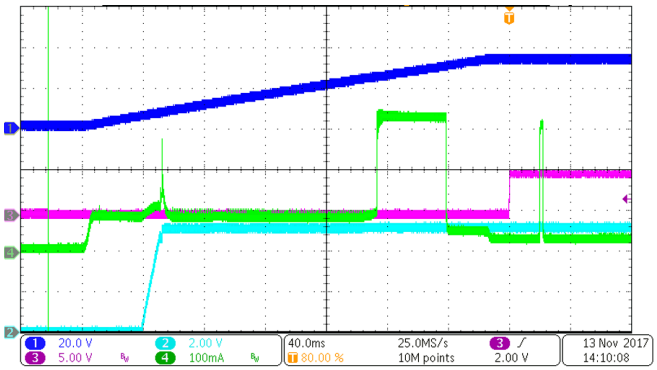


図 66. System Power Up 1

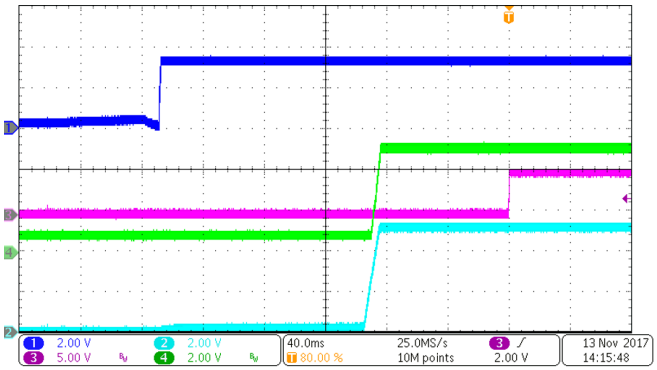


図 67. System Power Up 2

FILTER_OUT (can be considered to be equal to OUT pins of eFUSE on TP16	Channel 1	+3V3A on TP20
+5V_BUCK_OUT on TP22	Channel 2	+5V0 on TP23 (5-V rail controlled by the load switch U32)
eFuse $\overline{\text{FLT}}$ on TP28	Channel 3	eFuseFLT on TP28
System input current: current probe on J19 (pins 3 and 4)	Channel 4	+VDD_ISO on TP30 (isolated 5-V rail, loaded with 50 mA by 100 Ω)

3.2.5.2 5-V Buck

The evaluation of the 5-V buck converter includes probing its switch node waveform (TP18, channel 3) and of its output voltage ripple (TP22, channel 1) at 8-V and 36-V system input voltage. The isolated DC/DC is loaded with 100 Ω, causing 50 mA of current drawn from the isolated 5-V rail on TP30 and loading the non-isolated 5 V in the range of 100 mA, provided by the LM5165 (U31).

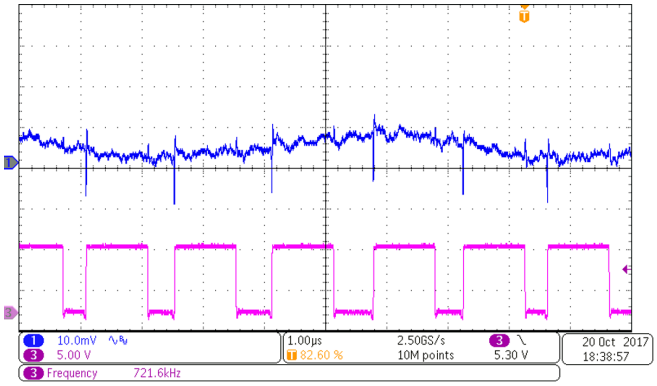


図 68. 5-V Buck: SW and VOUT Ripple; 8-V Input

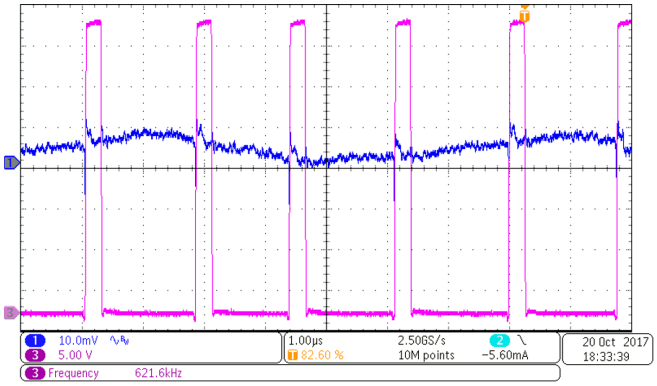


図 69. 5-V Buck: SW and VOUT Ripple; 36-V Input

The switch node waveforms are without any spikes. An additional snubber is therefore not needed. The output voltage ripple is in the range of 10 mVpp and is mainly related to the current consumption of U22, which is powered by the 5V.

3.2.5.3 eFuse

The current limit characteristic of the eFuse is evaluated for input voltages of 8 V, 24 V, and 36 V. The supply voltage is applied to J19. A power resistor decade is used to load the output of the eFuse. The current limit behavior is tested for the three selectable current limits by placing jumper SH-J20 on the respective pins of header J20. The test results are shown in 図 70.

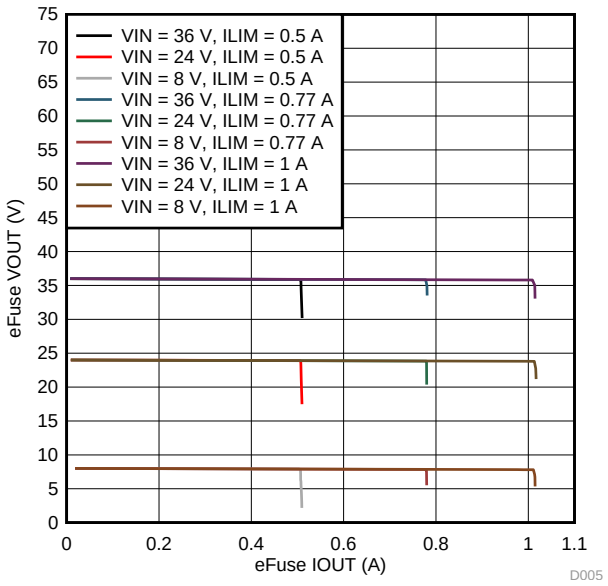


図 70. VOUT vs IOUT for Selectable Current Limit

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01081.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01081.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01081.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01081.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01081.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01081.

5 Software Files

To download the software files, see the design files at TIDA-01081.

6 Related Documentation

1. Texas Instruments, *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability Data Sheet*
2. Texas Instruments, *TPS92561 Phase-Dimmable, Single-Stage Boost Controller for LED Lighting Data Sheet*
3. Texas Instruments, *INA1x9 High-Side Measurement Current Shunt Monitor Data Sheet*
4. Texas Instruments, *TLV320x 40-ns, microPOWER, Push-Pull Output Comparators Data Sheet*
5. Texas Instruments, *UCC2751x Single-Channel, High-Speed, Low-Side Gate Driver Data Sheet*
6. Texas Instruments, *TPS7A41 50-V Input Voltage, 50-mA, Very High Voltage Linear Regulator Data Sheet*
7. Texas Instruments, *TPS2660x 60-V, 2-A Industrial eFuse With Integrated Reverse Input Polarity Protection Data Sheet*
8. Texas Instruments, *DAC082S085 8-Bit Micro Power DUAL Digital-to-Analog Converter With Rail-to-Rail Output Data Sheet*
9. Texas Instruments, *LM5165 3-V to 65-V Input, 150-mA Synchronous Buck Converter With Ultra-Low IQ Data Sheet*
10. Texas Instruments, *Input EMI Filter Design for Offline Phase-Dimmable LED Power Supplies Seminar*
11. OSRAM Opto Semiconductors, *OSLON Black Flat LUW HWQP Data Sheet*

6.1 商標

7 About the Authors

JÜRGEN SCHNEIDER is a systems engineer at Texas Instruments, where he is responsible for developing TI Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in industrial electronics and has worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems, and electro-medical devices before joining TI in 1999. Jürgen has worked with TI as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars and has been one of the presenters of the industry-wide known TI Power Supply Design Seminar for multiple years. Jürgen also has the distinguishment of being elected as a Member, Group Technical Staff.

STEFFEN GRAF is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. He earned his master of science in electrical engineering at the University of applied science in Darmstadt, Germany.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。