参考資料

TI Designs: TIDA-01540
デッド・タイム挿入が組み込まれたゲート・ドライバを使用する三相インバータのリファレンス・デザイン

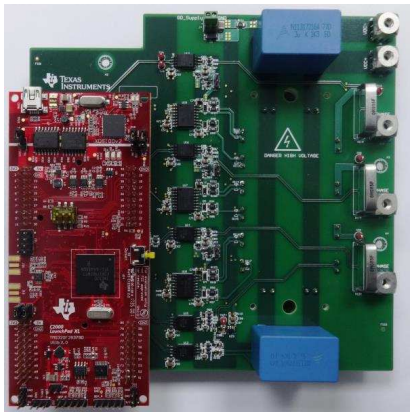
TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、強化され、絶縁された10kWの三相インバータのシステム・コスト低下と、小型の設計を実現します。単一のパッケージに格納されたデュアル・ゲート・ドライバを使用し、ブートストラップ構成によりゲート・ドライブの電源用にフローティング電圧を生成することで、システム・コストの低減と小型化を達成しています。デュアル・ゲート・ドライバUCC21520には、デッド・タイム挿入機能が搭載されており、抵抗オプションにより構成が可能です。この独自のデッド・タイム挿入により、入力PWM信号のオーバーラップに起因するシュートスルーから三相インバータが保護されます。過負荷、短絡、地絡、DCバスの低電圧と過電圧、およびハードウェアのIGBTモジュール過熱に対する保護により、システムの信頼性が向上します。

リソース

TIDA-01540	デザイン・フォルダ
UCC21520	プロダクト・フォルダ
AMC1301	プロダクト・フォルダ
AMC1311	プロダクト・フォルダ
OPA320	プロダクト・フォルダ
TLC372	プロダクト・フォルダ
TLV1117	プロダクト・フォルダ
TLV704	プロダクト・フォルダ
REF2033	プロダクト・フォルダ
TL431B	プロダクト・フォルダ
SN74LVC1G10	プロダクト・フォルダ
TIDA-00366	ツール・フォルダ



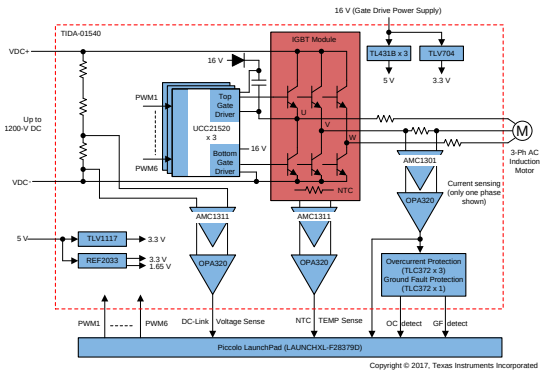
特長

- 強化された絶縁インバータで、定格10kWまでの200V～690V AC駆動に適切
- 強化された絶縁ハーフ・ブリッジ・ゲート・ドライバは伝搬遅延マッチングが非常に優れており、デッド・タイムが短縮(低い歪みと低い電力損失)
- インターロック、デッド・タイム、挿入機能の搭載により、PWM入力信号のオーバーラップ時にIGBTを保護(デッド・タイムはプログラム可能)
- 一次側ロジック障害に対するSTOおよびフェイルセーフ対策を備え、IGBTへのゲート駆動出力をハイサイドとローサイドの両方同時にシャットダウンするディセーブル信号を使用することで、さらに高い信頼性を実現
- UCC21520はCMTIが高く(100kV/µs)、スイッチング過渡に対して高い堅牢性を実現
- UCC21520はIGBTの誤ったターンオンおよびターンオフを回避するため、5nsよりも短い入力パルスおよび過渡ノイズを除去

アプリケーション

- ACインバータおよびVFドライブ
- サーボCNCおよびロボティクス
- 三相UPS
- 太陽光インバータ

TI E2E™ Community　E2E™エキスパートに質問



1 System Description

Insulated gate bipolar transistors (IGBTs) are mostly used in three-phase inverters that have numerous applications like variable-frequency drives that control the speed of AC motors, uninterruptible power supply, solar inverters, and other similar inverter applications. IGBTs have advantages such as high input impedance as the gate is insulated, a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation, and controllability of switching behavior to provide reliable short-circuit protection. The IGBT is a voltage-controlled device, which gives it the ability to turn on and off very quickly.

図 1 shows atypical application of a three-phase inverter using six isolated gate drivers. Note that each phase uses a high-side and a low-side IGBT switch to apply positive and negative high-voltage DC pulses to the motor coils in an alternating mode. The output voltage to the motor is controlled by pulse width modulation (PWM). The output voltage is an average of the peak or maximum voltage and the amount of time the transistor is turned on or off.

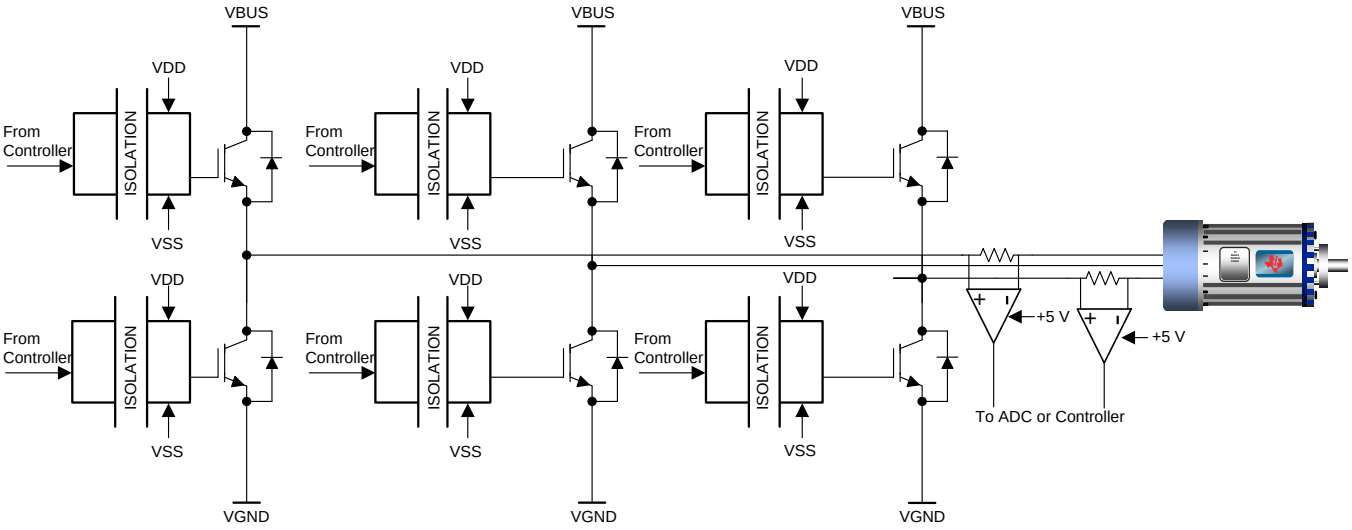


図 1. Three-Phase Inverter With Isolated Gate Drive

Apart from isolated gate-drivers for IGBTs, the three-phase inverters include DC bus voltage sensing, inverter current sensing, and IGBT protection (like overtemperature, overload, ground fault, and so on).

There are many end applications such as HVAC, solar pumps, and appliances where cost is major concern without compromising the performance. High-end three-phase inverters use sigma-delta (ΣΔ) modulators for current sensing, which also ask for using expensive controllers with built-in SINC filters. Using an isolated amplifier enables interfacing with low-cost M4-core MCU or TI's Piccolo™ with a built-in SAR analog-to-digital converter (ADC). The overload protection can be implemented in external hardware, which reduces software complexity. The isolated gate drivers need different supplies for both high-side and low-side gate drivers. Instead of using expensive isolated supplies for powering the gate drivers, using a bootstrap power supply reduces BOM cost on the power supply and also reduces the board space.

This reference design is based on the hardware of the TIDA-00366 design. The system design theory and test results relating to the power stage and current sensing are described in the design guide *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection* .

This reference design details a gate driver circuit for a three-phase inverter. The gate drive circuit comprises of three UCC21520 devices, which are dual IGBT gate drivers. The UCC21520 has many features to design a reliable three phase inverter.

The UCC21520 has a built-in dead-time insertion feature, which can insert a dead time into a complementary PWM for a half-bridge even if the PWMs overlap. The PWM overlap can be due to noise, damage of the connectors, wires connecting between the controller and gate diver, or a false PWM output. This feature is useful considering drives are trending to a more compact form factor. This new size can cause the PWM signals to have spacing and routing inside the drive if they are placed next to noise generators like high frequency signals, switching nodes, and so on. The simplest way to protect against IGBT shoot-through in this situation is to have interlock and dead band insertion.

The low propagation delay of the UCC21520 between the input and output contribute to reducing the deadband distortion in an inverter. In the reference design of the three-phase IGBT inverter, the deadband time is the sum of the time required for one IGBT to turn off and the other IGBT to turn on and the propagation delay. The low propagation delay allows the designer to use the minimum dead time possible for an IGBT module and reduce the related distortion in the current waveform.

The UCC21520 also has the single enable pin to disable the top and bottom IGBT, which can be used to implement safe torque of features in a motor drive.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
DC-Link input voltage	400 V to 1200 V
Gate driver supply voltage	16 V for low-side IGBT gate driver, 15 V (bootstrapped) for high-side IGBT gate driver
IGBT power module	Voltage rating: 1200 V, current rating: 50 A or more
Rated power capacity	10 kW
Inverter switching frequency	4 kHz (minimum) to 16 kHz; adjustable through software
Isolation	Reinforced (IEC 61800-5)
Gate drive	Unipolar 0 to 16 V, built-in PWM interlock and programable dead time insertion from 0 to 5 µs, input pulse rejection < 5 ns
Microcontroller	TMS320F28379D
Operating ambient temperature	–25°C to +85°C
Motor	Three-phase 400-V AC induction motor (ACIM)

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS
Power supply specification for MCU	3.3 V ± 5%
Feedbacks	Current sensing (±50 A), DC-Link bus voltage sensing (0 to 1026 V), IGBT module temperature sensing Interface for an external 3.3-V MCU with 3.3-V unipolar output input
Protections	Overload, overvoltage, undervoltage, ground fault, overtemperature
PCB	160 × 156 mm, four layers, 2-oz copper

2 System Overview

図 2 shows the system level block diagram for this reference design.

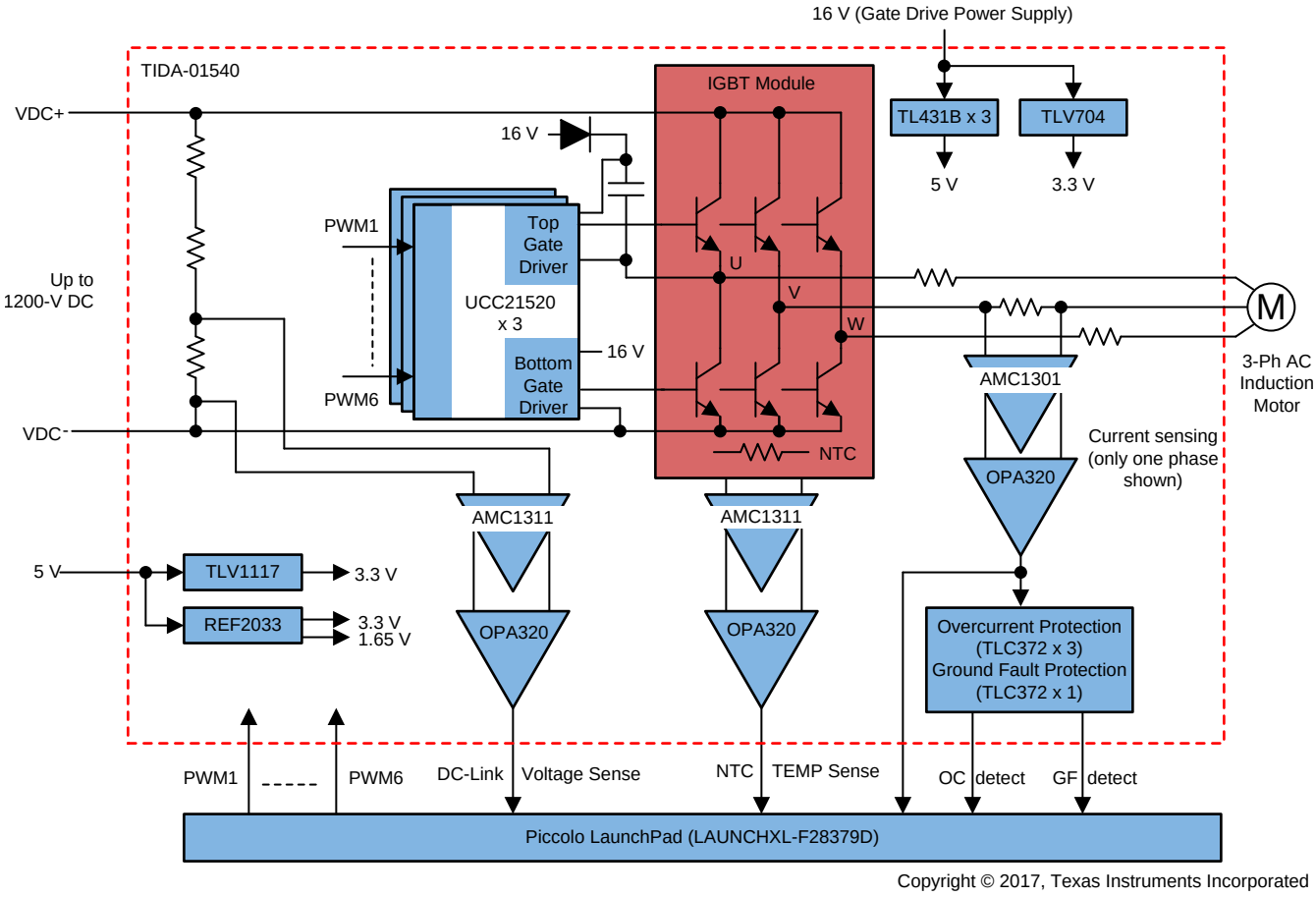


図 2. System Level Block Diagram for TIDA-01540

This reference design implements a three-phase inverter rated up to 10 kW. As shown in 図 2, the design uses three reinforced, isolated, dual IGBT gate drivers (UCC21520) to drive six IGBTs. The IGBTs are integrated into a module along with a temperature sensor (NTC). The IGBTs inside the module are configured in half-bridge configurations. Each half-bridge is driven by two IGBT gate drivers—top (high-side) and bottom (low-side). The design is interfaced with TI's Piccolo LaunchPad™, LAUNCHXL-F28379D, through two 20-pin connectors. The complementary PWM signals are generated from the LaunchPad. The three mid-points of IGBT half-bridges are connected. The board is designed to operate up to 1200-V DC for the inverter DC bus voltage.

Accurate phase current sensing with three-phase brushless motors is critical for motor drive performance, efficiency, and protection. This design uses in-phase current sensing using three 5-mΩ shunts and three reinforced isolated amplifiers (AMC1301). The benefits of using in-phase current sensing are:

1. Constant motor current flowing through the shunt, independent of IGBT switching
2. Easy detection of terminal-to-terminal short and terminal-to-GND short

The voltage generated across the shunt is amplified using the reinforced isolated amplifier AMC1301. The output of the AMC1301 is signal conditioned and converted to a single-ended signal using the OPA320. Outputs of all the three channels are fed into a microcontroller (MCU).

The inverter protects against overload, short circuit, ground fault, DC bus undervoltage and overvoltage, and IGBT module overtemperature. The DC bus voltage is dropped down using the resistor divider and fed to the AMC1311 for sensing. The under- and overvoltage are programmed in the MCU using the sensed signal. Similarly, the signal from NTC (integrated into IGBT module) is sensed using the AMC1311, and the sensed signal is fed to the MCU for over-temperature protection. The overload, short-circuit, and ground fault protections are implemented using comparators TLC372, which use the current sensed from the three shunts.

The board is powered through two external power supplies: one 16 V and the other 5 V. The low-side IGBT gate drivers are powered using 16 V, and high-side IGBT gate drivers are powered using a bootstrapped supply generated from 16 V. The MCU, op amps, and comparators are powered using 3.3 V generated from a 5-V supply using the TLV1117 (3.3 V). The design uses the TLV704 (3.3 V), TL431B, and REF2033 to generate other rails and references on the board.

Lower system cost is achieved by using the isolated amplifiers (AMC1301 and AMC1311) to measure motor current, DC-link voltage, and NTC voltage. The signals are interfaced with an internal ADC of the MCU. The system cost is also reduced by using a bootstrap power supply configuration for IGBT gate drivers.

2.1 Highlighted Products

2.1.1 UCC21520

The UCC21520 is an isolated dual-channel gate driver with a 4-A source and 6-A sink peak current. This device is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with best-in-class propagation delay and pulse-width distortion. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} reinforced isolation barrier with a minimum of 100-V/ns common-mode transient immunity (CMTI). Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1500-V DC. A disable pin shuts down both outputs simultaneously when it is set high and allows normal operation when left floating or grounded. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers.

- Operating temperature range: –40 to +125°C
- Switching parameters:
  - 9-ns typical propagation delay
  - 10-ns minimum pulse width
  - 5-ns maximum delay matching
  - 5-ns maximum pulse-width distortion
- CMTI greater than 100 V/ns
- Programmable overlap and dead time
- Rejects input pulses and noise transients shorter than 5 ns

2.1.2 AMC1311

The AMC1311 device is a precision, high-impedance input isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV_{PEAK} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry. The high-impedance input of the AMC1311 device is optimized to connect to high-voltage resistive divider circuits or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate voltage or temperature sensing and control in closed-loop systems. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1311 device simplify system-level design and diagnostics.

- 2-V input voltage range optimized for isolated voltage measurement
- Low offset error and drift: ±1.6 mV at 25°C, ± 21 µV/°C
- Fixed gain: 1
- Very low gain error and drift: ±0.3% at 25°C, ± 60 ppm/°C
- Very low nonlinearity and drift: 0.05%, 1 ppm/°C

2.1.3 AMC1301

The AMC1301 is a precision isolation amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. The input of the AMC1301 is optimized to connect directly to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control, resulting in system-level power saving and, especially in motor control applications, lower torque ripple.

- ±250-mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift: ±200 µV at 25°C, ± 3 µV/°C
- Fixed gain: 8.2
- Very low gain error and drift: ±0.3% at 25°C, ± 50 ppm/°C
- Very low nonlinearity and drift: 0.03%, 1 ppm/°C

2.1.4 OPA320

The OPA320 is precision, low-power, single-supply op amp optimized for very low noise. Operated from a voltage range from 1.8 V to 5.5 V, this device is well-suited for driving ADCs. With a typical offset voltage of 40 µV and very low drift overtemperature (1.5 µV/°C typical), this op amp is very well suited for applications like control loop and current sensing in motor control.

2.1.5 TLC372 (Q-Version)

The TLC372 consists of two independent voltage comparators, each designed to operate from a single power supply (3-V to 16-V range). The outputs are open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The TLC372Q is characterized to operate from –40°C to +125°C. The typical response time of comparators for the switching is 200 ns.

2.1.6 TLV1117 (I-Version)

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents. With excellent line and load regulations, the device is available in multiple packages and works for a temperature range from –40°C to +125°C.

2.1.7 TLV704

The TLV704 is a 3.3-V LDO with ultra-low quiescent current and operates over a wide operating input voltage of 2.5 V to 24 V. The device is an excellent choice for industrial applications that undergo large line transients. The TLV704 is available in a 3-mm × 3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.

2.1.8 REF2033

The REF2033 offers excellent temperature drift (8 ppm/°C, max) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 μA. In addition, the VREF and VBIAS outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to +85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. An extremely low dropout voltage of 10 mV allows this device to operate from very low input voltages.

2.1.8.1 TL431B (Q-Version)

The TL431 is a three-terminal adjustable shunt regulator with specified thermal stability over temperature ranges. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in many applications. The "B-grade" version comes with initial tolerances (at 25°C) of 0.5% and TL431BQ devices are characterized for operation from –40°C to +125°C.

2.1.8.2 SN74LVC1G10

The SN74LVC1G10 performs the Boolean function Y = !(A × B × C) or Y = !A + !B + !C in positive logic. With a supply range from 1.65 V to 5.5 V and availability in multiple packages. This NAND gate is characterized to operate from –40°C to +125°C.

2.2 System Design Theory

This reference design is based on the hardware of the TIDA-00366 design. The information on the IGBT inverter, IGBT gate driver, onboard power supply, and fault protection feature are given in the design guide *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection* .

注: This reference design is designed for a three-phase inverter, but 2.2.1 explains the circuits and components for one channel (U-Phase) only. The same explanation is applicable to other two channels (V-Phase and W-Phase).

2.2.1 Isolated IGBT Gate Driver

A three-phase inverter application uses six power switches (IGBTs in this case). To drive these switches, six totally independent gate drivers are required. Also, with a high-voltage operation, it is necessary to have enough isolation between primary and secondary side of the gate driver. The UCC21520 is an isolated dual-channel gate driver with a 4-A source and a 6-A sink peak current. The device drives power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with best-in-class propagation delay and pulse width distortion. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} reinforced isolation barrier with a minimum of 100-V/ns CMTI. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1500-V DC. 図 3 shows the internal structure of the UCC21520 gate driver.

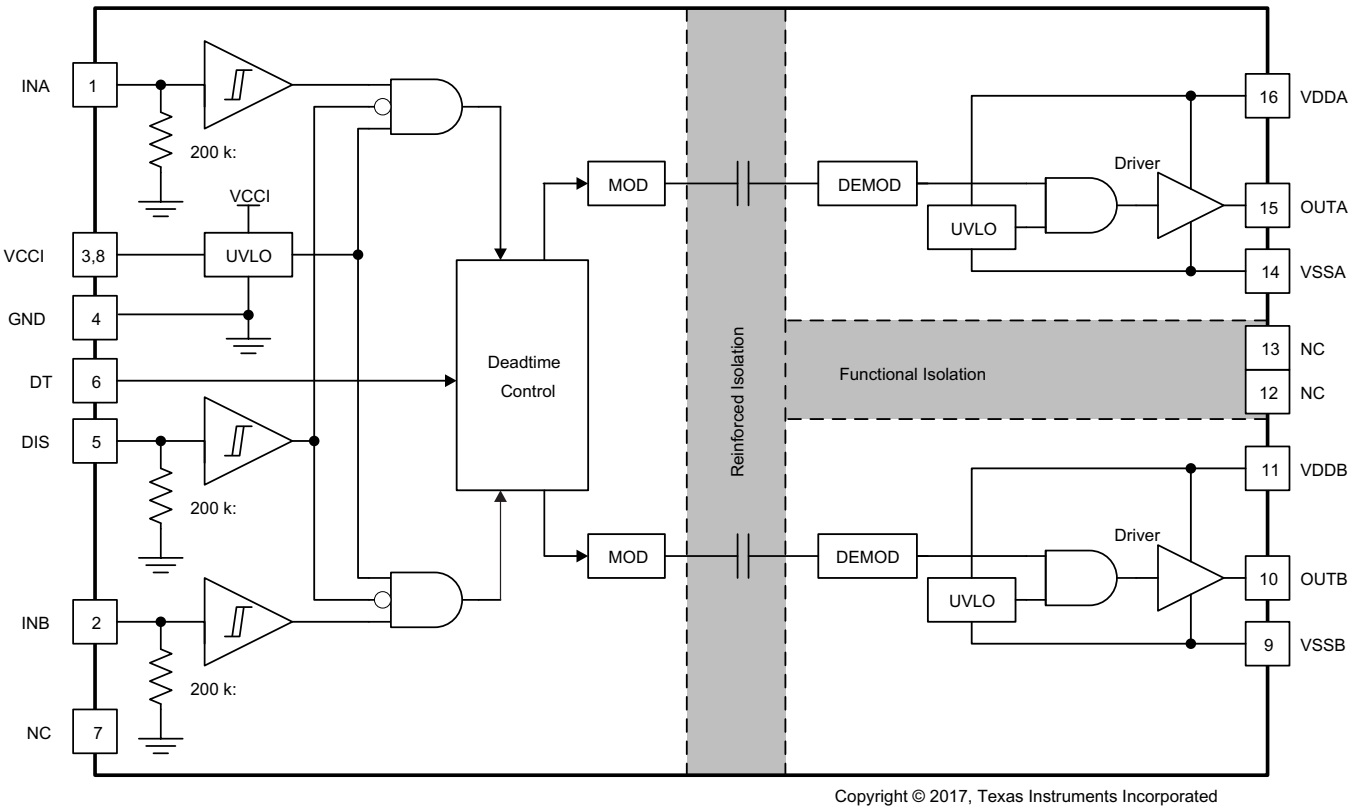


図 3. Functional Block Diagram of UCC21520

This driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). A disable pin shuts down both outputs simultaneously when it is set high and allows normal operation when left floating or grounded. As a fail-safe measure, primary-side logic failures force both outputs low. The device accepts VDD supply voltages up to 25 V. A wide-input VCCI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have undervoltage lockout (UVLO) protection. With all these advanced features, the UCC21520 enables high efficiency, high power density, and robustness in a wide variety of power applications.

図 4 shows the circuit for the UCC21520 and associated components implemented for half-bridge configuration for a three-phase inverter.

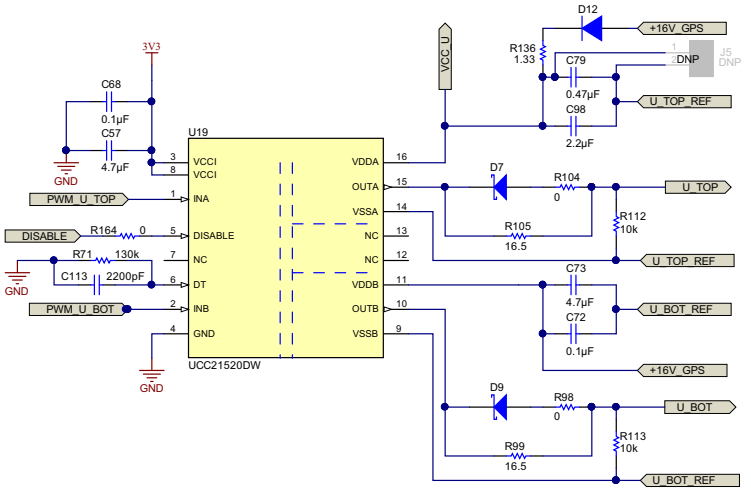


図 4. Gate Driver UCC21520 and Related Components and Circuits

2.2.1.1 Control Supply for Primary Side

VCCI pins (Pin 3 and Pin 8) are supplied with 3.3 V generated using the TLV1117 (3.3 V) (as explained in 2.1.6). C57 (4.7 µF) and C68 (0.1 µF) are used as local decoupling capacitors for VCCI pins.

2.2.1.2 Dead Time Control

The UCC21520 has a programmable dead time function using DT pin. Tying DT to VCCI allows the outputs to overlap. Leaving DT floating sets the dead time to < 15 ns. Placing a 500-Ω to 500-kΩ resistor between DT and GND adjusts dead time according to 式 1.

$$DT\ (in\ ns) = 10 \times RDT\ (in\ k\Omega) \quad (1)$$

A 130-kΩ resistor is connected between DT pin and GND pin, which sets the dead time to 1.3 µs as per 式 1. Select this resistor for a 1% tolerance to prevent any drift in the dead time. For this reference design, the dead time is controlled by the UCC21520 to ensure that there is always a minimum deadband. This deadband is useful in case a proper deadband is missing in the input PWM signal. C113 is a 2.2-nF capacitor used for filtering noise at the DT pin.

2.2.1.3 DISABLE Signal for Gate Drivers

The DISBALE pin is used to disable the gate drivers. The pin disables both driver outputs if asserted high and enables if set low or left open. This pin is pulled low internally if left open or floating. Tie this pin to ground if it is not used to achieve better noise immunity. For this reference design, the DISABLE pin is generated using a three-input NAND gate.

2.2.1.4 Supply for Low-Side Gate Drivers

The low-side gate drivers for all three channels are powered using 16V_GPS, which is supplied externally from connector J4 as shown in 図 5. VDDB is secondary-side power for driver B. It is supplied with 16V_GPS and locally decoupled to VSSB using low ESR and ESL capacitors C72 (0.1 µF) and C73 (4.7 µF), which are located as close to the device as possible. VSSB is ground for the secondary-side driver B and a ground reference for the secondary-side B channel.

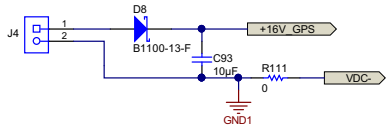


図 5. Gate Driver Power Supply

2.2.1.5 Bootstrap Power Supply for High-Side Gate Drivers

One of the most widely used methods to supply power to the high-side drive circuitry of a gate driver is the bootstrap power supply. The bootstrap power supply consists of a bootstrap diode and a bootstrap capacitor (with an optional series resistor). This method has the advantage of being both simple and low cost. The maximum voltage that the bootstrap capacitor (V_{BS}) can reach is dependent on the elements of the bootstrap circuit. Consider the voltage drop across R_{BOOT}, V_F of the bootstrap diode, and the drop across the low-side switch (VCE(ON) or VFP, depending on the direction of current flow through the switch).

2.2.1.6 Selection of Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the IGBT high without depleting the bootstrap capacitor more than 10% and the AMC1301 used for current sensing. A good guideline is to size C_{BOOT} to be at least 10 times as large as the equivalent IGBT gate capacitance (Cg) and capacitance required to supply the AMC1301 with constant current for one PWM period. Calculate Cg based on the voltage driving the high-side gate of the IGBT (V_{GE}) and the gate charge of the IGBT (Qg). V_{GE} is approximately the bias voltage supplied to VDD after subtracting the forward voltage drop of the bootstrap diode D12 (V_{DBOOT}). In this design example, the estimated V_{GE} is approximately 15 V, as式 2 shows.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 16\ V - 1\ V = 15\ V \quad (2)$$

The IGBT module in this reference design has a specified Qg of 0.47 µC. The equivalent gate capacitance of the IGBT can be calculated as 式 3 shows.

$$C_g = Q_g / V_{GE} = (0.47\ \mu C) / 15 = 0.0313\ \mu F \quad (3)$$

The bootstrap capacitor also has to supply the AMC1301 on the high-voltage side with a maximum of 6.5 mA. Considering the lowest PWM frequency that needs to be supported is 4 kHz, this implies the bootstrap capacitor must hold this charge for one PWM period (that is, ¼ kHz = 250 µs). The total charge consumed is 250 µs × 6.5 mA = 1.625 µC. At 15 V, the capacitance required to store this charge is calculated using 式 4:

$$C_a = Q_a / V_{GE} = (1.625\ \mu C) / 15 = 0.1083\ \mu F \quad (4)$$

After estimating the value for Cg, C_{BOOT} must be sized to at least 10 times larger than Cg, as 式 5 shows.

$$C_{BOOT} \geq 10 \times (C_g + C_a) = 10 \times (0.0313\ \mu + 0.1083) = 1.396\ \mu F \quad (5)$$

This reference design uses a parallel combination of 0.47-µF and 2.2-µF capacitors.

2.2.1.7 Selection of Bootstrap Diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case, a maximum of 1200-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 16-V supply. The diode must be able to carry a pulsed peak current of 11.28 A (as per 式 6). However, the average current is much smaller and depends on the switching frequency and the gate charge requirement of the high-side IGBT. This reference design uses a 1300-V, 1-A, fast recovery diode BYG23T-M3.

The bootstrap diode power dissipation (P_{DBOOT}) can be estimated based on the switching frequency, diode forward voltage drop, and the switching frequency of the PWM signal (f_{SW}). In this reference design, the switching frequency has been set to 16 kHz. 式 6 calculates the estimated power loss for the bootstrap diode.

$$P_{DBOOT} = 1/2 \times Q_g \times f_{sw} \times V_{DBOOT} = 1/2 \times 0.47\,\mu C \times 16\,kHz \times 1\,V = 3.76\,mW \quad (6)$$

2.2.1.8 Selection of Current Limiting Resistor for Bootstrap Diode

Considering that having a 1.5-$V_{(p-p)}$ ripple on the bootstrap capacitor, the charge on the 0.47-µF and 2.2-µF capacitors is:

$$Q = C \times V = (0.47\,\mu + 2.2\,\mu) \times 1.5 = 4\,\mu C \quad (7)$$

For a capacitor charging period of 5 µs, the same charge is also represented as 式 8.

$$Q = 4\,\mu C = I_{CH} \times 5\,\mu s \quad (8)$$

This gives ICH = 0.8 A.

With a voltage drop across diode being 1 V, the R_{BOOT} is calculated as:

$$R_{BOOT} = V_{DBOOT} I_{CH} = 10.8 = 1.25\ \Omega \quad (9)$$

This reference design uses a R_{BOOT} value of 1.33 Ω.

With R_{BOOT} = 1.33 Ω, the bootstrap diode current is calculated as 式 10.

$$I_{DBOOT(pk)} = (V_{DD} - V_{DBOOT}) R_{BOOT} = (16 - 1) 1.33 = 11.28\ A \quad (10)$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor.

2.2.1.9 Gate Resistors

The gate current and the appropriate power of the voltage supply depend on the operating frequency, bias control voltages, and total gate charge. The total gate charge is published in IGBT data sheets, depending on gate control voltage. The gate charge necessary for switching is very important to establish the switching performance of the IGBT. The lower the charge, the lower the gate drive current needed for a given switching time. The gate current can be controlled using an external gate resistor between driver output and gate of the IGBT. The value of the gate resistor determines the peak charge and discharge currents. The most classical way to influence the switching behavior of an IGBT is by selecting the gate resistors. The gate resistors can be different for the on and off switching process. In such cases, the turnon gate resistor is denominated with RGon and for turning off with RGoff as shown in 図 6. The effective values of gate resistors become:

- Effective RGon = R_{Gon}
- Effective RGoff = R_{Gon} // R_{Goff}

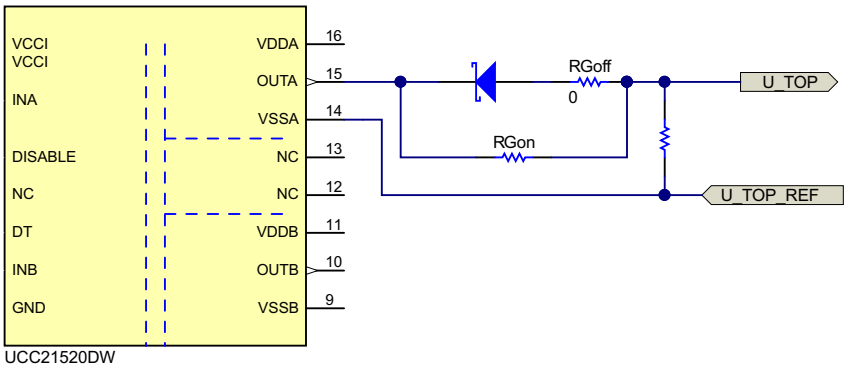


図 6. Gate Resistors

Depending on the gate resistor, both the voltage gradient (dv/dt) as well as the current gradient (di/dt) are modified. The higher the resistance of $R_{G(on)}$, the softer the switching of the IGBT (and correspondingly, the turnoff of the free-wheeling diode). As a consequence, however, the turnon losses of the IGBT increase (and the recovery losses of free-wheeling diode decrease).

For this reference design, R_{Gon} = 16.5 Ω and RGoff = 0 Ω.

With the internal gate resistance of 4 Ω, the gate currents are calculated as:

- Source current = 16 V / (16.5 + 4) Ω = 780 mA
- Sink current = 16 V / 4 Ω ≈ 4 A (considering zero on-resistance of diode)

Another important point to highlight is that 図 4 shows 10-kΩ resistors across the gate and emitter terminals of the IGBTs. These resistors are a safety precaution and are placed across these nodes to ensure that the IGBTs are not turned on if the UCC21520 device is not in place or not properly soldered on the circuit board.

2.2.1.10 Power Dissipation in Gate Driver

This section explains the calculation power dissipated in the gate driver related to this reference design. For more information on the power loss, see *UCC21520 4-A, 6-A, 5.7-kV$_{RMS}$ Isolated Dual-Channel Gate Driver* .

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{DDA} \times I_{DDA} + V_{DDB} \times I_{DDB} \quad (11)$$

Where

- V_{VCCI} and I_{VCCI} are the low-voltage sides bias voltage and quiescent current, 5 V and 2.5 mA respectively
- V_{DDA} and V_{DDB} are gate drive supply voltage for top and bottom gate drivers, which is 16 V
- I_{DDA} and I_{DDB} are the quiescent current taken from the gate drive power supply
- P_{GDQ} is calculated to be 60.5 mW

The power dissipation due to switching of the gate driver is given in 式 12:

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \quad (12)$$

Where

- V_{DD} is gate drive supply voltage of 16 V
- Q_G is the IGBT gate charge, which is 0.47 µF

- f_{SW} is the PWM switching frequency of 16 kHz

P_{GSW} is calculated to be 240.64 mW

The power dissipation in gate driver due to this switching is given in 式 13:

$$P_{GDO} = P_{GSW} \times (R_{OH} \,||\, R_{NMOS} \,||\, R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_INT} + R_{OLROL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_INT}) \quad (13)$$

Where

- R_{OH}, R_{NMOS}, and R_{OL} is from the UCC21520 data sheet; values are 5 Ω, 1.47 Ω, and 0.55 Ω, respectively
- R_{ON} is the turnon gate resistance which is 16.5 Ω
- R_{OFF} is the turnoff gate resistance which is 0 for TIDA-01540
- R_{GFET} is the IGBT internal resistance, which is 4Ω
- P_{GDO} is calculated to be 41.72 mW

The total power dissipation is $P_G = P_{GDO} + P_{GSW}$ = 102.22 mW. Considering the UCC21520 has a junction to ambient thermal resistance of $R_{\Theta JC}$ = 11.1°C/W, the temperature rise due to this is calculated as $R_{\Theta JA} \times P_G$ = 102.22 mW × 11.1°C/W = 1.13°C.

2.2.2 Connectors to Connect C2000™ Piccolo™ LaunchPad™

表 2 shows the pinout for C2000 Piccolo LaunchPad. The highlighted pins are used for connecting the reference design board.

表 2. C2000™ LaunchPad™ Pinout

SIGNAL NAME ON TIDA-01540	MUX VALUE				J1 PIN	J3 PIN	MUX VALUE				SIGNAL NAME ON TIDA-01540
	X	2	1	0			0	ALT FUNCTION	2	X	
				3.3V	1	1	5V				
				GPIO32	2	2	GND				GND
		SCIRXDB		GPIO19	3	3	ADCIN14	CMPIN4P			1V65_REF
		SCITXDB		GPIO18	4	4	ADCINC3	CMPIN6N			I_U/ V_DC
				GPIO67	5	5	ADCINB3	CMPIN3N			I_U
				GPIO111	6	6	ADCINA3	CMPIN1N			3V3_REF
	SPICLKA			GPIO60	7	7	ADCINC2	CMPIN6P			I_V
				GPIO22	8	8	ADCINB2	CMPIN3P			I_W
			SCLA	GPIO105	9	9	ADCINA2	CMPIN1P			V_DC
			SDAA	GPIO104	10	10	ADCINA0	DACOUTA			MODULE_TEMP
SIGNAL NAME ON TIDA-01540	**MUX VALUE**				**J4 PIN**	**J2 PIN**	**MUX VALUE**				**SIGNAL NAME ON TIDA-01540**
	X	**2**	**1**	**0**			**0**	**1**	**2**	**X**	
PWM_U_TOP			EPWM1A	GPIO0	1	1	GND				GND
PWM_U_BOT			EPWM1B	GPIO1	2	2	GPIO61				
PWM_V_TOP			EPWM2A	GPIO2	3	3	GPIO123			D1_C1	DISABLE
PWM_V_BOT			EPWM2B	GPIO3	4	4	GPIO122			D1_D1	
PWM_W_TOP			EPWM3A	GPIO4	5	5	RST				
PWM_W_BOT			EPWM3B	GPIO5	6	6	GPIO58			SPISIMOA	TRIP
			OUTPUTXBAR1	GPIO24	7	7	GPIO59			SPISOMIA	
	OUTPUTXBAR7			GPIO16	8	8	GPIO124			SD1_D2	

表 2. C2000™ LaunchPad™ Pinout (continued)

SIGNAL NAME ON TIDA-01540	MUX VALUE				J1 PIN	J3 PIN	MUX VALUE				SIGNAL NAME ON TIDA-01540
	X	2	1	0			0	ALT FUNCTION	2	X	
				DAC1/ GPIO20	9	9	GPIO125			SD1_C2	
				DAC2/ GPIO21	10	10	GPIO29			OUTPUTXB AR6	

On reference design board, two 20-pin connectors are used to connect with the C2000 LaunchPad as shown in 図 7. The PWM signals for inverter are generated using the LAUNCHXL-F28027 board. The PWM signals generated from the MCU are filtered using an RC filter with values of R = 10 Ω and C = 10 pF. This filter corresponds to a cutoff frequency of 159 MHz and an RC time delay of 1 ns. GND_FAULT and OVERLOAD signals are generated from the respective comparators connected to the MCU on GPIOs and also connected to a three-input NAND gate as explained in 2.2.1.3 to generate the DISABLE signal for gate drivers. The TRIP signal is generated from the MCU in case the user wants to interrupt the PWM signals or if the GND_FAULT and OVERLOAD signals need to be latched.

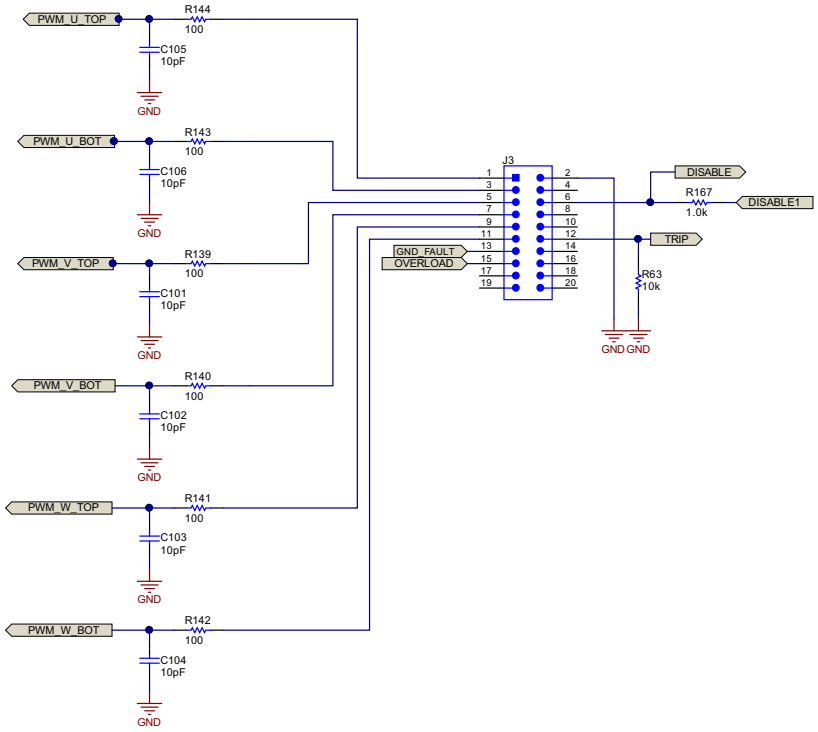


図 7. 20-Pin Connector to Connect With Connectors J1 and J3 on LAUNCHXL-F28379D

The 3.3-V supply generated using the TLV1117 is provided as a supply to the LaunchPad as shown in 図 8. The supply can also power the MCU from an external 5 V by populating onboard components R7, C10, and C11. The sensed signals I_U, I_V, I_W, V_DC, and MODULE_TEMP are connected to ADC input pins after the RC filtering (for aliasing). 1V65_REF and 3V3_REF are also provided to ADCs for any ratiometric measurements.

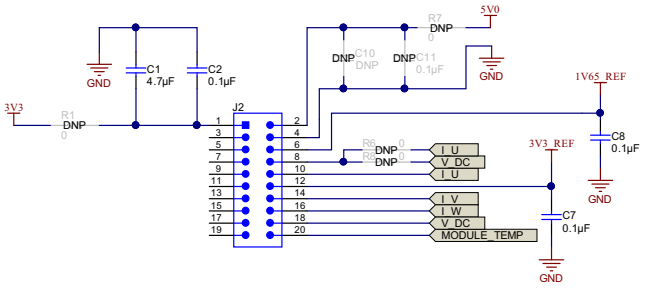


図 8. 20-Pin Connector to Connect With Connectors J4 and J2 on LAUNCHXL-F28379D

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

This section explains the top and bottom views of the PCB for this reference design. This section also explains the power supply requirement and connectors used to connect the external world.

3.1.1 TIDA-01541 PCB Overview

図 9 shows the top view of the PCB. The three phases (U, V, and W) have current sensing circuit and dual channel gate drivers as highlighted in the figure.

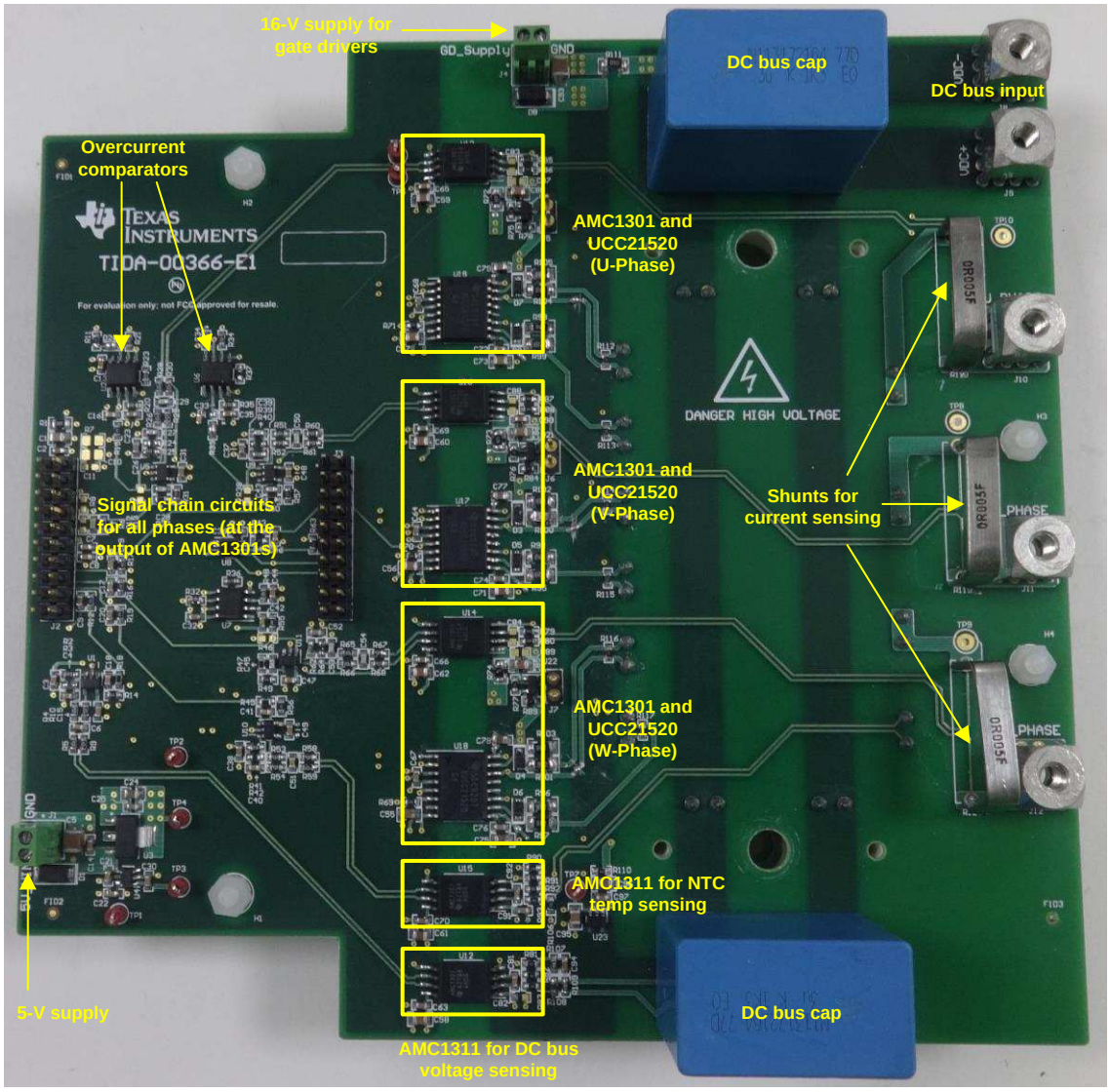


図 9. Top View of PCB for TIDA-01540

図 10 shows the bottom view of the PCB. The IGBT module is mounted on the bottom layer so that the heat sink can be connected to it as required by the output power levels.

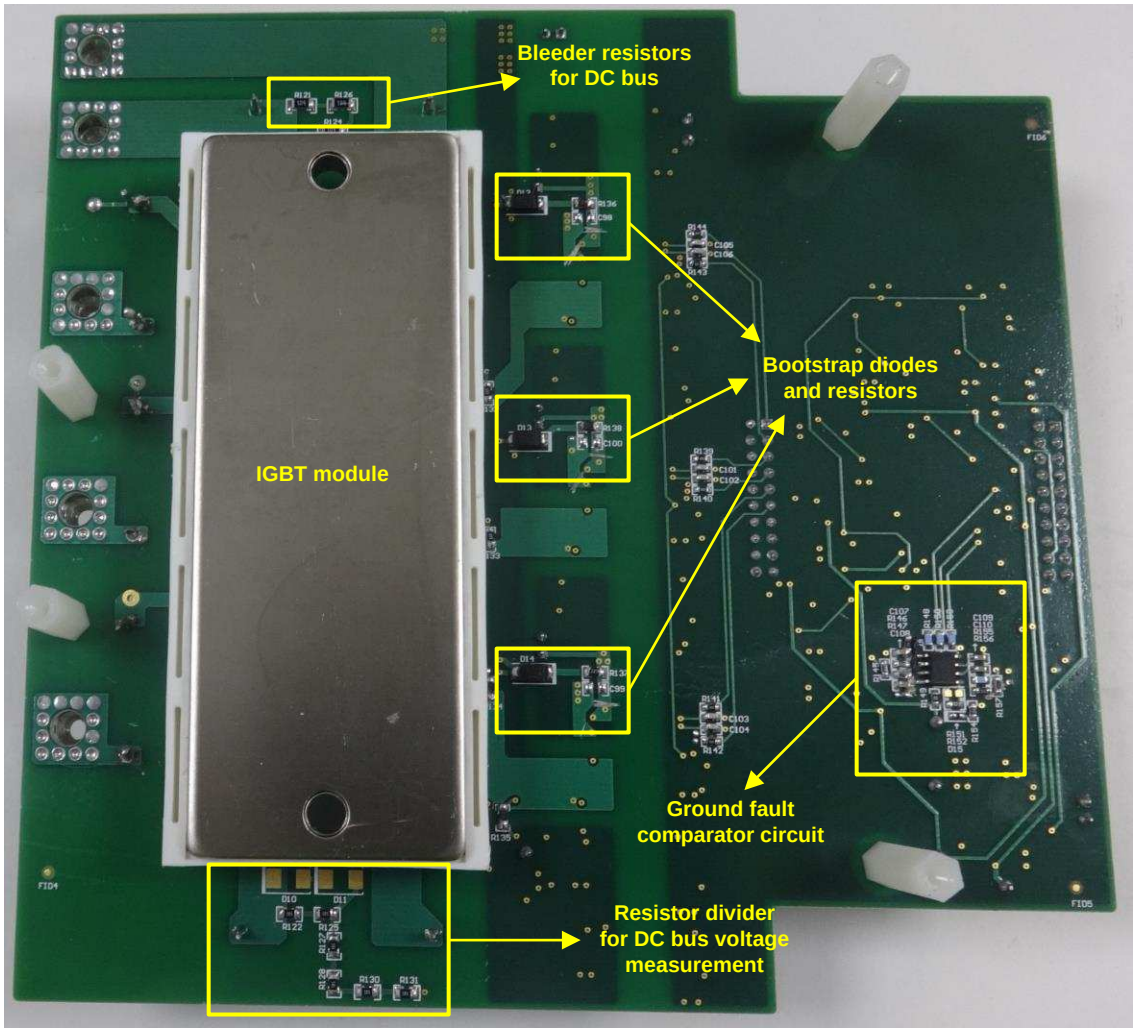


図 10. Bottom View of PCB for TIDA-01540

3.1.2 Connector

表 3 shows the connectors used on the reference design PCB and their purposes.

表 3. Connectors

CONNECTOR	PURPOSE
J1	5V_VIN power supply to power MCU, op amps, low-side of AMC1301, low-side of AMC1311, and comparators
J2	To connect to J1–J5 of LAUNCHXL-F28379D
J3	To connect to J6–J2 of LAUNCHXL-F28379D
J4	16-V GD_Supply to power low-side gate drivers
J5	To supply external isolated 16 V for U-Phase low-side gate driver if bootstrap configuration is not used
J6	To supply external isolated 16 V for V-Phase low-side gate driver if bootstrap configuration is not used
J7	To supply external isolated 16 V for W-Phase low-side gate driver if bootstrap configuration is not used
J13	VDC input
J14	Output for connecting to motor

3.2 Testing and Results

3.2.1 Test Setup

The following subsections provide descriptions and pictures of the test setup. 表 4 lists the key test equipment used in the subsequent tests.

表 4. Key Test Equipment

DESCRIPTION	TEST EQUIPMENT PART NUMBER
C2000 F28379D LaunchPad	Texas Instruments LAUNCHXL-F28379D
Adjustable power supply	Keithley 2230G-30-1 (two power supplies are used to ensure isolation between 16-V and 5-V rails)
High-voltage power supply	Keysight N5751A (300 V and 2.5 A)
Load motor	ACIM, three-phase AC, 415 V (L-N, delta connected), 8.4 A_{RMS} (max) , 3.7-kW rated, 50 Hz, 1460 RPM
Oscilloscope	Tektronix MSO2024B
Oscilloscope	Tektronix MDO3024
High-voltage differential probes	Tektronix THDP0200
Low-voltage probes	Tektronix TPP0200

図 11 shows the test setup used. The board is powered from three power supplies: 0 V to 1000 V for the DC-Link, 16 V for the power supply of the gate drive, and 5 V for the low-voltage side bias. The C2000 LaunchPad is powered from 3.3-V power supply. The 1000-V power supply and the power supply of the gate drive are isolated from each other and also isolated from the 3.3-V and 5-V power supply.

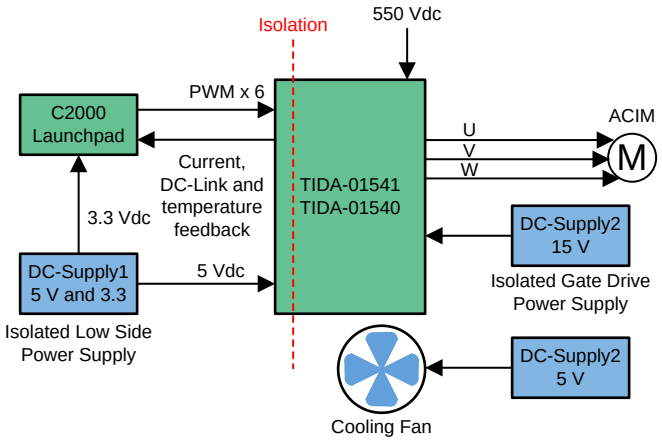


図 11. TIDA-01540 Test Setup

3.2.2 Test Results

This section shows the test results relating to the DC-Link accuracy, current and voltage sensing histogram, step response of the AMC1301, and short-circuit response time.

3.2.2.1 Thermal Image

図 12 is the thermal image of the board. For this test, the board is supplied with 3.3 V to the LaunchPad and the 5-V power rail of this reference design, and the gate drive power supply is 16 V. However, the DC-Link turned off. All three half bridges of the inverter are driven with a complementary PWM of 50%. This PWM is required to generate the bootstrap power supply, which supplies the UCC2150 on the high-voltage side. Because the DC-Link is turned off, the thermal image captures temperatures due to the self-heating of the UCC21520 and not the power dissipation of the IGBT module. The temperature of the UCC21520 is 27.6°C, which is a temperature rise of 4.8°C from the ambient temperature of 22.8°C.

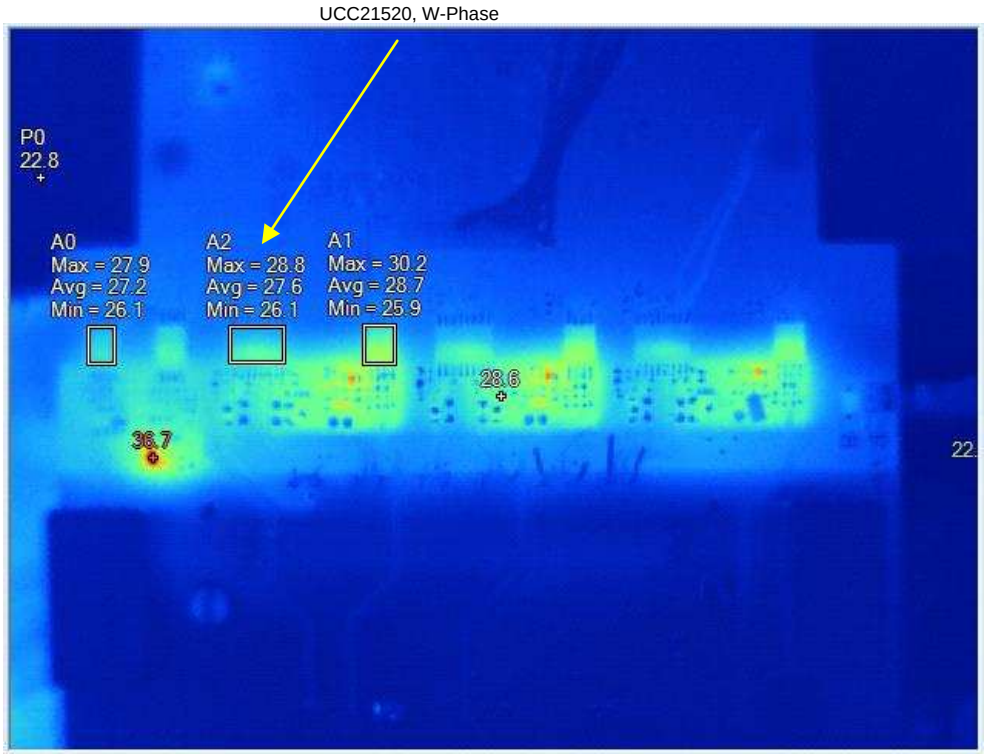


図 12. UCC21520 Surface Temperature

3.2.2.1.1 Propagation Delay of UCC21520

The propagation delay for the gate driver is obtained with the DC-Link disconnected. The half bridge of the inverter is driven with a complementary PWM of 50%. The motor is disconnected in this test. 図 13 is an oscilloscope capture of the input PWM signal and output gate drive of the UCC21520. 図 14 and 図 15 are the propagation delays for the rising and falling edge for the gate signal of the top IGBT in the half bridge. Similarly, 図 16 and 図 17 are the propagation delays for the rising and falling edge for the gate signal of the bottom IGBT in the half bridge.

表 5. Propagation Delay Measurement for UCC21520

PARAMETER	PROPAGATION DELAY (ns)
Top IGBT gate driver rising edge propagation delay	30.44
Top IGBT gate driver rising edge propagation delay	29.64
Top IGBT gate driver rising edge propagation delay	20.84
Top IGBT gate driver rising edge propagation delay	24.84

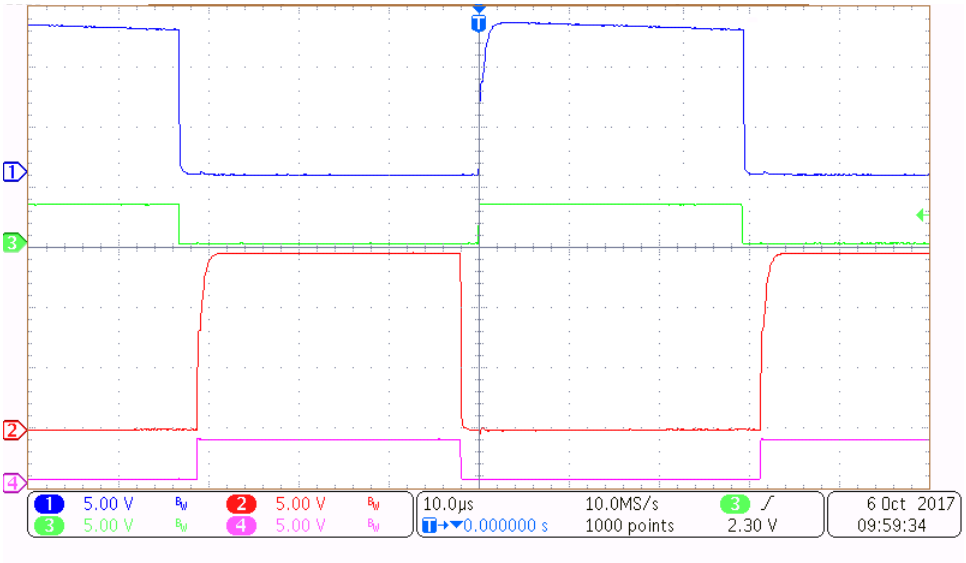


図 13. UCC21520 Half-Bridge Input and Output PWMs

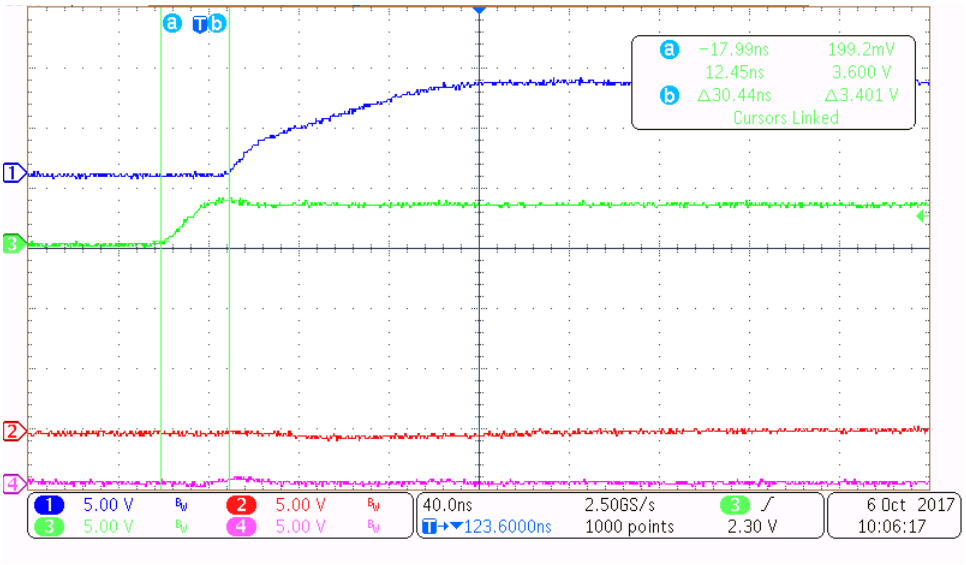


図 14. Top IGBT Gate Driver Rising Edge Propagation Delay

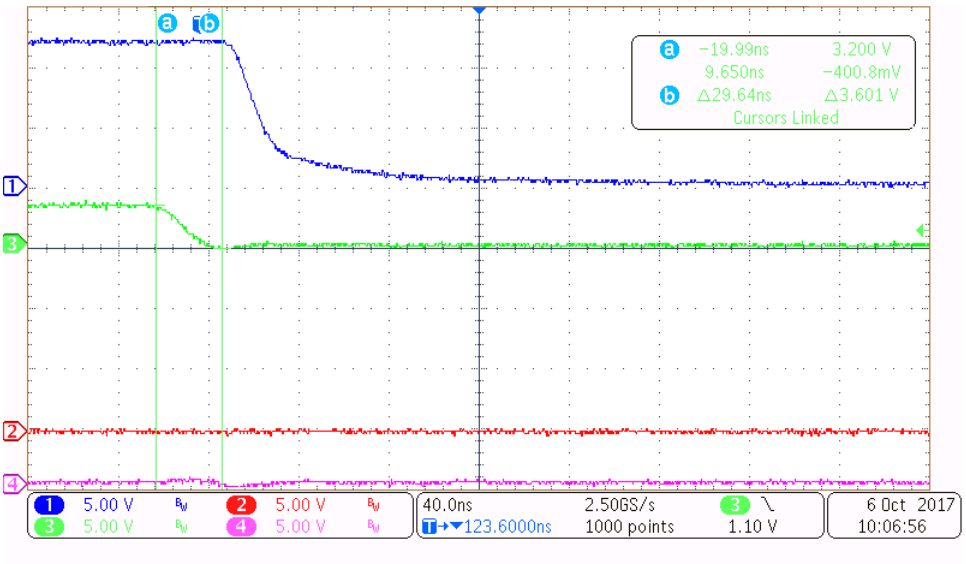


図 15. Top IGBT Gate Driver Falling Edge Propagation Delay

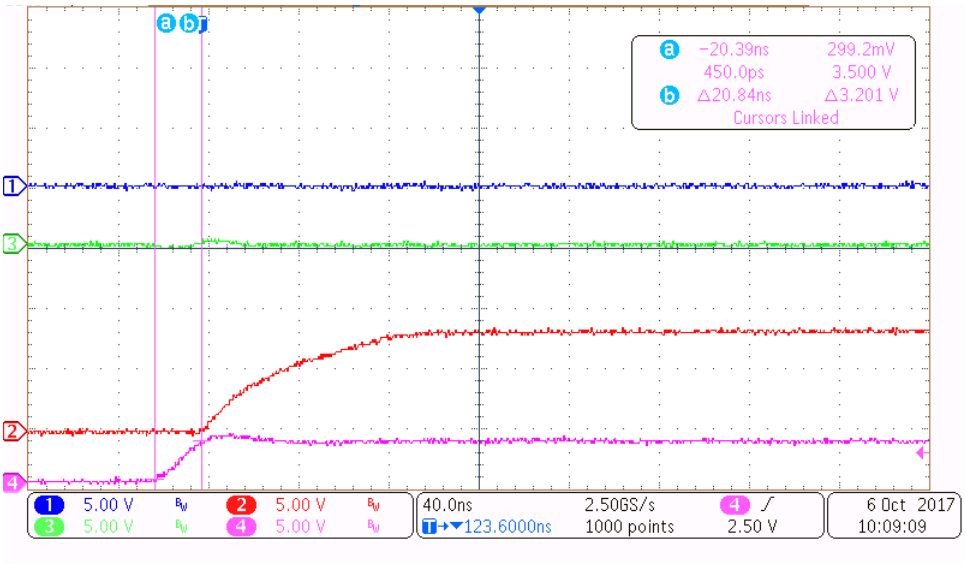


図 16. Bottom IGBT Gate Driver Rising Edge Propagation Delay

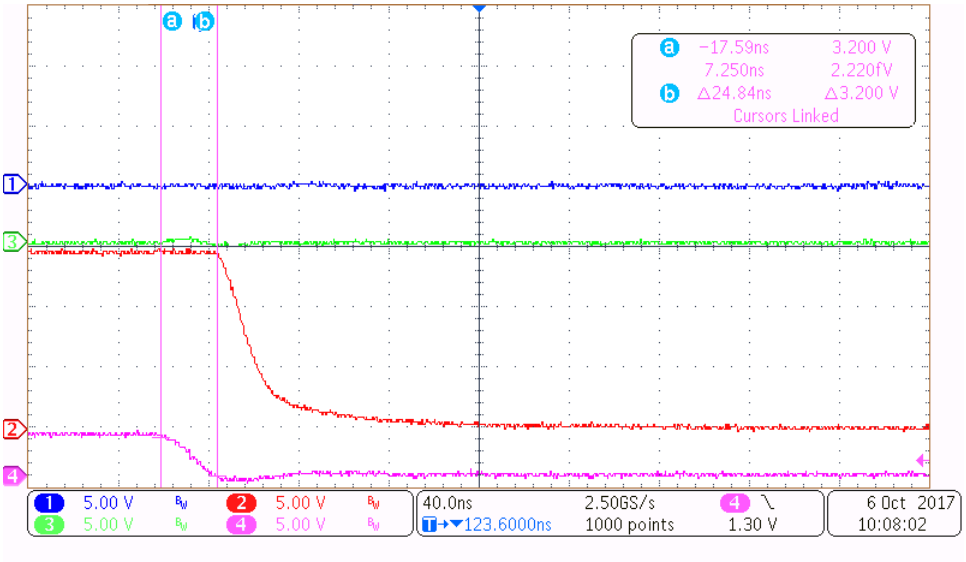


図 17. Bottom IGBT Gate Driver Falling Edge Propagation Delay

The consequence of the propagation delay for a three-phase inverter is that the dead time between the top and bottom IGBT must be increased to accommodate the propagation delay time. The IGBT module on this reference design uses a dead time of 1.3 µs. The dead time must be adjusted by 60 ns (30 ns each for the top and bottom IGBT gate driver). The effect of the dead time is to increase the distortion on the current waveform. To demonstrate the effect of the dead band, an ACIM motor is connected and the inverter run in open loop at 10 Hz, The DC-Link is supplied with 600 V and a three-phase current of 1.5 A_{RMS} is injected into the motor.

図 18 shows one motor line current waveform with the dead time set to 1.3 µs. 図 19 shows is for a dead time of 1.8 µs, which would be the dead time if using an optocoupler-based gate driver with a propagation delay of 250 ns. Notice the waveform becomes more non-sinusoidal as the dead time increases.

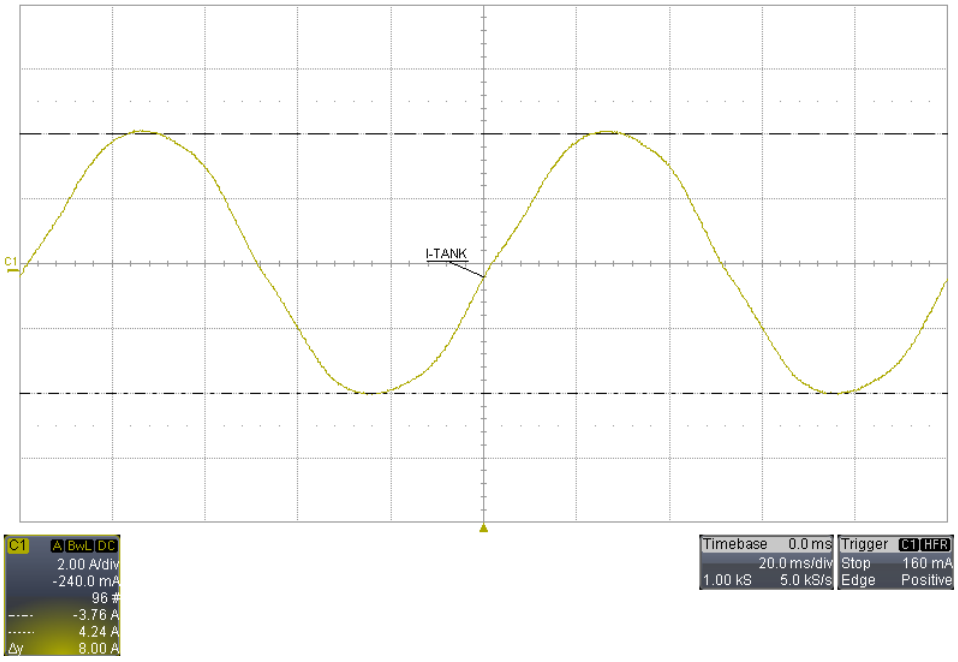


図 18. Open-Loop Current Waveform With 1.3 µs

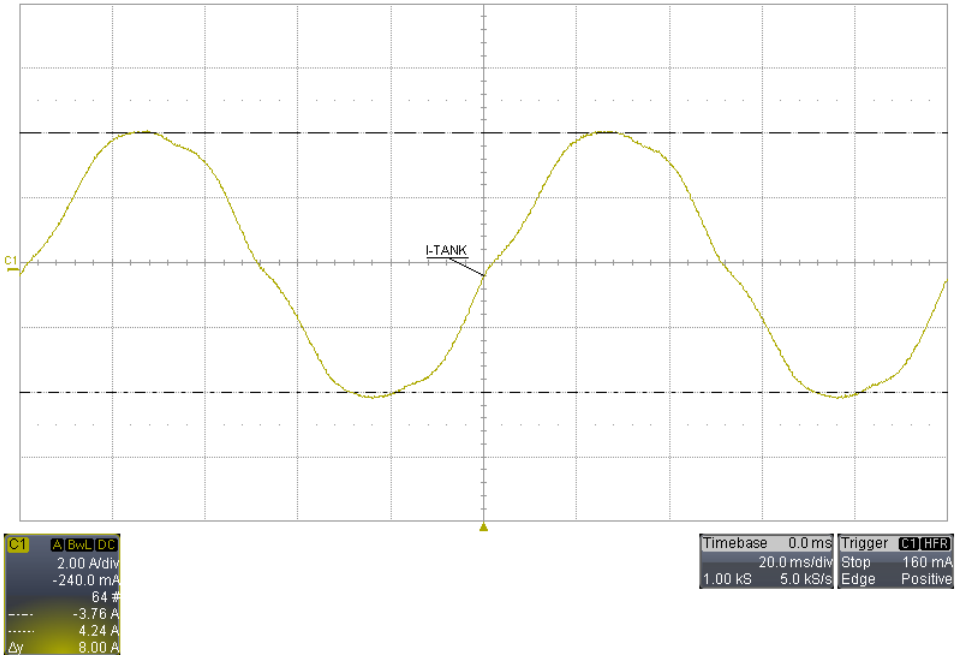


図 19. Open-Loop Current Waveform With 1.8 µs

3.2.2.1.2 Deadband Insertion and Interlock

The deadband and interlock feature of the UCC21520 are tested by driving the inverter with a complementary PWM of 50%; however, the PWM inputs to the UCC21520 are made to overlap by 2 µs. 図 20 is the oscilloscope capture of the input PWM signal and output gate drive signals of the UCC21520. 図 21 and 図 22 are the zoomed-in waveforms for the switch node turnon and at switch node turnoff. Notice when the input PWMs overlap the interlock is active, hence both IGBTs are kept off. In an off state period, the interlock is active. After the end of the overlap, a time period of 1.3 µs elapses before the IGBT is turned on. This period corresponds to the deadband insertion of 1.3 µs.

This test simulates an overlap to check the interlock and dead time insertion; however, the overlap could be due to an software fault, damage to the gate drive signal connectors, or an EFT condition picked up on the input PWM signal. Without the interlock feature, this overlap would have caused the top and bottom IGBTs of the gate driver to turn on and cause a shoot-through condition that would damage the inverter.

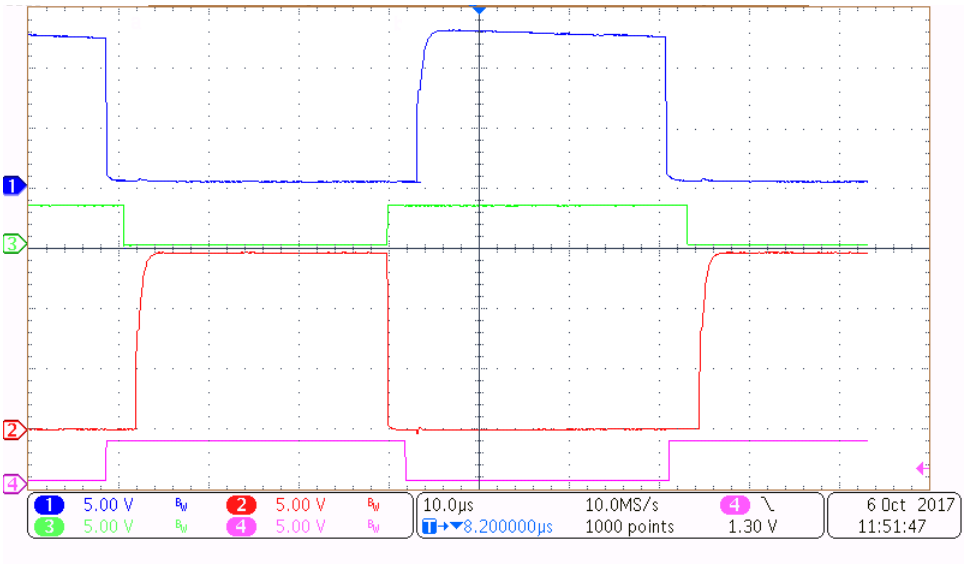


図 20. Dead Time Insertion for Overlapping PWMs

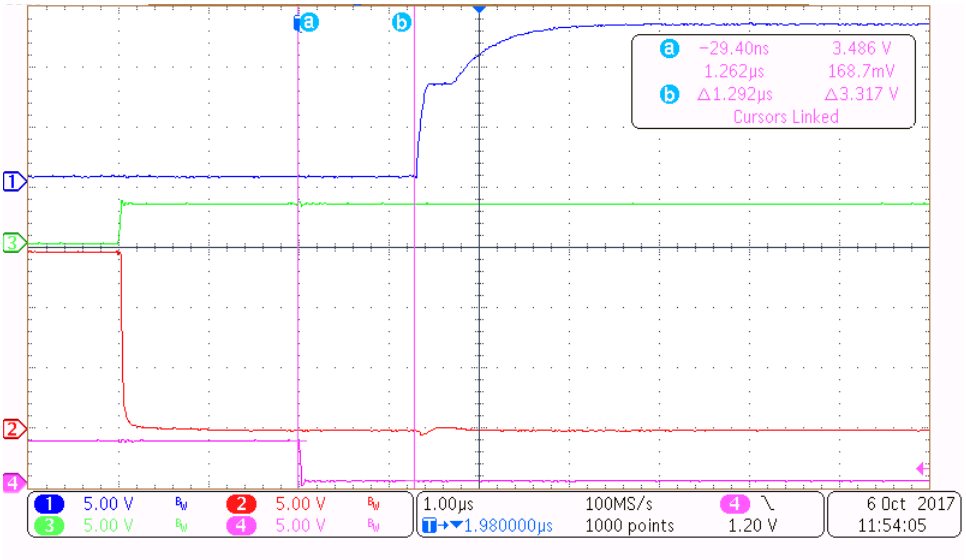


図 21. Dead Time Insertion for Overlapping PWMs for Switch Node Turnon

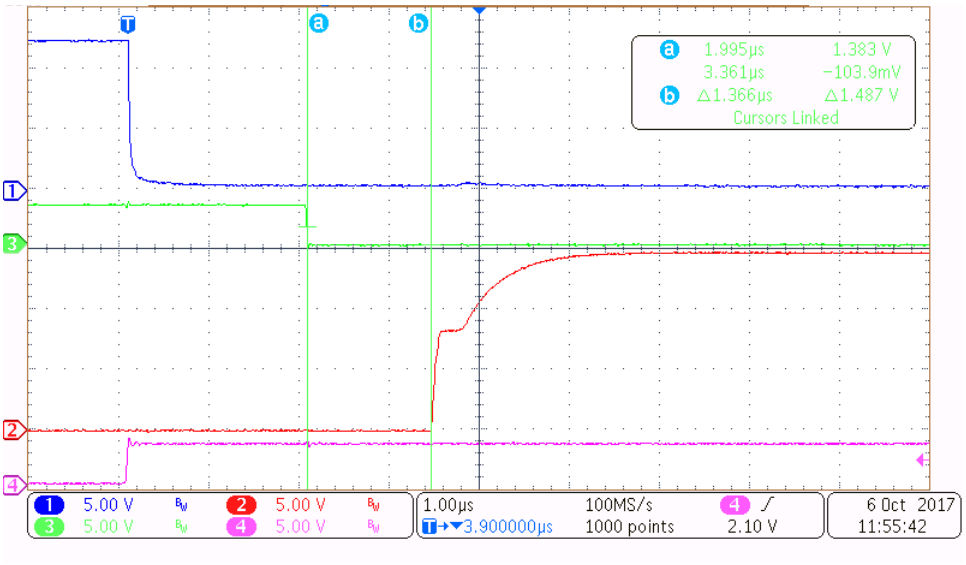


図 22. Dead Time Insertion for Overlapping PWMs for Switch Node Turnoff

3.2.2.1.3 Bootstrap Power Supply Ripple

図 23 and 図 24 show the voltage rail and ripple for the bootstrap supply for the high-side gate driver, respectively. The PWM frequency is 4 kHz for this test. The top IGBT is turned on for 90% of the time and the bottom IGBT is turned on for the remaining 10%. The motor is disconnected in this test. 図 23 shows the bootstrap supply voltage and the ripple when the DC-Link power supply is disconnected. 図 24 shows the bootstrap supply voltage and the ripple when the DC-Link is powered with 600-V DC.

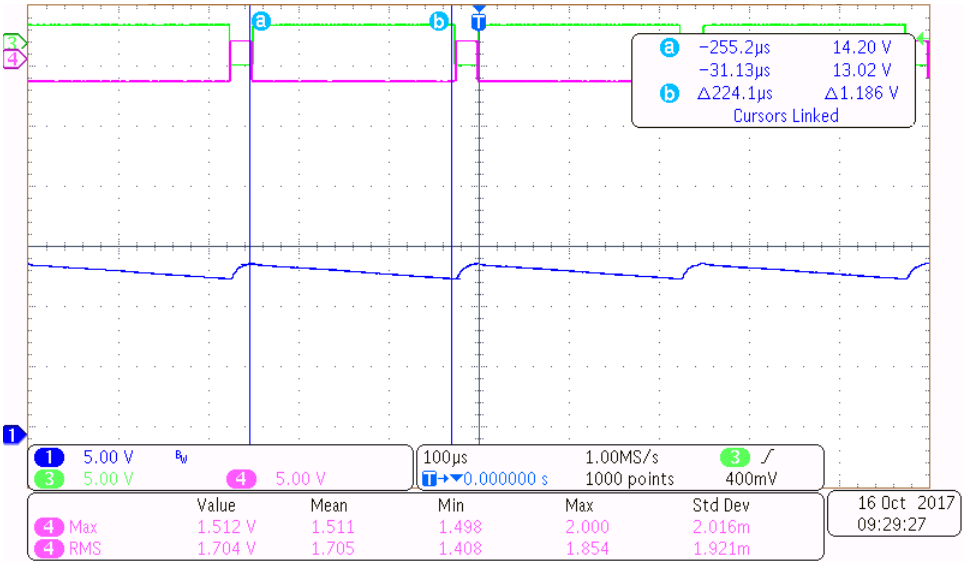


図 23. Bootstrap Power Supply Voltage and Ripple With DC-Link at 0 V

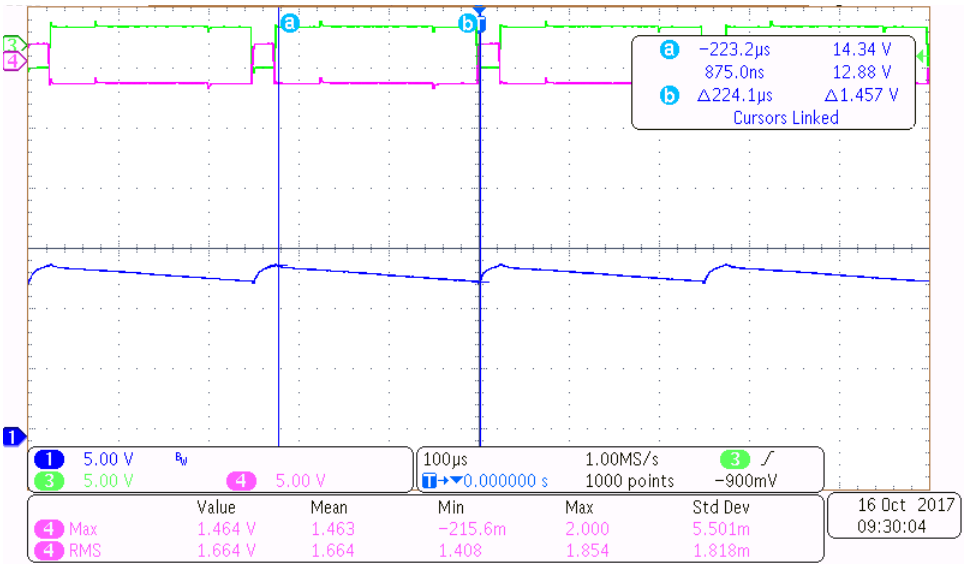


図 24. Bootstrap Power Supply Voltage and Ripple With DC-Link at 600 V

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01540.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files atTIDA-01540.

4.3 PCB Layout Recommendations

The hardware for this reference design is based on the TIDA-00366 design. For PCB layout recommendations, refer to *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection* .

4.3.1 Layout Prints

To download the layer plots, see the design files atTIDA-01540.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01540.

4.5 Gerber Files

To download the Gerber files, see the design files atTIDA-01540.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01540.

5 Related Documentation

1. Texas Instruments, *LAUNCHXL-F28379D Overview User's Guide*
2. Texas Instruments, *TIDA-01541 High-Bandwidth Phase Current and DC-Link Voltage Sensing Reference Design for Three-Phase Inverters*

5.1 商標

6 Terminology

PWM— Pulse width modulation

MCU— Microcontroller unit

IGBT— Insulated bipolar gate transistor

RPM— Rotation per minute

RMS— Root mean square

NTC— Negative temperature coefficient thermistor

7 About the Authors

NELSON ALEXANDER is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Nelson has been with TI since 2011, has been involved in designing embedded systems, and has experiences in microcontrollers, isolation, analog signal chains, and IGBT gate drivers. Nelson earned his bachelor of engineering in electrical and electronics engineering at MSRIT, Bangalore.

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TIの設計情報およびリソースに関する重要な注意事項

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