参考資料

TI Designs: TIDA-01323
クワッド4Gbps FPD-Link III、デュアルCSI-2出力、PoC対応 ADASマルチセンサ・ハブのリファレンス・デザイン

概要

このカメラ・ハブのリファレンス・デザインでは、最大4台の2メガピクセル/60fpsカメラを同軸ケーブルで接続できます。この同軸ケーブルを用いて、センサへの電力供給やバックチャネル通信、クロック同期を実行します。4Gbps FPD-Link IIIクワッド・デシリアライザは、Samtecコネクタを介したアプリケーション・プロセッサへのデュアル出力MIPI (Mobile Industry Processor Interface) CSI-2 (Camera Serial Interface-2)をサポートしています。またセンサ・フュージョン・アプリケーションでは、他種センサを接続することもできます。

リソース

TIDA-01323		デザイン・フォルダ
DS90UB960-Q1	LM74700-Q1	プロダクト・フォルダ
TPS55340-Q1	TPS62162-Q1	プロダクト・フォルダ
TPS62160-Q1	TPS4H160-Q1	プロダクト・フォルダ
SN74LVC1G125-Q1	TS3USB221A-Q1	プロダクト・フォルダ
MSP430F2272		プロダクト・フォルダ

TI E2E™ Community

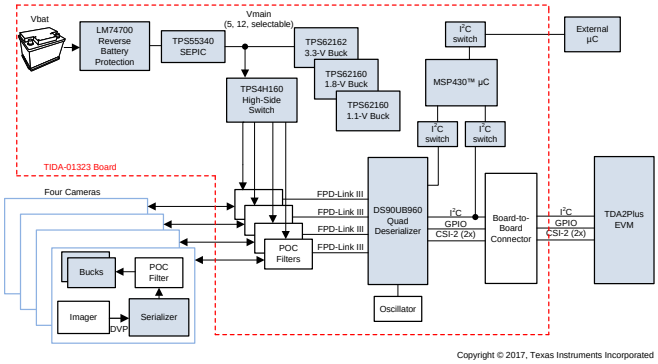
E2Eエキスパートに質問

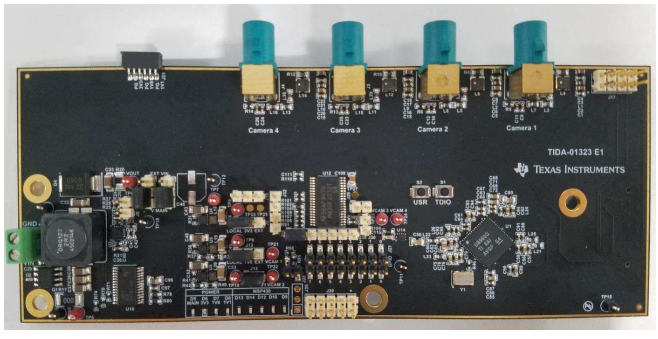
特長

- FPD-Link III経由で4台のカメラからの入力を受け入れ、センサ同期をサポート
- 同軸ケーブルを使用した電力供給(Power Over Coax)に適した広い電源電圧範囲(4V～14V)に対応
- CSI-2インターフェイスを介してTDA3およびTDA2Plus EVMに直接接続
- 逆電流保護機能を備えており、自動車のバッテリからボードへの直接的な電力供給が可能
- MSP430™マイクロコントローラ(MCU)を使用してビデオ・パイプラインを初期化および構成
- オンボードMCU、MCUなし、または外付けMCUに対応
- 対応するFPD-Link III DS90UB953シリアライザを使用するカメラとの組み合わせが可能

アプリケーション

- ADASシステム
- サラウンド・ビュー
- CMSおよびミラー代用
- リア・カメラ





1 System Overview

1.1 System Description

Many automotive advanced driver assistance systems (ADAS) require multiple cameras. This reference design addresses these requirements by combining the outputs from four 2-megapixel imagers into two MIPI CSI-2 video ports. These video ports are available on an external connector that can attach to a TDA3 or TDA2Plus EVM and other similar processors.

1.2 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Supply voltage	4 V < 12 V (typ) > 17 V	From external supply
Total power consumption without cameras	1.7 W (typ), > 2 W	At 12 V
Total power consumption with four TIDA-01130 cameras	5.5 W (typ), > 6 W	At 12 V

1.3 Block Diagram

The block diagram in 図 1 highlights the parts of a surround view system in red that are included in the TIDA-01323 design. For the applications processor and output-to-video display, the design utilizes the Samtec connector to interface with the TDA processor EVMs to provide complete functionality of the ADAS surround-view system.

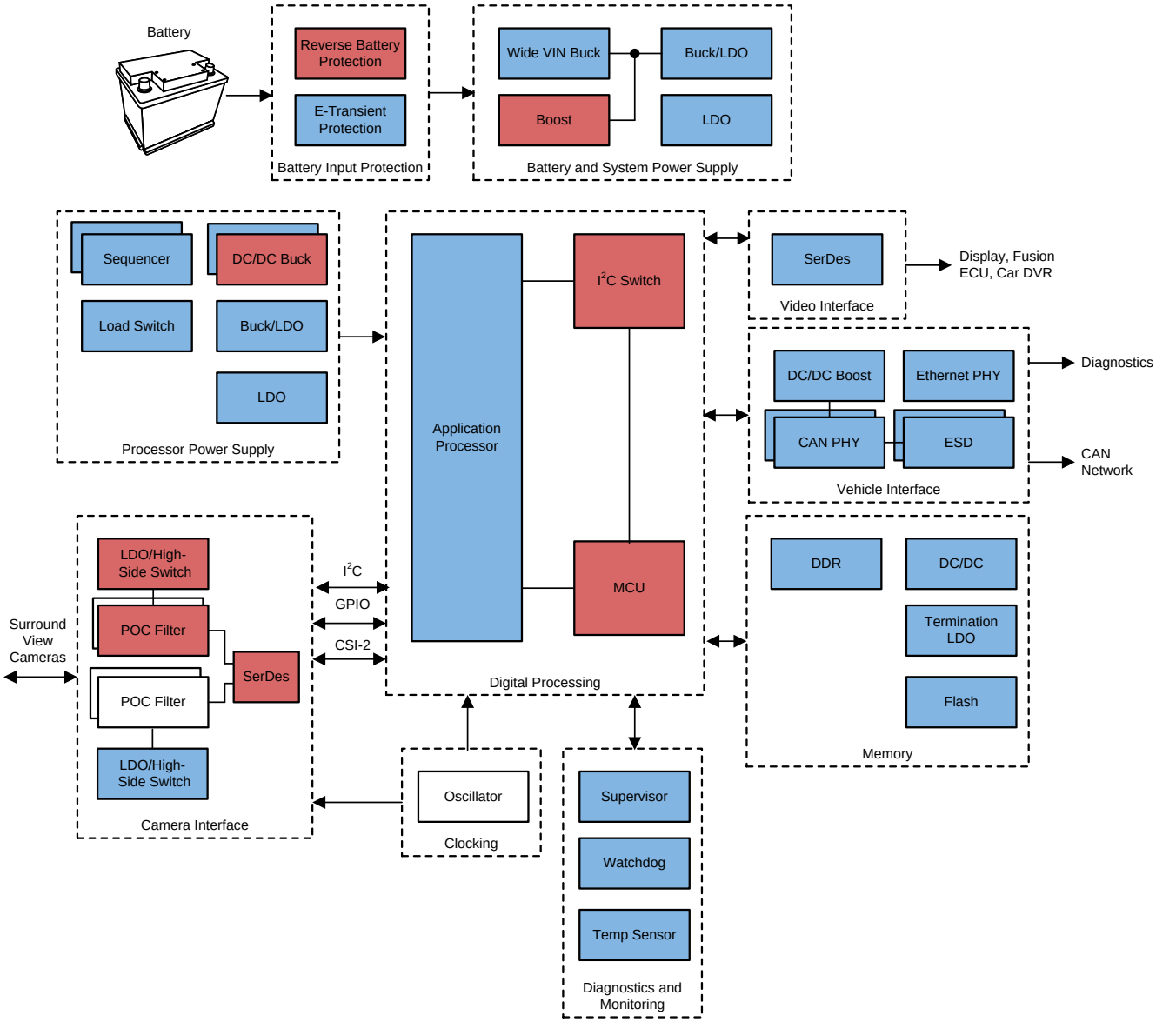


図 1. TIDA-01323 Block Diagram and System Partition

1.4 Highlighted Products

1.4.1 DS90UB960-Q1

The DS90UB960-Q1 is a quad-channel deserializer which offers an FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).

1.4.2 LM74700-Q1

The LM74700-Q1 is a smart diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss reverse polarity protection. The wide-supply input range of 3 V to 65 V allows control of many popular DC bus voltages. The device can withstand and protect loads from negative supply voltages down to –65 V.

1.4.3 TPS55340-Q1

The TPS55340-Q1 is a monolithic non-synchronous switching converter with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies including boost, single-ended primary-inductor converter (SEPIC), and isolated flyback. The device has a wide input voltage range to support applications with input voltage from 2.9 V to 38 V.

1.4.4 TPS62162-Q1 and TPS62160-Q1

The TPS62162-Q1 is a fixed voltage and the TPS62160-Q1 is an adjustable-voltage, synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response.

1.4.5 TPS4H160-Q1

The TPS4H160-Q1 device is a quad-channel, smart high-side switch with four integrated 160-mΩ NMOS power field-effect transistors (FETs). This device has full diagnostic and high-accuracy current sense capability. In addition with an external adjustable current limit, this switch improves the reliability of the entire system by protecting from inrush and overload current conditions.

1.4.6 SN74LVC1G125-Q1

The SN74LVC1G125-Q1 is an automotive-qualified version of a single-bus buffer gate with a three-state output.

1.4.7 TS3USB221A-Q1

The TS3USB221A-Q1 is a high-bandwidth switch which is specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB input and output (I/O) connections.

1.4.8 MSP430F2272-Q1

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers (MCUs) consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 1 µs.

1.4.9 TIDA-01130

This reference design frequently makes references to the TIDA-01130 TI Design, which is an automotive 2-megapixel camera module built around a DS90UB953 serializer and an OmniVision OV2775 imager. For more details, see *Automotive 2-MP Camera Module Design with MIPI CSI-2 Video Output Interface and Power Over Coax*.

1.5 Design Considerations

1.5.1 DS90UB960-Q1

Using a serializer and deserializer to combine video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements.

The DS90UB960-Q1 four-channel deserializer takes this simplification one step further. Each camera in the system is connected to the deserializer through a single coax cable. Using power-over-coax (PoC) filters, the power for each camera is also included on the single coax connection. By using these filters, the designer can transmit video, I^2C control, diagnostics, and power up to 15 m on a single inexpensive coax cable. For more information on the cable itself, see *Cable Requirements for the DS90UB913 & DS90UB914A*.

In this design, the DS90UB960-Q1 device pairs with a DS90UB953-Q1 device that is on a separate camera board (TIDA-01130). The DS90UB953-Q1 FPD-Link III 4.16-Gbit/s serializer is intended to link with megapixel image sensors. The serializer transforms CSI-2 MIPI data along with a bidirectional control bus (I^2C port) into a single, high-speed differential pair. The DS90UB953-Q1 can accept up to four lanes of CSI-2 data at 832 Mbps/lane. The integrated, bidirectional control channel transfers data over the same differential pair; therefore, it eliminates the requirement for additional wires to program the registers of the image sensors. In addition, the serializer provides up to four general purpose input and output (GPIO) pins, which can act as outputs for the signals that are fed into the deserializer GPIO pins that are triggering the image sensors logic. For example, the designer can configure the deserializer and serializer in such a way so that one GPIO pin on the deserializer side causes one GPIO pin on the serializer side to toggle. In other words, the output pins of the serializer reflect the assigned input pins from the deserializer.

1.5.2 LM74700-Q1

For this design, the LM74700 device controls the N-Channel MOSFET to enable the 12-V bus voltage for the system input supply. The external MOSFET controlled by the LM74700 must be able to withstand currents up to 1 A, though nominally up to 0.5 A. Utilizing a transient voltage suppression (TVS) diode on the input anode side of the LM74700 also allows for noise suppression to transient conditions on the battery input supply.

1.5.3 TPS55340-Q1

For this design, the supply for the cameras must be configurable from 5 V to 12 V. Some of this range is above and below the input battery supply—use a single-ended primary inductance converter (SEPIC) as an effective means to solve this problem. By using a simple jumper setting, the user can choose one of the two most common camera power supplies: 5 V and 12 V. To select other voltages, the user can modify the feedback resistor network.

1.5.4 TPS62162-Q1 and TPS62160-Q1

To generate the low-voltage rails for this design, one of the TPS62162-Q1 step-down switching power supplies are tied to the main 5-V or 12-V rail to generate a 3.3-V output rail. Two TPS62160-Q1 regulators are used for the 1.8-V and 1.1-V output system rails. With a maximum input voltage of 17 V, this specification provides a lot of flexibility for the designer when choosing the main rail. This flexibility allows the designer to set the main rail to directly output to cameras, directly supply a controller area network (CAN) physical layer (PHY), or optimize efficiency in the system.

Camera sensor circuits are typically sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This specification means that a TPS6217x-Q1 switching regulator operating up to 2.5 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

1.5.5 TPS4H160-Q1

Limiting the current available to the cameras is a wise choice for many applications. In this design, the TPS4H160-Q1 switch limits the current available to the four cameras. Control of this switch from the MCU also allows the designer to decide when the power is to supply each camera and provides the flexibility for the host system to cycle the power to the cameras if this feature is ever required during start-up, diagnostics, or in response to a detected fault.

1.5.6 SN74LVC1G125-Q1

This one-bit buffer has been used in this design to allow the user to quickly determine if the power rails are present and functioning normally. Each of the buffers is connected directly to the power good output of the TLV62160-Q1 power supplies. The output is connected to a light-emitting diode (LED). This circuitry is likely to be removed from a production system.

1.5.7 TS3USB221A-Q1

This design utilizes these high-bandwidth USB switches to dynamically configure the I^2C bus on the board. These parts are much faster than what is required but they work well and are very simple to implement. For more information on the configuration of the I^2C bus, see the following 1.5.8, which addresses the MCU.

1.5.8 MSP430F2272-Q1

This version of MSP430 is used in this design as a housekeeping and configuration MCU, which allows the main SoC in the system to boot in parallel with the configuration of the SER/DES links and camera imagers. For more information on this topic, see 4.1.

2 System Design Theory

2.1 PCB and Form Factor

This design is primarily specified for use in connection with the TDA2Plus EVM. The printed-circuit board (PCB) has been designed to mate to the CSI-2 connector on the outer edge of the TDA2Plus EVM (see 図 2 and 図 3). If desired, reduce the size of the design by removing the GPIO jumpers and power-supply selection jumpers. Furthermore, use of the MCU is unnecessary if the host processor completely handles the setup of the system configuration over I^2C. LEDs are a luxury during system and software debug, but they are not required in a production design, either.

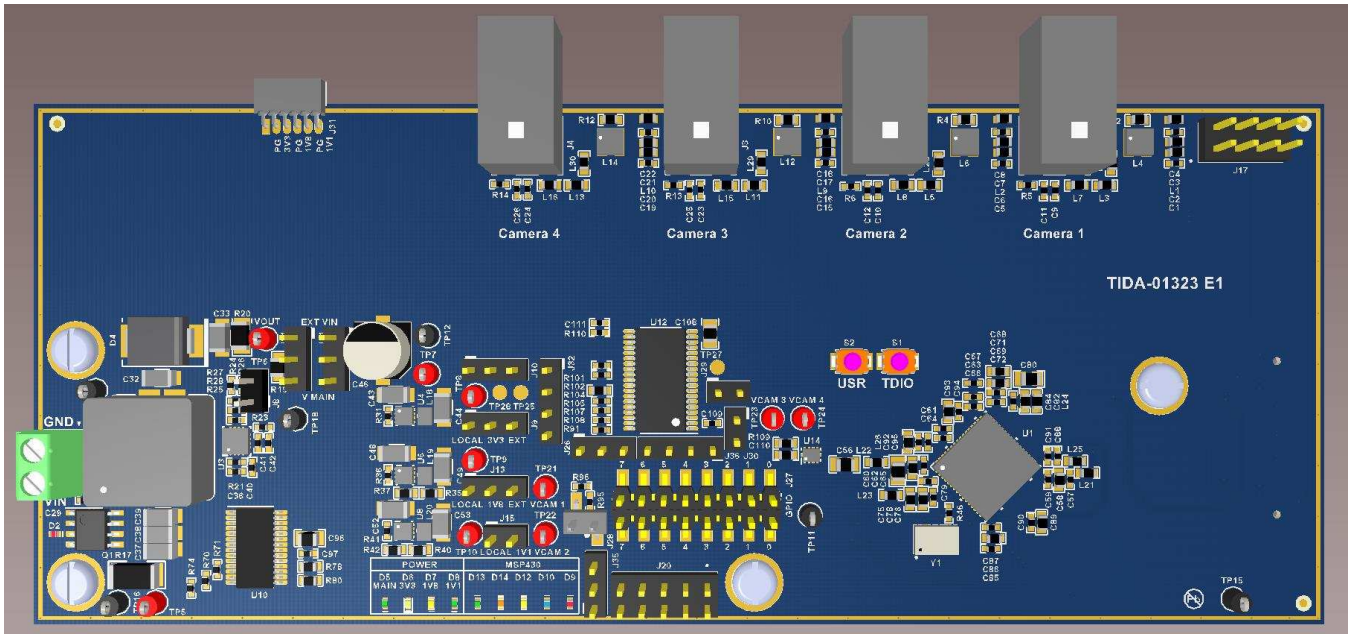


図 2. Board—Top View

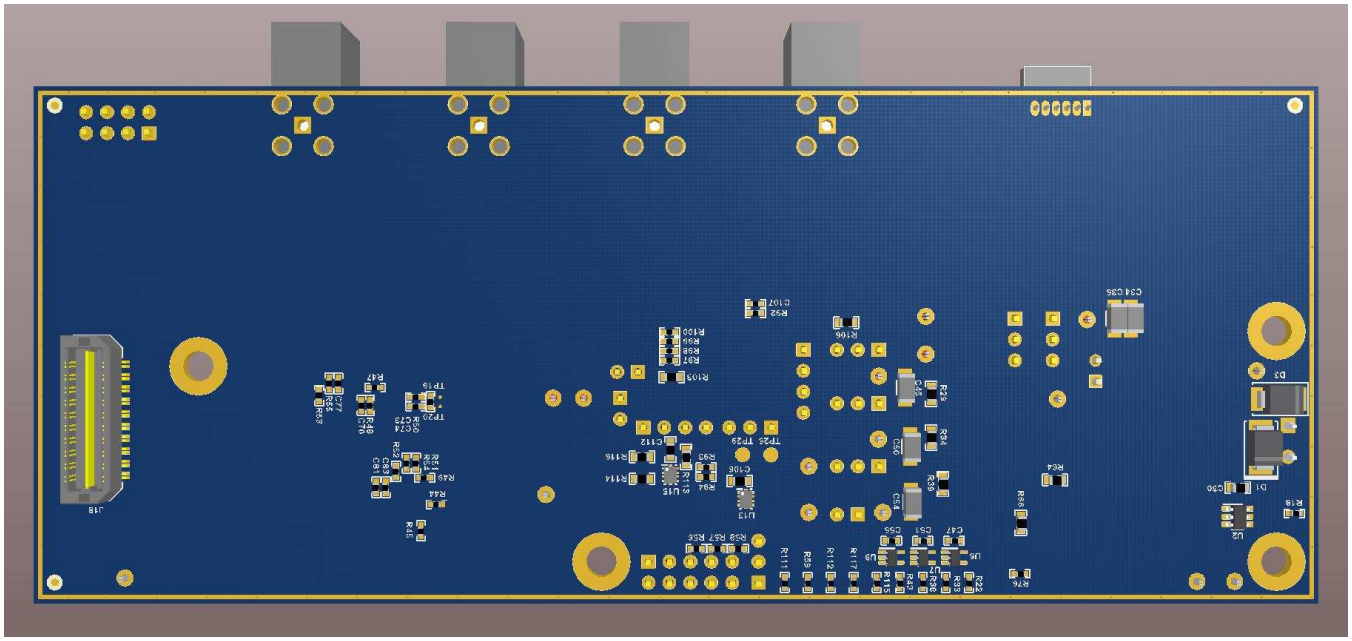


図 3. Board—Bottom View

2.2 I²C Addressing

2.2.1 Multiple Device Addressing (Aliasing)

If the user intends to access all four cameras on the same I²C bus, they must follow a method of assigning an alias to each camera for use when addressing them. The FPD-Link SER/DES parts provide this functionality to assign a slave ID (alias) to each camera. This feature allows the slave devices to be independently addressed. The physical address of the slave and its associated alias IDs are configured by programming the “Slave ID” and “Slave Alias” registers on the deserializer. From the I²C host perspective, this task remaps the address of each slave to its slave alias.図 4 shows an example of I²C address aliasing.

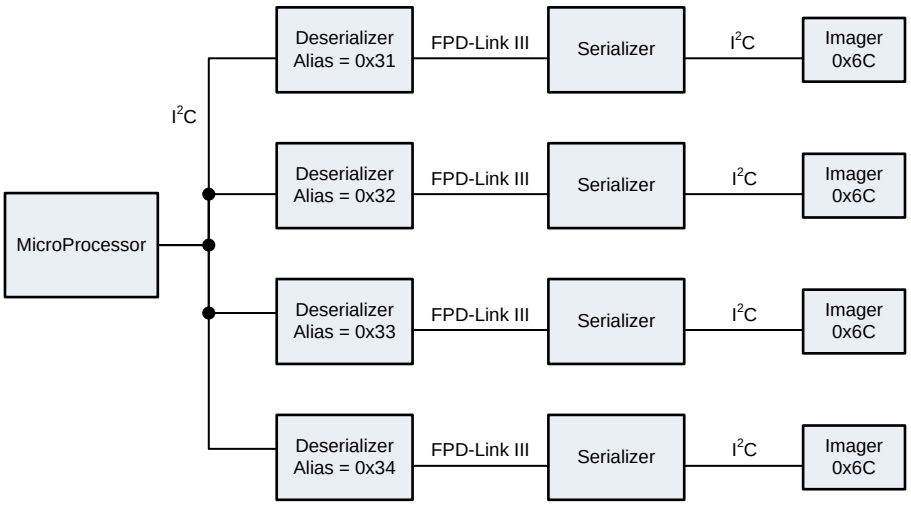


図 4. I²C Address Aliasing

2.2.2 I²C Bus Switches and Connections

This system offers four possible I²C hosts. Each host has a role to perform and a slave that they must configure. This requirement complicates the I²C bus connections. 図 5 shows three I²C switches, which are used to configure the I²C bus to accomplish all of the tasks required for initialization of the system. A GPIO has been stationed on the MCU connected to the control pin of each switch. These control pins are labeled with red text under the switch in 図 5. The functionality of these control pins can be described as:

- I²C_SW_EXT: When this switch is open, either the MSP430 or the SoC functions as the I²C host in the system. When this switch closes, it allows the external MCU to take over as host of the I²C bus. If an external MCU is used, place the MSP430 into external MCU mode by setting the jumper J19.
- I²C_SW_SOC: When this switch is open, all SoC I²C traffic is isolated from the TIDA-01323 board. This isolation allows either the local MCU or the external MCU to act as the host. Depending on when this switch is closed, the SoC can either initialize the board or just control the camera after one of the MCUs has initialized the board. Control of the cameras is done by writing I²C commands into the UB96x during normal operation.
- I²C_SW_UB960: When this switch is closed, the main I²C bus on the UB960 is connected to the main I²C bus on the board.

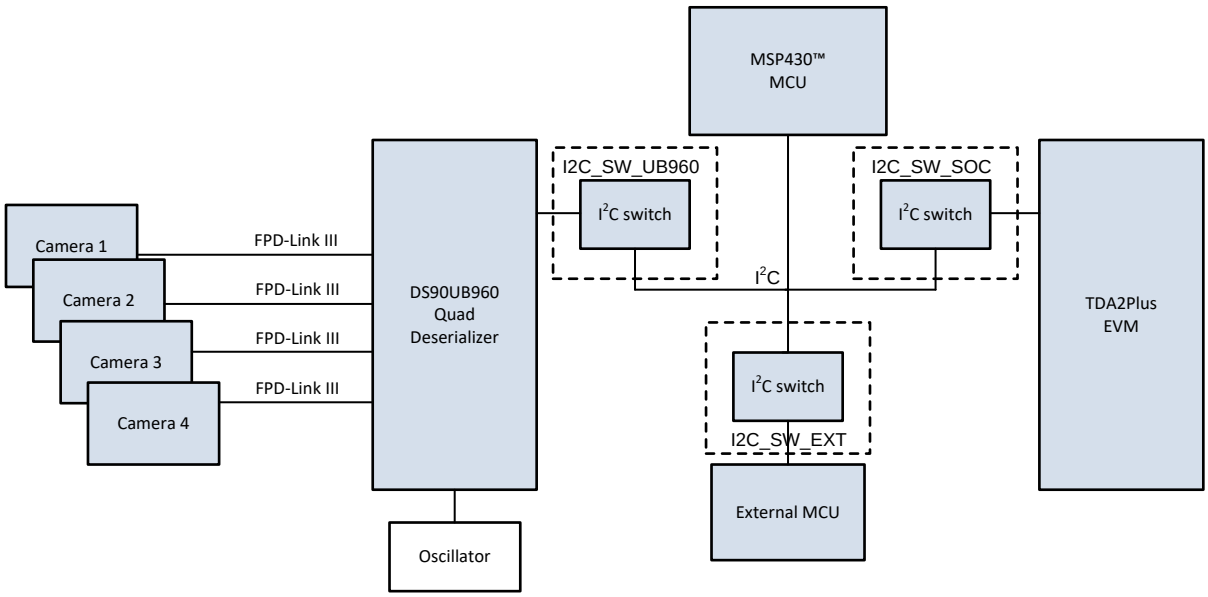


図 5. I²C Bus Diagram

2.2.3 Power-Over-Coax (PoC) Filter

One of the most critical portions of a design that uses PoC is the filter circuitry. The goal is twofold: 1. Deliver a clean DC supply to the input of the switching regulators. 2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB953 serializer on the TIDA-01130 and DS90UB960 deserializer on this design communicate over two carrier frequencies: 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers while attempting to only pass DC.

The PoC design requires an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth to enable the forward channel and backchannel to pass uninterrupted over the coax. To accomplish this uninterrupted passing, select an inductor for filtering the 10-MHz to 1-GHz range in addition to selecting a ferrite bead for filtering the 1- to 2.2-GHz frequency band. L1 in 図 6 represents the complete filter for inductor and ferrite beads. L2, which is shown in 図 6, is the same filter design as L2; however, L1 is located on the TIDA-01130 camera module design.

Ensuring that this filter has the smallest footprint is imperative. The LQH3NPZ100MJRL 10-µH inductor has been chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. Using this inductor eliminates the requirement for a solution that typically demands two inductors, one for the low-end frequency band and another for the high-end frequency band.

For the high-frequency, forward-channel filtering, inductors are usually not sufficient to filter above 1 GHz. Therefore, the TIDA-01323 design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because, when in operation, the current through these devices reduces the effective impedance. Therefore, three ferrite beads instead of two allows for more headroom across the whole frequency band. Lastly, for good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the designer can minimize the solution size on the board for the PoC inductor filtering. For more details, see *Sending Power Over Coax in DS90UB913A Designs*.

Another important requirement to note in regards to filtering is to ensure that the FPD-Link signal is not interrupted by allowing DC offset on the data. Choose the AC coupling caps shown by the 0.033 µF and 0.015 µF in such a way to ensure the high-speed AC data signals pass through but also blocks the DC from coupling on the data lines. Capacitive values for the DS90UB953/DS90UB960 pair are smaller than previous generations due to their requirement to pass 4 Gbps of data versus the previous 2 Gbps of video data transmission from 1-MP cameras.

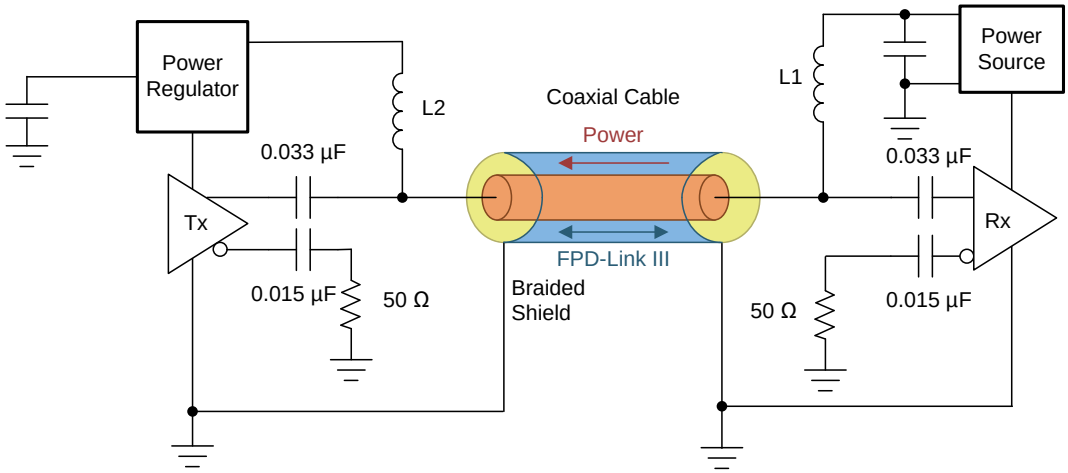


図 6. Power Over Coax

2.3 Step-Down Converter

図 7 shows the typical application circuit of the step-down converter. Much of the component selection and design theory can be found in the *Application Information* section of *TPS6216x 3-V to 17-V, 1-A Step-Down Converters with DCS-Control™*. Only a few external components are available from which to choose during component selection of the step-down converter.

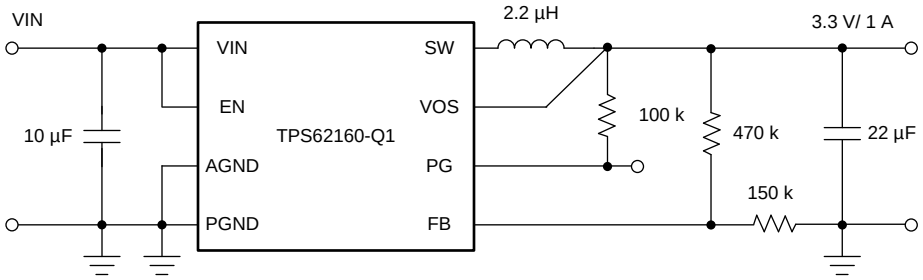


図 7. Typical Application Circuit

2.3.1 Choosing Output Inductance Value

As previously mentioned, maintaining the switching frequency of the converter above 2 MHz is important in this design, which means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and easy to predict, the minimum inductance (L) for the converter to operate with continuous inductor current can be calculated using the following 式 1:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN} \times I_{OUT} \times f} = \frac{3.3\ V\left(12\ V - 3.3\ V\right)}{2 \times 12\ V \times 0.4\ A \times 2.1\,MHz} = 1.42\ \mu H \quad (1)$$

The 400-mA current budget has a safety margin; therefore, a 2.2-uH works well for this application.

After choosing the inductance, the next step is to select an inductor with a proper saturation current. The maximum current through the inductor is the combination of the steady-state supply current as well as the inductor ripple current. The goal is to obtain a sufficiently high current rating that can be minimized as much as possible to reduce the physical size of the inductor. The following 式 2 is used to calculate the inductor ripple current (from the data sheet):

$$\Delta I_L = VOUT \times \left(\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}} \right) \quad (2)$$

式 3 shows the parameters for this design using the TPS62160-Q1:

$$V_{OUT} = 3.3\ V,\ V_{IN} = 12\ V,\ L = 2.2\ \mu H,\ f_{SW} = 2.25\ MHz \quad (3)$$

式 3 yields an inductor ripple current of ΔI_L = 483 mA. The maximum current draw of the system through this regulator is 250 mA. Finally, the following 式 4 is used to calculate the minimum saturation:

$$L_{SAT} \geq \left(I_{MAX} + \frac{I_{RIPPLE}}{2} \right) \times 1.2 = \left(400\ mA + \frac{483\ mA}{2} \right) \times 1.2 = 770\ mA \quad (4)$$

A TDK VLS201610HBX-2R2M has been selected for this design, which has a saturation current of 1700 mA with only a 10% drop in inductance. This part comes in a 2×1.6-mm package.

2.3.2 Choosing the Output Capacitor

Because the device is internally compensated, it is only stable for certain component values in the LC output filter. *Optimizing the TPS62130/40/50/60/70 Output Filter* provides the chart of stable values (see 表 2). The selected 2.2-uH inductor paired with a 22-uF capacitor yields a 32.4-kHz corner frequency, which is well within the recommended stable range for the TPS6216x family.

表 2. Stability Versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL) EFFECTIVE CORNER FREQUENCIES								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
0.47 µH	151.4 kHz	103.8 kHz	70.0 kHz	47.9 kHz	32.8 kHz	23.2 kHz	16.4 kHz	11.6 kHz	8.2 kHz
1.00 µH	103.8 kHz	71.2 kHz	48.0 kHz	32.8 kHz	22.5 kHz	15.9 kHz	11.3 kHz	8.0 kHz	5.6 kHz
2.2 µH	70.0 kHz	48.0 kHz	32.4 kHz	22.1 kHz	15.2 kHz	10.7 kHz	7.6 kHz	5.4 kHz	3.8 kHz
3.3 µH	57.2 kHz	39.2 kHz	26.4 kHz	18.1 kHz	12.4 kHz	8.8 kHz	6.2 kHz	4.4 kHz	3.1 kHz
4.7 µH	47.9 kHz	32.8 kHz	22.1 kHz	15.1 kHz	10.4 kHz	7.3 kHz	5.2 kHz	3.7 kHz	2.6 kHz
10.0 µH	32.8 kHz	22.5 kHz	15.2 kHz	10.4 kHz	7.1 kHz	5.0 kHz	3.6 kHz	2.5 kHz	1.8 kHz
	Recommended for TPS6213x/4x/5x/6x/7x								
	Recommended for TPS6213x/4x/5x only								
	Stable without Cff (within recommended LC corner frequency range)								
	Stable without Cff (outside recommended LC corner frequency range)								
	Unstable								

2.3.3 Choosing Feedback Resistors

For the 3.3-V rail, using the TPS62162 does not require feedback resistors because this device is a fixed voltage device. For the 1.8-V rail and 1.1-V rail, the designer can repeat the steps for all design calculations as outlined in 2.3.2. Then, for those two rails, perform the feedback resistor calculation as outlined in the data sheet.

3 Getting Started Hardware

3.1 Hardware Configuration

The TIDA-01323 design requires configuration before use. Perform the following configuration steps to avoid damage to system components. The following configuration is for a four-camera surround view system using TIDA-01130 cameras and a TDA2Plus EVM. The included power supply powers the EVM while a supply similar to a car battery is used to power the TIDA-01323.

1. Configure the power supply. Add and verify jumpers in the following locations (see 図 8):
   a. J8 (open) – Sets SEPIC output to 12 V; if PoC of 5 V is required, short J8
   b. J11 pins 2 to 3 – Connects output of SEPIC to input of buck converters and provides power to DS90UB960 and MCU
   c. J21 pins 2 to 3 – Connects output of SEPIC to the high-side switch for camera power
   d. J9 pins 1 to 2 – Selects output from 3.3-V buck instead of external supply
   e. J13 pins 1 to 2 – Selects output from 1.8-V buck instead of external supply
   f. J15 pins 1 to 2 – Selects output from 1.1-V buck
2. Set the MCU mode by installing J26. Pins 1 and 2 place the board in local MCU mode and is initialized by the MSP430 MCU.
3. Connect TIDA-01323 to the TDA2Plus EVM.
4. Connect four TIDA-01130 cameras using FAKRA coax cables.
5. Connect HDMI OUT on the TDA2Plus EVM to monitor using an HDMI cable.
6. Connect the power supply provided with the TDA2Plus EVM to the input power connector on the EVM.
7. Connect 12 V of input power to J5. Pin 1 is marked VIN. Pin 2 is marked GND. The board is protected against reversing the input voltage. If the polarity of the input voltage is reversed, LED D2 illuminates and Q1 prevents damage to the board.
8. Press the MSP430 RESET button (S1) on the TIDA-01323 board.

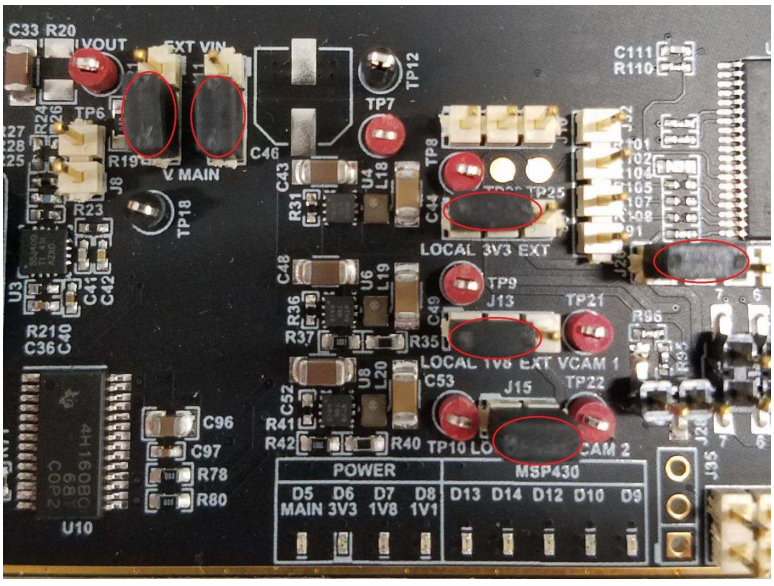


図 8. Board Jumpers

3.2 Software

GPIO configuration: Header J27 is available for eight GPIOs for the MCU and deserializer, which allows for maximum flexibility when utilizing these GPIOs as required in each application. This setup also indicates that the jumpers must be correctly set for any configuration. In the case of this design, the use any of the MCU GPIOs is not required, so none of the jumpers are installed.

4 Getting Started Firmware

4.1 Board Boot Sequence

If the board has been placed into local MCU mode (J26), the MSP430 MCU is in control of the start-up sequence of the board. At start-up, pulldown resistors hold the UB960 in RESET mode. When the MCU initializes, it begins the start-up of the rest of the board. The configuration sequence is as follows:

1. MCU (MSP430) boots
2. MCU enables power to all four cameras by enabling TPS4H160 channels
3. MCU opens external I^2C switch using: I2C_SW_SOC
4. MCU opens SoC I^2C switch using: I2C_SW_DES
5. MCU closes UB964 I^2C switch using: I2C_SW_EXT
6. MCU holds reset (PDB) pin low on UB960 deserializer
7. MCU closes I^2C switch using: I2C_SW_DES and the UB960 PDB pin is pulled out of reset
8. MCU closes I^2C switch I2C_SW_SOC and I2C_SW_EXT to allow the user to have control from TDA2Plus or other processor
9. MCU changes I^2C pins to inputs (high Z) and loops infinitely
10. With Board initialized, the UB960, attached DS90UB953 serializer, and OV2775 imager can be initialized from TDA2Plus

5 Test Setup

5.1 Video Hardware Setup

図 9 shows the setup to test the video output for the four TIDA-01130 camera modules using the TIDA-01323 design.

To enable video output from the DS90UB960, connect the TIDA-01323 to the CSI-2 Samtec connector on the TDA2Plus EVM. The TDA2Plus EVM enables video output by writing all the backchannel I²C setting configurations for the OV2775, DS90UB953, and DS90UB960 devices. When these writes complete, Vision SDK software enables video output to an HDMI connected monitor.

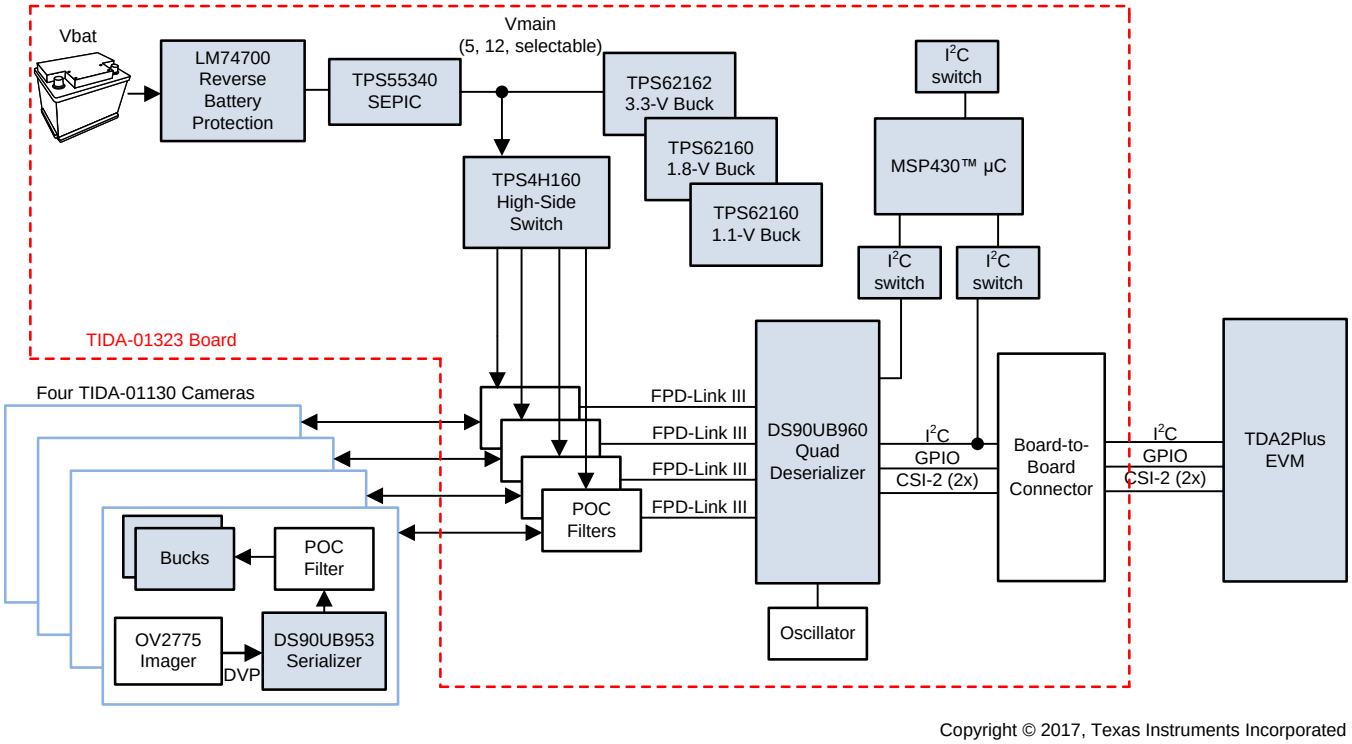


図 9. Surround View Setup

5.2 FPD-Link III I²C Initialization

With the setup in 図 9 connected, the TIDA-01323 design supplies the power through PoC for the camera power of this reference design. The power is also used to step down to 1.8 V and 1.1 V for the DS90UB960 supplies. Now the OV2775, DS90UB953, and DS90UB960 have power. Lastly, by connecting the TDA2Plus EVM to the TIDA-01323 design, the I²C writes for initialization can begin. The writes to initialize the deserializer and serializer are as follows:

- Deserializer slave I²C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x6E with 0xA8: BC_GPIO_CTL0 FrameSync signal to GPIO1
  - Register 0x58 with 0x5E: I²C pass through enabled and backchannel frequency select
  - Register 0x5C with 0x31: Sets serializer alias to 31 for camera on port 0
  - Register 0x5D with 0x6C: Sets slave ID for imager to 6C

- Register 0x65 with 0x6C: Sets slave alias for imager to 6C
- Register 0x6D with 0x7C: Configures port to coax mode and FPD III to CSI mode
- Register 0x19 with 0x00: Sets FS_HIGH_TIME_1
- Register 0x1A with 0x8A: Sets FS_HIGH_TIME_0
- Register 0x1B with 0x04: Sets FS_LOW_TIME_1
- Register 0x1C with 0xE1: Sets FS_LOW_TIME_0
- Register 0x18 with 0x01: Enables FrameSync
- Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
- Register 0x33 with 0x01: Enables 960 CSI output and sets to 4 lane mode
- Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
- Register 0x20 with 0x08: Forwarding enabled for all RX ports. RX3 forwarded to CSI-2 Port 1 TX and other three ports forwarded to CSI-2 Port 0 TX.

- Serializer slave I^2C address 0x31, 0x32, 0x33 and 0x34 (write to all cameras)
  - Register 0x06 with 0x41: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from 953 to OV2775
  - Register 0x07 with 0x28: Sets DIV_N_VAL for CLKOUT from 953 to OV2775
  - Register 0x0E with 0xF0: Sets GPIOs on 953 as outputs
  - Register 0x0D with 0x00: Drives GPIOs from 953 low to force imager PWDN and RESET pins low
  - Register 0x0D with 0x0C: Pulls PWDN and RESET pins on OV2775 high to bring imager out of reset

Keep in mind that the deserializer setup registers listed are only showing writes for one camera. To initialize all four cameras, select each camera using port select register 0x4C. This selection allows for the similar writes for each camera, where the serializer, imager, and framesync have been set up.

5.3 OV2775 Initialization

After the FPD-Link III setup completes for the DS90UB953 and DS90UB960 devices, the I^2C initialization can begin on the OV2775. For these writes, see the OV2775 data sheet for register settings. There are many register settings, but as long as the 953 and 960 FPD-Link III parts have been configured, the I^2C backchannel allows for the OV2775 to be accessed at address 0x6C in 8-bit addressing or 0x36 in 7-bit addressing.

5.4 Setup for Verifying Power Supply Start-Up: V_{IN}, 3.3-V, 1.8-V, and 1.1-V Rails

図 10 shows the setup for measuring the V_{IN}, 3.3-V, 1.8-V, and 1.1-V rails.

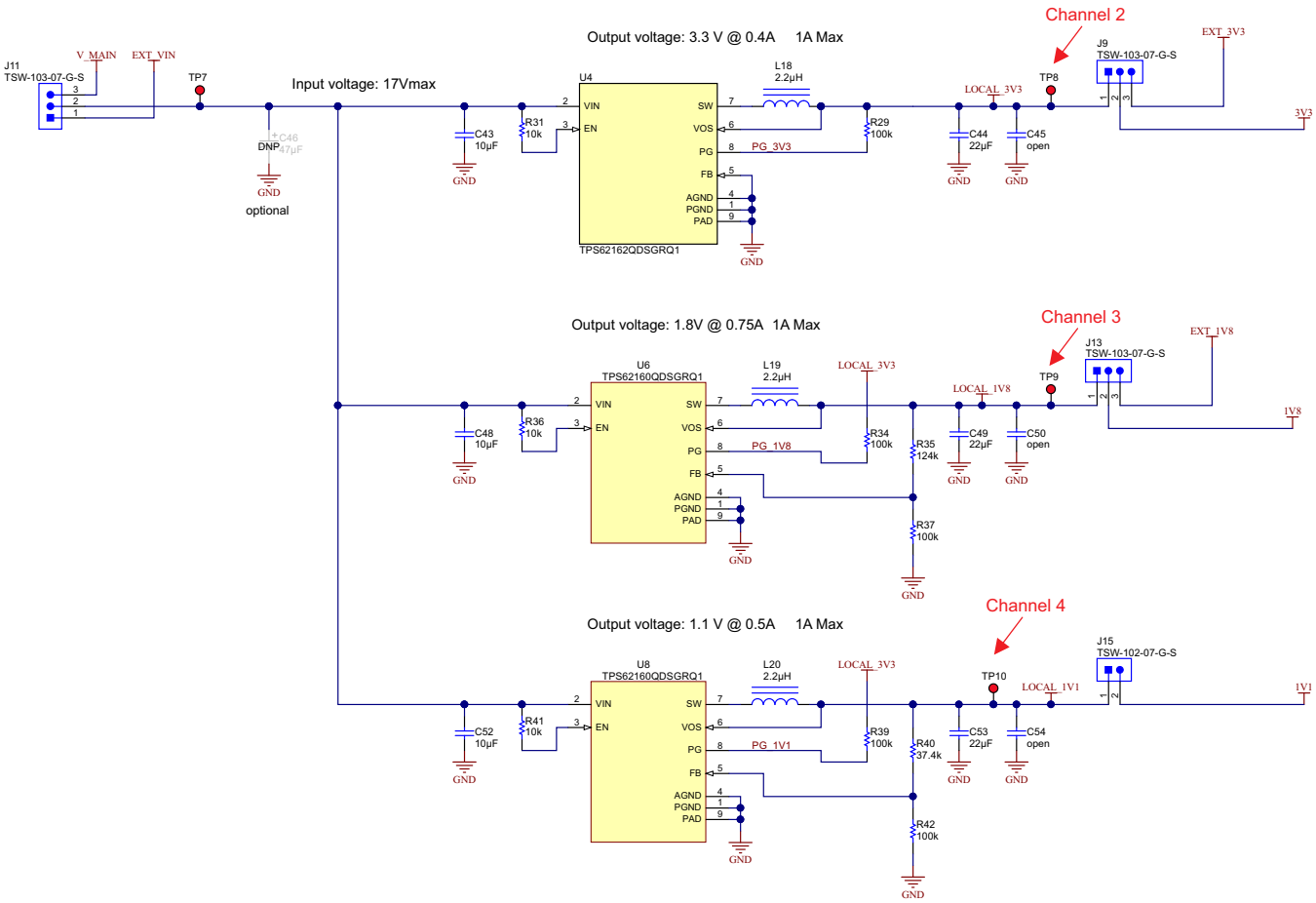


図 10. Setup for Measuring All Power Rails

The waveforms for the power supply start-up are as follows (see 図 11):

- Channel 1 (blue): 12-V regulated power out from SEPIC supply (TP7)
- Channel 2 (red): 3.3-V switching converter output (TP8)
- Channel 3 (green): 1.8-V switching converter output (TP9)
- Channel 4 (pink): 1.1-V switching converter output (TP10)

All channels are displayed at 1 V per division. The time scale is 100 µS per division.

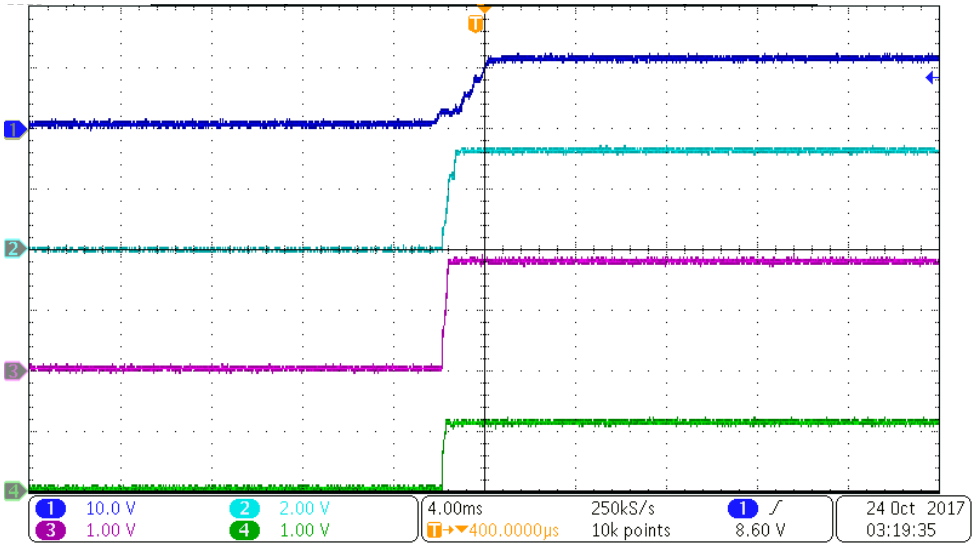


図 11. Power Supply Start-Up

5.5 Camera Power and Monitoring

This reference design utilizes the TPS4H160-Q1 switch to supply power to the four remote cameras. With the TPS4H160-Q1 being a quad high-side switch, the designer can control the power of each camera individually if utilizing the enable control of each channel. Also, in addition to the hub being able to supply 12 V or 5 V to the cameras utilizing the TPS55340 and jumper J8, the hub can also supply power to each camera by setting the J21 on the TIDA-01323.

The TPS4H160-Q1, when used with the MSP430, allows the designer to monitor the power to the camera module. To measure current, the CS pin is routed to the MSP430 to monitor the voltage level corresponding to the output current. To monitor this current, the DIAG_EN pin must be driven high from the MSP430 so that the current sense and fault pin can be activated. Otherwise, if the DIAG_EN pin is low, these two pins are high impedance. The fault pin is also routed to the MCU, which provides indication of a fault condition (voltage or current) on the channel. To select the channel on which these diagnostics features are performed, the SEH and SEL pins can be toggled by the ECU in the high and low values according to the TPS4H160 data sheet. Lastly, the power to each camera is current limited with a setting from the high side switch. This limitation is a pulldown resistor set to 1.3 kΩ on the CL pin, which sets the current limit to 1.53 A. The range of current operation for each camera channel is 0.1 A to 1 A, which allows designers to use high current, high resolution imagers, or radar modules without issue.

6 Board Programming or Reprogramming

If the board has not been programmed or if the software requires an update, use the following procedure.
MSP430 code:

1. Connect EZ430 development tool to J23
2. Connect USB cable to PC and to EZ430 development tool
3. Open the TI Code Composer Studio™ (CCS) software
4. Open project files for software to be loaded
5. Select "Debug" to load the software into MSP430
6. Press "Run" to run in a debug environment or remove EZ430
7. Press the MSP430 RESET button (S1) on the TIDA-01323 board
8. The software begins to run on the board

To use the TDA2Plus software, see the TDA2Plus EVM documentation for further details.

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-01323.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01323.

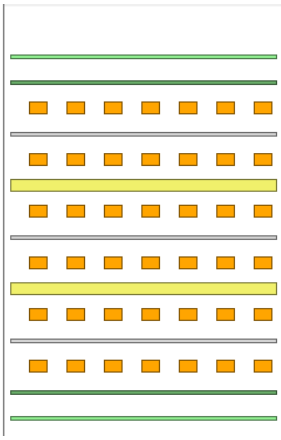
7.3 PCB Layout Recommendations

7.3.1 PCB Layer Stackup Recommendations

The PCB layer recommendations are as follows:

- Use at least a four-layer board with a power and ground plane. Locate the low-voltage complementary-metal-oxide semiconductor (LVCMOS) signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this configuration reduces the inductive effect of the vias when currents are returned through the plane.

An additional two layers have been used in this board to simplify ball-grid array (BGA) fanout and routing. 図 12 shows the six-layer stackup used in this board.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Layer 1 - Top Lay...	Signal	Copper	1.4				Top	
Dielectric 1	Dielectric	Prepreg	10	370HR	4.2			
Layer 2 - GND	Signal	Copper	1.417				Not Allowed	
Dielectric 2	Dielectric	Core	7	370HR	4.2			
Layer 3 - Sensitive	Signal	Copper	1.417				Not Allowed	
Dielectric 3	Dielectric	Prepreg	20	370HR	4.2			
Layer 4 - GND	Signal	Copper	1.417				Not Allowed	
Dielectric 4	Dielectric	Core	7	370HR	4.2			
Layer 5 - PWR	Signal	Copper	1.417				Not Allowed	
Dielectric 5	Dielectric	Prepreg	10	370HR	4.2			
Layer 6 - Bottom...	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

図 12. Layer Stackup

7.3.2 Switching DC-DC Converter

During part placement and routing, always consider the path the current takes through the circuit. The yellow line in 図 13 shows the input current path travels from the input capacitor (C43), through the switch in the converter (U4), to the inductor (L18), and then out across the output capacitors (C44 and C45). Any return currents from the input capacitor (C43) or the output capacitors (C44 and C45) are joined together on the top side of the board before they are connected to the ground (return) plane (inside the green circle). This occurrence reduces the amount of return currents in the internal ground plane, which allows other circuits on the board to register voltage gradients. This occurrence may not be noticeable in the performance of the converter, but it does reduce its coupled noise into other devices. 図 13 shows the layout of the switch-mode power supply with the routing outlined and solid.

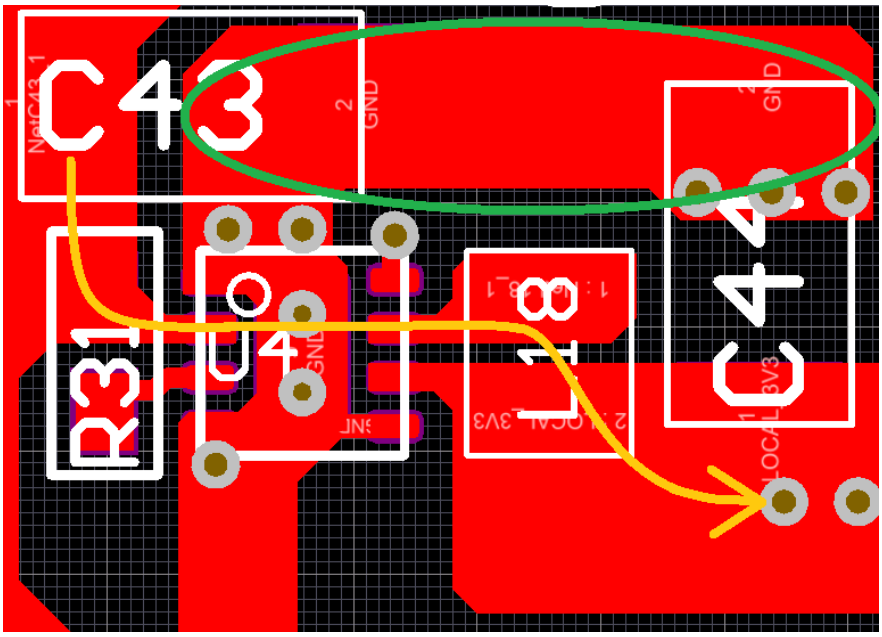


図 13. Step-Down Switched-Mode Power Supply Routing

Input capacitors must be placed as close to the integrated circuit (IC) as possible to reduce the parasitic series inductance from the capacitor to the device that it supplies. This placement is especially important for DC-DC converters because the inductance from the capacitor to the high-side switching FET can cause high-voltage spikes and ringing on the switch node, which can be damaging to components and cause problems such as electromagnetic interference (EMI).

7.3.3 Deserializer Layout Recommendations

Decoupling capacitors must be located very close to the supply pin on the serializer. Again, this placement requires the designer to consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. An ideal placement is not always possible due to space constraints. Place smaller value capacitors that provide higher-frequency decoupling closest to the device.

図 14 shows the decoupling capacitors C60, C62, and C65. The loop from 1.8 V to GND is short because of the small capacitor value for C65 and because the accompanying larger capacitors are kept very close to U1, which results in a very-small current loop.

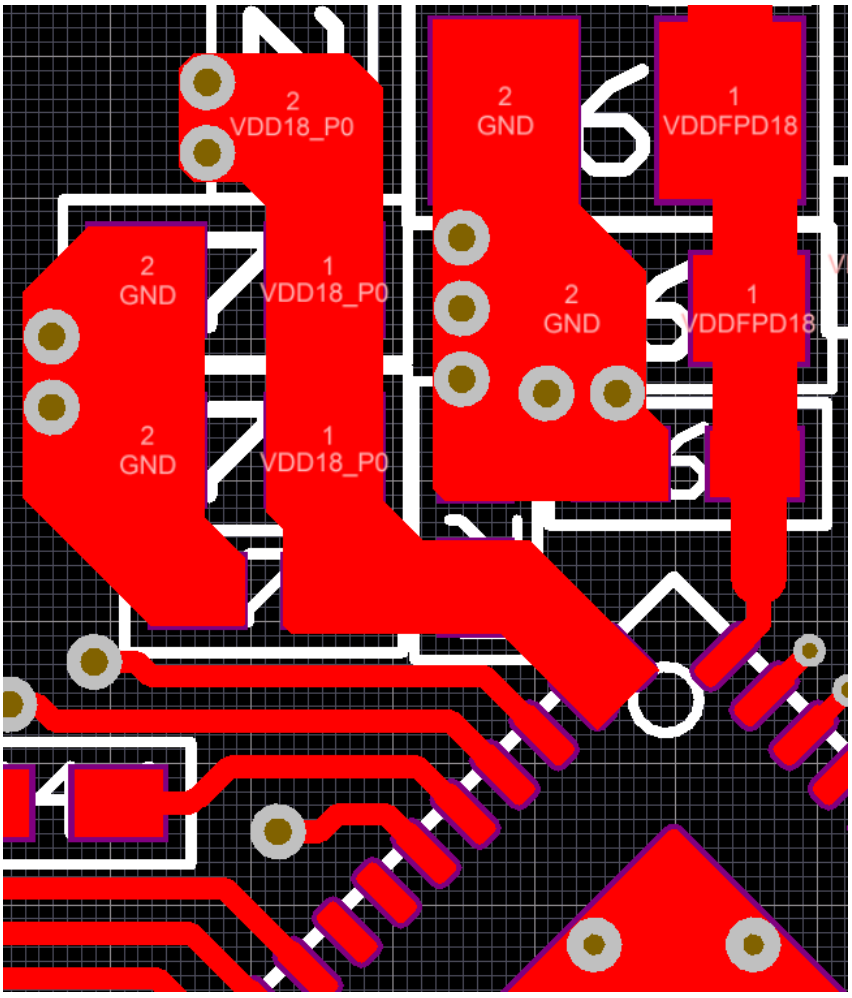


図 14. Decoupling Current Loop

When routing the coaxial input to the PoC filter, be aware of potential stubs on the low-voltage differential signaling (LVDS) nets. In 図 15, the high-speed signal comes in from J1 and passes through C19 to U1 (DS90UB960). DC is blocked by C9 and the DC current path is through ferrite beads L7, L3, L27, which blocks high-frequency AC data and inductor L4, which blocks low-frequency AC data. For the high-speed signal, the DC path through L7 is a stub. Minimizing the length of this stub reduces reflections on the LVDS lines and leads to better signal integrity.

In addition, the high-speed signal path trace from the C9 and C11 AC caps must be length- and impedance-matched with each other to reduce reflections. Also, the length of these traces must be length-matched with the other camera input traces so that there is no skew between the data transmitting from the TIDA-01323 Fakra connector to the deserializer.

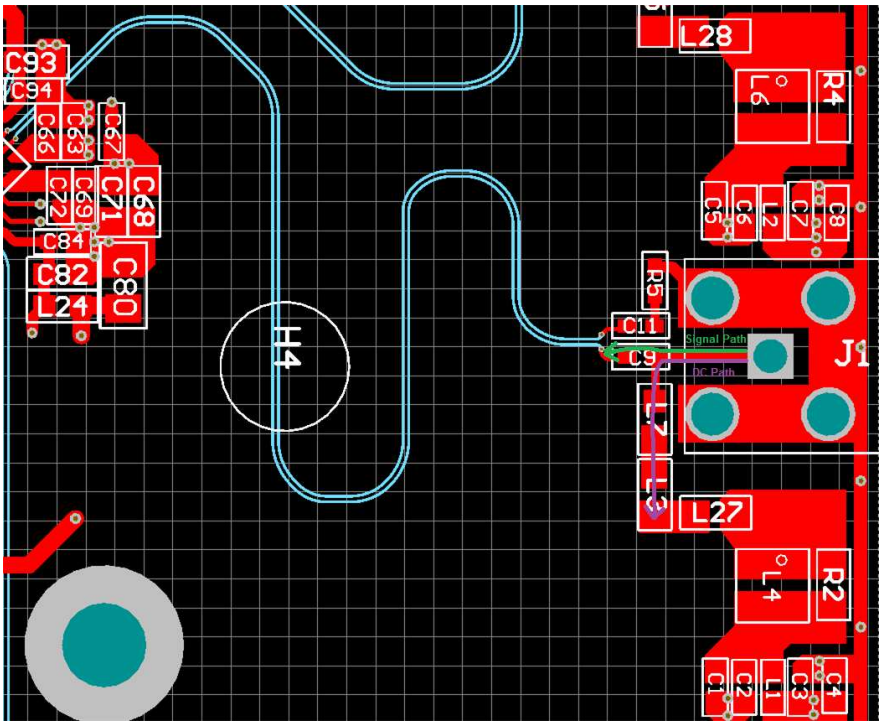


図 15. LVDS Signal Pair Routing

The last layout guideline, which is most important, is the CSI-2 routing from TX port 0 and port 1 to the SAMTEC connector for interfacing with TDA2Plus. The following list provides the guidelines for routing the differential CSI-2 traces. 図 16 shows the routing for the TIDA-01323 and 図 17 confirms that the routed lengths are within the guidelines for trace length matching within and between pairs.

1. Route CSI0_D*P/N and CSI1_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep length difference between a differential pair to 5 mils of each other.
3. Match trace lengths between pairs to be < 25 mils.
4. Each pair must be separated by at least three times the signal trace width.
5. Length matching must be near the location of mismatch.
6. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥ 135°. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on the same layer.
8. Keep the number of VIAS to a minimum—TI recommends keeping the VIA count to two or fewer.
9. Keep traces on layers adjacent to the ground plane.
10. Do *NOT* route differential pairs over any plane split.

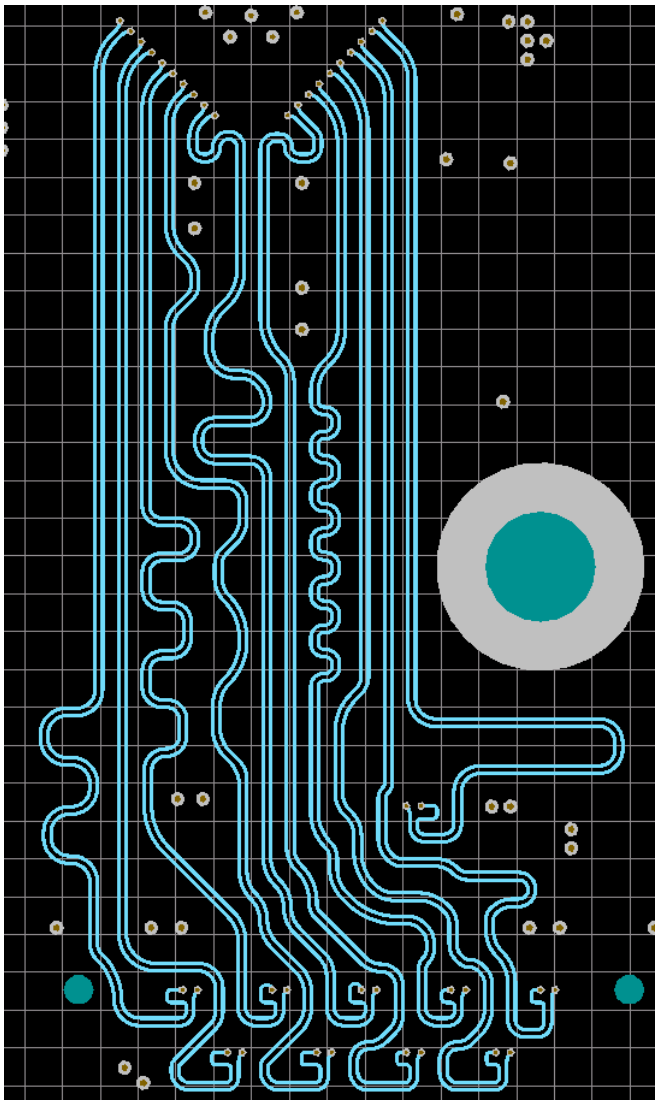


図 16. CSI-2 Differential Trace Routing

15 Differential Pairs (10 Highlighted)

Designator	Average Length (mil)	Longest Signal Len...
CSI0_D0	1760.21	1760.416
CSI1_CLK	1759.438	1760.497
CSI1_D2	1759.926	1760.939
CSI1_D3	1760.218	1761.31
CSI0_CLK	1761.817	1762.038
CSI1_D0	1760.552	1762.091
CSI0_D2	1762.503	1762.31
CSI0_D3	1762.344	1762.779
CSI1_D1	1763.283	1764.301
CSI0_D1	1762.505	1764.651

Add Delete Edit

20 Nets (0 Highlighted)

Name	Routed Length (mil)
CSI0_CLK_N (-)	1762.025
CSI0_CLK_P (+)	1761.609
CSI0_D0_N (-)	1760.413
CSI0_D0_P (+)	1760.007
CSI0_D1_N (-)	1763.636
CSI0_D1_P (+)	1761.375
CSI0_D2_N (-)	1762.275
CSI0_D2_P (+)	1762.731
CSI0_D3_N (-)	1761.307
CSI0_D3_P (+)	1763.38
CSI1_CLK_N (-)	1760.442
CSI1_CLK_P (+)	1758.434
CSI1_D0_N (-)	1761.056
CSI1_D0_P (+)	1760.047
CSI1_D1_N (-)	1764.293
CSI1_D1_P (+)	1762.273
CSI1_D2_N (-)	1760.937
CSI1_D2_P (+)	1758.916
CSI1_D3_N (-)	1760.697
CSI1_D3_P (+)	1759.74

図 17. CSI-2 Trace Length Matching

7.4 Layout Prints

To download the layer plots, see the design files at TIDA-01323.

7.5 Altium Project

To download the Altium project files, see the design files at TIDA-01323.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-01323.

7.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01323.

8 Software Files

To download the software files, see the design files at TIDA-01323.

9 Related Documentation

1. Texas Instruments, *Automotive 2-MP Camera Module Design with MIPI CSI-2 Video Output Interface and Power Over Coax*
2. Texas Instruments, *DS90UB953-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer*
3. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™*
4. Texas Instruments, *TLV702-Q1 300-mA, Low-I_Q , Low-Dropout Regulator*
5. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs*
6. Texas Instruments, *Cable Requirements for the DS90UB913A & DS90UB914A*
7. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter*
8. Texas Instruments, *TDA3 – SoC Processor for Advanced Driver Assist Systems (ADAS)*

9.1 商標

MSP430, Code Composer Studio are trademarks of Texas Instruments.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。