参考資料

TI Designs: TIDM-1018
産業用ゲートウェイ向け PoE (Power over Ethernet) のリファレンス・デザイン

概要

このリファレンス・デザインは PoE (Power over Ethernet) と高性能の SimpleLink™MSP432E4 イーサネット・マイクロコントローラ (MCU)、イーサネットを統合しており、産業用ゲートウェイなどの IoT (モノのインターネット) 製品を開発できます。このデザインにより、既存のネットワーク・ケーブルから電力の供給を受け、クラウドとの間でインテリジェントにデータを収集、処理、交換できるため、最終製品の価値が高まります。

設計リソース

TIDM-1018	デザイン・フォルダ
MSP432E401Y	プロダクト・フォルダ
TPS23753A	プロダクト・フォルダ
TPD2E2U06	プロダクト・フォルダ
TLV431A	プロダクト・フォルダ
TPS737	プロダクト・フォルダ

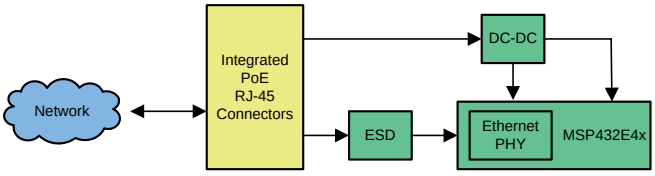
TI E2E™ Community　E2Eエキスパートに質問

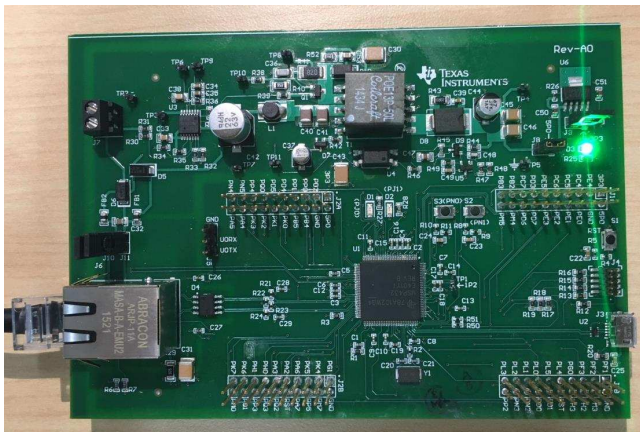
特長

- PoE 電力段用に RJ45、変圧器、ダイオード・ブリッジを統合し、コスト効率の優れた BOM を実現
- 7W のフライバック・コンバータ絶縁出力、5V と 3.3V の両方の出力電源レールに対応
- オプションの電力ヘッダにより、ネットワーク電源障害の発生時に UPS から外部 DC 電源を供給
- デュアル BoosterPack™プラグイン・モジュール・ヘッダにより、TI (SimpleLink ワイヤレス・デバイスを含む) およびサードパーティが供給する広範な BoosterPack モジュールを使用して最終アプリケーションのプロトタイプを作成可能
- 評価用に、SimpleLink MSP432E4 ソフトウェア開発キット (SDK) の例を少し変更するだけで実行可能

アプリケーション

- HVAC ゲートウェイ
- HVAC システム・コントローラ
- セキュリティ・ゲートウェイ
- 状態監視ゲートウェイ





1 System Description

The MSP432™ SimpleLink MCUs with Ethernet are high-performance Arm® Cortex®-M MCUs with integrated Ethernet MAC and PHY and a wide variety of wired communication interfaces such as universal serial bus (USB), controller area network (CAN), Quad-SPI (QSSI), I²C, SPI, UART, and other serial protocols. Featuring a 120-MHz Arm Cortex-M4F CPU, 1MB of Flash and 256kB of SRAM, and advanced cryptography accelerators, MSP432E4 MCUs offer an ample amount of processing resources for developers to implement wired and wireless connectivity stacks and processing algorithms to build IoT-ready, intelligent industrial gateway applications. When integrated with PoE solutions from TI, the MSP432E4 adds a layer of intelligence at the remote node. The MSP432E4 allows customers to leverage their existing network to not only communicate and control devices securely with the PoE solution but also to deliver power, which reduces the system cost in IoT space and adds value to their industrial gateway products. This reference design files include schematics, bill of materials (BOM), layer plots, Altium files, and Gerber files.

Using this reference design as the baseline, customers can further extend their design to develop a smart PoE industrial gateway to connect wired and wireless sensors to the cloud. The MSP432E4 MCUs offer a rich number of additional wired interfaces including USB, CAN, QSPI, SPI, I²C, and UART to connect to additional wired sensors and actuators. In addition, customers can also add wireless connectivity such as Sub-1 GHz, *Bluetooth*® low energy, and Wi-Fi® using SimpleLink wireless MCUs and SimpleLink SDK wireless plugins. Finally, the PoE gateway can enable cloud integration by leveraging the network services provided by the SimpleLink MSP432E4 SDK and the cloud plugins.

2 System Overview

2.1 Block Diagram

図 1 shows the PoE for connected IoT block diagram.

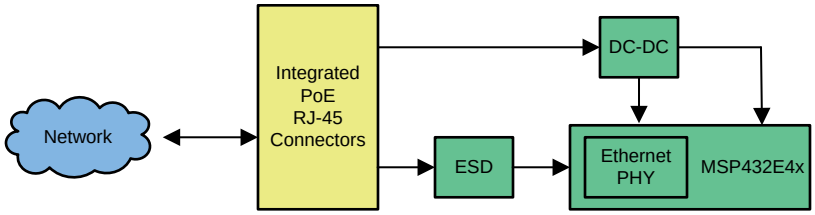


図 1. PoE for Connected IoT Block Diagram

2.2 MSP432E401Y

The MSP432E401Y is a 120-MHz high-performance MCU with 1MB on-chip flash and 256KB on-chip SRAM. The MSP432E401Y MCU also features an integrated Ethernet MAC + PHY for connected applications and cryptographic modules of AES, DES, and SHA for encryption, decryption, and authentication. The device has high-bandwidth interfaces such as memory controller and a high-speed USB 2.0 digital interface. With integration of a number of low- to mid-speed serial interfaces, up to 4-MSPS 12-bit analog-to-digital converter (ADC), and motion control peripherals, the device makes a unique design for a variety of intelligent industrial gateway applications ranging from building automation zone controller and smart grid data concentrators to factory automation and control gateways.

図 2 shows the high-level block diagram of the MSP432E401Y MCU.

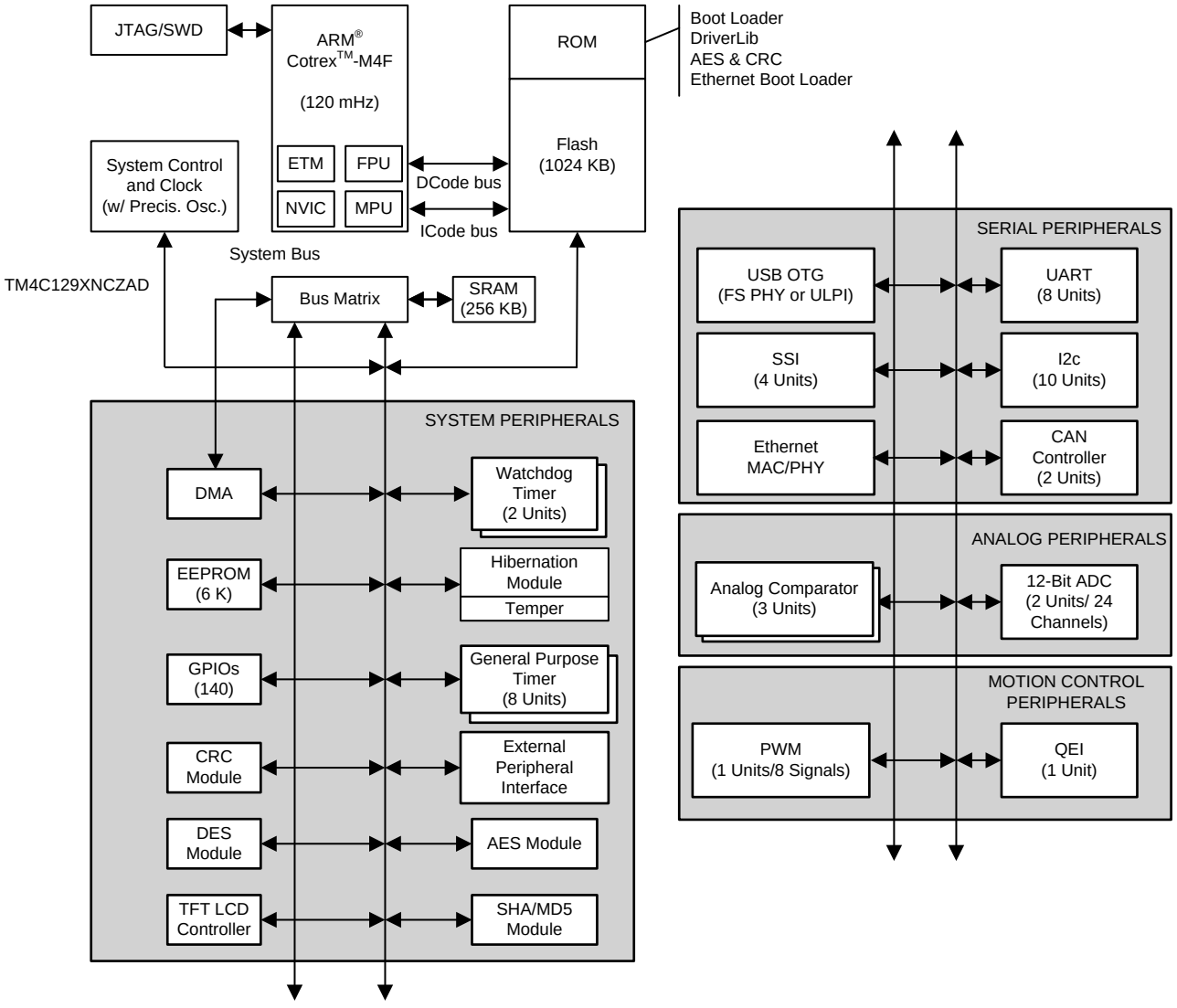


図 2. MSP432E401Y MCU High-Level Block Diagram

2.3 TPS23753A

The TPS23753A is a combined Power over Ethernet (PoE) powered device (PD) interface and current-mode DC-DC controller optimized specifically for isolated converter designs. The PoE implementation supports the IEEE 802.3at standard as a 13-W, type 1 PD. The requirements for an IEEE 802.3at type 1 device are a superset of IEEE 802.3-2008 (originally IEEE 802.3af).

The TPS23753A supports a number of input-voltage ORing options including highest voltage, external adapter preference, and PoE preference.

The PoE interface features an external detection signature pin that can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off. Classification can be programmed to any of the defined types with a single resistor.

The DC-DC controller features a bootstrap start-up mechanism with an internal, switched current source. This provides the advantages of cycling overload fault protection without the constant power loss of a pullup resistor.

The programmable oscillator can be synchronized to a higher-frequency external timing reference. The TPS23753A features improvements for uninterrupted device operation through an ESD event.

2.4 TPD2E2U06

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I^2C.

2.5 TLV431A

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

When used with an optocoupler, the TLV431 device is an ideal voltage reference in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. These devices have a typical output impedance of 0.25 Ω. Active output circuitry provides a very sharp turn-on characteristic, making them excellent replacements for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

2.6 TPS737

The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1-µF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when the device is not enabled, is less than 20 nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

3 Hardware, Software, Testing Requirements and Test Results

This design is a plug-and-play system with minimal user intervention required for either supplying or managing any control I/Os for power to the device.

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Test Points, Connectors, Jumpers, Switches, and LEDs

This section gives details about the connectors, test points, and the jumpers that are available on the design for debug, probe, and flexibility of evaluation.

表 1 lists the test points.

表 1. Test Points

Designator	Description
TP1	MSP432E401YTPDT 1.2-V core voltage test point
TP2	DC-DC converter return
TP3	PoE input, low side
TP4	DC-DC converter output voltage
TP5	Digital ground
TP6	DC-DC converter bias supply
TP7	DC-DC converter return
TP8	Drain terminal of the primary-side switching MOSFET
TP9	Bias voltage regulator
TP10	Gate driver for the primary-side switching MOSFET
TP11	Control loop input to the pulse width modulator (PWM)

表 2 lists the connectors and jumpers.

表 2. Connectors and Jumpers

Designator	Description
J1A	BoosterPack header
J1B	BoosterPack header
J2A	BoosterPack header
J2B	BoosterPack header
J3	USB header
J4	JTAG debug header
J5	UART header for debug COM port
J6	Integrated RJ45 connector, transformer and rectifier diode
J7	External adapter input connector
J8	5-V output jumper
J9	3.3-V output jumper
J10	PoE input low side from the RJ45 jack
J11	PoE input high side from the RJ45 jack

3.1.1.2 Power

There are four potential sources of power in this design:

- The primary power is through the Ethernet RJ45 (J6). The user must ensure that the switch or hub used is PoE PSE equipment.
- The user can power the design by using the external adapter input connector (J7) through a 12-V DC power supply.
- The user can power the design from a 5-V DC power supply by removing the header (J8) and applying 5-V input to Pin-1 of J8.

  注: GND from the external power supply must be connected to TP5.

- The user can power the design from a 3.3-V DC power supply by removing the header (J9) and applying 3.3-V input to Pin-1 of J9.

  注: GND from the external power supply must be connected to TP5. In this configuration, the 5 V is not available on the BoosterPack headers.

3.1.1.3 Connecting a Debugger

To be able to download an application to the MSP432E401Y MCU, the header J4 is provided. This header is a 10-pin 50-mil spacing connector and is compliant to the Arm Cortex 10-pin JTAG standard. If the debugger does not have an Arm Cortex 10-pin header, a small adapter board may be required, and is easily available with most manufacturers of debug pods.

3.1.2 Software

Any example from the SimpleLink MSP432E4 SDK or SimpleLink SDK Plugins that supports MSP432E4 can be run on this design. Some minor updates (for example, to the pins used for LEDs and switches) are required while using examples that are built for the MSP-EXP432E401Y LaunchPad kit to be run on this design. 表 3 lists a comparison of pin functions.

表 3. Comparison of Pin Functions

Device Port Pin	MSP-EXP432E401Y LaunchPad Kit	TIDM-1018
PN0	LED D2	Switch S3
PN1	LED D1	Switch S2
PJ0	User switch 1	LED D1
PJ1	User switch 2	LED D2

Recommended gateway and IoT examples:

- Sub-1GHz and MSP432E4 based Gateway running TI 15.4 Stack
- MSP-EXP432E401Y Out of Box

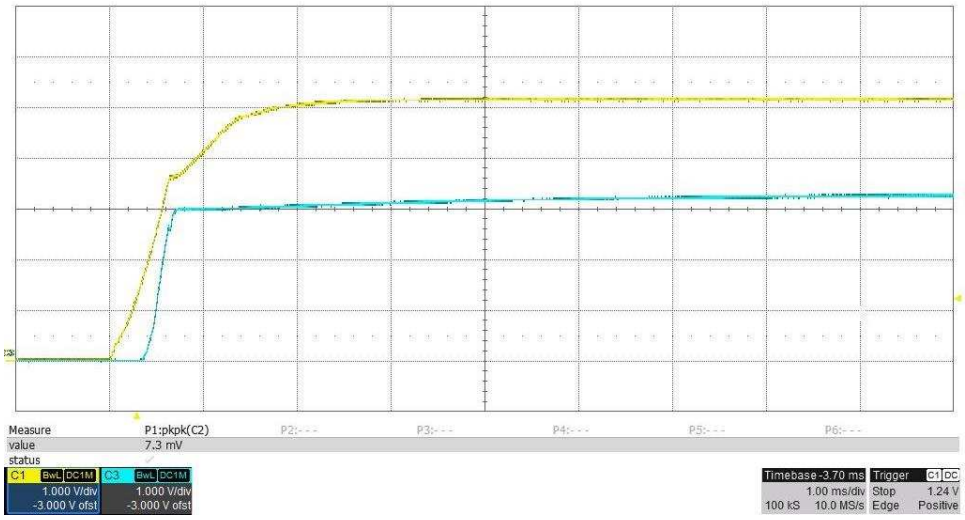
3.2 Testing and Results

3.2.1 Test Results

The following section gives details of the electrical tests completed on the design for PoE power front end.

3.2.1.1 Startup

図 3 shows the 5-V and 3.3-V output voltage startup waveforms with no external load and a 48-V input at J6.



CH1 (5 Vout): 1 V/div;
CH2 (3.3 Vout): 1 V/div;
1 ms/div

図 3. Start-Up Under No Load

図 4 shows the 5-V and 3.3-V output voltage startup waveforms with a 160-mA external load and 48-V input at J6.

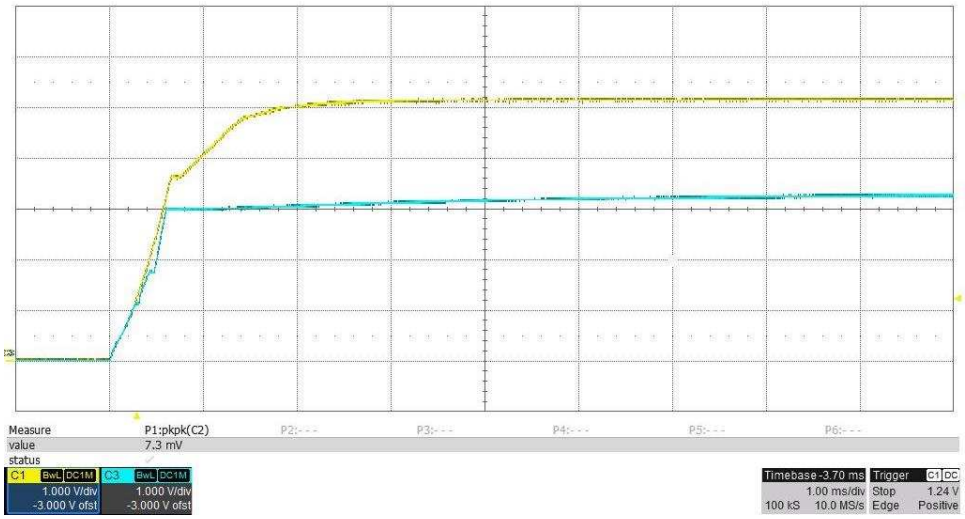


図 4. Start-Up Under Load Conditions

3.2.1.2 Efficiency

図 5 shows the converter efficiency with a 48-V input at J6. Jumper J8 was removed, and all loading is on the 5-V output.

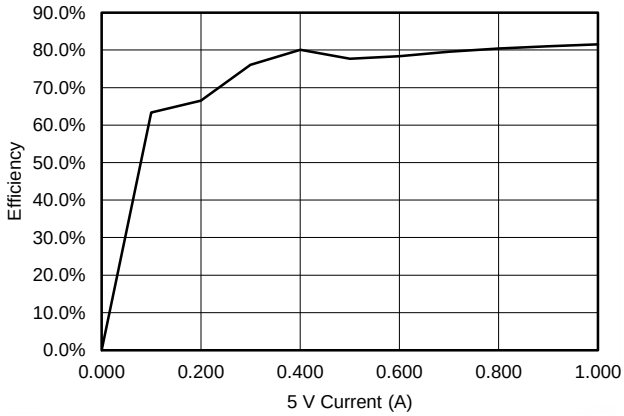
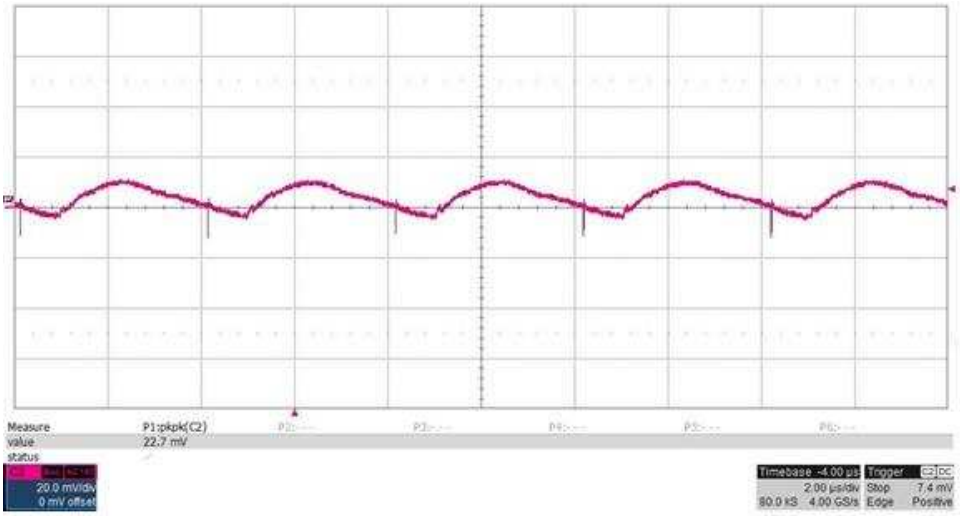


図 5. Efficiency Chart

3.2.1.3 Output Ripple Voltage

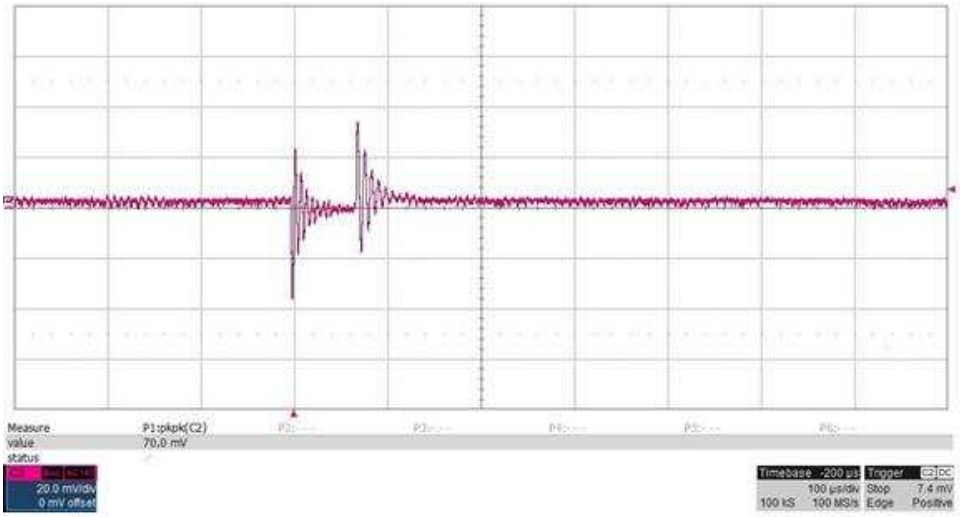
図 6 shows the 5-V output ripple voltage measured across C46. The 5-V output is loaded by the 3.3-V LDO (approximately 90 mA plus an external 160-mA load on the 5 V.



(20 mV ÷ div, 2 µs ÷ div)

図 6. Ripple Voltage on 5-V Load

図 7 shows the 3.3-V output ripple voltage measured across C52. There is a load on the 3.3-V load that repeats approximately every 60 ms, which results in the noise shown in 図 7.

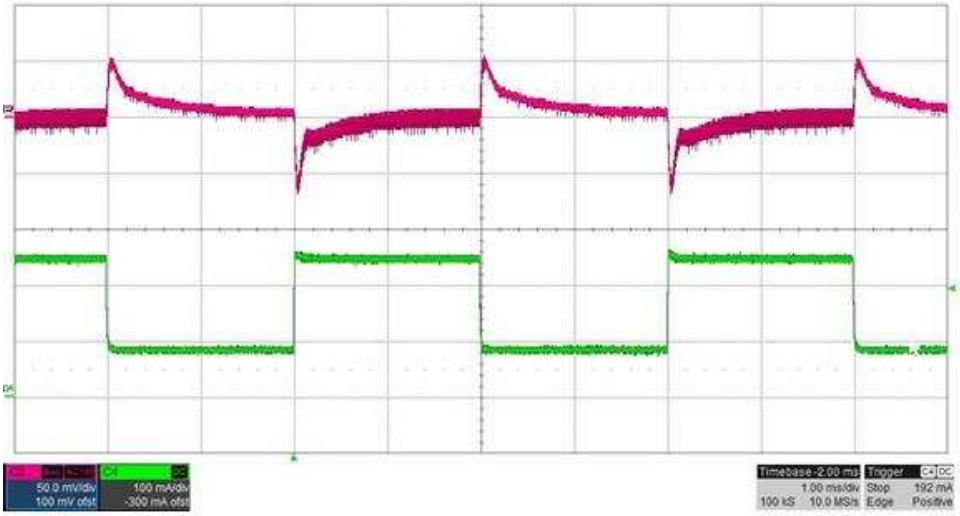


(20 mV ÷ div, 100 µs ÷ div)

図 7. Ripple Voltage on 3.3-V Load

3.2.1.4 Load Transients

図 8 shows the 5-V output voltage response (AC-coupled) to a load current step from 90 mA to 250 mA. The 90-mA load is the LDO with an external 160-mA load step applied.

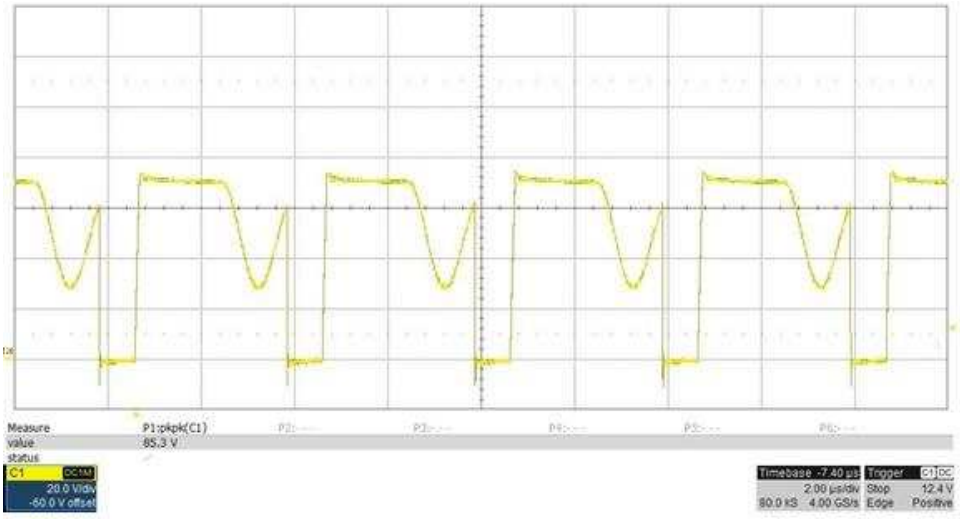


(50 mV ÷ div, 100 mA ÷ div, 1 ms ÷ div, 25 mA ÷ µs slew rate)

図 8. Load Transients on 5-V Output

3.2.1.5 Switching Waveforms

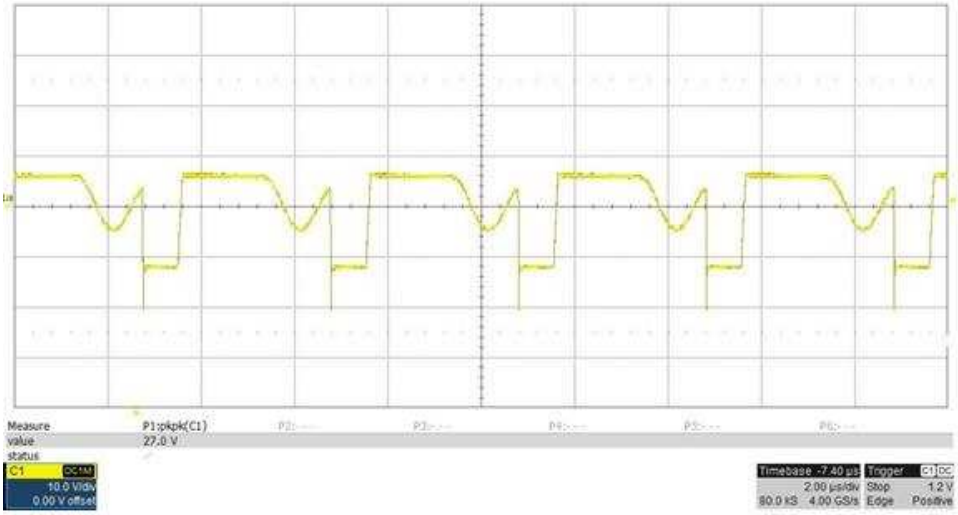
図 9 shows the drain voltage of Q1 with respect to GNDX. The input voltage is 48 V, and the 5-V output is loaded with the 3.3 V-LDO (90 mA) plus an external 160-mA load.



(20 V ÷ div, 2 µs ÷ div)

図 9. Switching Waveforms for Q1

図 10 shows the anode voltage of D8 with respect to GND. The input voltage is 48 V, and the 5-V output is loaded with the 3.3-V LDO (90 mA) plus an external 160-mA load.



(10 V ÷ div, 2 µs ÷ div)

図 10. Switching Waveform for D8

3.2.1.6 Control Loop Gain Stability

図 11 shows the converter's loop gain and phase margin. The 5 V is loaded with the 3.3-V LDO (90 mA) plus a 160-mA external load. The input is 48 V at J6.

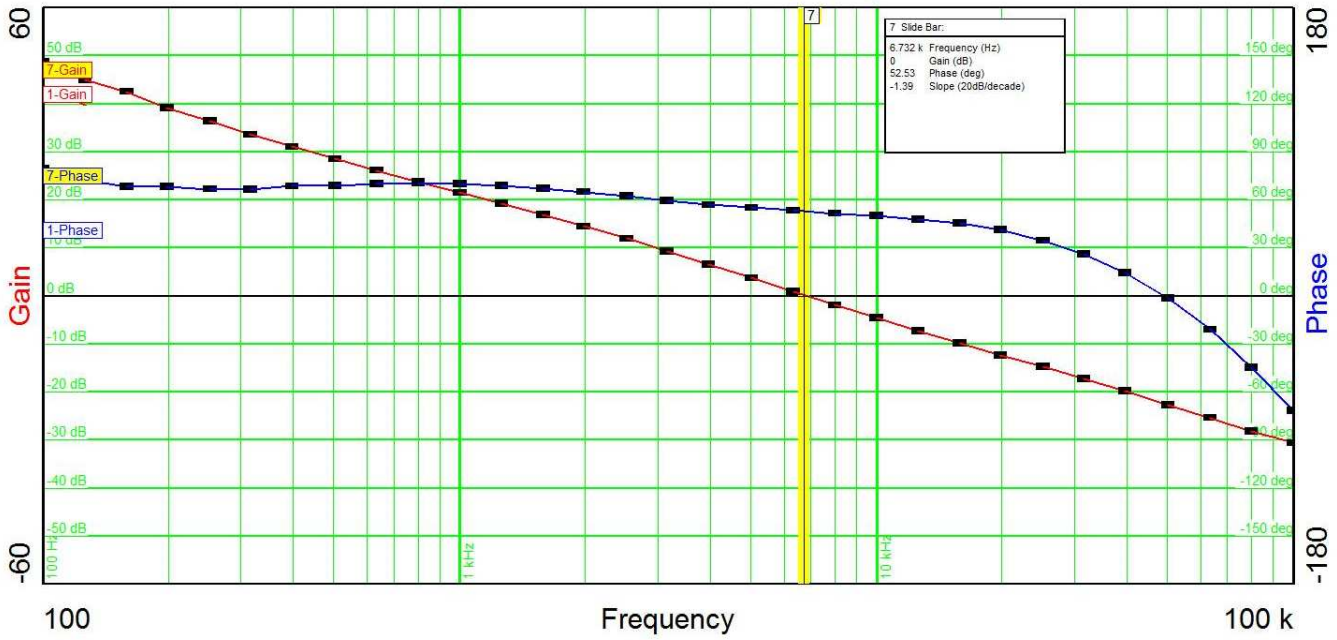


図 11. Control Loop Gain Stability

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDM-1018.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-1018.

4.3 PCB Layout Recommendations

An important consideration when doing the layout is the trace width for Ethernet and USB signals. The Ethernet and USB interfaces have critical differential impedance requirements. Both Ethernet signal pairs must be routed as a 100 Ω ± 10% differential pair on the top layer of the PCB with a ground plane as a reference. The USB signal pair must be routed as a 90 Ω ± 10% differential pair on the top layer of the PCB with a ground plane as a reference.

The most optimal solution is if the PCB fab house can adjust the stack up and provide for controlled dielectric. The designer must use the PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance. The PCB fab house can then adjust the trace space and width to their specific materials and process.

During the PCB layout, if the PCB fab house has a predefined layer stack up for low-cost process, the user must find the layer stack up information then use this information in PCB tools to get the optimum trace width. The design files have used a low cost variant with the following PCB stack up for four layer PCB's.

図 12 shows the PCB layer stack up for TIDM-1018.

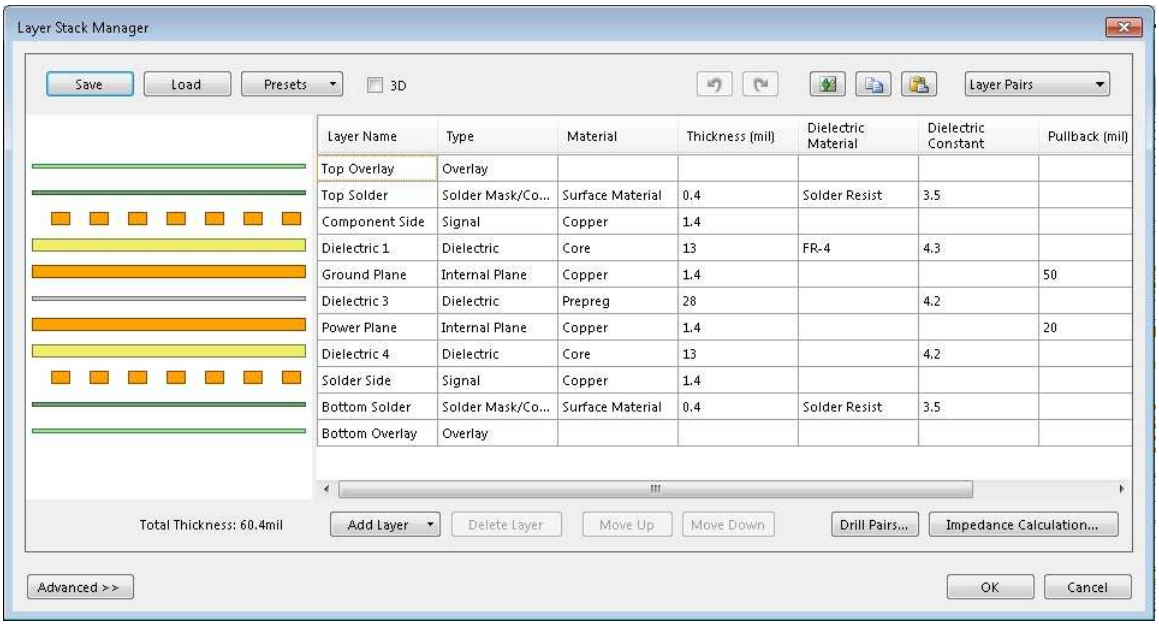


図 12. PCB Layer Stack Up for TIDM-1018

When the data shown in 図 12 is entered into the PCB tool, the trace width and space for Ethernet and USB signals are computed, which are listed in 表 4. The most important parameter is the Z_{DIFF}, which must be within ±10% tolerance.

表 4. Differential Signals Trace Information

Trace Width (mil)	Trace Thickness (mil)	Trace Height (mil)	Trace Spacing (mil)	E_R	Z_{DIFF}	Z_O
10	0.4	15.8	5	4.2	109.476	84.766
12.8	0.4	15.8	5	4.2	99.336	76.915

4.4 Altium Project

To download the Altium project files, see the design files at TIDM-1018.

4.5 Layout Guidelines

To download the layout guidelines, see the design files at TIDM-1018.

4.5.1 Layout Prints

To download the layout prints for each board, see the design files at TIDM-1018.

4.6 Gerber Files

To download the Gerber files, see the design files at TIDM-1018.

4.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-1018.

5 Software Files

To download the software files, see the **Software** section under **Related Tools & Software** at TIDM-1018.

6 Related Documentation

1. Texas Instruments, *System Design Guidelines for the MSP432E4xx Microcontrollers*
2. Saturn PCB Design Toolkit

6.1 商標

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7 About the Author

AMIT ASHARA is an Application Engineer and Member Group Technical Staff at TI, where he works on developing applications for SimpleLink MSP432E4x family of high performance wired connectivity MCUs. Amit brings to this role his extensive experience in high-speed digital and MCU system-level design expertise. Amit earned his Bachelor of Engineering (BE) from University of Pune, India.

DAVID STRASSER is an Applications Engineer and Member Group Technical Staff at TI, working in the Power Design Services group. David specializes in custom power converter designs Power over Ethernet applications. David earned his Bachelor of Science in Electrical Engineering degree (BSEE) from Western Michigan University and his Master of Science in Electrical Engineering degree (MSEE) from the Illinois Institute of Technology.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年11月27日発行分から2019年1月14日発行分への変更 **Page**

- ドキュメント・タイトルおよびドキュメント全体の対象製品を変更して「産業用ゲートウェイ」と記述 1
- 「特長」の「小さなフォームファクタの基板...」で始まるリスト項目を削除 1
- 「特長」の最後の項目で「例を変更なしで実行可能」を「例を少し変更するだけで実行可能」に変更 1
- 「アプリケーション」のリストを更新 1
- Updated the first paragraph in 3.1.2, *Software* 7
- Added recommended examples in 3.1.2, *Software* 7

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