参考資料

TI Designs: TIDA-01130
MIPI CSI-2ビデオ・インターフェイス、FPD-Link III、POCを搭載した、車載用2MPカメラ・モジュールのリファレンス・デザイン

概要

このリファレンス・デザインは車載用カメラ・モジュールで、高速シリアル・ビデオ・インターフェイスによりマシン・ビジョン処理またはディスプレイ・システムに接続します。このデザインは、TIの4Gbps FPD-Link III SerDes技術を使用し、非圧縮の2メガピクセルのビデオ・データ、双方向の制御信号、電力(POC)を、1本の同軸ケーブルで伝送します。

リソース

TIDA-01130	カメラ・モジュール	デザイン・フォルダ
DS90UB953-Q1	FPD-Link IIIシリアライザ	プロダクト・フォルダ
TPS62172-Q1	バック・コンバータ	プロダクト・フォルダ
TLV70218-Q1	LDO	プロダクト・フォルダ
TLV70213-Q1	LDO	プロダクト・フォルダ

TI E2E™ Community

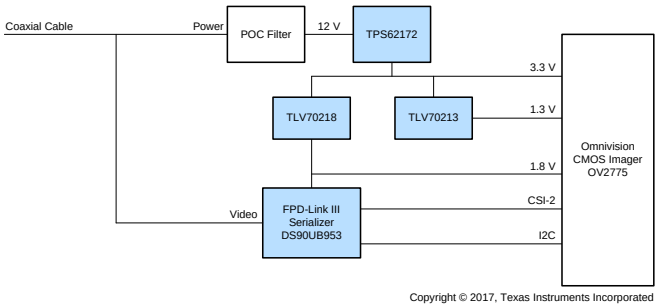
E2E™エキスパートに質問

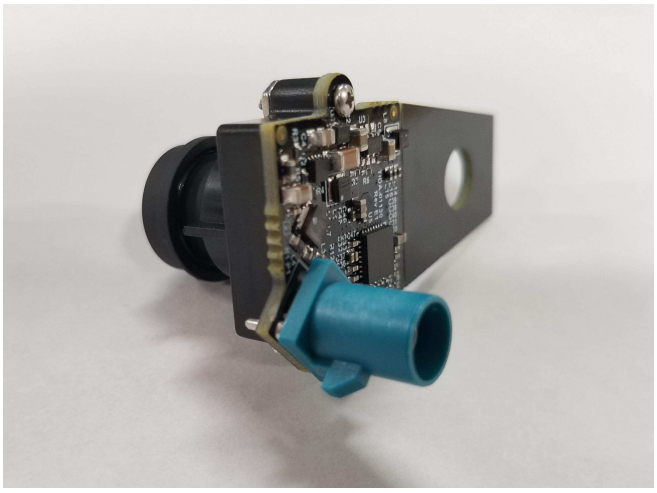
特長

- 1枚の20×20mmのPCBに搭載された省スペースのデザイン
- 小さなサイズに最適化された電源
- Omnivision製の2MP OV2775イメージ・センサにより、12ビットDVPまたはMIPI CSI-2のRAWイメージ・データを供給
- 単一のRosenberger Fakra製の同軸コネクタで、デジタル・ビデオ、電力、制御、診断信号を伝送
- 設計上の考慮事項とテスト結果を記載

アプリケーション

- ADASビジョン・システム
- フロント・カメラ
- カメラ監視システム(ミラーの代替品)
- サラウンド・ビュー・システム





1 System Description

For many automotive safety systems, small cameras are required. This reference design addresses these needs by combining a 2-megapixel (MP) imager with a 4Gbit/s serializer and providing the necessary power supply for both. All of this functionality is contained on a 20×20-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power, the FPD-Link front and backchannels enter the board through the FAKRA coax connector. The filter shown in 図 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

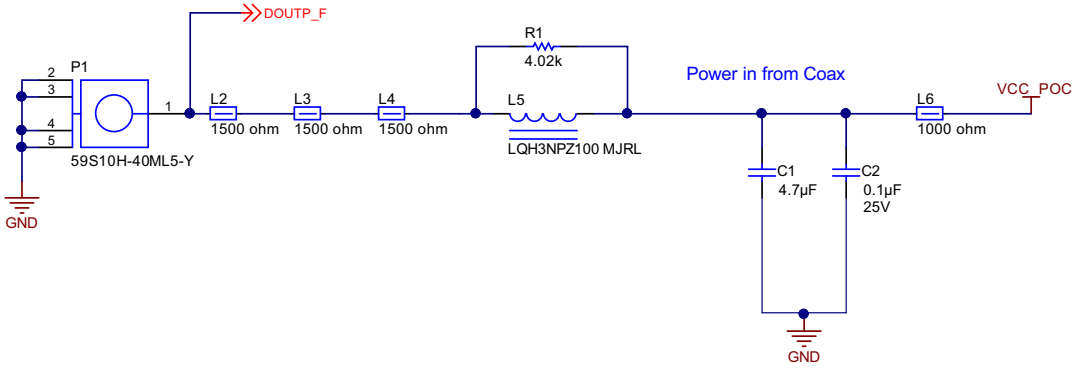


図 1. FPD-Link III Signal Path

The DC portion is connected to the input of the TPS62172 buck converter to output 3.3 V. The 1.8-V rail required by the serializer and the imager are created by the TLV70218. The 1.3 V only required by the OV2775 imager is output from the TLV70213.

The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel takes between the serializer and deserializer.

The output of the imager is connected through a four-lane MIPI CSI-2 interface to the serializer. Then the serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

On the same coax cable, there is separate low-latency, bidirectional control channel that transmits control information from an I^2C port. This control channel is independent of video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	4	12	17	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V	—	0.6	1	W

2 System Overview

2.1 Block Diagram

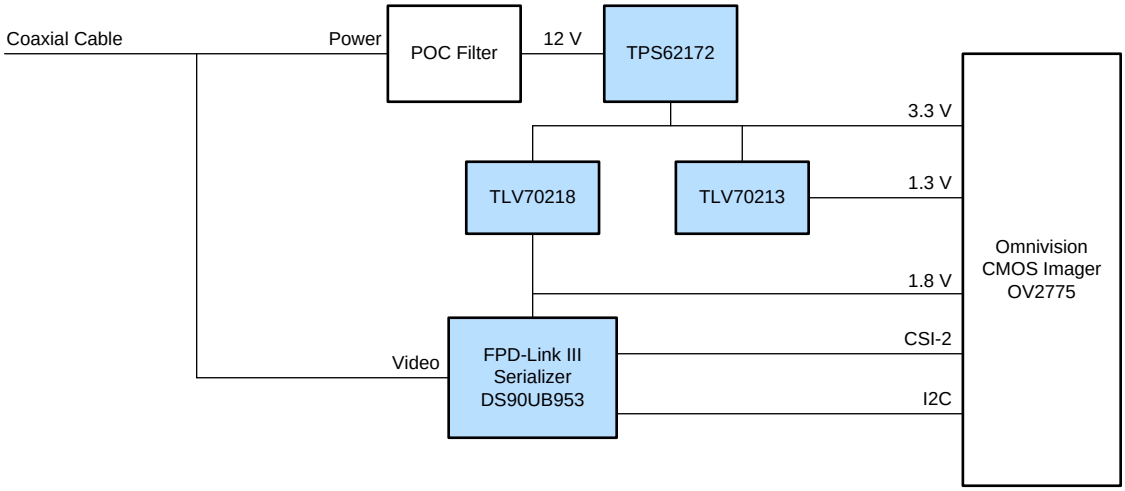


図 2. Camera Block Diagram

2.2 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU)
- TPS62172-Q1: an automotive qualified step-down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response
- TLV70218-Q1: an automotive qualified 300-mA, low I_Q, low-dropout (LDO) regulator with a fixed output voltage of 1.8 V
- TLV70213-Q1: an automotive qualified 300-mA, low I_Q, LDO regulator with a fixed output voltage of 1.3 V

Find more information on each device and why they were chosen for this application in the following subsections.

2.2.1 OV2775 Imager

Available from the Omnivision, this imager is a 1/2.9", 2-MP CMOS 1080p imager with high dynamic range (HDR). It is suitable for automotive systems and can provide a parallel 12-bit DVP or four-lane MIPI CSI-2 output. Some additional features of the imager are:

- Supports image sizes: 1920×1080, VGA, QVGA and any cropped size
- Low power consumption
- Requires three voltage rails (3.3 V, 1.8 V, and 1.3 V)
- Can be configured using an I^2C-compatible two-wire serial interface

2.2.2 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 mates well with the MIPI CSI-2 video output of the OV2775 imager. Once combined with the filters for the POC, video, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the *Cable Requirements for the DS90UB913A and DS90UB914A Application Report*.

2.2.3 TPS62172-Q1

To keep the camera small, the power supply must be small. The supply must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but it can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This means that the TPS62172-Q1 switching regulator operating at 2.25 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

2.2.4 TLV70218-Q1 and TLV70213-Q1

The TLV702xx-Q1 series of LDO linear regulators are low quiescent current devices with excellent line and load transient performance. These automotive qualified LDOs are very small, allowing the 1.3-V and 1.8-V rails to be created in a very small space. A precision band gap and an error amplifier provide overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR) make these LDOs ideal for this application.

2.3 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.3.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor. The only goal of the design with regards to the PCB is to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

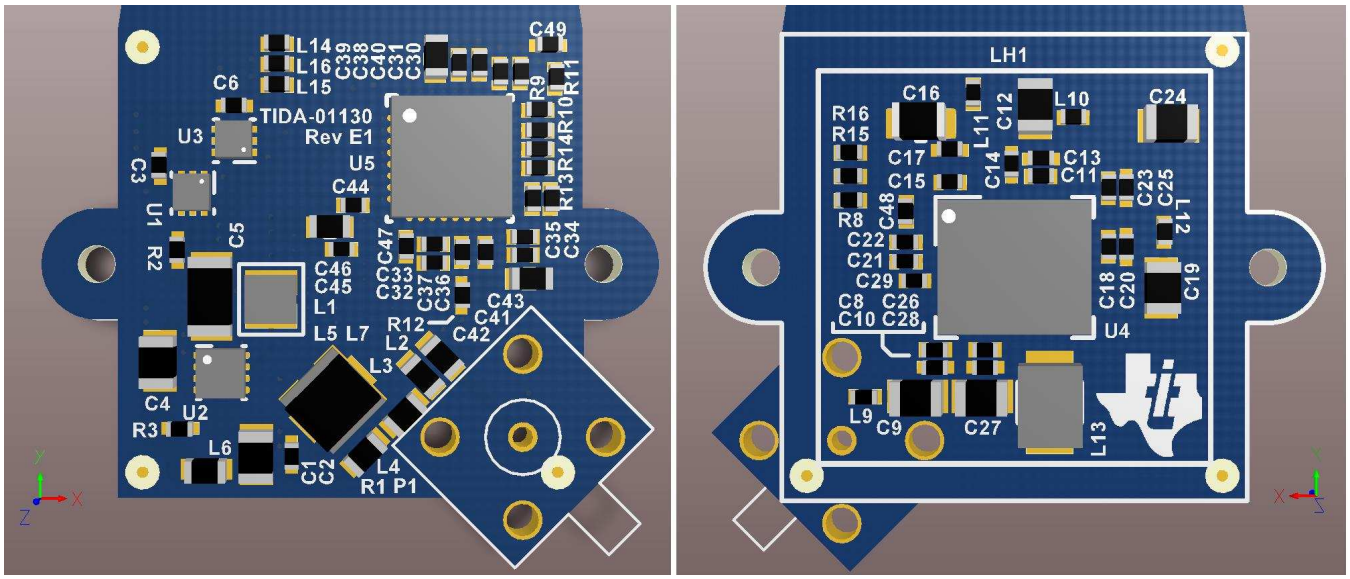


図 3. PCB Top and Bottom Views

2.3.2 Power Supply Design

2.3.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB953 and DS90UB954 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC.

For the POC design, to enable the forward channel and backchannel to pass uninterrupted over the coax, an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 10-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2.2-GHz frequency band. This complete filter is shown by L2 in 図 4. L1 would be the same but its POC filter for the deserializer side of the FPD-Link III transmission.

In this camera design, it is imperative that this filter has the smallest footprint. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the low end frequency and another for the high end.

For the high-frequency forward channel filtering, inductors usually are not sufficient to filter above 1 GHz. This reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore three ferrite beads instead of two allows for more headroom across the whole frequency band. Lastly, for good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized on board for the POC inductor filtering. For more details, see the *Sending Power Over Coax in DS90UB913A Designs Application Report*.

Lastly with regard to filtering is ensuring that the FPD-Link signal is uninterrupted just as much as power needs to be clean for the DC supplies. To achieve this, the AC coupling caps shown by the 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through but that the DC is blocked from getting on the data lines. Capacitive values for the DS90UB953/DS90UB954 pair are smaller than previous generations due to them need to pass 4Gbps of data versus the previous 2Gbps of data seen on 1-MP cameras.

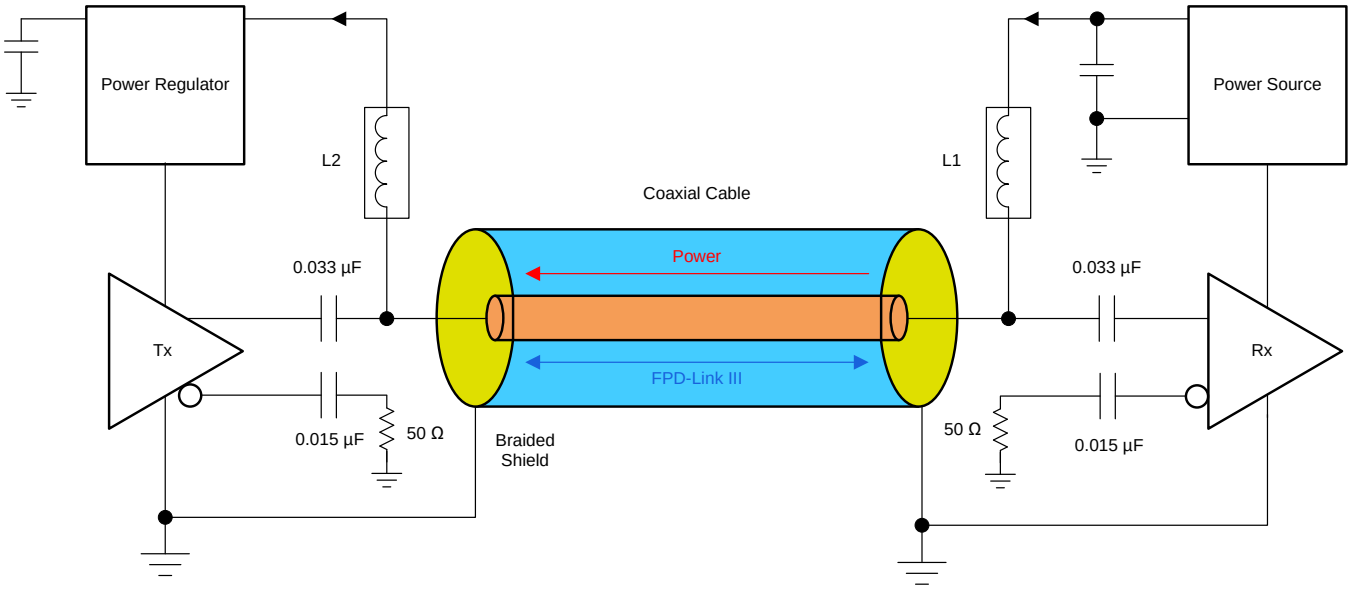


図 4. Power Over Coax

2.3.2.2 Power Supply Considerations

Because this reference design is targeted at automotive applications, there are a few considerations that constrict design choices. In addition, there are few systems-level specifications that shaped the overall design:

- The total solution size needs to be minimized to meet size requirement of this design, which is less than 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design looks at higher frequency switchers.
- All devices need to be AEC Q100-Q1 rated.

Before choosing parts, know the input voltage range, rails needed, and current required by each rail. In this case, the input voltage is a pre-regulated 12-V supply coming in over coax. This system has only two main devices, which consume the majority of the power. The requirements for each supply on these devices are shown in 表 2:

表 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (MAX) (A)	POWER (MAX) (W)
DS90UB953			
VDD	1.8	0.156	0.2810
OV2775			
VDD-1.3	1.3	0.227	0.2950
VDD-1.8	1.8	0.017	0.0306
VDD-3.3	3.3	0.020	0.0660
RAIL TOTAL			
1.3-V rail	1.3	0.227	0.2950
1.8-V rail	1.8	0.173	0.3110
3.3-V rail	3.3	0.420	1.3860

Summing these values, the 3.3 V needs to be able to supply power to the OV2775 imager and also support 1.8-V and 1.3-V rails. The 3.3-V rail requires 420 mA, the 1.8-V rail requires 173 mA, and the 1.3-V rail requires 20 mA.

Because the input and output voltages, output current requirements, and total wattage consumption are known, calculate what the input currents will look like with 式 1:

$$P_{OUT} = P_{IN} = I_{IN} \times V_{IN} \rightarrow 673\ mW = I_{IN} \times 12\ V \rightarrow I_{IN} = 56.1\ mA\ (max) \quad (1)$$

These numbers give a good starting point for selecting the parts and topology for the regulators as well as inductor selections later on. However, this does not take into account the efficiencies of the power supplies.

As previously mentioned, the parts in the power supply need to be Q100 rated, switch outside the AM band, and satisfy the voltage and current requirements as listed. Because the input voltage is a regulated voltage that will always be greater than any of the power rail needs, only choose from step-down converters and LDOs.

The key feature of the system is the small size, so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback, can significantly reduce total solution size. Many buck regulators integrate everything but the input/output caps and the inductor into very small packages. High integration also loses a lot of efficiency across different operating points. However, this reference design sacrifices some efficiency for size and simplicity reasons.

Ultimately, two device families are good candidates, the TPS621x0 switcher (TPS62172 for the 3.3-V rail) and the TLV702xx LDO (TLV70213 and TLV70218, fixed 1.3-V and 1.8-V options).

Clearly the largest trade-off with using LDOs is that the efficiency drops significantly, raising the total power draw. This reference design is a lower-power design; however, in some situations a designer may sacrifice the efficiency to avoid the inherent noise and EMI issues associated with switching power supplies. Also with the TLV702 LDOs, these are very small in 1.5-mm×1.5-mm package and do not require an inductor like a switching converter does.

Ultimately, this reference design uses the TPS62172 cascaded with the TLV70213 and TLV70218. Functionally, the cascaded topology means that the output current is sufficient such that the TPS62172 does not operate in discontinuous mode, allowing better predictions and control of the switching noise produced by the devices, and operate with better efficiency.

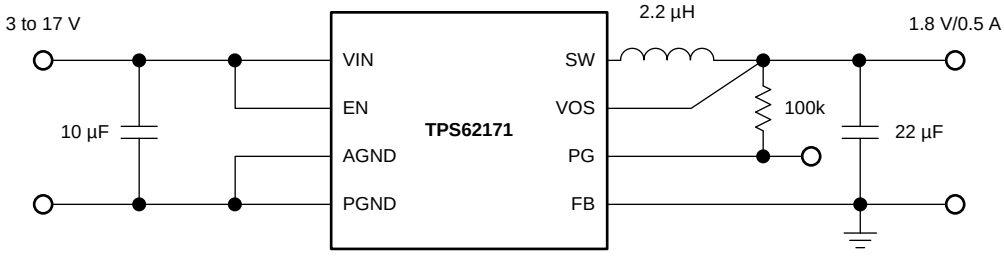


図 5. Typical Application Circuit

Component selection and design theory can be found in the Application Information section of the device datasheet[2].

2.3.2.2.1 Choosing the Output Inductor

As mentioned in 2.3.2.2, the switching frequency of the converter must remain above 2 MHz. This means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using 式 2:

$$L = \frac{\left[V_{OUT} \times \left(V_{IN} - V_{OUT}\right)\right]}{\left(2 \times V_{IN} \times I_{OUT} \times f\right)} = \frac{\left[3.3\ V \times \left(14\ V - 3.3\ V\right)\right]}{\left(2 \times 14\ V \times 0.42\ A \times 2.1\,MHz\right)} = 1.43\ \mu H \quad (2)$$

Because 1.43 µH is not a standard value and the design must use an inductor value above this, a higher value of 2.2 µH is chosen.

2.3.2.2.2 Choosing the Output Capacitor

Because the device is internally compensated, it is only stable for certain component values in the LC output filter. The application note on optimizing the output filter[6] has the chart of stable values shown in 表 3. The value 2.2 µH is on this chart and with these recommended values, this reference design uses a 22-µF output capacitor and remains in the stable region of effective corner frequencies.

表 3. Stability versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES (kHz)								
0.47 µH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 µH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 µH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 µH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 µH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 µH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8

	Recommended for TPS6213x/TPS6214x/TPS6215x/TPS6216x/TPS6217x
	Recommended for TPS6213x/TPS6214x/TPS6215x only
	Stable without Cff (within recommended LC corner frequency range)
	Stable without Cff (outside recommended LC corner frequency range)
	Unstable

With the inductance value chosen, the design now needs an inductor with a proper saturation current. This is going to be the combination of the steady-state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current (from the TLV7021x-Q1 data sheet[2]) using 式 3:

$$\Delta I_L = V_{OUT} \times \frac{\left(\frac{1 - V_{OUT}}{V_{IN}}\right)}{\left(L \times f_{SW}\right)} \tag{3}$$

The parameters for this reference design using the TPS62172 are:

- V_{OUT} = 3.3 V
- V_{IN} = 14 V
- L = 2.2 µH
- f_{SW} = 2.25 MHz

These parameters yield an inductor current of ΔI_L = 510 mA. The maximum current draw of the system through this regulator is 420 mA. Finally, 式 4 gives the minimum saturation:

$$L_{SAT} \geq \left(I_{MAX} + \frac{I_{RIPPLE}}{2}\right) = \left(420\ \text{mA} + \frac{510\ \text{mA}}{2}\right) = 675\ \text{mA} \tag{4}$$

This reference design uses a Coilcraft® XPL2010-222MLB, which has a saturation current of 940 mA and with a 10% drop-in inductance. This part comes in a very small 1.9-mm × 2.0-mm package.

2.3.2.3 TLV70218-Q1 and TLV70213-Q1

These LDOs are a bit simpler to design with as they do not require any output inductor. The only considerations for these LDOs are sizing the input and output capacitance. For the input capacitance, a capacitor is not required for stability but for improved transient response performance a 0.1-µF effective capacitance is recommended. The output capacitor requires a minimum effective capacitance of 0.1 µF for stability. In both cases, the input and output capacitor can benefit from using a 1-µF X5R/X7R capacitor so that when experiencing derating, they will be above 0.1 µF.

3 Hardware, Testing Requirements, Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in 図 6.

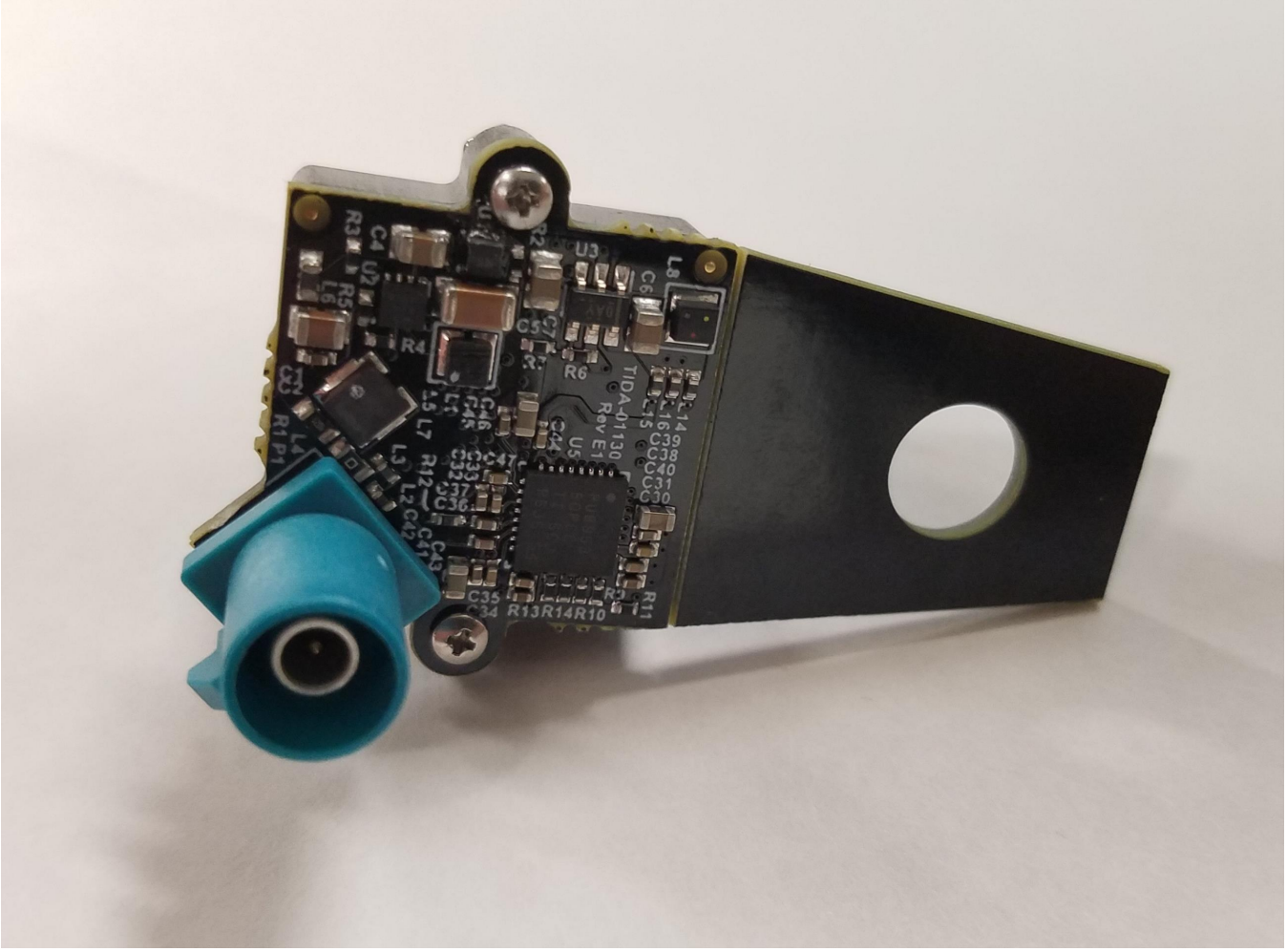


図 6. Getting Started With Board

3.1.1 Video Output Hardware Setup

図 7 shows the setup to test the video output of the camera module on this reference design. This reference design includes an OV2775 image sensor, which connects to the DS90UB953 serializer over CSI-2 and I²C interfaces. The DS90UB953 serializer then connects through POC to a DS90UB960 quad deserializer. Note that for test setup, only one channel is used from the DS90UB960.

To enable video output from the DS90UB960, the EVM is connected to the CSI-2 Samtec connector on the TDA3x EVM. The TDA3x EVM enables video output by writing all the backchannel I²C setting configurations for the OV2775, DS90UB953, and DS90UB960. When these writes are completed, Vision SDK software enables video output to an HDMI connected monitor.

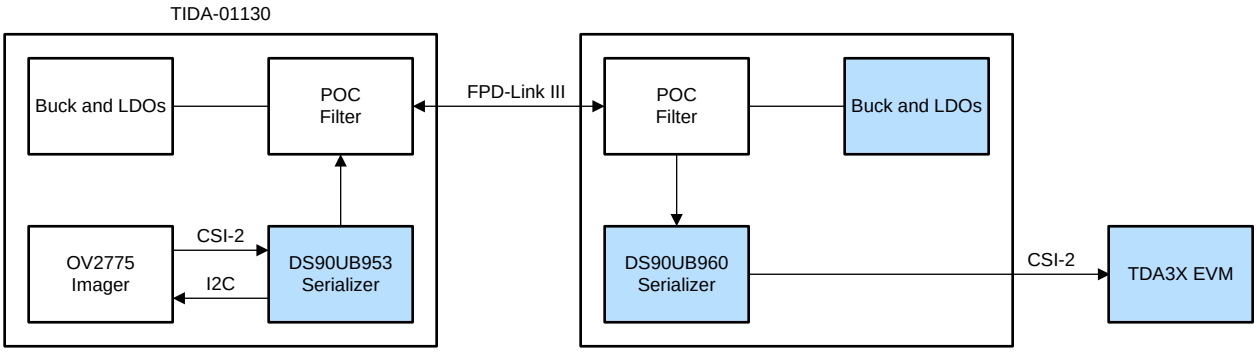


図 7. Block Diagram of Video Output Setup

3.1.2 FPD-Link III I²C Initialization

With the setup in 図 7 connected, the TIDA-01323 design is supplied input power and this is delivered to the POC supply for the camera power of this reference design and also is used to step down to 1.8 V and 1.1 V for the DS90UB960 supplies. Now the OV2775, DS90UB953, and DS90UB960 have power. Lastly, by connecting the TDA3x EVM to the TIDA-01323 design, the I²C writes for initialization can begin. Note that the following writes are only showing one channel camera and may not be the mode wanted for specific multi-camera mode. For example, each camera requires its own port initialization using address 0x4C for that specific port. The writes to initialize the deserializer and serializer are as follows:

- Deserializer slave I²C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x5E: I²C passthrough enabled and backchannel frequency select
  - Register 0x5C with 0x30: Sets serializer Alias to 30
  - Register 0x5D with 0x6C: Sets slave ID for imager to 6C
  - Register 0x65 with 0x6C: Sets slave alias for imager to 6C
  - Register 0x6D with 0x7C: Configures port to coax mode and FPD III to CSI mode
  - Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
  - Register 0x33 with 0x01: Enables 960 CSI output and sets to 4 lane mode
  - Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
  - Register 0x20 with 0x00: Forwarding enabled for all ports and ports forwarded to CSI-2 Port 0
- Serializer slave I²C address 0x30 (8-bit) or 0x18 (7-bit):

- Register 0x06 with 0x41: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from 953 to OV2775
- Register 0x07 with 0x28: Sets DIV_N_VAL for CLKOUT from 953 to OV2775
- Register 0x0E with 0xF0: Sets GPIOs on 953 as outputs
- Register 0x0D with 0x00: Drives GPIOs from 953 low to force imager PWDN and RESET pins low
- Register 0x0D with 0x0C: Pulls PWDN and RESET pins on OV2775 high to bring imager out of reset

3.1.3 OV2775 Initialization

Once the FPD-Link III setup is done for the DS90UB953 and DS90UB960, the I^2C initialization can now be done on the OV2775. For these writes, see the OV2775 data sheet for register settings. There are many register settings listed, but as long as the 953 and 960 FPD-Link III parts are configured, the I^2C backchannel allows for the OV2775 to be accessed at address 0x6C in 8-bit addressing or 0x36 in 7-bit addressing.

3.2 Testing and Results

3.2.1 Characterization Test Setup

For the following tests to verify power supply and I^2C communication, the camera is connected to a multiple camera surround view system (see 図 8).

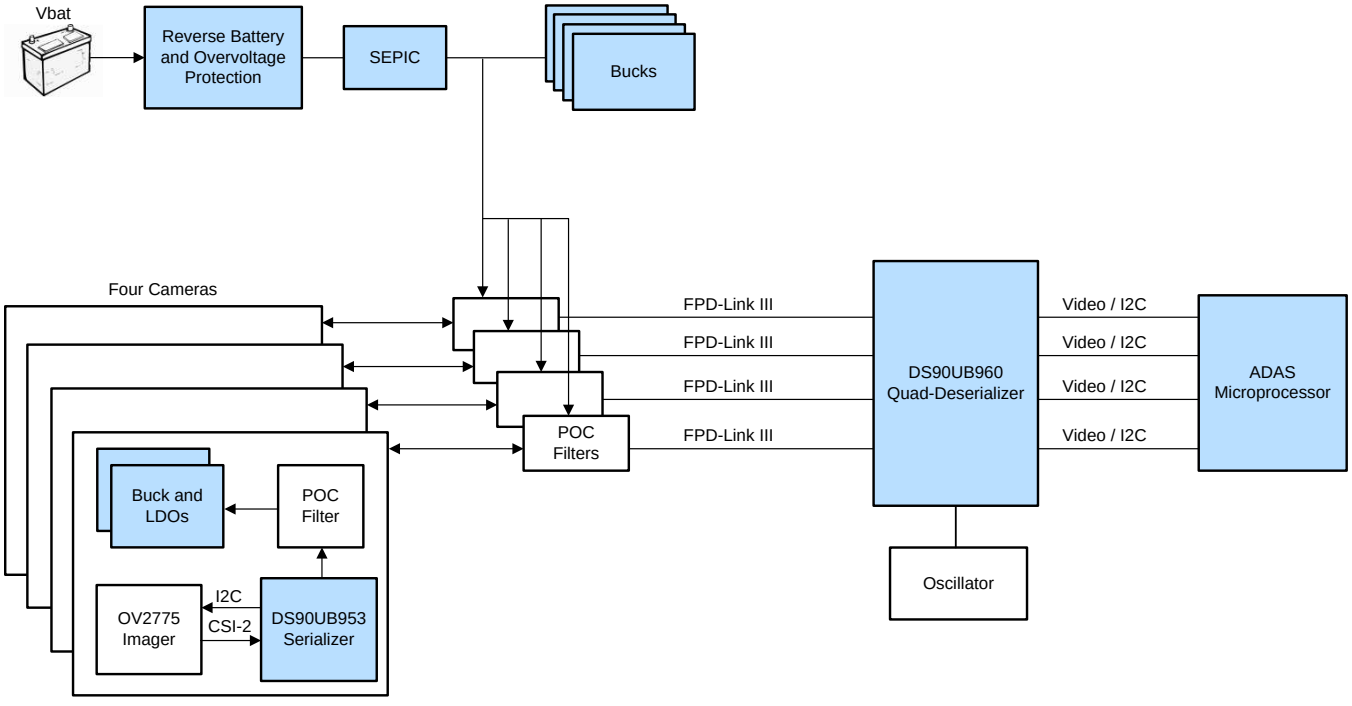


図 8. Block Diagram of Simplified Surround View

3.2.1.1 Power Supplies Startup

図 9 shows the probe setup to measure the power sequence turnon for the 12-V input from POC, 3.3-V supply to imager, 1.3-V supply to imager, and 1.8 V to the imager and serializer.

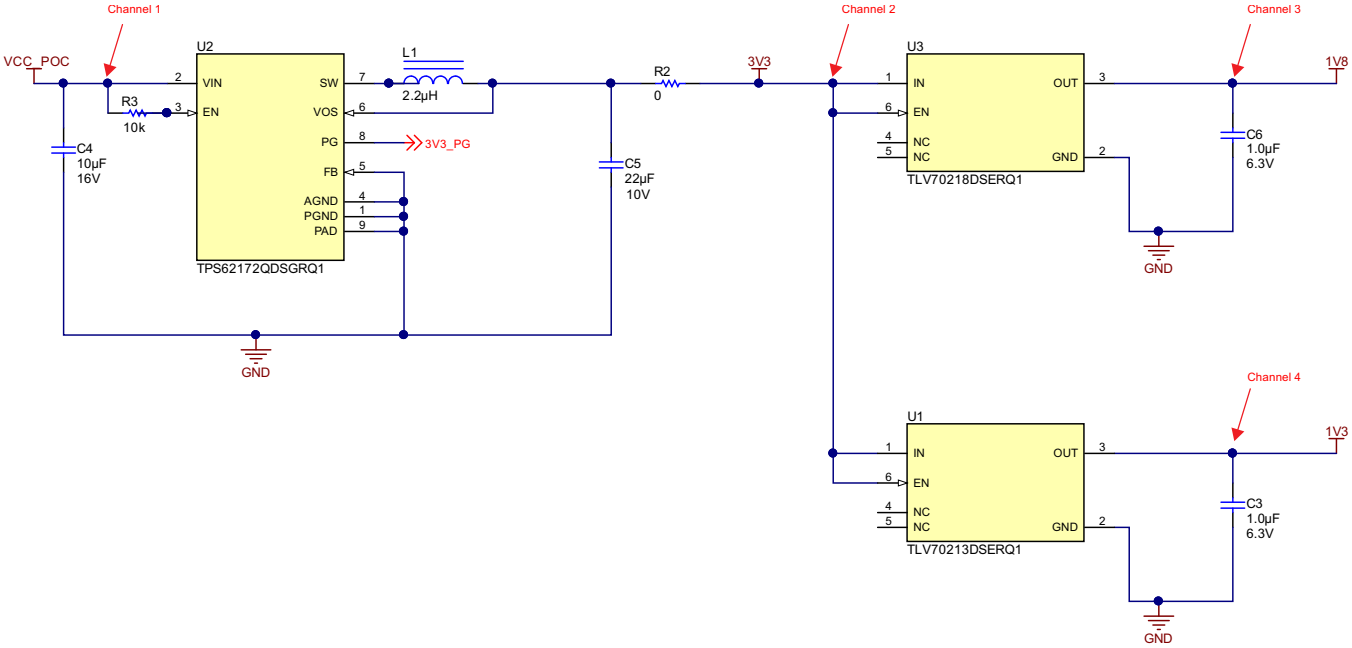


図 9. Measuring All Power Supplies

3.2.1.2 Power Supply Startup—1.8-V Rail and Serializer PDB Setup

For the serializer to be initialized after the 1.8-V power supply comes up, a RC time constant delay is added to the 3V3_PG of the TPS62172, which controls the serializer PDB so that PDB reset line goes high after all the supplies are high.

3.2.1.3 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Make connections to both the clock and data lines of each bus as shown in 図 10.

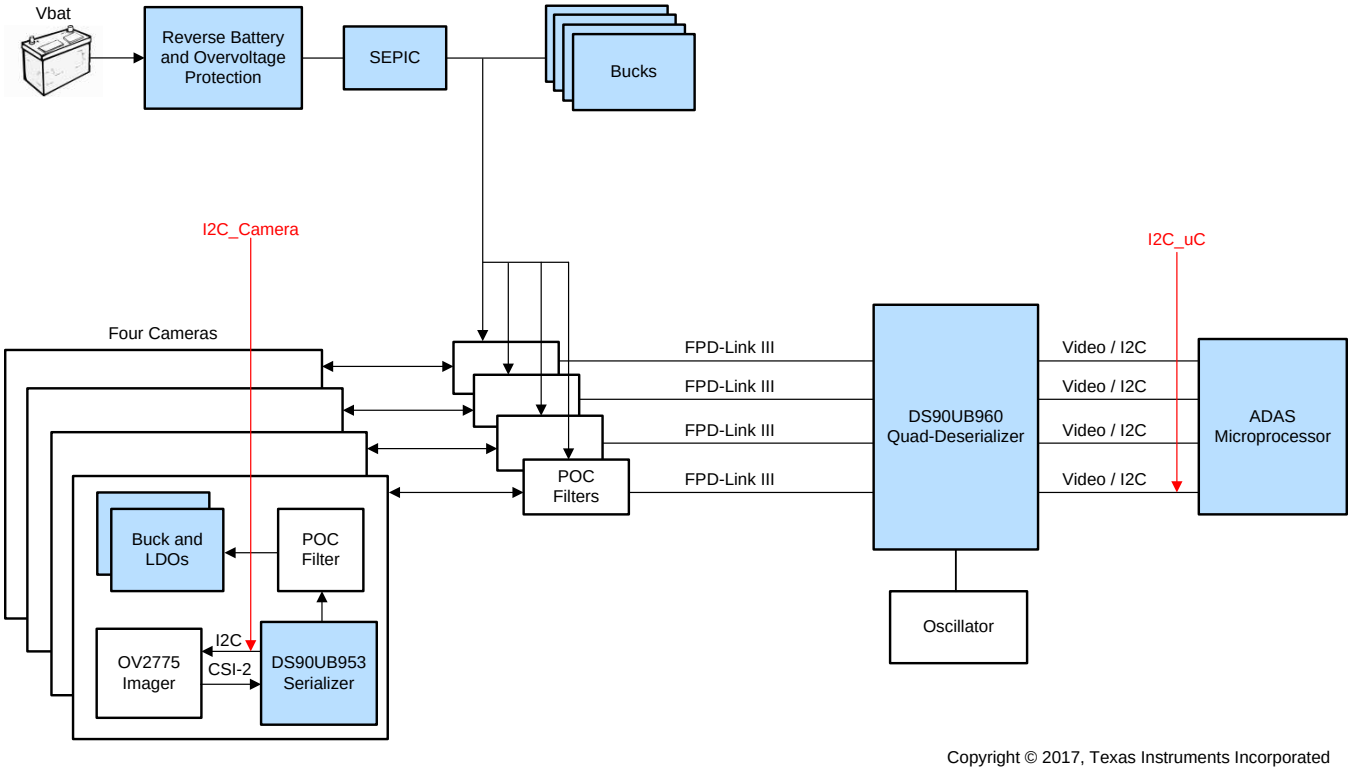


図 10. Setup for Monitoring I²C Transactions

3.2.2 Characterization Test Data

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Startup

Power startup behavior for the input power supply, 3.3-V, 1.8-V, and 1.3-V system supplies are shown in 図 11. The startup sequence shows that when the 12-V input reaches turnon voltage for the TPS62172, the 3.3-V supply starts turning on. The same behavior is exhibited for the 1.8-V and 1.3-V supplies, which start turning on when the 3.3-V output has reached 2 V, the minimum input needed for the TLV702-Q1 LDOs.

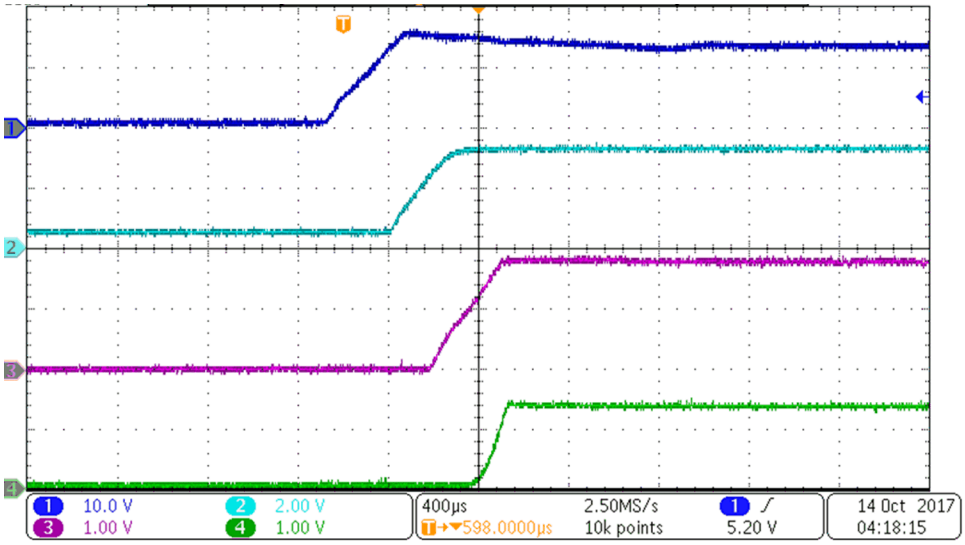


図 11. Power Supplies Startup

3.2.2.2 Power Supply Startup—1.8-V Rail and PDB

The only startup requirement is that the PDB pin of the serializer remains low until all power supplies stabilize to their final voltages. The power supply startup is shown in 図 12.

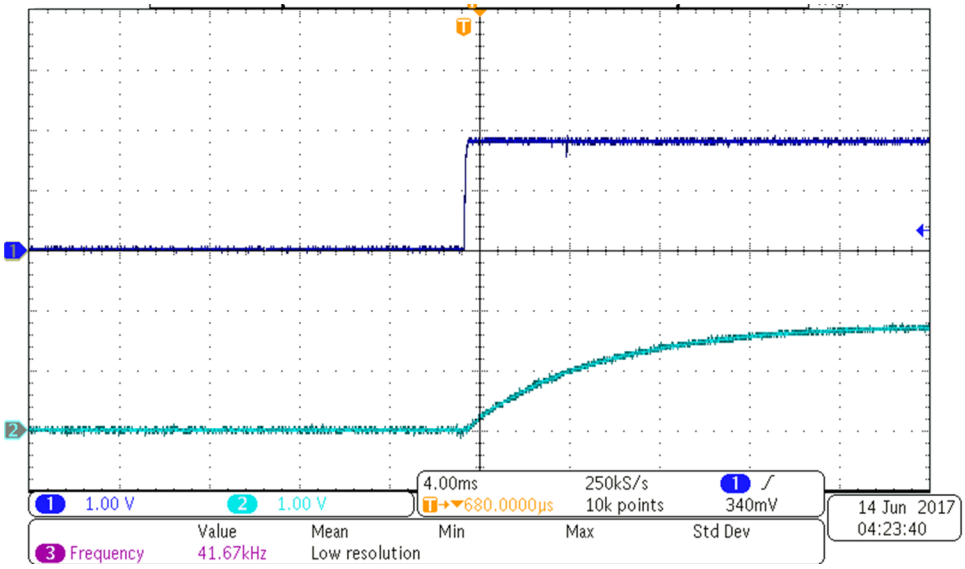


図 12. Serializer Power-Up Sequence

注: Channel 1 (blue) 1.8 V; Channel 2 (turquoise) PDB

図 12 shows that PDB comes to V_{DD} × 0.65 in 5 ms because of the 0.047-µF delay capacitor on the PDB pin. This 5-ms delay is sufficient for the PDB pin because 1.8 V and 1.3 V come up at the same time, and based on 図 12, 5 ms after those are up, PDB is registered as high.

3.2.2.3 Power Supply Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the OV2775 and DS90UB953 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. Measurements for 3.3-V, 1.8-V, and 1.3-V rails are shown in 図 13, 図 14, and 図 15, respectively. The key rails that are significant to impact on the imager are the 3.3-V and 1.8-V rails because 3.3 V is the analog rail and 1.8 V is the AVDD rail for the imager and serializer. As measured, the 3.3-V and 1.8-V rails have less than a 1% ripple. The 1.3-V rail has good ripple performance as well at 1.3%. This ripple on the rails is low enough for video output to be successfully transmitted.

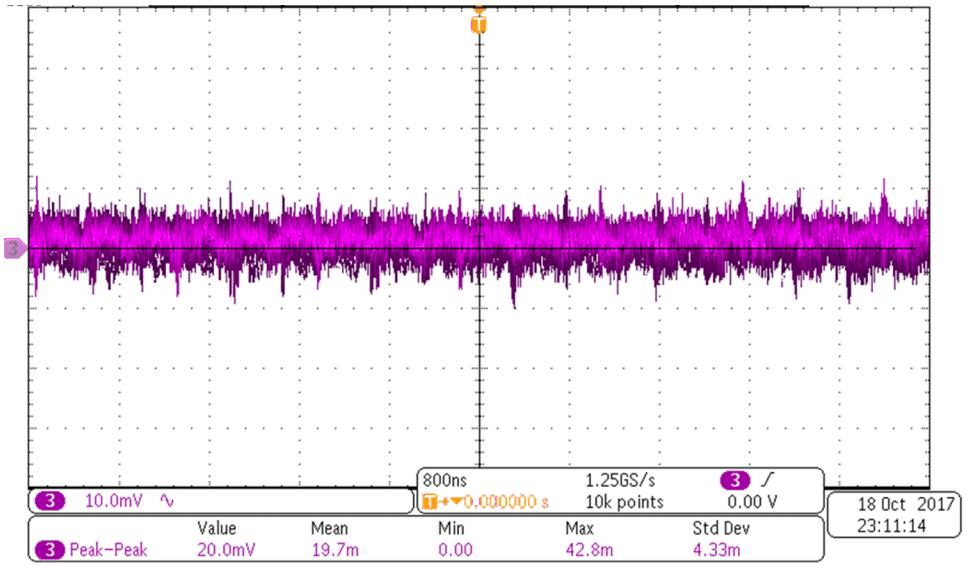


図 13. 3.3-V Output Voltage Ripple

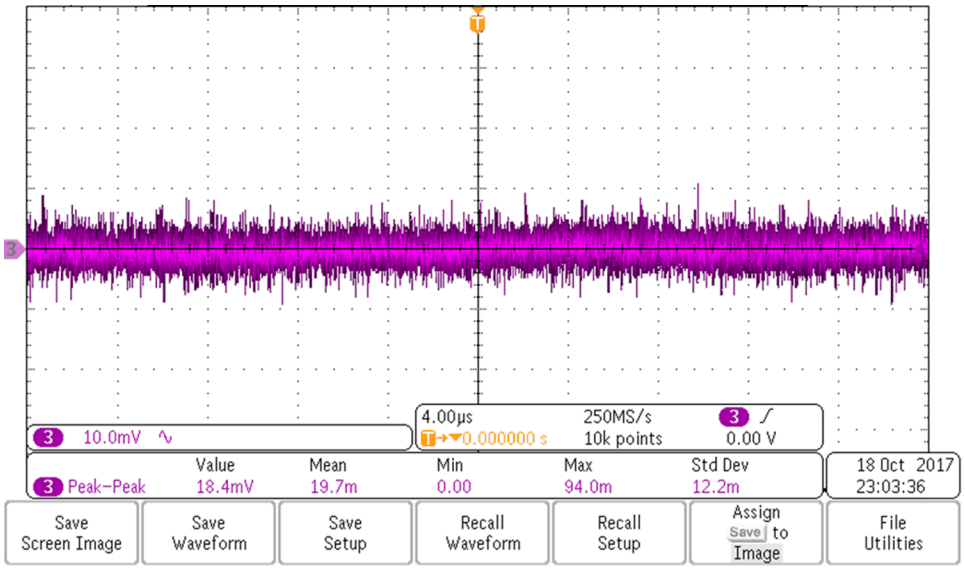


図 14. 1.8-V Output Voltage Ripple

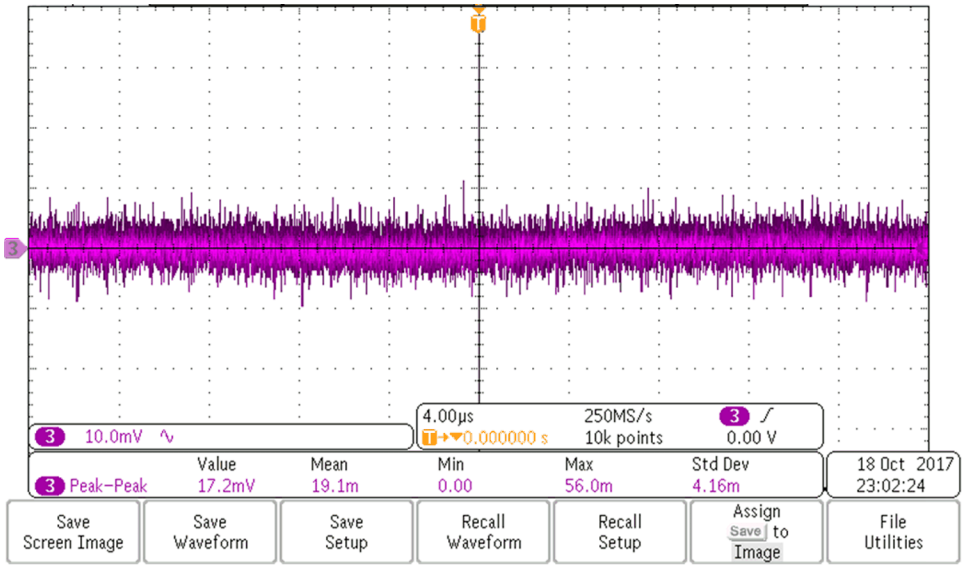


図 15. 1.3-V Output Voltage Ripple

3.2.2.4 Power Supply Load Currents

The last measurements to take in regard to the power supplies on the camera module are the load currents for the 12-V input supply. These measurements verify total power consumption of the camera module as well as the load current for each individual rail. For the following test data, each rail is drawing the specific load current outlined for serializer and imager. The 3.3-V rail for these testing purposes is only supplying current for the analog rail to the OV2775 instead of supplying power needed for 1.8 V and 1.3 V. This allows one to confirm each individual load draw on the imager and serializer. Note that all load current measurements are taken while a video output stream is present.

図 16 and 図 17 shows the 12-V and 3.3-V load currents measured on this reference design. The 12-V load current is the total input load for the camera module and measures at 55 mA. With this amount of current, the total input power consumption of the camera module is 660 mW. The 3.3-V analog rail on the OV2775 is measured to be drawing 16.1 mA.

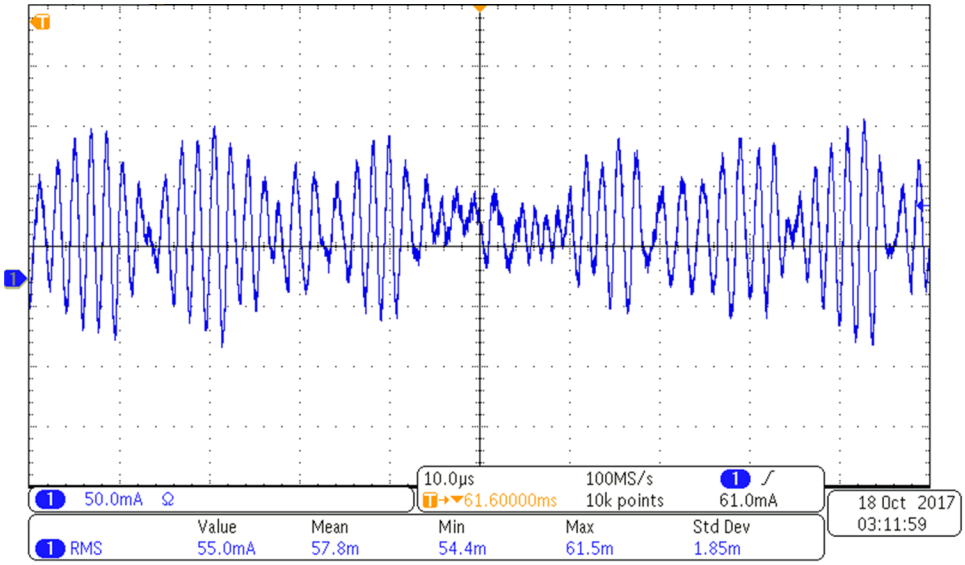


図 16. 12-V Input Load Current

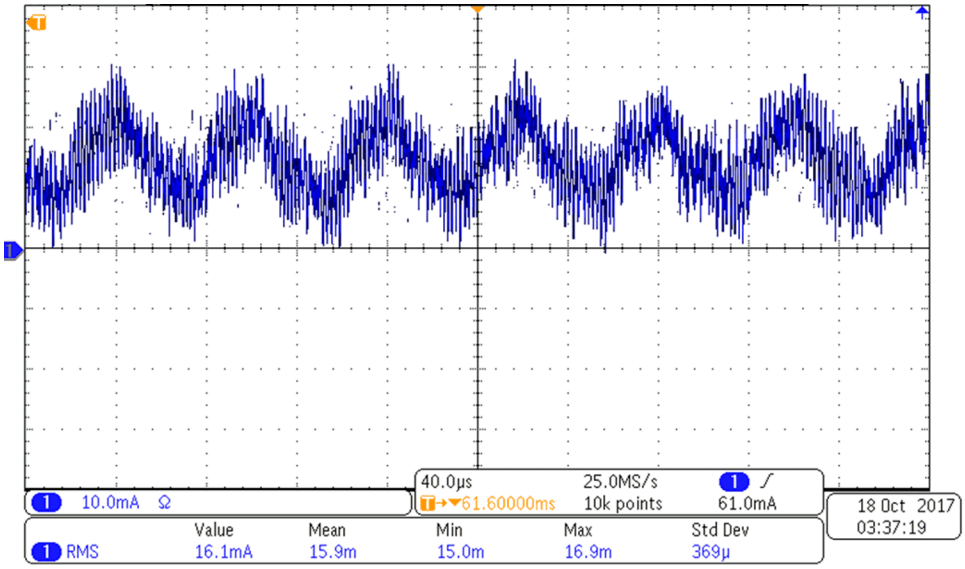


図 17. 3.3-V Output Load Current

図 18 and 図 19 show the measurements for the 1.8-V and 1.3-V load currents, respectively. The 1.8-V load supplies power for both the OV2775 and the DS90UB953. The 1.3-V load only supplies power to the digital circuitry of the imager. For these rails, the 1.8-V load is consuming 117 mA and the 1.3-V load is consuming 107 mA.

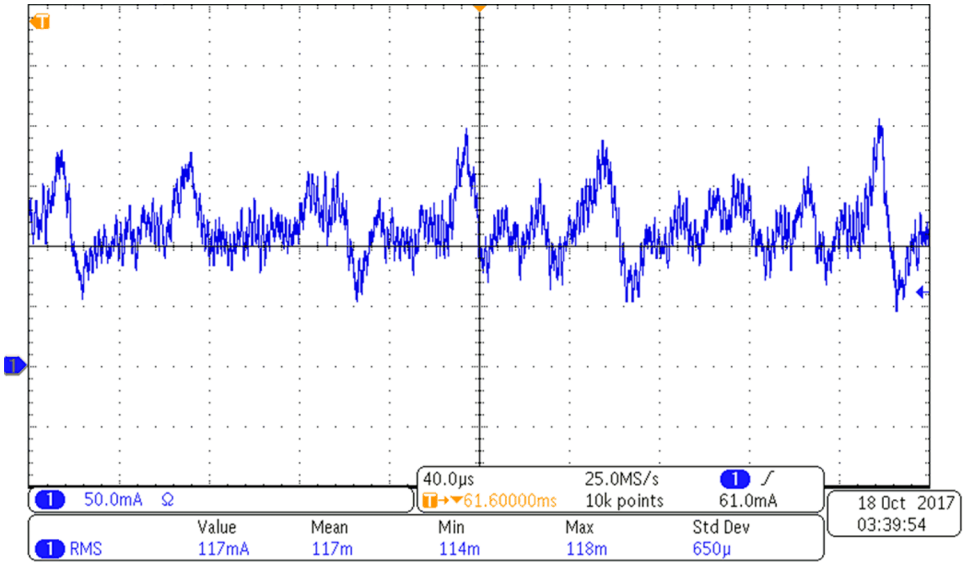


図 18. 1.8-V Output Load Current

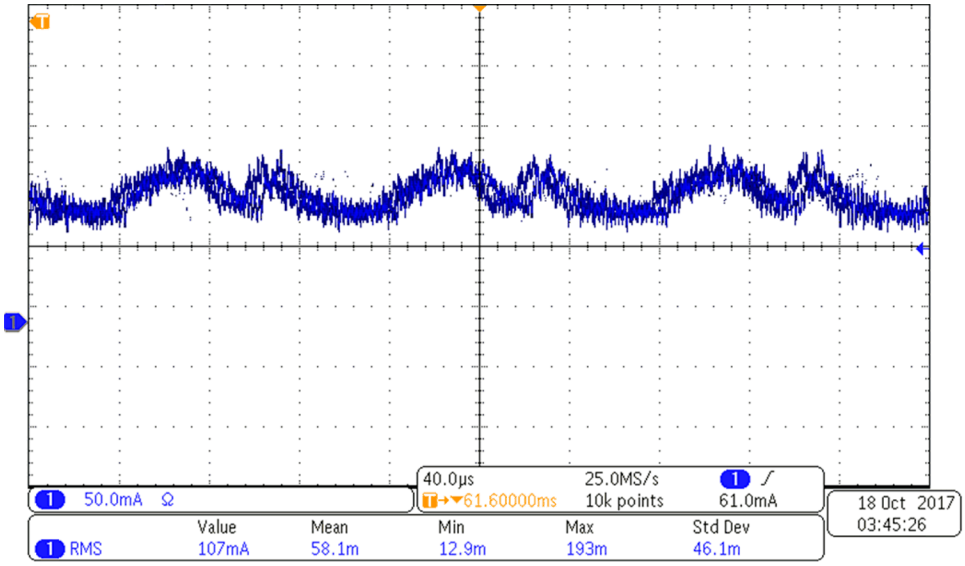


図 19. 1.3-V Output Load Current

Taking into account all output voltages and output currents gives an estimate for the system efficiency of the camera module. The input power already mentioned is 660 mW. For the output power, using measured voltages of 3.32 V, 1.84 V, and 1.31 V on the board and 16.1 mA, 117 mA, and 107 mA, the total output power is 409 mW. To calculate system efficiency, the output power is divided by the input power to get 62%. With two LDOs and a buck switcher, 62% is reasonable. As discussed, this design targets a small solution size using fixed voltage LDOs. If efficiency is key, consider replacing LDOs with switchers to increase efficiency.

3.2.2.5 I²C Communications

Now that the power supplies are up and running, the I²C communication between the processor and the OV2775 over the FPD-Link III backchannel can be confirmed. 図 20 shows a read I²C communication from the TDA3x EVM to the OV2775 on this reference design.

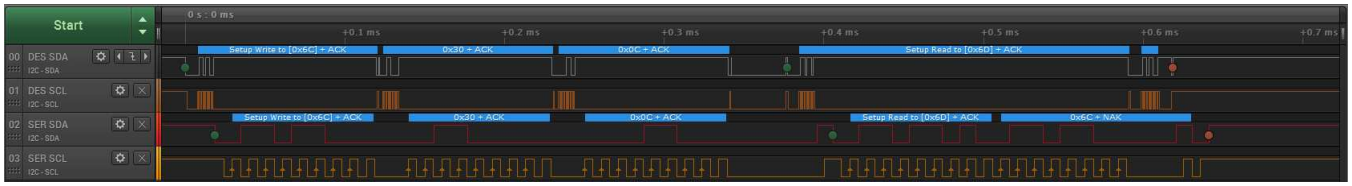


図 20. I²C Transactions

Channel 00 and 01 is the read I²C transactions at the processor and is measured at the deserializer side between the host microprocessor and the DS90UB960. The read is to the imager, which is at slave alias address 0x6C. The read to the imager is for its register 0x300c with data 0x6C, which is the register that confirms the slave ID of the imager is in fact correct.

Channel 02 and 03 are the I²C transactions at the camera, measured on the reference design SCL and SDA lines connecting the DS90UB953 and the OV2775. This shows that the read initiated from the master and measured at the deserializer is successfully getting across the FPD-Link III connection and reading the imager on the camera module.

By acknowledging the I²C read, the imager has confirmed that it is present and at the correct slave address.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01130.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01130.

4.3 PCB Layout Recommendations

4.3.1 Switching DC/DC Converters

During part placement and routing, it is helpful to always consider the path current will be taking through the circuit. The green line in 図 21 shows the current path from the coax in through the POC filter, inductor L5, and capacitors C1 and C2, and then out to the ferrite bead, L6, input capacitor, C4, to U2, or the TPS62172-Q1. The yellow line follows the 3.3-V output of the switcher to the output inductor L1 and output capacitor C5. Any return currents from the input capacitor C4 or the output capacitor C5 are joined together at the top left of U2 before they are connected to the ground plane. This is shown inside the blue lines. This reduces the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

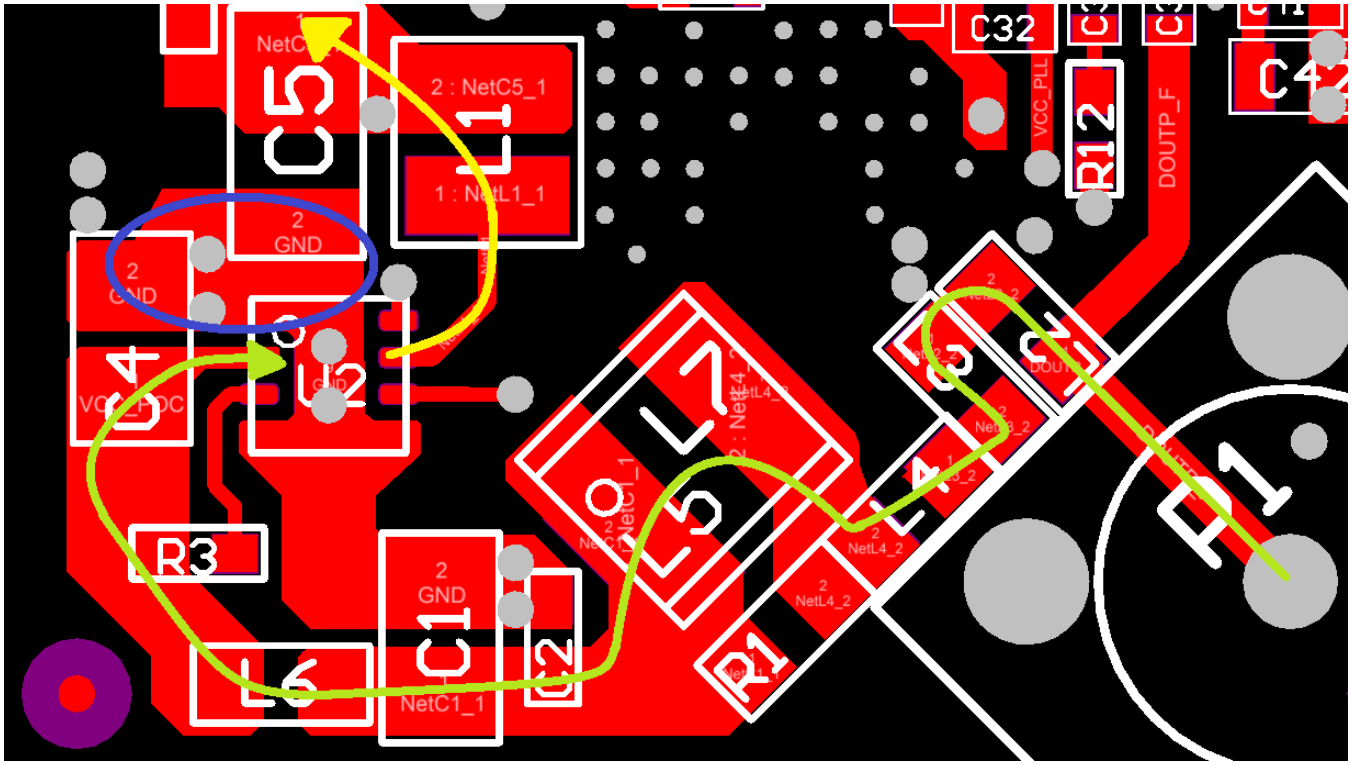
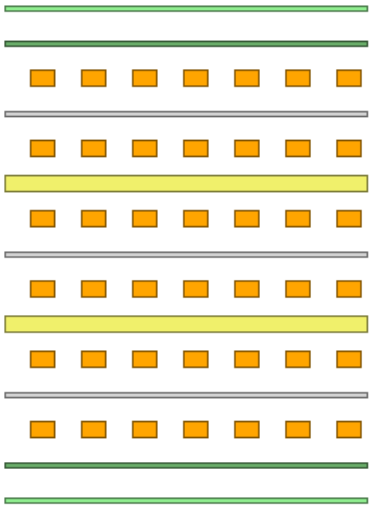


図 21. Routing FB Traces Around SW Nodes

4.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs:

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers are used in this board to simplify BGA fan out and routing. 図 22 shows the stackup used in this board:



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	16.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.417		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

図 22. Layer Stackup

4.3.3 Serializer Layout Recommendations

High-speed CSI-2 routing is an important design aspect for the DS90UB953 on this reference design. Layout considerations for trace impedance and length matching must be a high priority for good signal quality of the high-speed video data. For location of the CSI-2 traces, crosstalk can easily happen with high-speed signals, so it is important on this camera module design that the traces are away from the FPD-Link III RX traces to reduce coupling.

Trace impedance is one critical aspect to the CSI-2 lane routing. Route the differential pairs for CLK and DATA with a controlled 100-Ω differential impedance (±20%). For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specs, length specifications also need to be strict within the positive to negative differential pair length and pair to pair length. If the length is not matched, at these high data switching speeds, the data can arrive at the 953 at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. The vias must ideally be two or fewer to minimize stubs that cause reflections. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees. When these layout considerations are followed, the video data integrity can be maintained. If for any reason there are high-speed concerns on the CSI-2 lane design, debug tools are available to run video data over the 1, 2, or 4 lanes. The imager must be set to output over the specified number of data lanes, and the DS90UB953 can then be set to correct number of lanes in register 0x02.

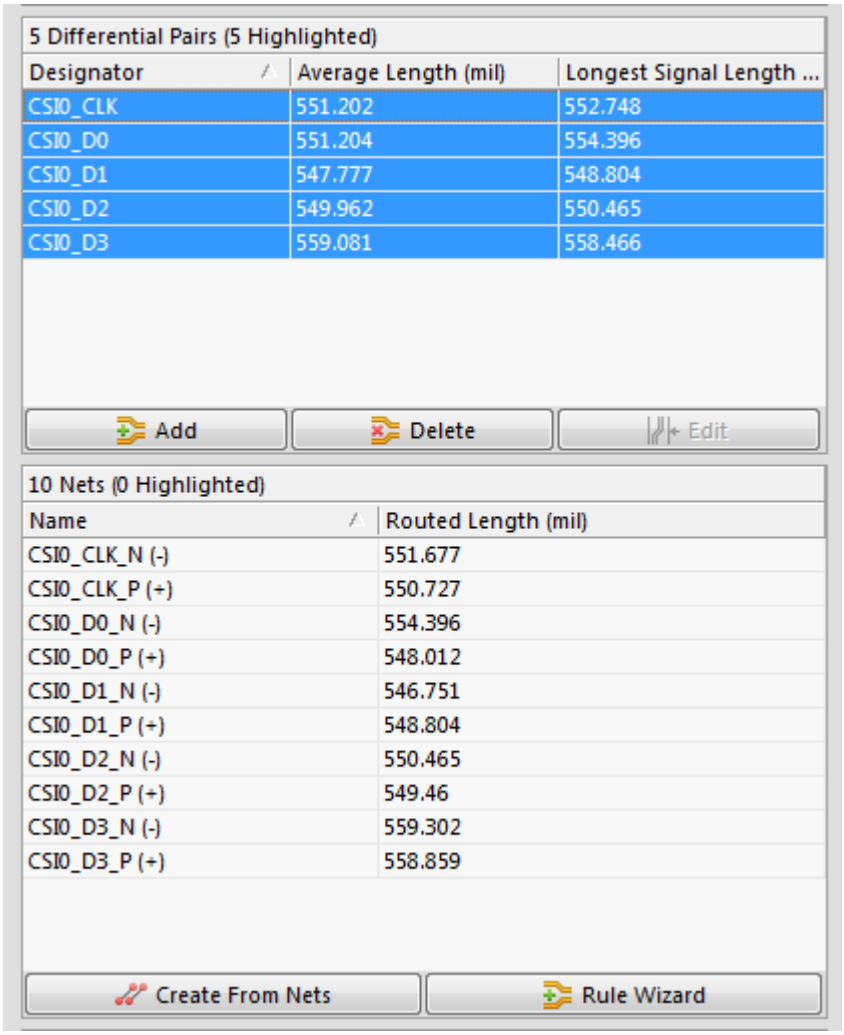


図 23. CSI-2 Differential Trace Routing

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

図 24 shows the supply current from C43 in yellow. The green line is the return path. The cross sectional area of this loop is very small.

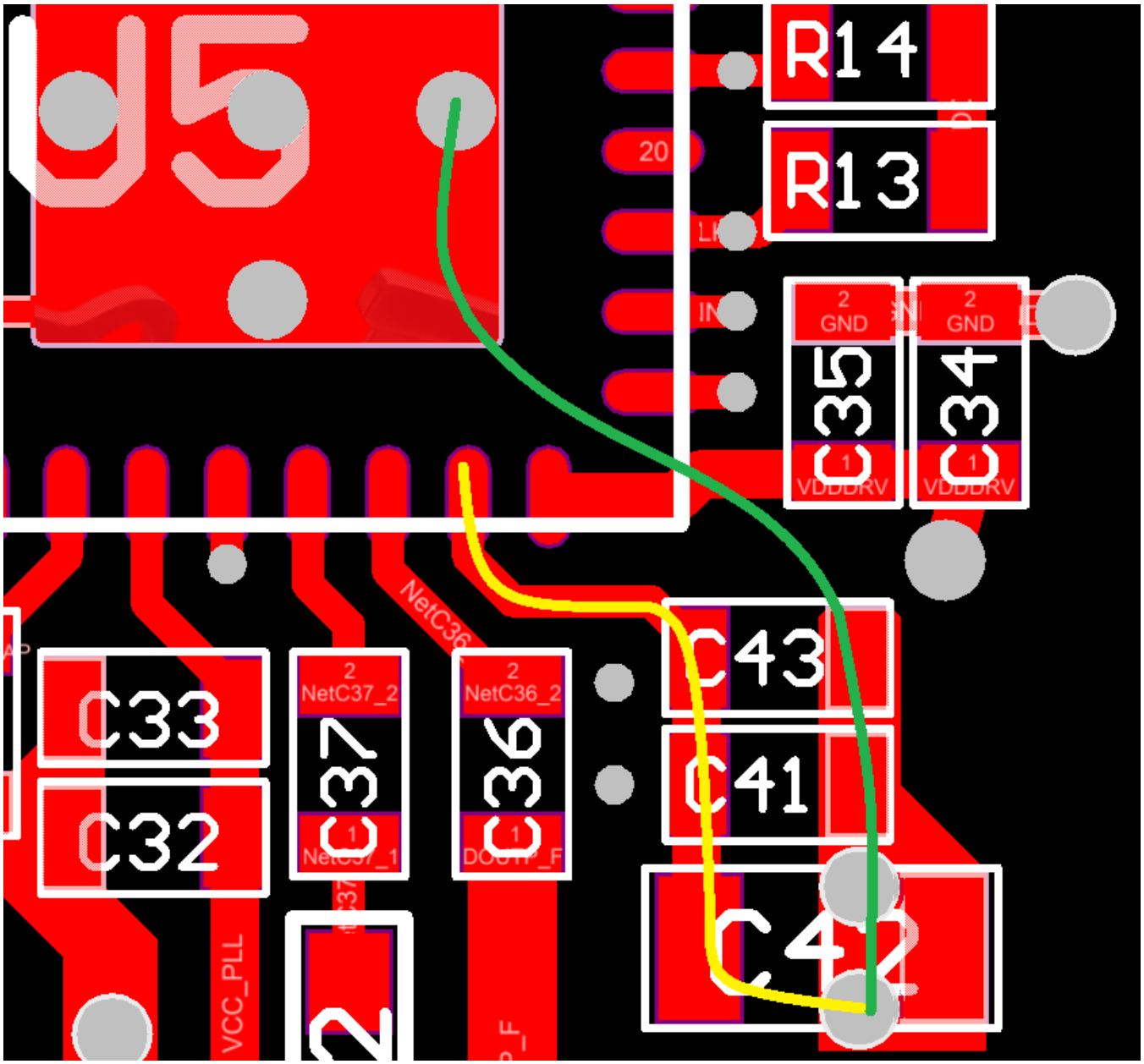


図 24. Decoupling Current Loop

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. The routing of the high-speed serial line is shown in 図 25, highlighted by the yellow line. The total length of the yellow line is about ½ inch.

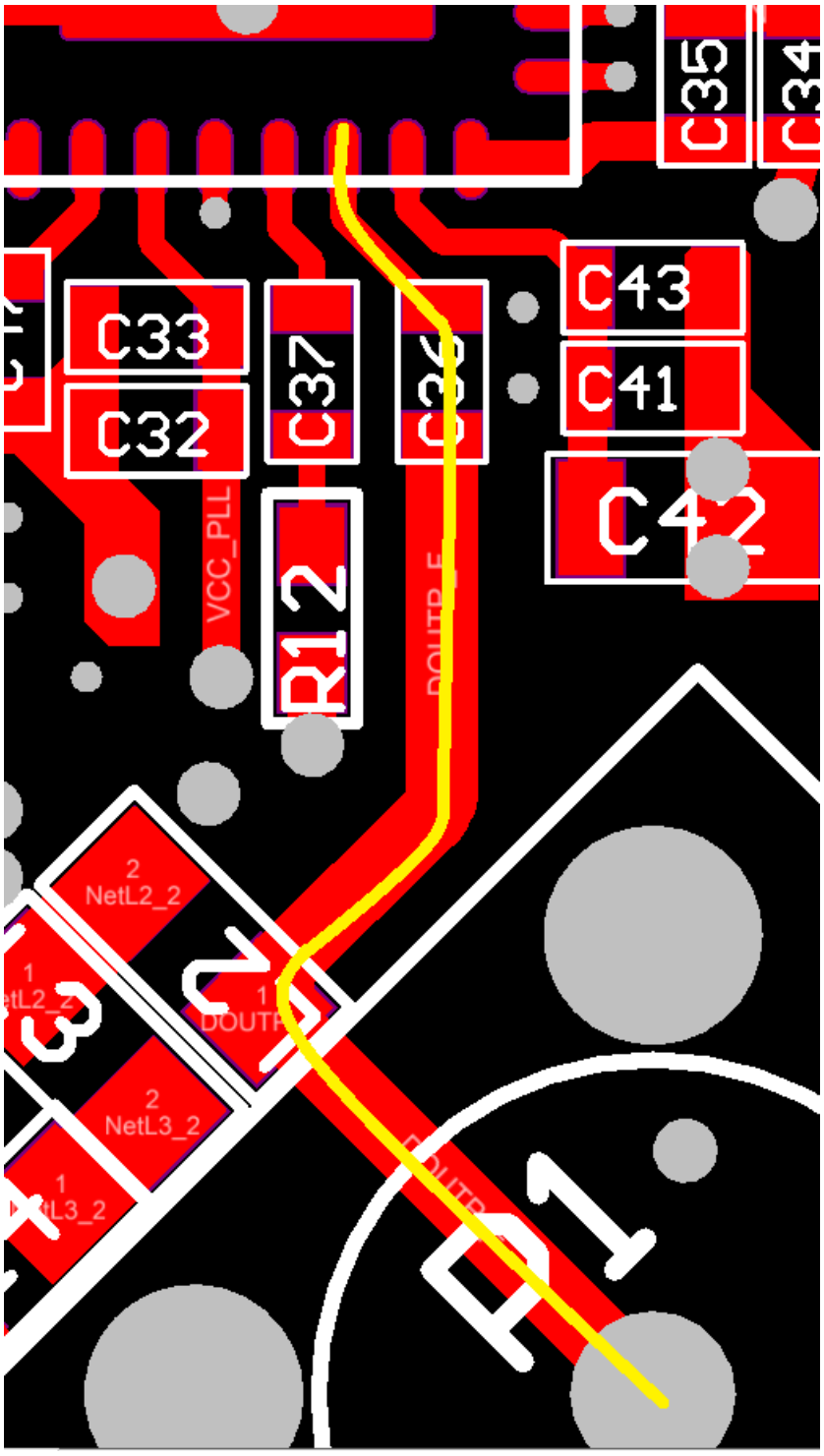


図 25. High-Speed Serial Trace

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01130.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01130.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01130.

5 Related Documentation

1. Texas Instruments, *DS90UB953-Q1 MIPI CSI-2 FPD-Link III Serializer for 2-MP/60-fps Cameras and RADAR Data Sheet*
2. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*
3. Texas Instruments, *TLV7021x-Q1 300mA, Low-Iq, Low-Dropout Regulator in 1.5x1.5mm WSON Package Data Sheet*
4. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*
5. Texas Instruments, *Cable Requirements for the DS90UB913A and DS90UB914A Application Report*
6. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter Application Report*

5.1 商標

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年11月発行のものから更新 **Page**

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