参考資料

TI Designs: TIDA-01458
超音波CWパルサー用低ノイズ、固定ドロップアウト、±2.5～±12V$_{OUT}$、3A電源のリファレンス・デザイン

概要

このリファレンス・デザインでは、デジタル的にプログラミング可能な電源を使用して、24Vバスから連続波(CW)モードの超音波送信回路に給電することができます。±2.5～±12Vの可変出力が2つあり、いずれもユーザー・ソフトウェアで制御されます。これらの出力は最大2Aを提供し、正負のレギュレータ出力でリップルとノイズを極めて低く抑えることができます。この電源は拡張性に優れており、レギュレータを並列追加して、出力電流を3Aまで引き上げることができます。また、電源を外部クロックと同期することも可能です。

リソース

TIDA-01458	デザイン・フォルダ
TIDA-01352	デザイン・フォルダ
LMR14050	プロダクト・フォルダ
LM73605	プロダクト・フォルダ
TPS7A47	プロダクト・フォルダ
TPS7A33	プロダクト・フォルダ
TLV2171	プロダクト・フォルダ
TL431A	プロダクト・フォルダ

TI E2E™ Community

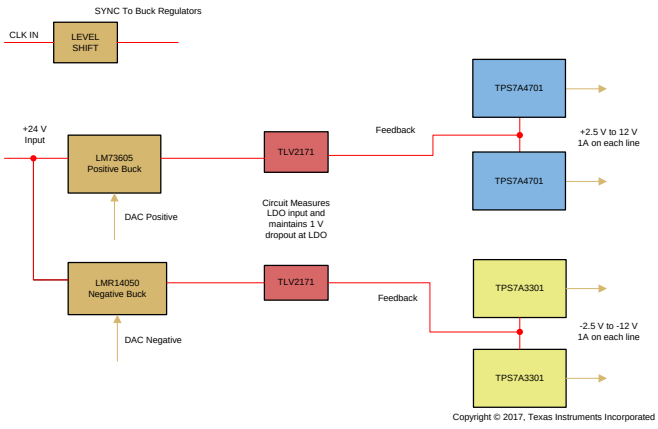
E2Eエキスパートに質問

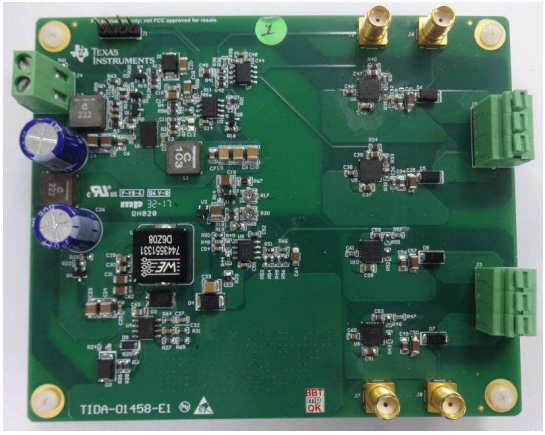
特長

- 超音波パルサーのCWモードに対応する、分離独立した正負電圧電源
- 2つの高性能な降圧レギュレータで構成され、可変出力を実現
- 出力時のリップルを低減するために、高性能かつ低ノイズのLDOがパワー・フィルタとして動作することにより、LDOの放熱を最小限に抑え、リップルを最低限に抑制(負荷1.6Aで100µV未満)
- LDOの適応型降下、特殊回路によりLDO出力を常にLDO入力より1V低く維持
  - LDOの消費電力を削減
- 超音波マスタまたはシステム・クロック周波数とのスイッチング周波数同期が可能
  - 高調波除去率の向上を支援
- モジュラー設計により、レギュレータ・ブロックの追加が可能

アプリケーション

- 医療用超音波スキャナ
- ソナー・イメージング機器
- 非破壊検査機器





1 System Description

This design guide describes a power supply for continuous wave (CW) mode. These typically need ±2.5 to ±12 V under software control. Budget a current delivery up to 3 A at outputs of DC-DC converters. In addition, the power supplies must have a very low level of ripple and noise at the output voltage.

1.1 Basic Ultrasound System

In an ultrasound system, the transmitter that generates high-voltage signals to excite a transducer is one of the most critical components in the entire ultrasonic diagnostic system. There are semiconductor devices available that can generate high-voltage signals to ensure the penetration depth of ultrasonic signals. A generic system-level block diagram for a cart-based ultrasound scanner is shown in 図 1.

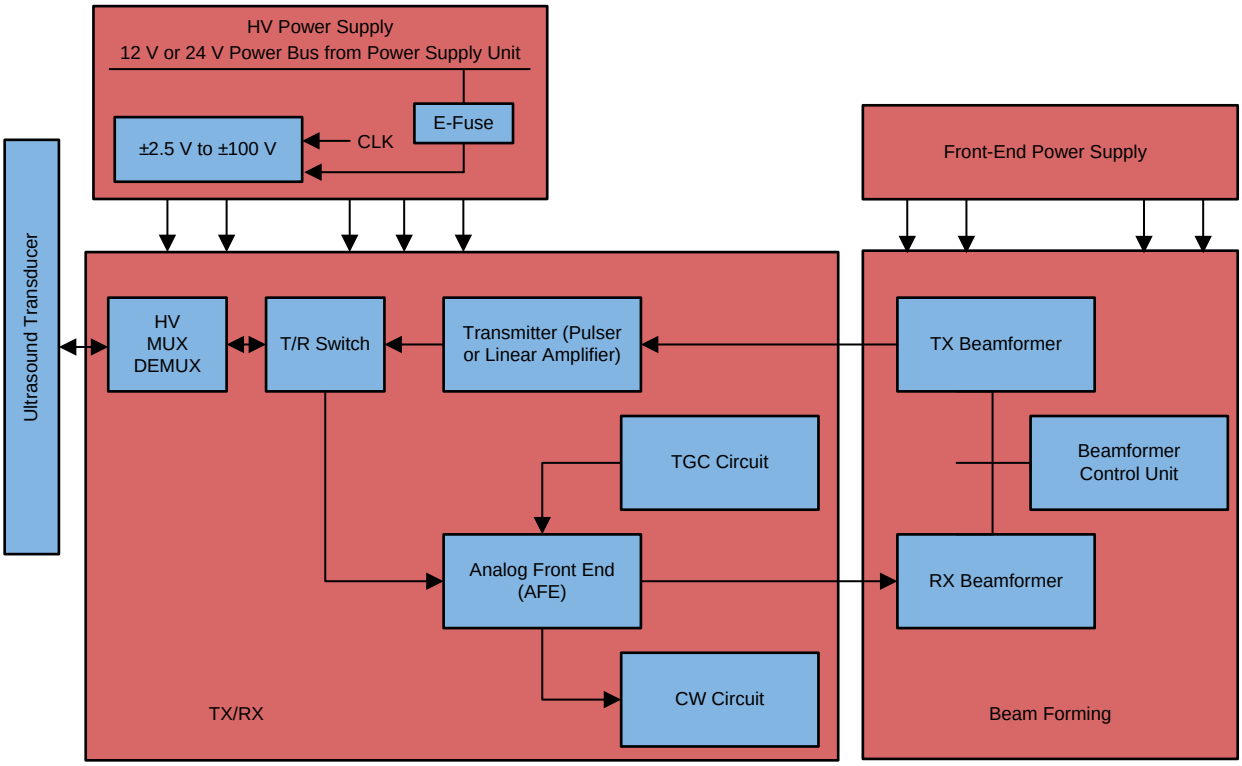


図 1. System-Level Block Diagram for Cart-Based Ultrasound Scanners

The high-voltage pulses (to be transmitted inside human body to get information about blood, organs, tissues, and so on) are bipolar in nature and are transmitted by transmitters (TXs). There are two modes in general:

1. Pulse (also known as brightness, or B) mode where high-voltage pulses (–100 V and 100 V, typically) are transmitted for a particular short time only.
2. CW mode where low-voltage (±2.5 to ±10 V, typically) pulses are continuously transmitted.

1.2 Key System Specifications

表 1 shows the key system specifications.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage (V_{IN})	24 V ±10%
V_{BUCK} positive output voltage range	2.5 to 12 V
Load current capacity positive buck	3 A
V_{BUCK} negative output voltage range	–2.5 to –12 V
Load current capacity negative buck	3 A
LDO (V_{IN}–V_O) drop across the LDO	1 V (adjustable through pre-set)
External clock synchronization	Yes
External sync frequency	400 kHz
LDO output current capacity	2 × 1 A positive
LDO output current capacity	2 × 1 A negative
Scalability	Yes

2 System Overview

2.1 Block Diagram

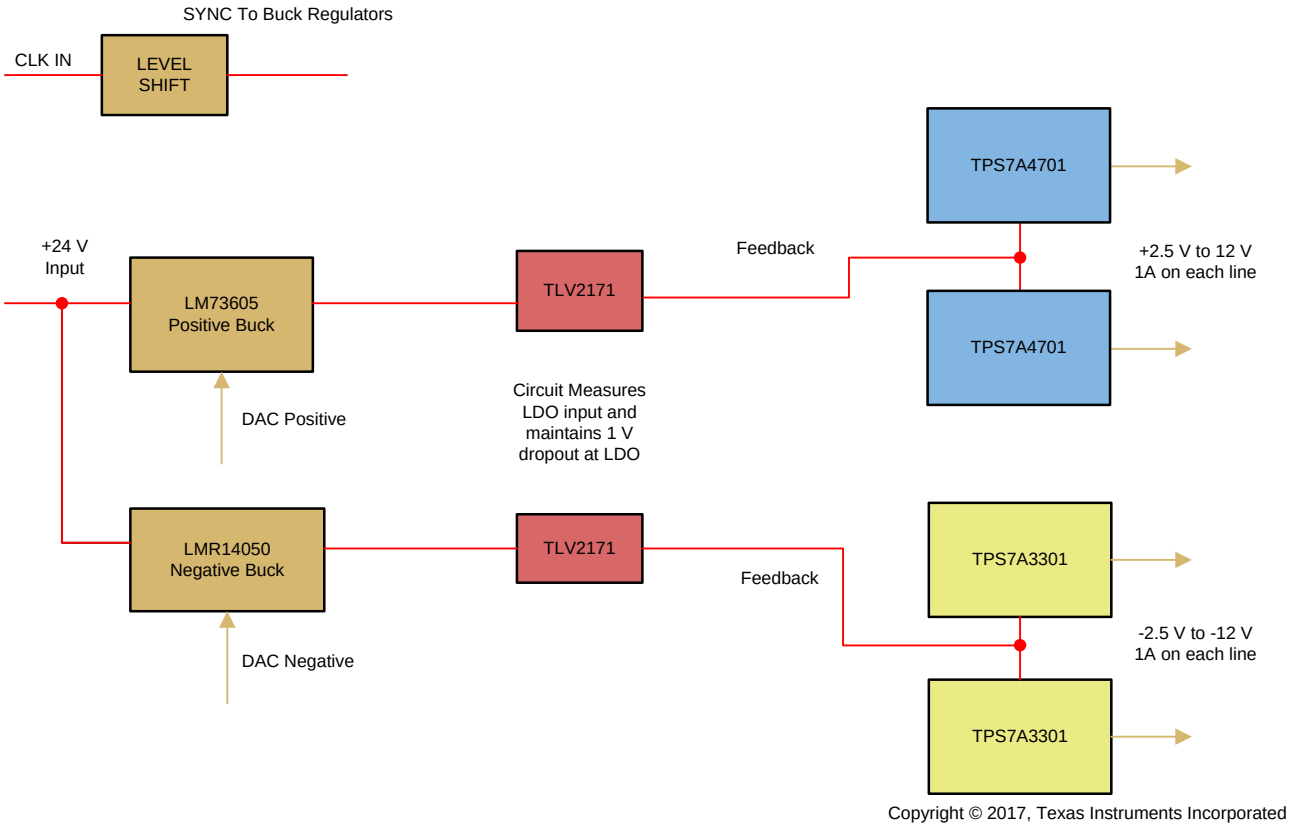


図 2. System Block Diagram

Positive Regulator Block

This reference design uses the LM73605 DC-DC converter as a synchronous buck regulator. The output is varied by changing the feedback factor of the regulator in response to a DC control voltage the output can vary from 2.5 to 12 V and the device can deliver load currents up to 5 A. To eliminate the ripple on the buck, the TPS7A4701 low-noise LDO is used as a power filter. The voltage drop (Vin-Vo) across the LDO is kept at 1 V. This drop is above the dropout of the regulator and thus the LDO can have low power dissipation as well as good PSRR performance. This drop across the LDO is maintained for all output voltage settings of the buck. This is done by an op amp feedforward circuit that monitors the DC voltage at the input of the LDO and adjusts the feedback pin of the LDO to keep a fixed Vin-Vo across the regulator.

Negative Regulator Block

This reference design uses the LMR14050 DC-DC converter setup as an inverting regulator. The output is varied by changing the feedback factor of the regulator in response to a DC control voltage. The output can vary from –2.5 to –12 V and the device can deliver load currents up to 3 A. To eliminate the ripple on the buck, the TPS7A3301 low-noise LDO is used as a power filter. The voltage drop (Vin-Vo) across the LDO is kept at 1 V. This drop is above the dropout of the regulator and thus the LDO can have low power dissipation as well as good PSRR performance. This drop across the LDO is maintained for all output voltage settings of the buck. This is done by an op amp feedforward circuit that monitors the DC voltage at the input of the LDO and adjusts the feedback pin of the LDO to keep a fixed Vin-Vo across the regulator.

The system is modular. More DC-DC converter sections that are identical to the ones demonstrated can be added to increase output current capacity. All sections are driven with the same DC control waveform as well as the sync waveform.

Presets in the board can adjust the dropout to values other than 1 V by the designer.

2.2 Highlighted Products

2.2.1 LM73605

The LM73605 device is a synchronous step-down DC-DC converter capable of driving 5 A from a supply voltage from 3.5- to 36-V DC. It has high efficiency and a high-output accuracy in a small solution size. Peak current mode control is employed. The device has an adjustable frequency and also allows frequency synchronization.

2.2.2 LMR14050

The LMR14050 device is an integrated 40-V, 5-A step-down regulator with an integrated switching FET. The device has an ultra-low quiescent current of 1 µA in sleep mode. It has an adjustable switching frequency range and internal loop compensation .It also has cycle-by-cycle current limit, thermal sensing, and shutdown.

2.2.3 TPS7A4701

The TPS7A4701 device is a positive voltage (36 V), ultra-low-noise (4 μV_{RMS}) low-dropout linear regulator (LDO) capable of sourcing a 1-A load.

2.2.4 TPS7A3301

The TPS7A3301 device is a negative voltage (–36 V), ultra-low-noise (16-μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 1 A.

2.2.5 TLV2171

The 36-V TLV2171 device provides a low-power option for cost-conscious industrial and personal electronics systems requiring an electromagnetic interference (EMI)-hardened, low-noise, single-supply operational amplifier (op amp) that operates on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V).

2.3 System Design Theory

This section explains the design theory and equations for each of the devices used in this reference design.

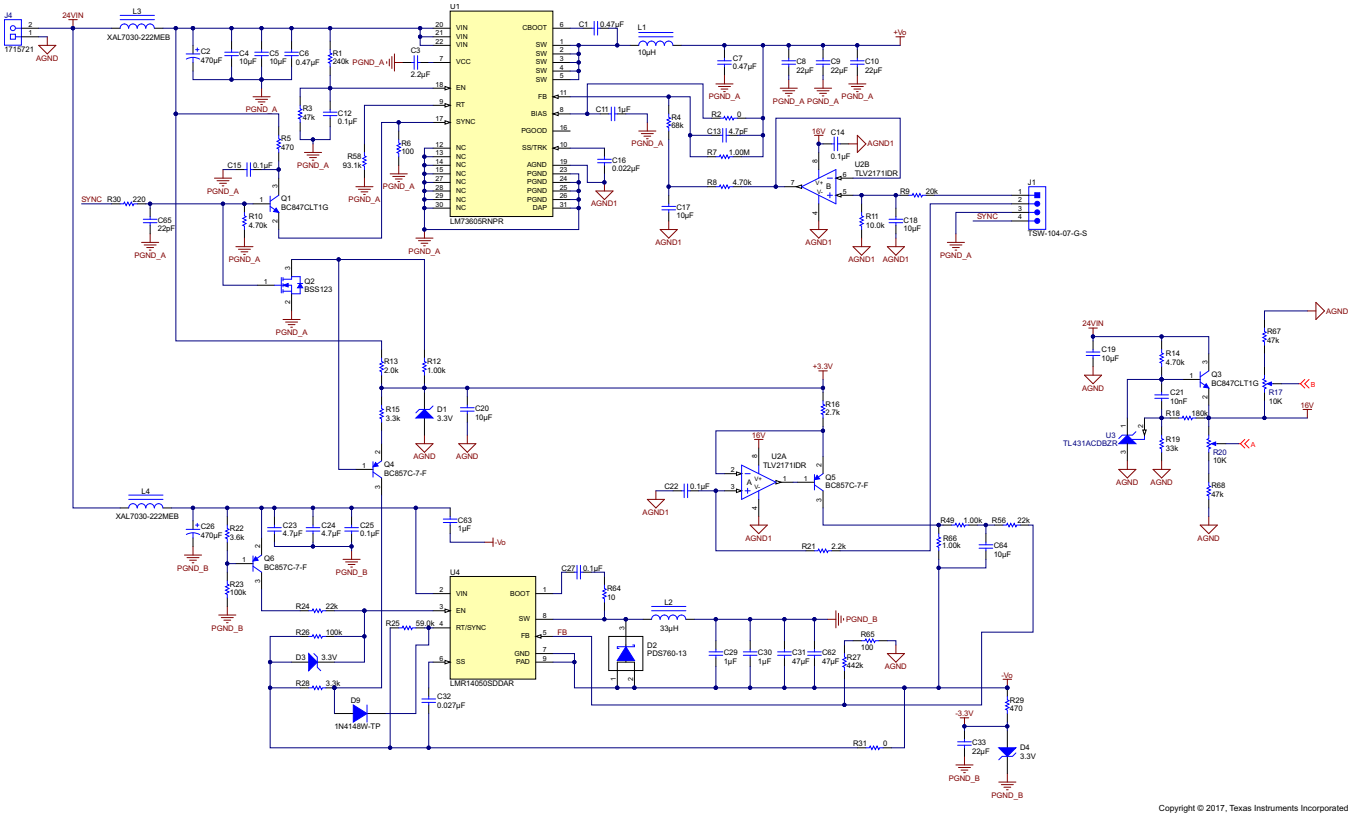


図 3. DC-DC Converters Schematic

2.3.1 Positive Switching Regulators

The LM73605 (U1) is a synchronous buck regulator that can drive 5 A of current. The output voltage is typically set up by R7 and R4. The feedback pin is normally regulated to 1 V. A DC control voltage between 0 and 3.3 V applied to Pin 1 of J1 is used to modify the output of the buck regulator from 2.5 to 15 V. This voltage is applied to U2B. This is an op amp buffer and its output is connected to a low-pass filter comprising of R8 and C17. The low-pass filter ensures that a pure DC voltage is applied to the feedback pin. Assume that the control voltage on Pin 1 of JI is 0 V. The output of op amp U2B is also 0 V.

$$V_O = \frac{R4}{(R7 + R4)} = 1\,V \tag{1}$$

$$V_O = \frac{1\,V\,(1M + 68\,k)}{68\,k} = 15.7\text{-V maximum output voltage}$$

Assume now that 3-V DC is applied on Pin 1 of J1. The output of the op amp is now 1-V DC. Applying the superposition theorem on the feedback pin:

$$\frac{V_O \times R4}{(R7 + R4)} + \frac{1\,V \times R7}{(R7 + R4)} = 1\,V \tag{2}$$

$$\frac{V_O \times 68k}{(1M + 68k)} + \frac{1\,V \times 1M}{(1M + 68k)} = 1\,V$$

Therefore, for a DAC control range of 0 3 V, the output voltage varies from 1 to 15.7 V.

$$V_O = 15.7 - 15 \times V_{CON} \tag{3}$$

This is an approximate equation describing the behavior given the resistors placed R58 on pin 9 of U1 sets the operating frequency of the DC-DC converter.

図 4 shows that a frequency of 400k is set for a 93k resistor. Transistor Q1 is set up as a buffer and is used to couple the sync signal to the sync pin. With no sync input, the sync pin is ground with a 10k resistor.

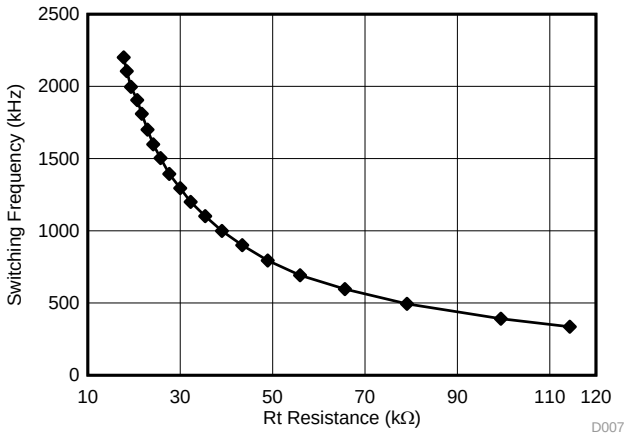


図 4. R_T Resistance versus Frequency

U4 (LMR14050) is a 5-A non-synchronous buck regulator. This regulator is set up as an inverting regulator. As shown in 図 5, to set up a buck regulator in inverting mode, the bottom of S2 is connected as a negative output. The output end of the inductor L is grounded. The circuit now looks like a traditional negative regulator.

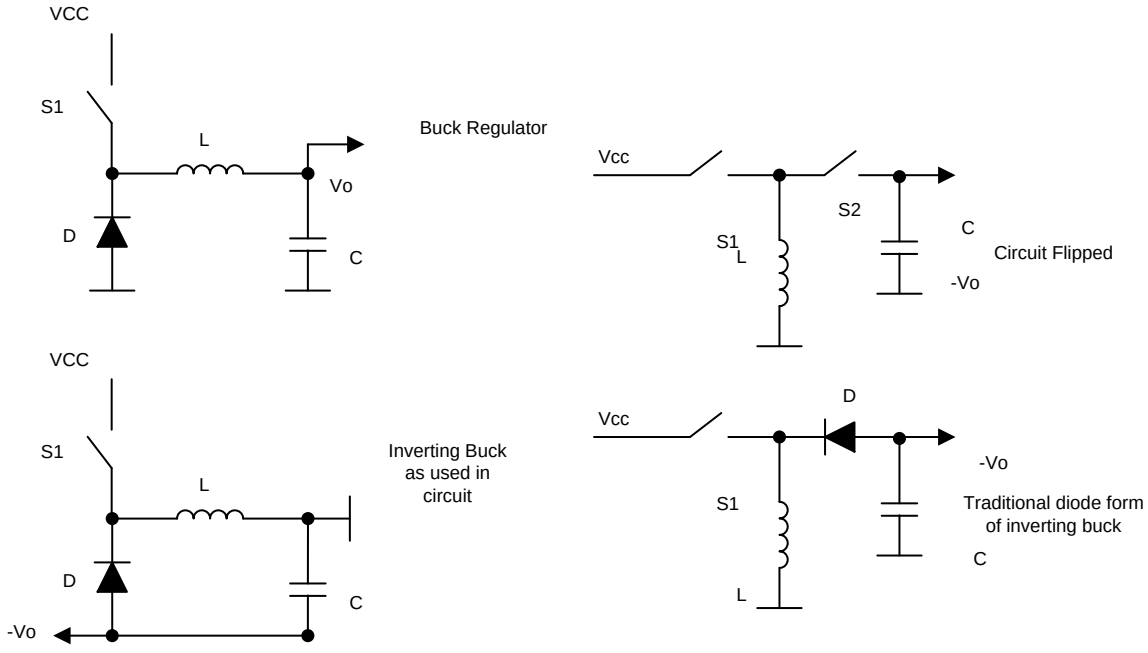


図 5. Basic Functionality of Negative Switching Regulators

Note that the maximum voltage that the device sees is as calculated using 式 4:

$$V_{STRESS} = (V_{IN} + V_{OMAX}) \quad (4)$$

For V_{IN} = 24 v and V_O = –15 V, the device sees 39 V, which is very close to the absolute maximum rating of the device. Therefore, a maximum of -12 V can be kept at the output.

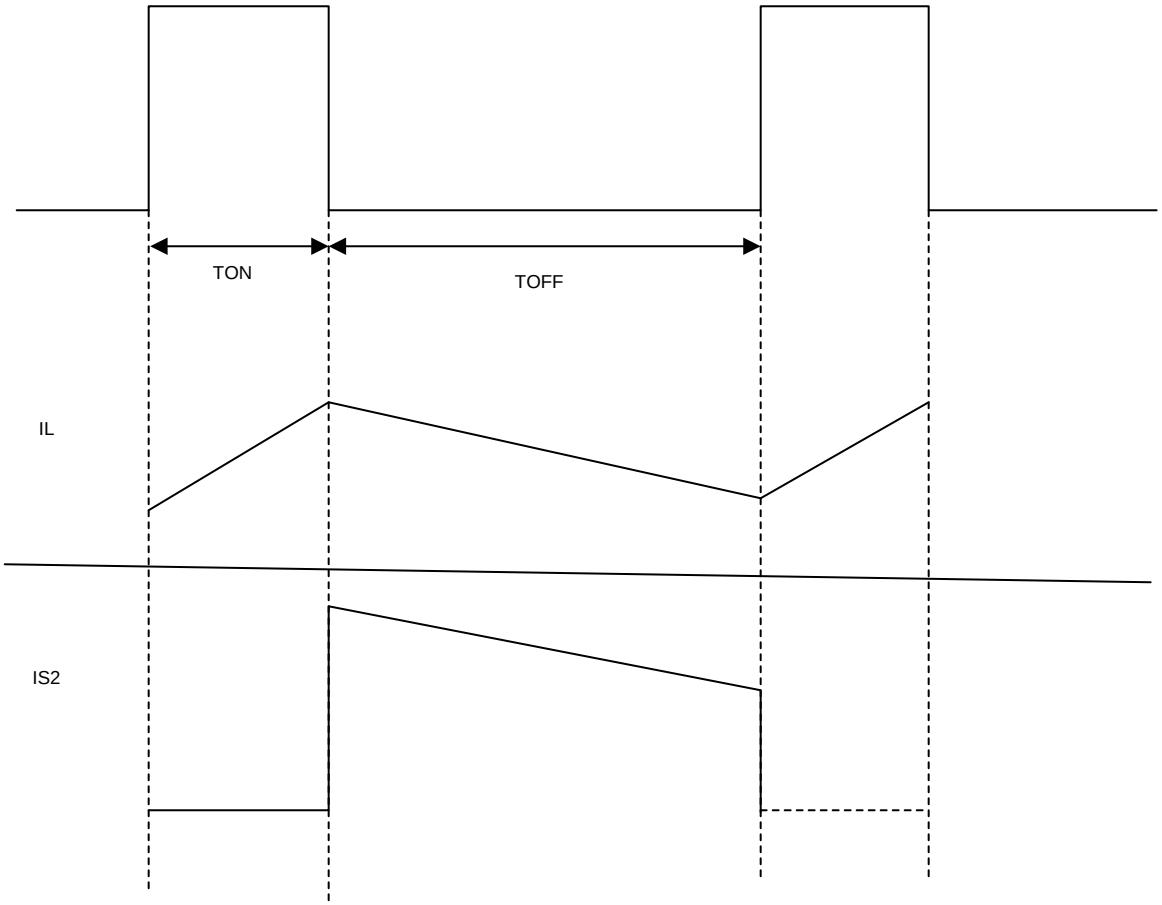


図 6. Theoretical Waveforms for Negative Buck

Regarding 図 6, assume TON is the time S1 conducts and TOFF is the time S2 conducts.

$$V \times TON = |V_O| \times TOFF \tag{5}$$

$$|V_O| = \frac{V \times D}{(1 - D)}$$

Note that I_O = Average of IS2.

$$I_O = \frac{I_{MAX} \times TOFF}{T} \tag{6}$$

$$I_O = I_{MAX} \times (1 - D)$$

Therefore, if V_O = –15 V, D = 0.36, I_O maximum = 3 A for a 5-A buck switcher. Resistors R27 and R56 are used to set the output voltage. The LMR14050 has a feedback voltage of 0.75 V.

$$\frac{V_O \times R56}{(R27 + R56)} = 0.75\ V \tag{7}$$

$$\frac{V_O \times 22\ k}{(22k + 442\ k)} = 0.75$$

$$V_O = -15\ V$$

To adjust the negative output, apply a DC control voltage between 0 and 3 V to Pin 2 of J1.

The collector of Q5 adds a voltage to the feedback pin of the LMR14050. When this voltage from the feedback pin to the device ground equals 0.75 V, the output of the negative converter drops to zero. The 0.75 V is obtained through the op amp current source. When the DC voltage applied to pin 3, U2A is 0 V. The current in Q5 = 3.3/R16 or 3.3/3K3 = 1 mA. R66 × 1 mA = 1 V. This is more than the 0.75 V needed to bring the output voltage to zero.

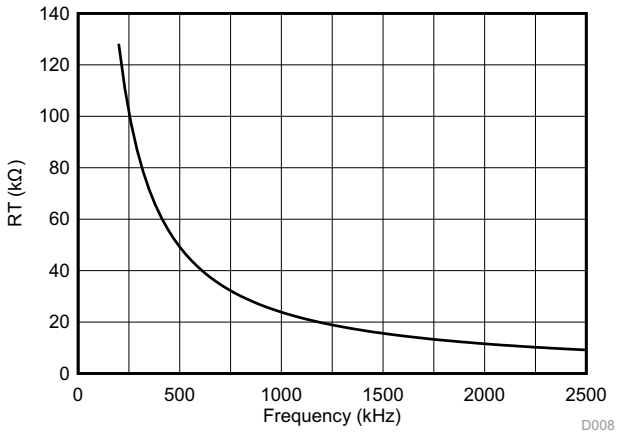


図 7. R_T versus Frequency

表 2. Typical Frequency Setting R_T Resistance

f_{SW} (kHz)	R_T (kΩ)
200	127.0
350	71.5
500	49.9
750	32.4
1000	23.7
1500	15.8
2000	11.5
2200	10.5

This is an approximate equation describing the behavior given the resistors placed R25 is used to set the oscillator frequency at 400k.

Transistor Q4 is used to couple the sync signals to the R_T pin. When there is no sync signal, the transistor is cut off. The Enable pin is driven by transistor Q6. This transistor acts as a level shifter as the Enable pin is referenced to $-V_O$. Resistors R22 and R23 act as a voltage divider and at a minimum supply voltage turn the PNP transistor on

$$\frac{V_{MIN} \times R22}{(R22 + R23)} = 0.65 \text{ V} \tag{8}$$

$$V_{MIN} = \frac{0.65 \times 103.6 \text{ k}}{3.6 \text{ k}} = 18 \text{ V}$$

2.3.2 Linear Regulators

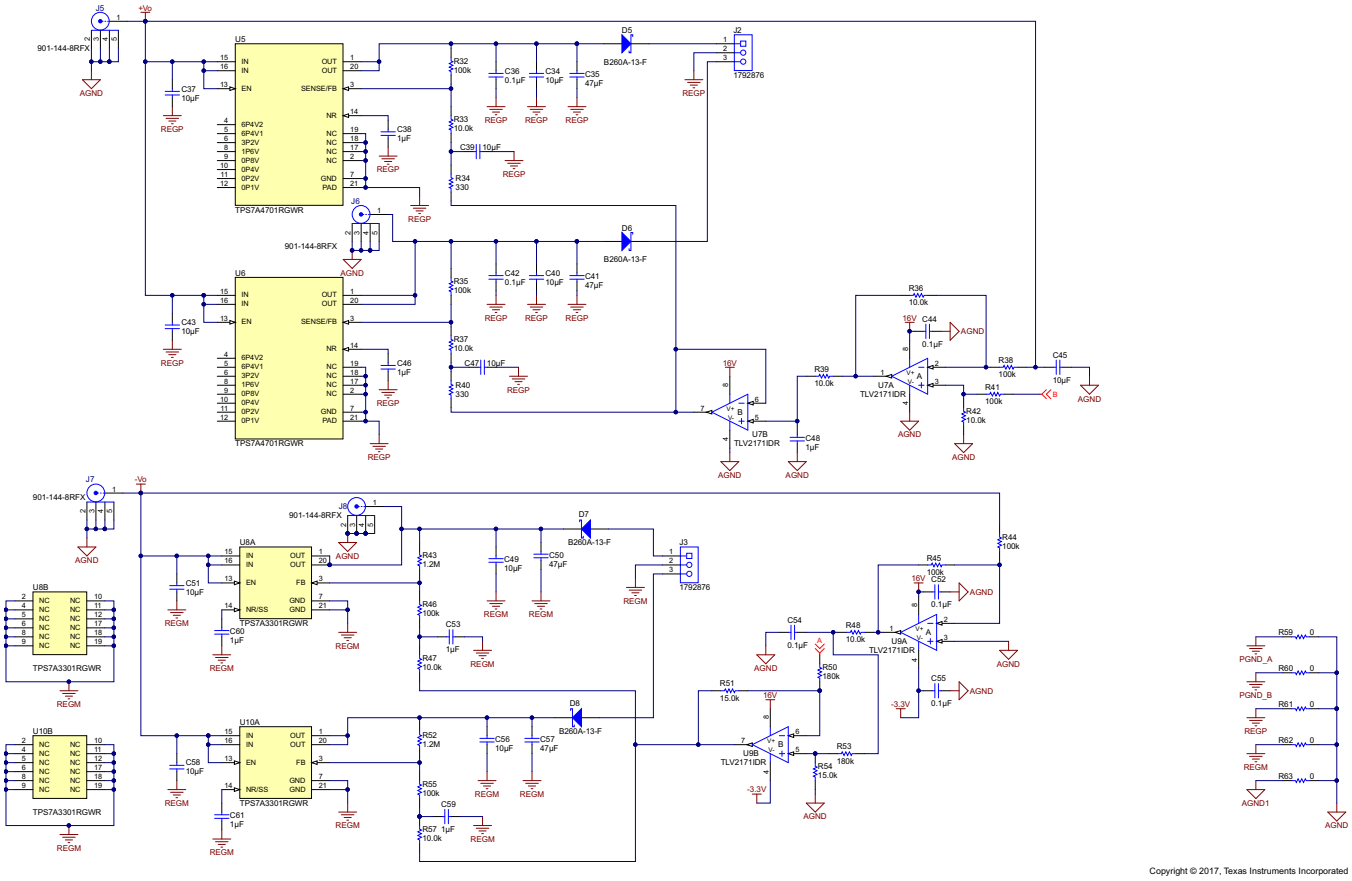


図 8. Linear Regulators Schematic

The LDO section filters out the ripple content in the switching regulators and leaves a very ripple-free and low-noise output to feed the CW power. It relies on the fact that a linear regulator is an active filter and can reduce the ripple seen at its input due to its excellent PSRR performance. For this to work well, the LDO must be in the active region well beyond the dropout; however, operating a regulator in the active region results in power dissipation [I × (V_{IN} – V_O)]. Therefore, to prevent dissipation, it is best to run the regulator just outside its minimum dropout. Because the input voltage of the regulator varies as it is set by software, the hardware circuitry on the board continuously monitors the input voltage, removes the ripple, and adjusts the feedback voltage so that the output voltage is always 1 V lower than input whatever input is present.

図 9 shows a positive LDO with a control voltage applied to R2.

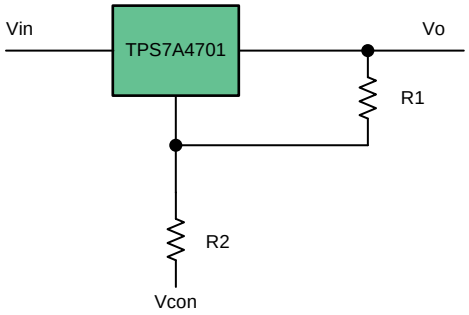


図 9. Positive LDO Controlled Using V_{CON}

Case 1: When V_{CON} = 0 V, let the maximum output voltage be 15 V (V_{FBK} = 1.4 V).

$$\frac{V_{OMAX} \times R2}{(R1 + R2)} = 1.4\ V \tag{9}$$

$$V_{OMAX} = \frac{1.4 \times 110\ k}{10\ k} = 15\ V$$

Case 2: With V_{CON} applied with R1 = 100K, R2 = 10K:

$$\frac{V_O \times R2}{(R1 + R2)} + \frac{V_{CON} \times R1}{(R1 + R2)}$$

$$\frac{V_O}{11} + \frac{V_{CON} \times 10}{11} = 1.4\ V$$

$$V_O + V_{CON} \times 10 = 15.4\ V \tag{10}$$

Assume $V_O = V_{IN} - 1$ and apply in 式 11:

$$V_{IN} - 1 + V_{CON} \times 10 = 15.4 \tag{11}$$

$$V_{CON} = \frac{(16.4 - V_{IN})}{10}$$

式 11 can be implemented in a differential amplifier: one input is a DC voltage of 16.4 V, the other being the regulator input voltage. The differential amp is set up with a gain of 1/10. In the schematic, U7A is the differential amplifier. R36, R38, R41, and R42 set up a differential gain of 1/10. R39 and C48 form a low-pass filter that removes any ripple on this line and leaves a DC equal to the average value of voltage at the input. U7B is a buffer and the output of this drives the feedback pin. This system is a feedforward system and must not face any stability issues.

For example: If V_{IN} = 10 V, then the differential amplifier output V_{CON} = (16.4 – 10)/10 = 0.64 V. Now:

- $V_O + 0.64 \times 10 = 15.4$
- $V_O = 15.4 - 6.4 = 9$ V
- $V_O - V_{IN} = 1$ V

図 10 assumes a negative LDO with a control voltage applied to R2.

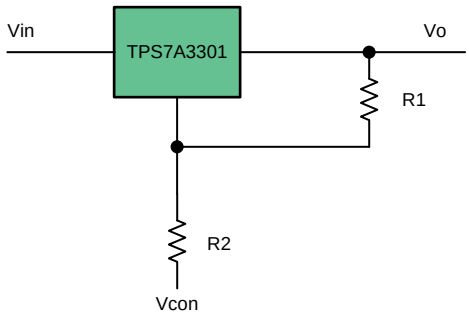


図 10. Negative LDO Controlled Using V_{CON}

Case 1: When V_{CON} = 0, let the maximum output voltage be –15 V, V_{FB} = –1.13 V.

$$\frac{V_{OMAX} \times R2}{(R1 + R2)} = -1.13 \text{ V}$$

$$V_{OMAX} = \frac{-1.13 \times 1.3M}{100k}$$

Case 2: With V_{CON} applied and with R1 = 1200k, R2 = 110k:

$$\frac{V_O \times R2}{(R1 + R2)} + \frac{V_{CON} \times R1}{(R1 + R2)} = -1.13 \text{ V}$$

$$\frac{V_O \times 110k}{(1.2M + 110k)} + \frac{V_{CON} \times 1.2M}{(1.2M + 110k)} = -1.13 \text{ V}$$

$$V_O + V_{CON} \times 10.9 = -13.45 \text{ V} \quad (12)$$

Assume $V_O = V_{IN} + 1$ and apply in 式 13:

$$V_{IN} + 1 + V_{CON} \times 10.9 = -13.45$$

$$V_{CON} = \frac{(-14.45 - V_{IN})}{10.9} \quad (13)$$

式 13 can be implemented in a differential amplifier: one input is a DC voltage of 15.7 V, the other being the regulator input voltage. U9A is a differential amplifier with a gain of –1. This converts the negative input voltage to a positive output level. U9B is a differential amplifier with a gain 1/10.9 that compares the positive output voltage seen on U9A with a fixed DC voltage of –14.45 V. For example: If the V_{IN} of the regulator is –10 V, pin 1 of U9A would be 10 V as U9A is an inverting amplifier with a gain of 1. The output of U9B that is a differential amplifier with an attenuation of 1/12 would be as follows:

- From 式 13:

$$V_{CON} = \frac{-\left(14.45 - \left(-10\right)\right)}{10.9} = -0.408 \text{ V}$$

- From 式 12:

$$V_O + V_{CON} \times 10.9 = -13.45 \text{ V}$$
$$V_O - 0.475 \times 10.9 = -13.45 \text{ V}$$
$$V_O = -9 \text{ V}$$

This is V_{IN} + 1. The drop across the LDO is 1 V. Therefore, the drop across the differential amplifier needs to be –0.4 V. The differential amplifier implements

$$\frac{\left(10 - 14.45\right)}{10.9} = -0.4 \text{ V}$$
$$V_O = 14.69 - 0.475 \times 12 = -9 \text{ V} \quad (14)$$

R47 and C53 form a low-pass filter that removes any ripple present on the input of the LDO. ORing diodes D5, D6, D7, and D8 are used to connect the output with the high-voltage supply. The diodes would block the high voltages from reaching the regulators. The control loop is common to all the LDOs, and it is possible to place many LDOs on the same control loop to share the currents.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

表 3. Connectors, Fuses, and Test Points on Board

REFERENCE	DESCRIPTION	PINOUT
J4	24-V input	24-V GNDA
J1	V_{CON} + Sync	V_{CON} positive V_{CON} negative Sync PGND_A
J2	Positive regulator output	Out_1 Reg_P Out_2
J3	Negative regulator output	out_1B Reg_M Out_2B
J5	$+V_O$ SMA	$+V_O$
J7	$–V_O$ SMA	$–V_O$
J6	SMA regulator positive output	—
J8	SMA regulator positive output	—

3.1.1 TIDA-01458 Board Images

図 11 and 図 12 show the top and bottom views of TIDA-01358 PCB, respectively.

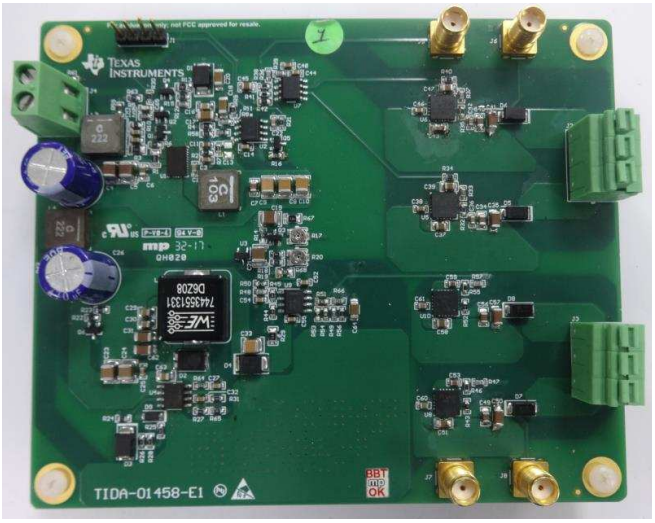


図 11. Top View

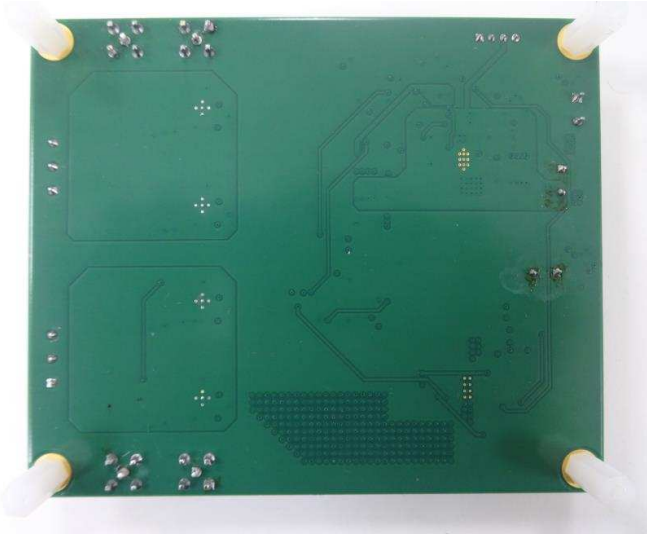


図 12. Bottom View

3.2 Testing and Results

To test the board, use the following equipment:

- 24-V DC input supply rated at 5 A
- 5-V variable DC source to provide a control signal to adjust the output voltages
- 15-Ω power resistors as well as an electronic load is also needed
- 5-V pulses frequency source capable of generating frequencies from 300 to 500 kHz
- Oscilloscope (100 MHz)
- Spectrum analyzer
- Thermal camera

3.2.1 Test 1: Output Voltages as a Function of Control Voltage-Negative Power Supply

A load of 0.8 A is put on the output of the LDO, and the output voltage is observed as a function of DC control voltage.

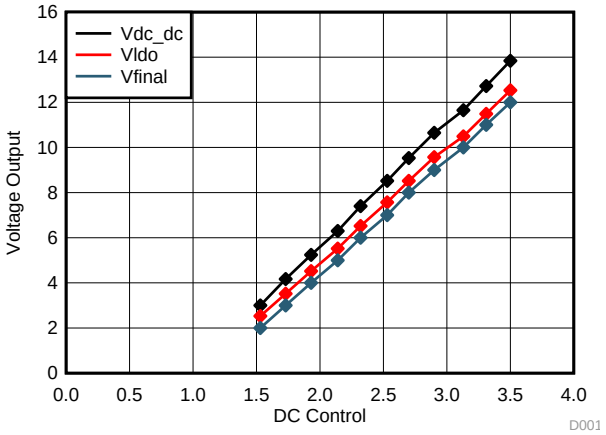


図 13. Output Voltage as Function of DC Control-Negative

3.2.2 Test 2: Voltage Drop Across Negative LDO as a Function of Control Voltage

A load of 0.8 A is put on the output of the LDO, and the voltage drop across the LDO is observed for varying DC-DC converter outputs.

注: Adjust R20 to 14 V.

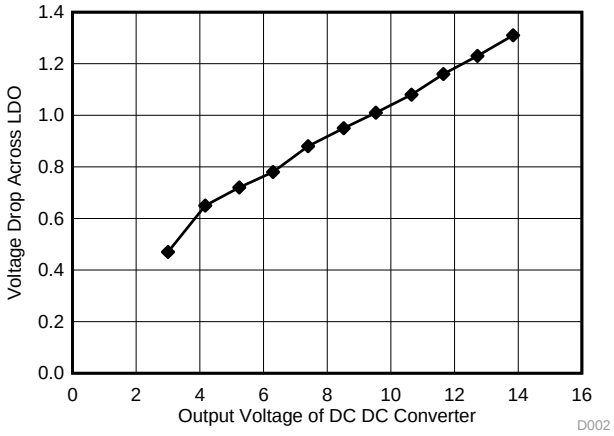


図 14. Voltage Drop Across Negative LDO

3.2.3 Test 3: Output Voltages as a Function of Control Voltage-Positive Power Supply

A load of 0.8 A is put on the output of the LDO, and the output voltage is observed as a function of DC control voltage.

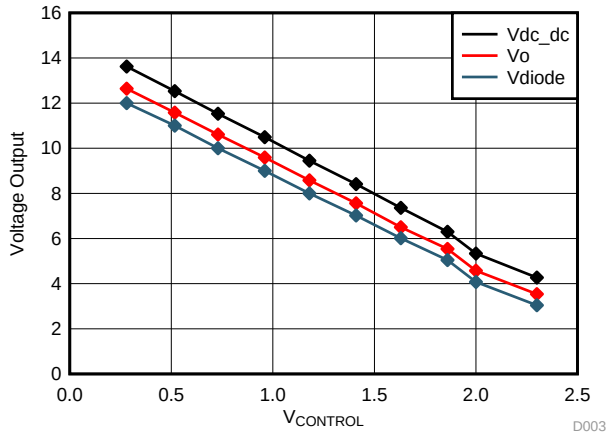


図 15. Output Voltage as Function of DC Control-Positive

3.2.4 Test 4: Voltage Drop Across Positive LDO as a Function of Control Voltage

A load of 0.8 A is put on the output of the LDO, and the voltage drop across the LDO is observed for varying DC-DC converter outputs.

注: Adust R17 to 15.47 V.

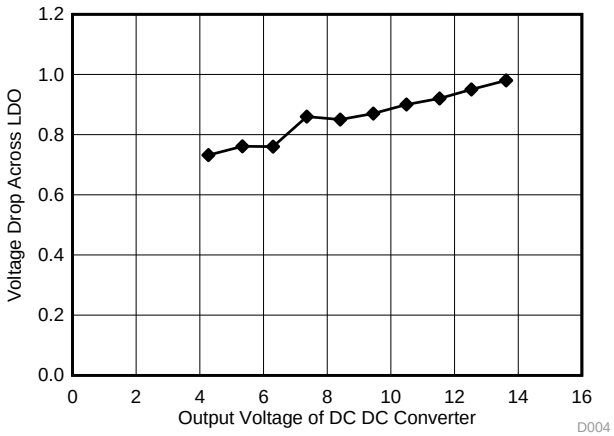


図 16. Voltage Drop Across Positive LDO

3.2.5 Test 5: Load Regulation Positive DC-DC

The load regulation is given in 図 17 and 表 4 for different load currents and output voltages.

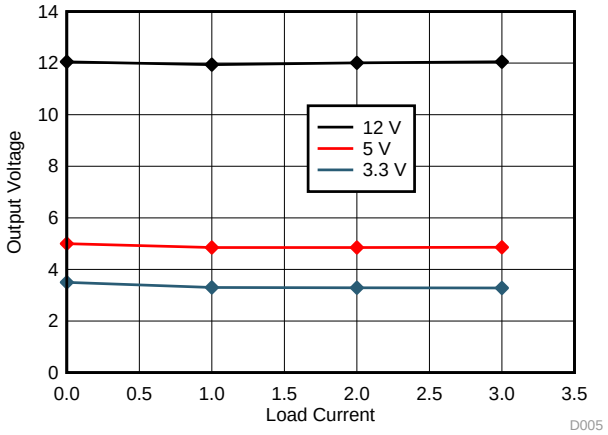


図 17. Load Regulation Positive DC-DC

表 4. Load Regulation Positive DC-DC Data

CURRENT	12 V	5 V	3.3 V
0	12.05	5.00	3.50
1	11.94	4.85	3.30
2	12.01	4.85	3.29
3	12.05	4.86	3.28

3.2.6 Test 6: Load Regulation Negative DC-DC Converter

The load regulation is given in 図 18 and 表 5 for different load currents and output voltages.

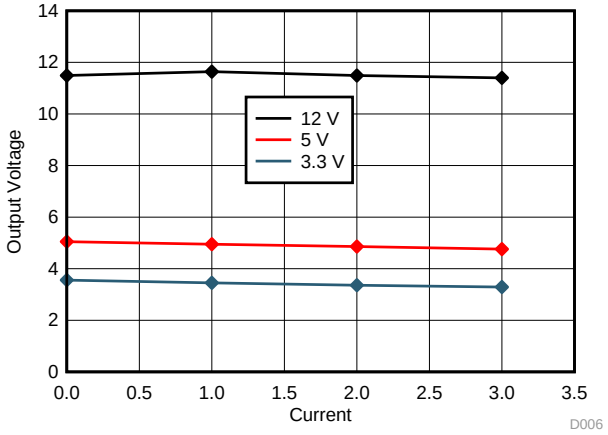


図 18. Load Regulation Negative DC-DC

表 5. Load Regulation Negative DC-DC Data

CURRENT	12 V	5 V	3.3 V
0	11.49	5.05	3.56
1	11.64	4.95	3.45
2	11.49	4.86	3.36

表 5. Load Regulation Negative DC-DC Data (continued)

CURRENT	12 V	5 V	3.3 V
3	11.40	4.76	3.29

3.2.7 Test 7: Voltage Ripple of Positive Power Supply

Load current of 0.8 A from the LDO, 12-V output on the LDO

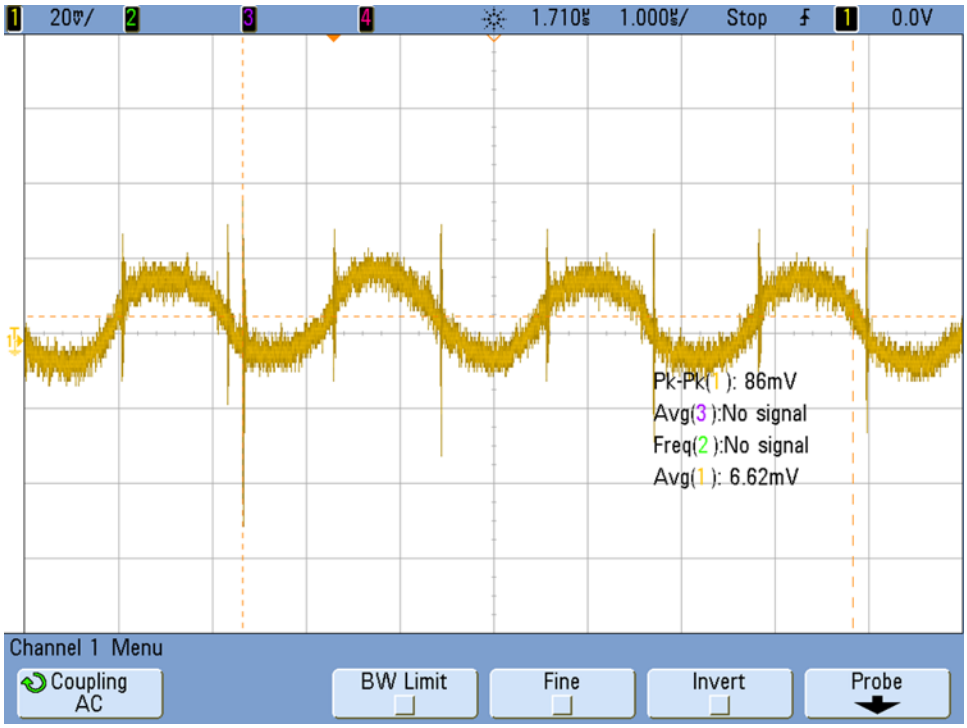


図 19. Voltage Ripple at Positive DC-DC Output

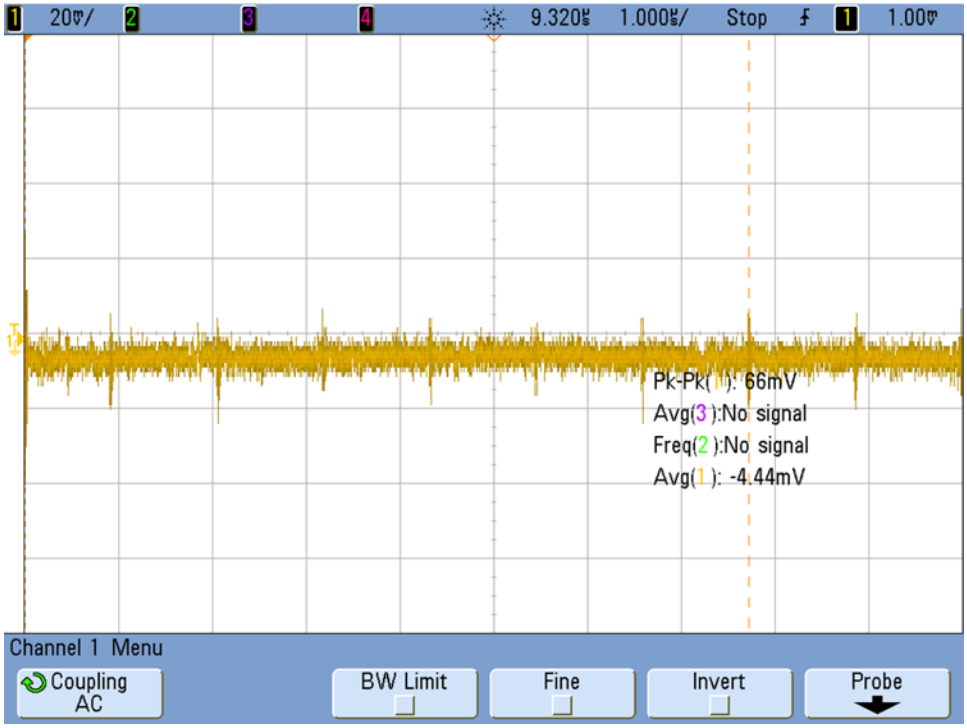


図 20. Voltage Ripple at Positive LDO Output

3.2.8 Test 8: Voltage Ripple of Negative Power Supply

This test shows the output ripple on the DC-DC converter output as well as LDO output with a load of 0.8 A on the LDO output.

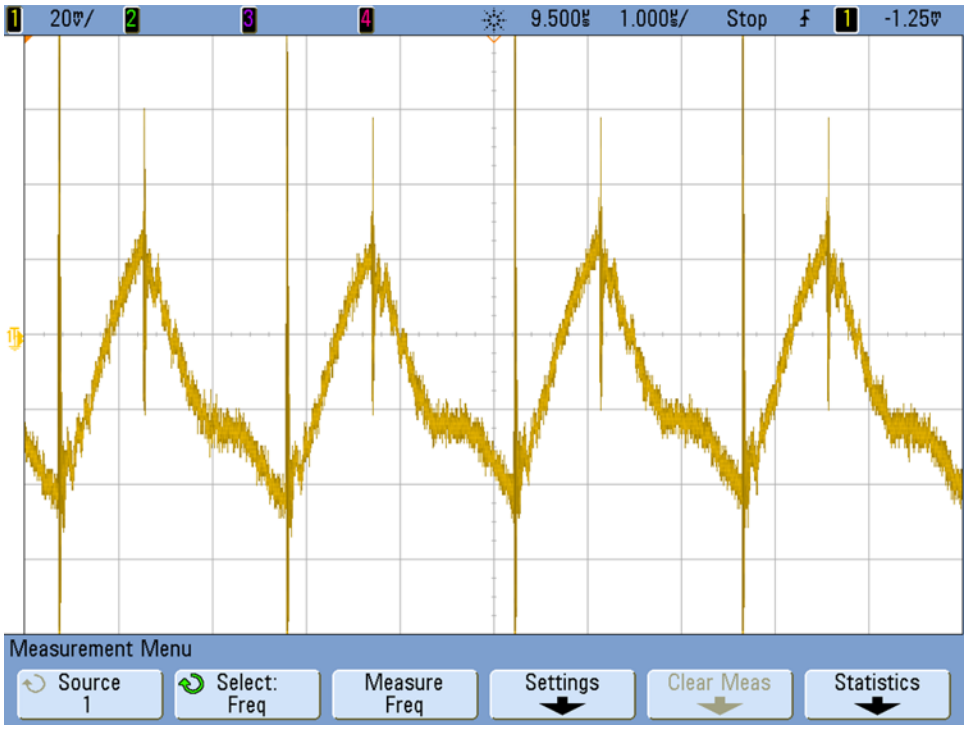


図 21. Voltage Ripple at Negative DC-DC Input

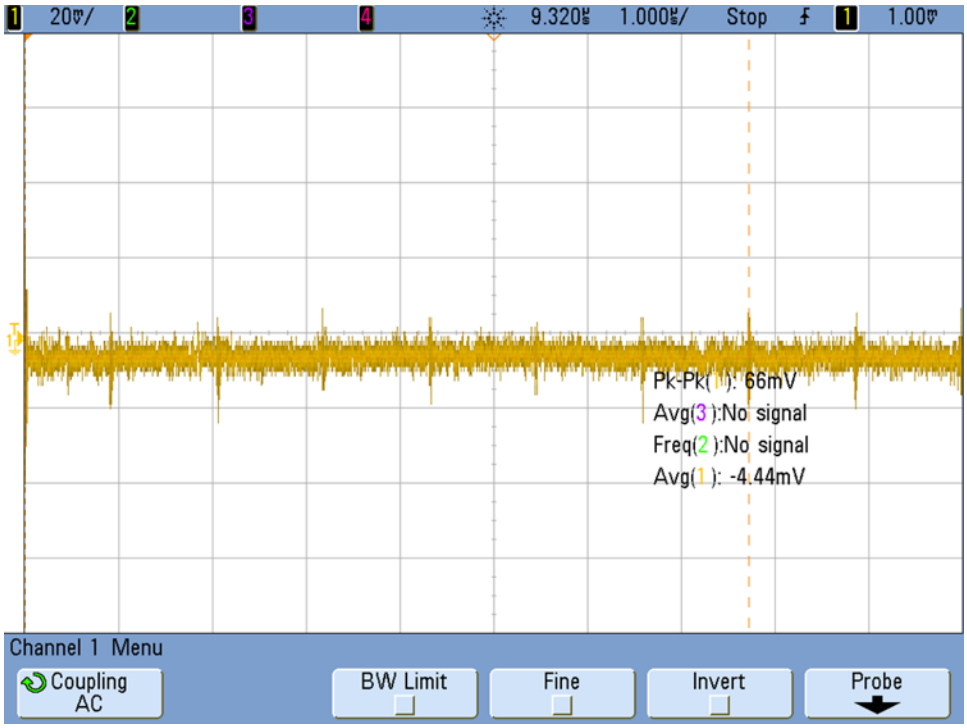


図 22. Voltage Ripple at Negative LDO Output

3.2.9 Test 9: Synchronization Test Positive DC-DC

This test applies an external sync waveform of 3.3-V amplitude to the sync input of the DC-DC converter. The test also observes the switching node of the buck and the sync waveform.

Output voltage for this test is at 12 V with a 2-A load drawn direct on the DC-DC converter.

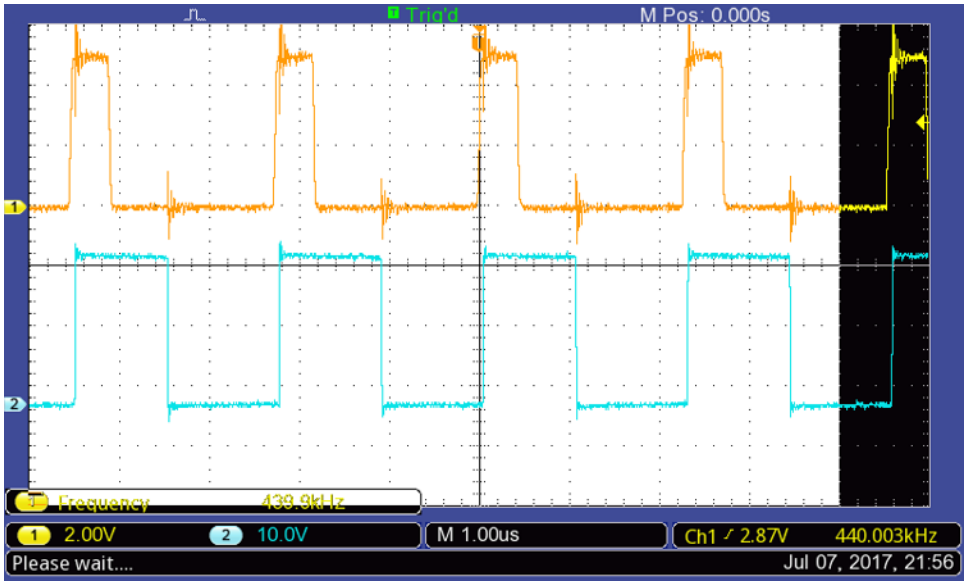


図 23. Sync and Output Switching Waveform of Positive DC-DC at 440 kHz

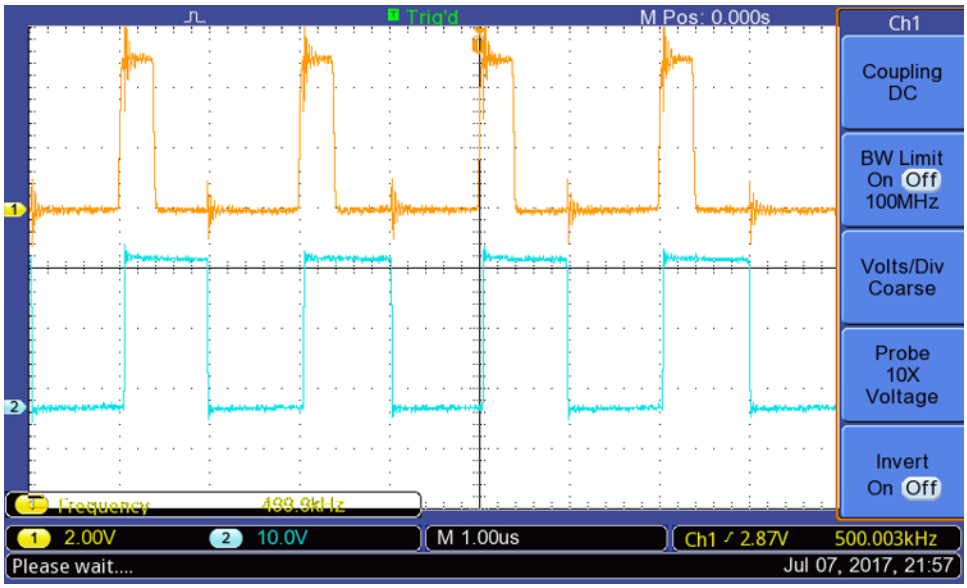


図 24. Sync and Output Switching Waveform of Positive DC-DC at 500 kHz

3.2.10 Test 10: Synchronization Test Negative DC-DC

This test applies an external sync waveform of 3.3-V amplitude to the sync input of the DC-DC converter. The test also observes the switching node of the buck and the sync waveform.

Output voltage for this test is at –12 V with a 2-A load drawn direct on the DC-DC converter.

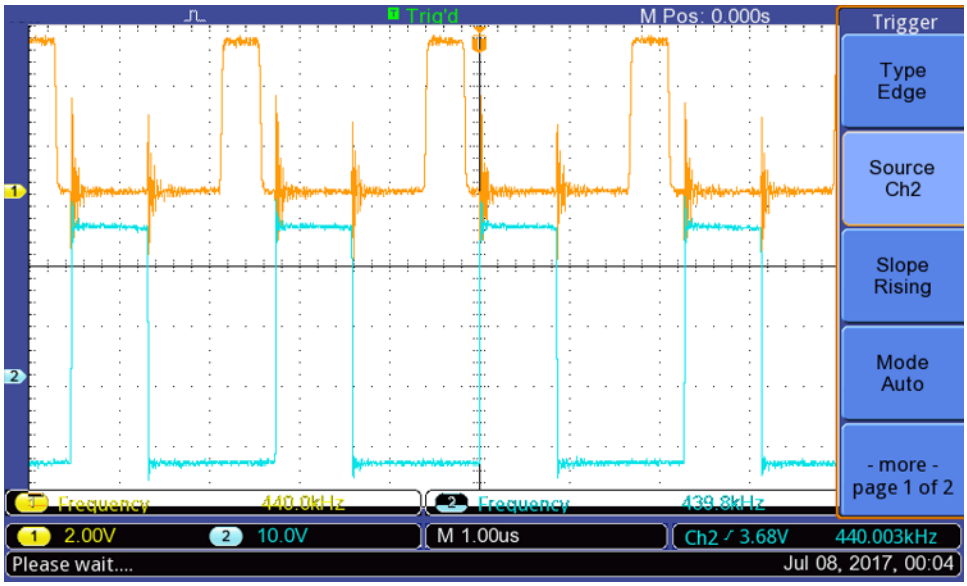


図 25. Sync and Output Switching Waveform of Negative DC-DC at 440 kHz

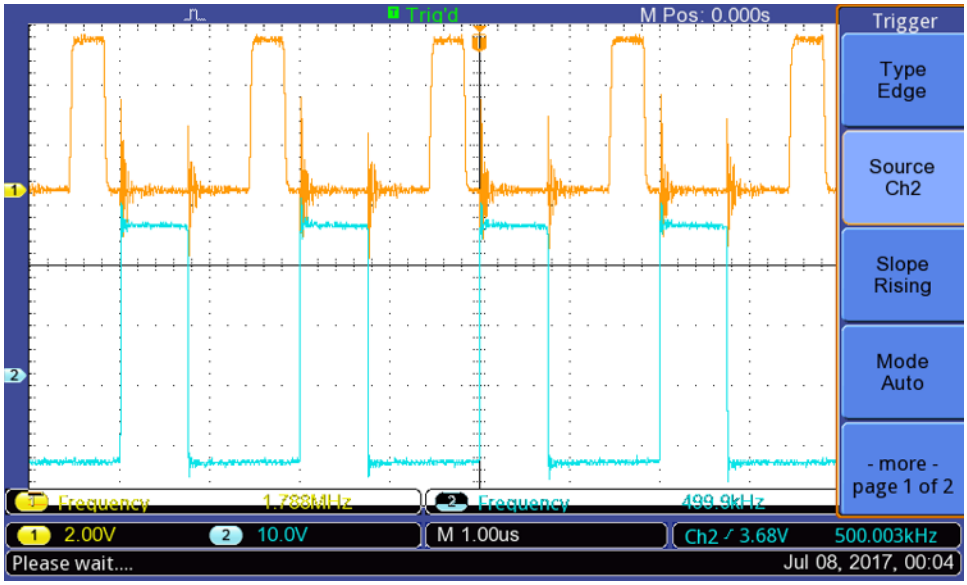


図 26. Sync and Output Switching Waveform of Negative DC-DC at 500 kHz

3.2.11 Test 11: Spectrum Analyzer

The following waveforms are plots on a spectrum analyzer. This test measures the level of the switching waveform on the output of the DC-DC converters as well as the LDOs. These plots are for both positive and negative sections. A load of 1 A is applied on the LDO output and the LDO is maintained at a dropout of 1 V for both positive and negative circuits.

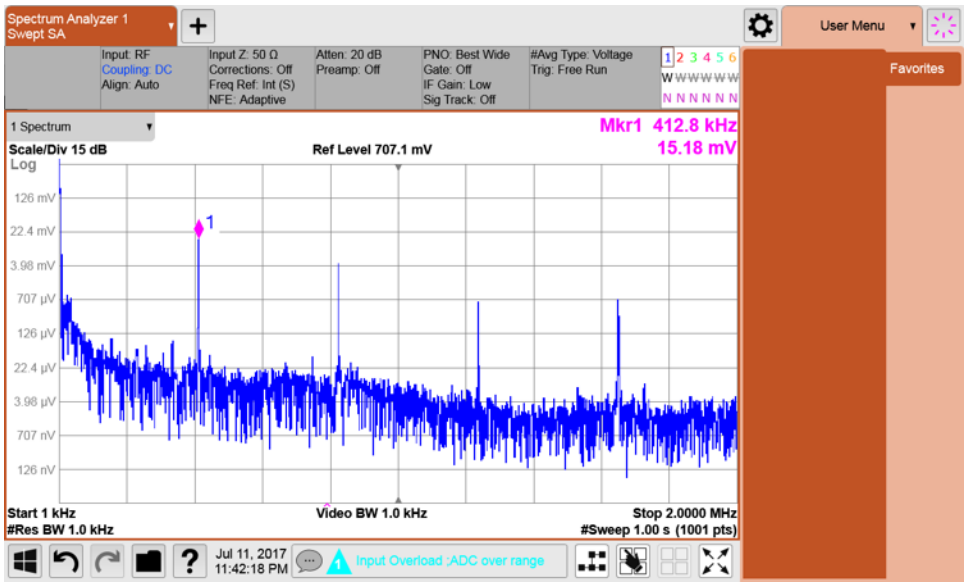


図 27. Spectral Plot of Negative DC-DC Output

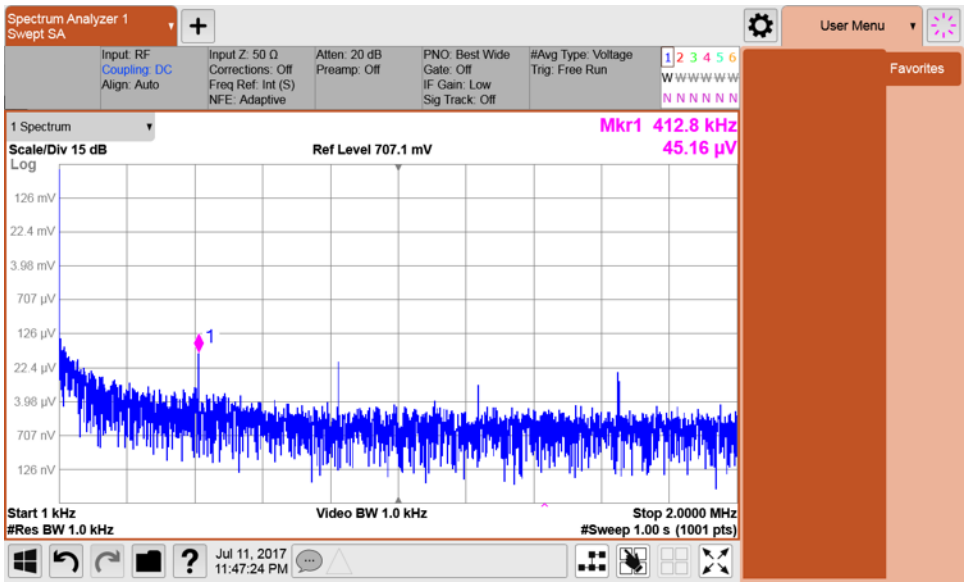


図 28. Spectral Plot of Negative LDO Output

PSRR = 20 × log(V_{IN} LDO/V_{OUT} LDO)

PSRR = 20 × log(15.8 mv/45.16 µV) = 50.8 dB

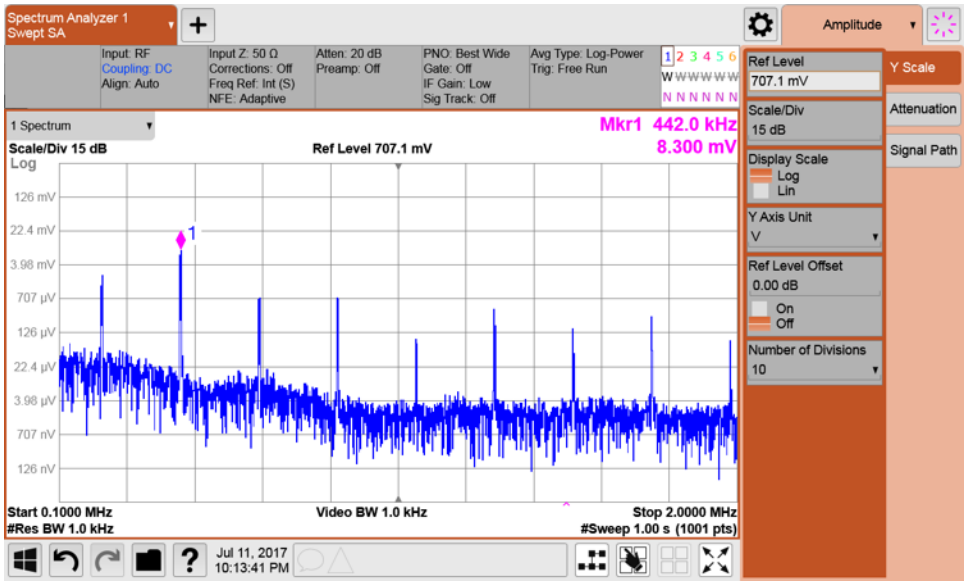


図 29. Spectral Plot of Positive DC-DC Output

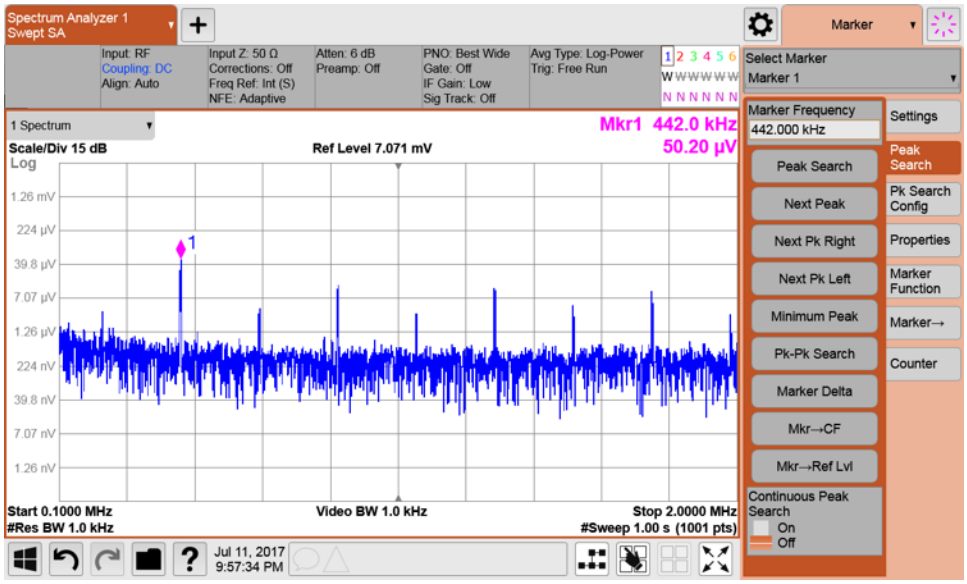


図 30. Spectral Plot of Positive LDO Output

PSRR = 20 × log(V_{IN} LDO/V_{OUT} LDO)

PSRR = 20 × log(8.3 mv/442 µV) = 44.04 dB

3.2.12 Test 12: Ramp of Control Voltage and Output Voltage LDO-Positive

A signal generator is used to give a ramp waveform on the DC control voltage input. The variation in the output voltage on the LDO was seen. A load resistance of 10 Ω was placed on the LDO output.

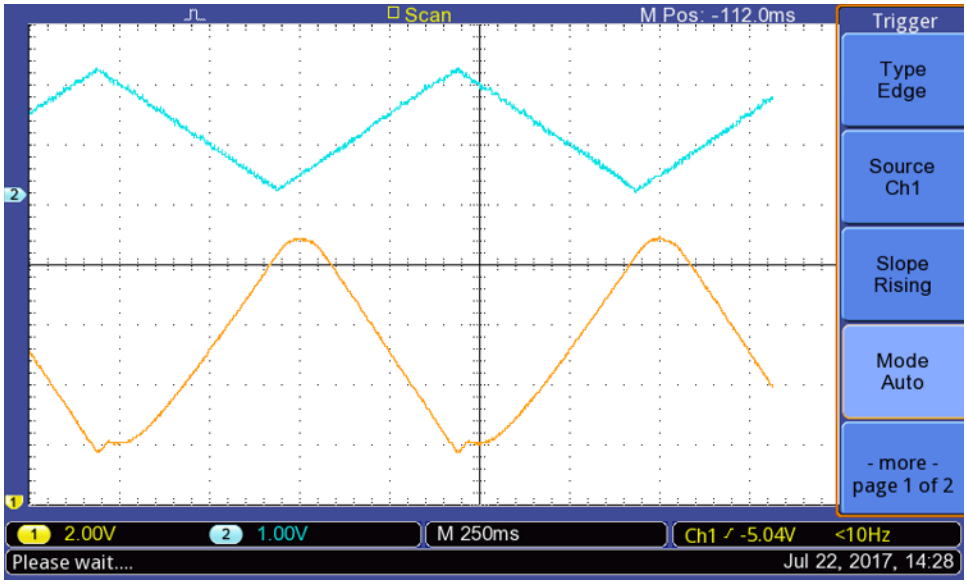


図 31. Ramp Waveform on Control Voltage-Positive DC-DC

A signal generator is used to give a square waveform on the DC control voltage input. The variation in the output voltage on the LDO is seen. A load resistance of 10 Ω is placed on the LDO output.

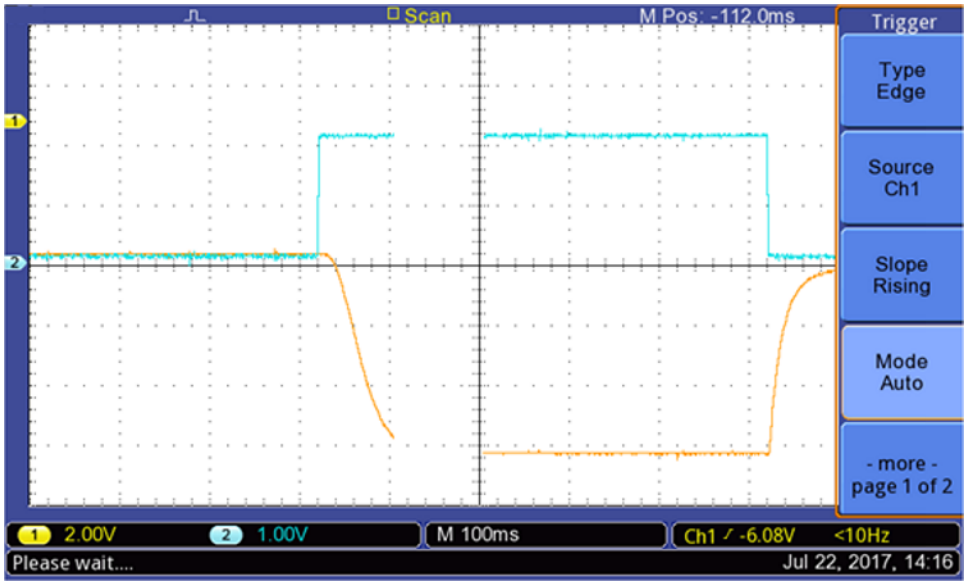


図 32. Square Waveform on Control Voltage-Positive DC-DC

3.2.13 Test 13: Ramp of Control Voltage and Output Voltage LDO-Negative

A signal generator is used to give a ramp waveform on the DC control voltage input. The variation in the output voltage on the LDO is seen. A load resistance of 10 Ω is placed on the LDO output.

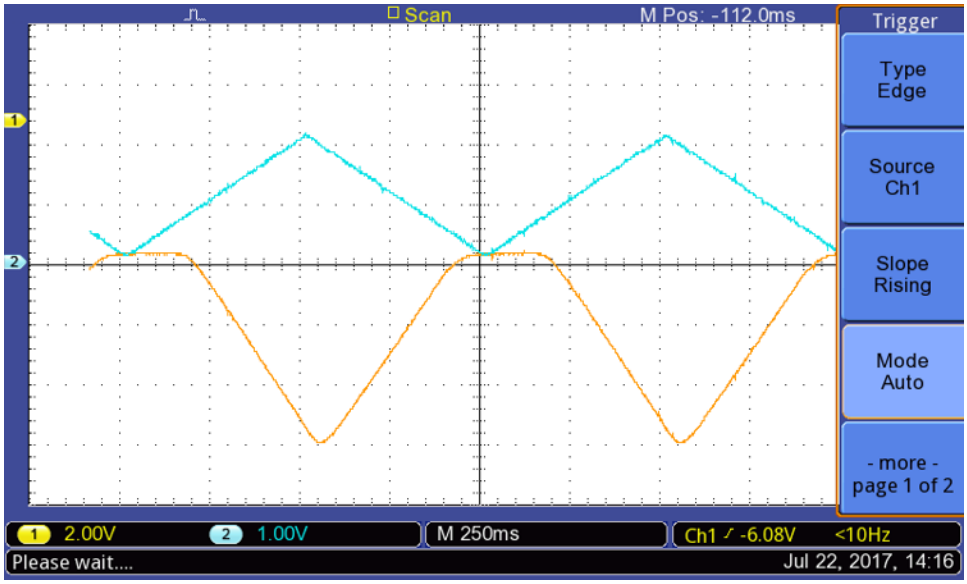


図 33. Ramp Waveform on Control Voltage-Negative LDO

A signal generator is used to give a ramp waveform on the DC control voltage input. The variation in the output voltage on the LDO is seen. A load resistance of 10 Ω is placed on the LDO output.

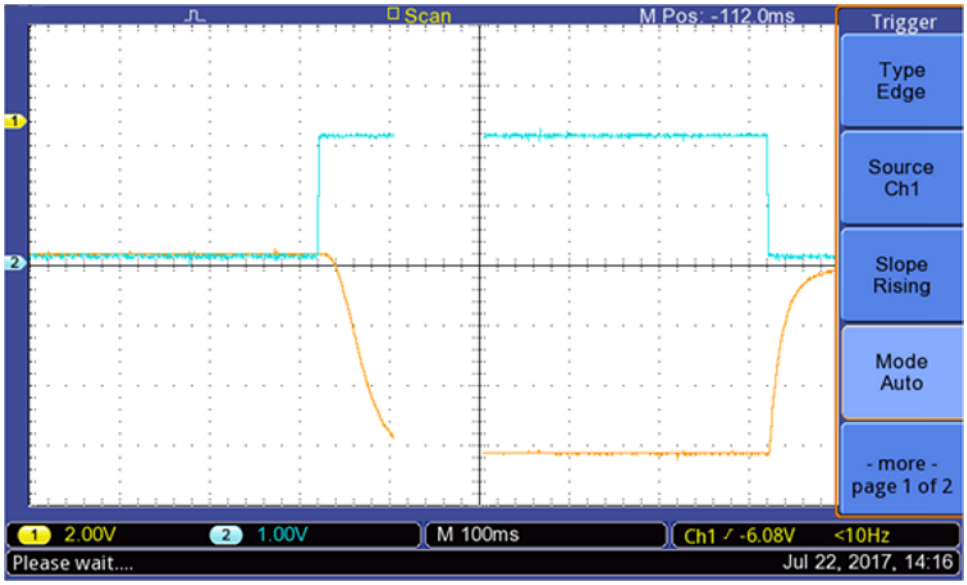


図 34. Square Waveform on Control Voltage-Negative LDO

3.2.14 Test 14: Load Switching of 1-A Load at LDO Output

A 10-Ω load is switched on and off at the LDO output periodically. The output voltage is 9 V.

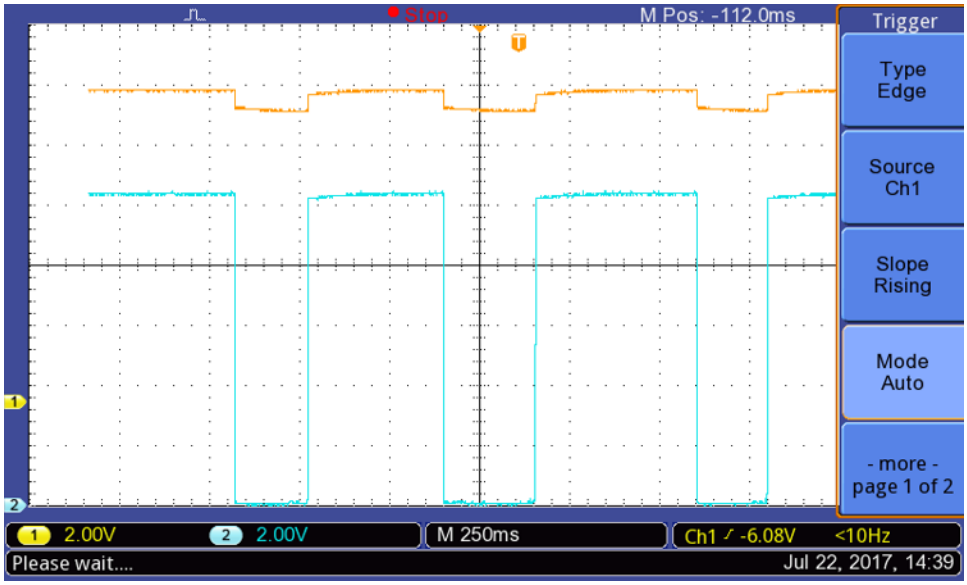


図 35. Load Switching-Positive LDO

A 10-Ω load is switched on and off at the LDO output periodically. The output voltage was –9 V.

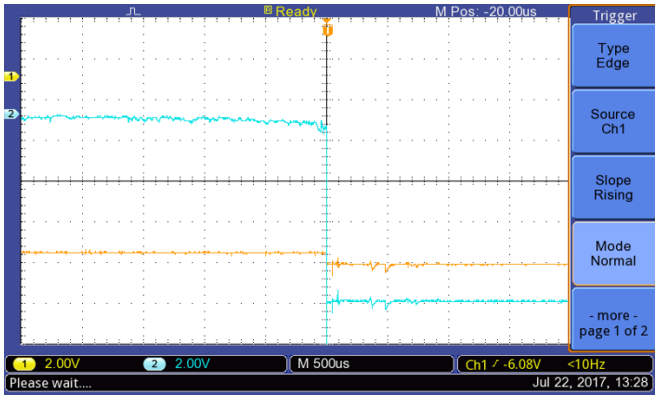


図 36. Load Switching-Negative LDO-A

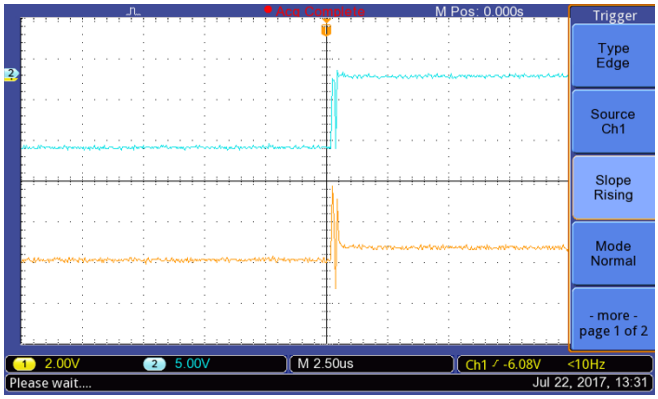


図 37. Load Switching-Negative LDO-B

3.2.15 Test 15: Temperature Test

This test applies 12 V and 0.8 A on each of the two positive LDOs and –12 V and 0.8 A on each of the two negative LDOs.

This test also applies a 0.5-V drop on the positive LDO and a 0.5-V drop across the negative LDO.

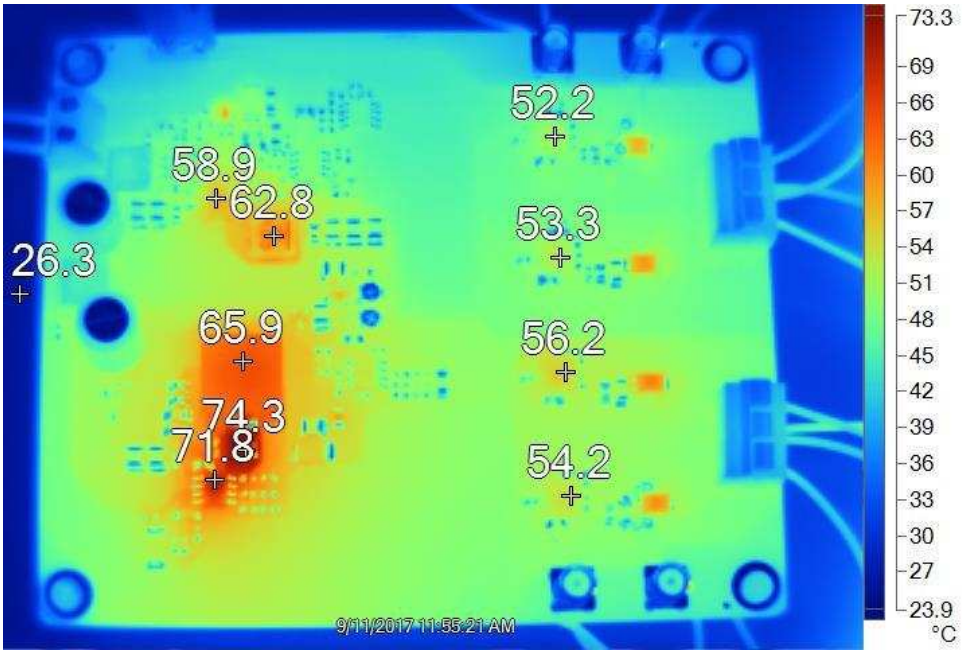


図 38. Temperature Test

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01458.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01458.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01458.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01458.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01458.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01458.

5 Related Documentation

This reference design did not use any related documentation.

5.1 商標

6 About the Author

SANJAY DIXIT is a system architect in the Industrial Systems-Medical Healthcare and Fitness Sector at Texas Instruments, where he is responsible for specifying reference designs.

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