参考資料

TI Designs: TIDA-00638
太陽光インバータ用のアクティブ・ミラー・クランプ付き絶縁ゲート・ドライバのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、専用のゲート・ドライブ用電源を持つ、強化絶縁されたIGBTゲート・ドライバを含む、単一のモジュールです。この小型のリファレンス・デザインは、太陽光インバータのIGBTを制御します。

このデザインは強化絶縁型のIGBTゲート・ドライバと、内蔵のIGBT DESAT検出およびミラー・クランプ保護機能を使用しているため、ゲート・ドライブにユニポーラ電源電圧を使用できます。各ゲート・ドライバ用に、オープン・ループのプッシュプル・トポロジをベースとする電源が存在するため、PCBを柔軟に配線できます。このリファレンス・デザインで使用されるプッシュプル変圧器ドライバは420kHzで動作するため、絶縁トランスのサイズを小さくでき、コンパクトな電源ソリューションを設計できます。このモジュールのピン配置は、TIの太陽光インバータ・プラットフォームのテストに適していますが、スタンドアロンのドライバとしても使用できます。

リソース

TIDA-00638	デザイン・フォルダ
SN6505B	プロダクト・フォルダ
ISO5451	プロダクト・フォルダ
TPS70633	プロダクト・フォルダ
TPS62143	プロダクト・フォルダ

TI E2E™ Community

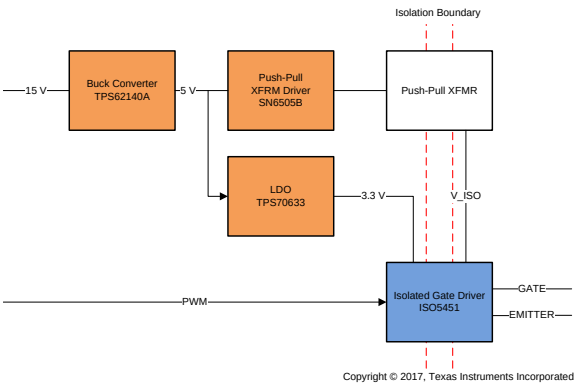
E2Eエキスパートに質問

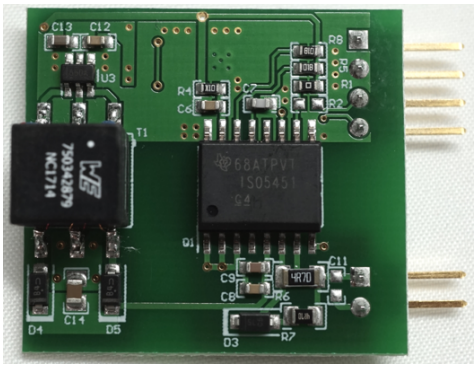
特長

- 低から中電圧のインバータに好適 (400V ACおよび690V AC)
- 内蔵の2.5Aソースおよび5Aシンク電流は、最大50Aの電流によるIGBTモジュールの駆動に最適
- ミラー・クランプ機能を内蔵しているため、IGBTの駆動にユニポーラ電源電圧(17V)を使用可能
- 8000V_{PK}の強化絶縁
- 非常に高いCMTI: 100kV/µs超
- 変圧器ドライバの拡散スペクトラム動作によりEMI放射が低減
- ゲート・ドライバのPWMおよびフォルト信号をコントローラと直接接続可能(3.3V動作)

アプリケーション

- 太陽光ストリング・インバータ
- 太陽光中央インバータ
- 太陽光マイクロ・インバータ
- 電力オプティマイザ





1 System Description

IGBT gate drivers are an inherent part of any three-phase inverter system. High-power inverter systems require isolation for:

- Meeting safety requirements (standards provided in ISO61800-5-1 for variable speed drives). The output power stage of the drive can have dangerously high voltages. Isolation is used to electrically separate the low-voltage operator side from the high-voltage drive stage.
- Driving the top switch of an inverter half bridge. To drive the top switch of an inverter half bridge, the applied gate voltage has to be with respect to the half-bridge phase terminal. This point is floating, meaning the phase terminal switches between the DC bus voltage and the ground.
- Managing voltage level translation. The MCU generates a PWM signal at low-voltage levels such as 3.3 or 5 V. The gate controls required by the IGBTs are in the range of 15 to 20 V and need high-current capability to drive the large capacitive loads offered by those power transistors.
- Avoiding high-current ground loops. High-current ground loops can be localized in the isolated ground plane, which protects the primary-side sensitive electronics from ground bounce and switching noise. This increases EMI and EMC performance by reducing the ground loop area.

This reference design provides a subsystem with a small form factor and a reinforced isolated gate driver for a single- or multi-phase inverter. The design uses the SN6505B push-pull transformer driver for generating the isolated power supply for the ISO5451 gate driver. The reference design offers these key benefits:

- Small size of magnetics due to the high switching speed (424 kHz) of the SN6505B transformer driver
- Integrated active Miller clamp circuit in the ISO5451 gate driver, enabling the use of a unipolar power supply to drive the IGBT
- Low EMI due to spread spectrum clocking of the push-pull transformer driver
- Distributed power supply architecture leading to PCB routing flexibility

1.1 Key System Specifications

表 1. Key System Specifications

SUBSYSTEM	PARAMETER	SPECIFICATION
System specifications	Input power supply voltage	15 V ± 5%
	Digital I/O nominal voltage	3.3 V
Gate driver	Voltage	17 V ± 2 V
	Current	5-A source, 2.5-A sink
	Output power	1W
Isolation	CMTI	100 kV/µs
	Isolation	5 kV_{RMS}
	Working voltage	1400 V_{DC}

2 System Overview

2.1 Block Diagram

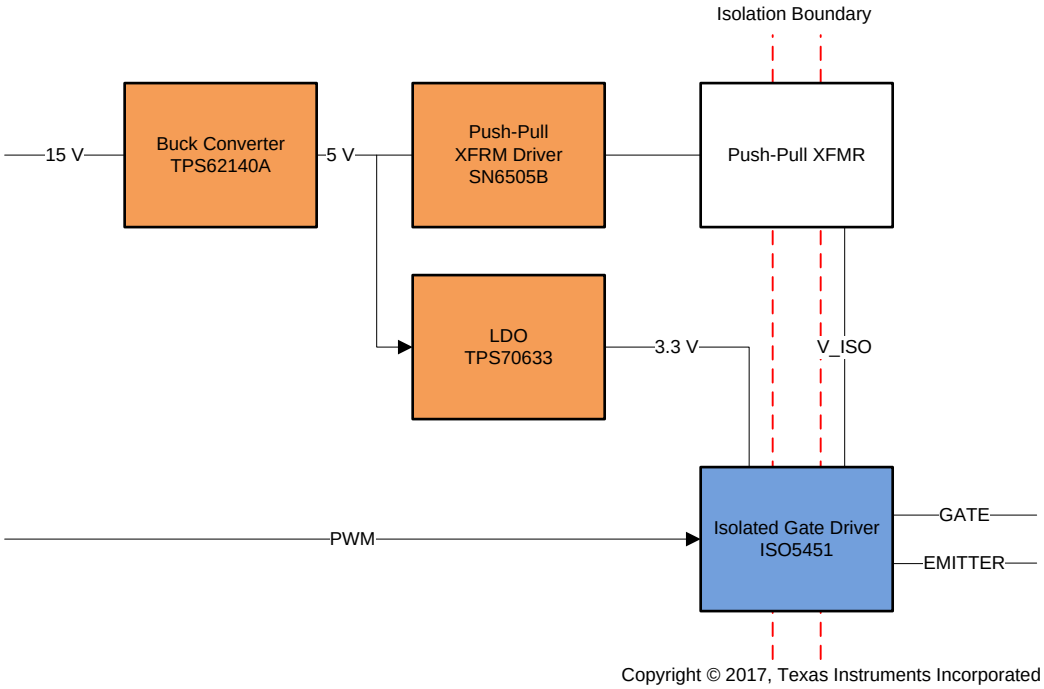


図 1. TIDA-00638 Block Diagram

The TIDA-00638 board consists of two main circuit blocks: the isolated gate driver (ISO5451) and the isolated power supply (SN6505 and transformer) for the gate drive. The primary side of the gate driver is powered from a 3.3-V power supply and the secondary, high-voltage side is powered from a 17-V isolated power supply. The 17-V isolated supply is derived from a 5-V input rail with the help of a push-pull converter. The converter uses the SN6505B push-pull transformer to drive a center tapped transformer to generate an isolated power supply rail.

This gate driver subsystem is specifically designed to be tested in the TI solar inverter evaluation kit. This kit provides a 15-V input to the existing optocoupler based drivers, so some voltage translation is required to power both the SN6505B and ISO5451 (5 V and 3.3 V, respectively). These voltage rails likely already exist on a purpose built test platform, thus the TPS62143 and TPS70633 devices would not be needed.

Due to limitations in the inverter motherboard, only the normal and inverted PWM control signals are brought out through the six pins on the card. The fault detection, reset, and ready features are disabled for the purposes of this evaluation. The PWM connections are capable of being directly connected to a 3.3-V microcontroller like the TMS320 series of digital signal processors.

2.2 Highlighted Products

2.2.1 ISO5451

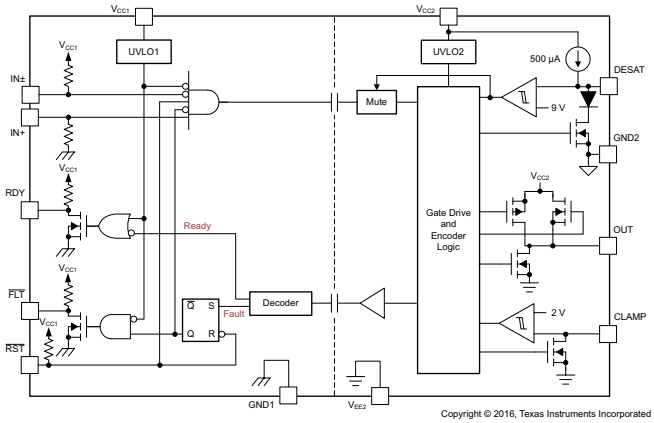


図 2. ISO5451 Functional Block Diagram

- 50-kV/µs minimum and 100-kV/µs typical common-mode transient immunity (CMTI) at V_{CM} = 1500
- 2.5-A peak source and 5-A peak sink currents
- Short propagation delay: 76 ns (typ), 110 ns (max)
- 2-A active Miller clamp
- Output short-circuit clamp
- Fault alarm upon desaturation detection is signaled on $\overline{FLT}$ and reset through $\overline{RST}$
- Input and output undervoltage lockout (UVLO) with ready (RDY) pin indication
- Active output pull-down and default low outputs with low supply or floating inputs
- 3- to 5.5-V input supply voltage
- 15- to 30-V output driver supply voltage
- CMOS compatible inputs
- Rejects input pulses and noise transients shorter than 20 ns
- Operating temperature: –40°C to 125°C ambient
- Isolation surge withstand voltage: 10000-V_{PK}
- Safety-related certifications:
  - 8000-V_{PK} V_{IOTM} and 1420-V_{PK} V_{IORM} reinforced isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5700-V_{RMS} isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - TUV Certification per EN 61010-1 and EN 60950-1
  - GB4943.1-2011 CQC Certification

2.2.2 SN6505B

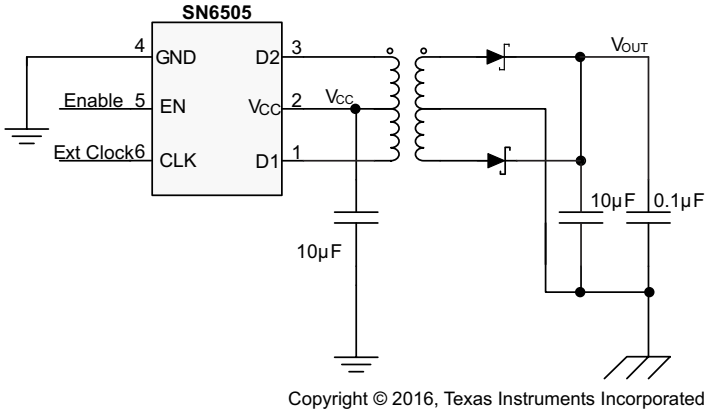


図 3. SN6505B Simplified Schematic

- Push-pull driver for transformers
- Wide input voltage range: 2.25 to 5.5 V
- High output drive: 1 A at a 5-V supply
- Low R_{ON} 0.25 Ω max at a 4.5-V supply
- Ultra-low EMI
- Spread spectrum clocking
- Precision internal oscillator options: 160 kHz (SN6505A) and 420 kHz (SN6505B)
- Synchronization of multiple devices with external clock input
- Slew-rate control
- 1.7-A current limit
- Low shutdown current: < 1 µA
- Thermal shutdown
- Wide temperature range: –55°C to 125°C
- Small 6-pin SOT23/DBV package
- Soft start to reduce in-rush current

2.2.3 TPS706

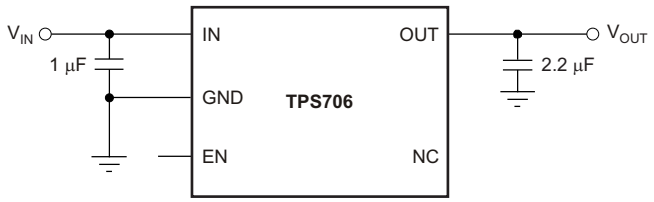


図 4. TPS706 Simplified Schematic

- Input voltage range: 2.7 to 6.5 V
- Ultra-low I_Q: 1 µA
- Reverse current protection
- Low I_{SHDN}: 150 nA
- Supports 200-mA peak output
- Low dropout: 245 mV at 50 mA
- 2% accuracy overtemperature
- Available in fixed-output voltages: 1.2 to 5 V
- Thermal shutdown and overcurrent protection
- Packages: SOT-23-5, WSON-6

2.2.4 TPS62143

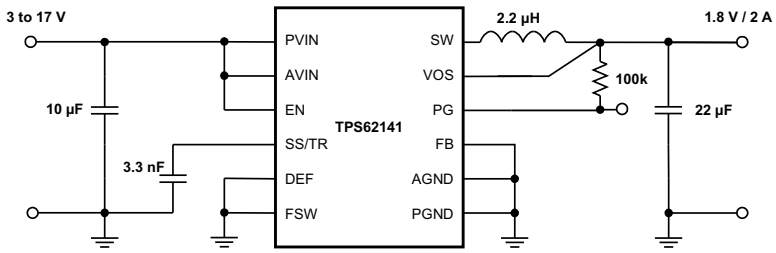


図 5. TPS62143 Simplified Schematic

- DCS-Control™ topology
- Input voltage range: 3 to 17 V
- Up to 2-A output current
- Adjustable output voltage: 0.9 to 6 V
- Pin-selectable output voltage (nominal, 5%)
- Programmable soft start and tracking
- Seamless power-save mode transition
- Quiescent current of 17 µA (typical)
- Selectable operating frequency
- Power-good output
- 100% duty-cycle mode

- Short-circuit protection
- Overtemperature protection
- Pin-to-pin compatible with TPS62130 and TPS62150
- Available in a 3-mm×3-mm, VQFN-16 package

2.3 System Design Theory

2.3.1 Design of Push-Pull Power Supply

This section describes the steps in designing a push-pull power supply with the help of an SN6505B device. 図 6 shows the application circuit. The power supply specifications are given in 表 2.

表 2. Push-Pull Power Supply Specification

PARAMETER	SPECIFICATION
V_{IN}	5 V ± 5%
V_{OUT}	17 V
Output ripple	< 200 mV when sourcing 2.5 A for gate drive
P_{OUT}	1 W

The design requires selection of minimal external discrete components: transformer, rectifier diodes, and input and output bulk capacitors.

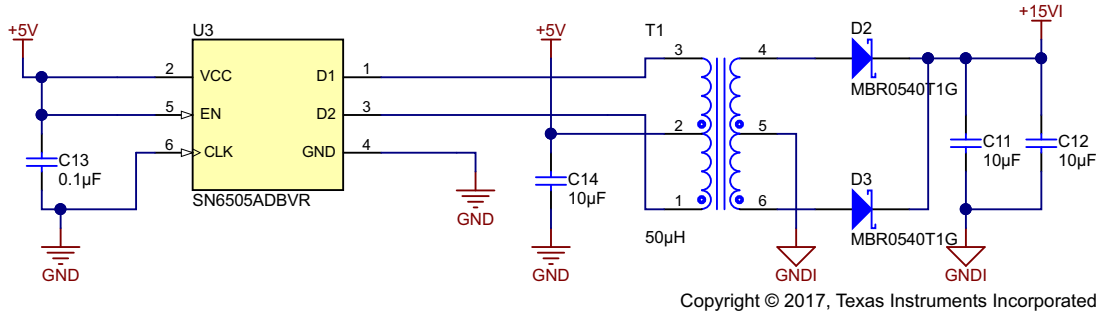


図 6. Isolated Power Supply Based on Push-Pull Topology

2.3.1.1 Design Theory

Push-pull converters use center tap transformers to transfer power from the primary side to the secondary side. 図 7 explains how the push-pull converter functions.

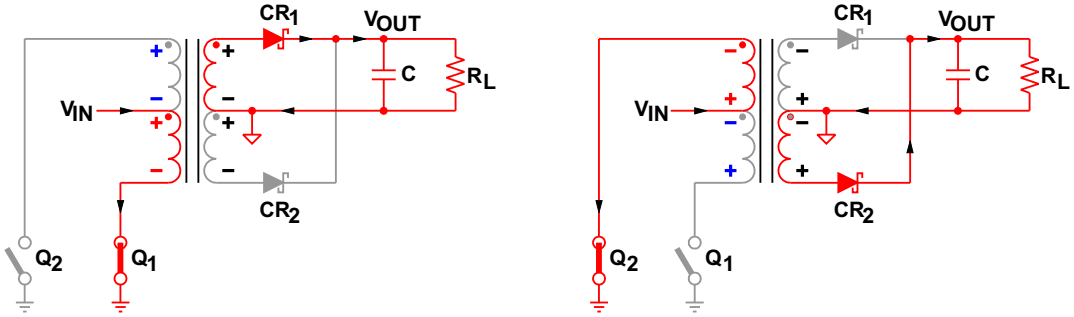


図 7. Push-Pull Converter Theory of Operation

When Q_1 conducts, current is sourced from V_{IN} into the ground through the lower half of the primary of the transformer, creating a negative potential at the lower half of the primary winding compared to the primary center tap. To maintain the previously established current through Q_2, which has now been opened, the upper half of the primary winding turns positive compared to the primary center tap. This voltage transfers to the transformer secondary according to the dot convention and the turns ratio of the transformer. CR_1 is now forward biased and CR_2 is reverse biased, causing a current to flow through the upper half of the secondary winding, passing through CR_1 into C, charging the capacitor and returning into the secondary center tap.

Similarly, when Q_2 conducts the voltage, polarities at the primary and secondary reverse. CR_1 is reverse biased and CR_2 is forward biased, which causes a current to flow from the bottom half of the secondary through CR_2 into C, charging the output capacitor and returning into the center tap of the transformer. Q_1 and Q_2 switch alternatively, with approximately 50% duty cycle to transfer power from the primary to the secondary of the transformer.

Before either switch is turned on, there must be a short period during which both transistors are high impedance. Known as break-before-make time, this short period is required to avoid shorting out both ends of the primary.

Another important aspect of push-pull designs is transformer core magnetization. 図 8 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts, the magnetic flux is pushed from A to A'. When Q_2 conducts, the flux is pulled back from A' to A. The difference in flux and in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, applied to the primary: $B = V_P \times t_{ON}$.

The volt-seconds (V-t) product determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results in an offset from the origin of the B-H curve. Unless balance is restored, the offset increases with each following cycle and the transformer slowly moves towards the saturation region.

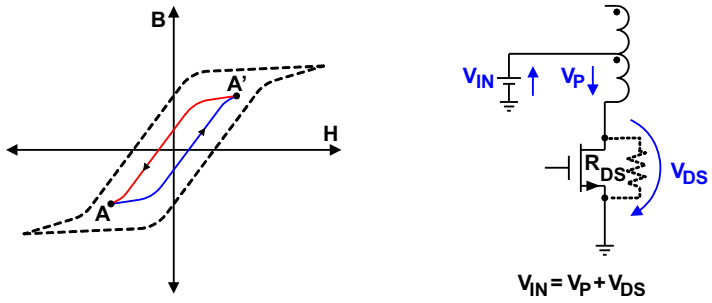


図 8. Push-Pull Transformer Core Magnetization and Self Regulation Through Positive Temperature Coefficient of R_{DSon}

The SN6505 push-pull transformer driver has integrated MOSFET switches. The positive temperature coefficient of these switches has a self-correcting effect on the V-t imbalance. During a slightly longer ontime, the prolonged current flow through a FET gradually heats the MOSFET, which leads to an increase in R_{DSon}. The higher resistance then causes the drain-source voltage, V_{DS}, to increase. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, V_P is gradually reduced and V-t balance is restored.

2.3.1.2 Rectifier Diode Selection

To increase the efficiency of the push-pull forward converter, minimize the forward voltage drop of the secondary side rectifier diodes. Because the SN6505B is a high-frequency switching converter, the diode must possess a short recovery time. Schottky diodes are selected as they meet the requirements of low forward voltage drop and fast recovery time. The diode must withstand a reverse voltage of twice the output voltage.

In this reference design, the nominal reverse voltage across the diode is 34 V. For 1 W at an output voltage of 17 V, the output current is approximately 60 mA. 図 9 shows the diode MBR0540T1G forward characteristics. The diode has a forward voltage drop of less than 0.39 V at 25°C. The reverse DC blocking voltage rating of this diode is 40 V.

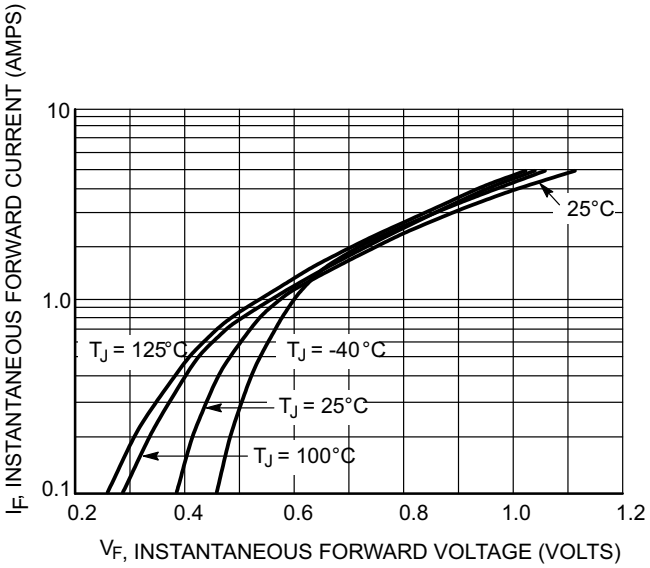


図 9. Instantaneous Current Versus Forward Voltage Drop

2.3.1.3 Capacitor Selection

Two capacitors are required at the input V_{CC} of SN6505B. A ceramic bypass capacitor of 100 nF is needed close to the power supply pin of the device for noise decoupling because the device is a high-speed CMOS device. Another bulk capacitor is needed at the center tap pin of the primary of the transformer. Large currents are drawn from this capacitor into the primary during the fast switching transients. For minimum ripple, select a 10-µF ceramic capacitor.

A bulk capacitor is required at the rectifier output stage to smooth the output voltage. The specification for the output voltage ripple is 200 mVpp. The maximum current that will be drawn out of this capacitor is 2.5 Apk, which is the gate sourcing capability of the gate driver. 式 1 shows how the capacitance required to meet this specification is calculated.

$$C \geq i \times d t d v = 2 . 5 A \times 0 . 5 \mu s 200 m V = 6 . 25 \mu F \quad (1)$$

Approximately, a 10-µF capacitor meets the ripple requirement. The DC bias effect must be considered when selecting the capacitor. 図 10 shows that for the C3216X7R1V106M160AC capacitor used in this design, the capacitance at 17 V calculates to 4.3 µF. Hence two capacitors are connected in parallel to achieve the required capacitance.

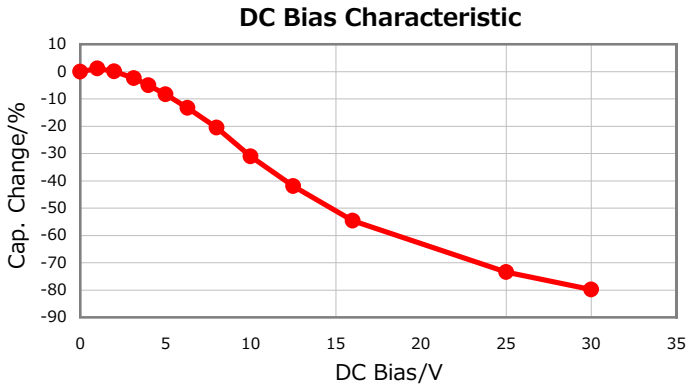


図 10. Variation of Capacitance With Applied DC Bias for C3216X7R1V106M160AC

2.3.1.4 Transformer Selection

表 3 lists the required specifications of the push-pull transformer, and the subsequent sections explain V-t product and turns ratio calculation.

表 3. Transformer Requirements

PARAMETER	SPECIFICATION
Output power	1 W
Output voltage	17 V
Input voltage	5 V
Minimum operating frequency	348 kHz
Working voltage	1400-V DC
Minimum creepage distance	9.2 mm (per IEC61800-5-1)
Minimum clearance distance	8 mm (per IEC61800-5-1)
Insulation	Reinforced
Operating temperature range	-40°C to 125°C

2.3.1.4.1 V-t Product Calculation

The V-t product of the transformer must be greater than the maximum V-t product applied by the SN6505B. Failure to meet this criteria leads to transformer core saturation. 式 2 calculates the worst case V-t product applied by SN6505B to the transformer:

$$V t m i n \geq V I N \_ m a x \times T m a x 2 = V I N \_ m a x 2 \times f m i n V t m i n = 5 . 25 V 2 \times 348 . 48 k H z = 7 . 53 \mu s \quad (2)$$

- V_{IN-max} is the maximum input voltage = 5 V + 5% = 5.25 V
- f_{min} is the minimum frequency of operation = $F_{sw-min} – \Delta F_{sw}$ = 363 kHz – 14.52 kHz = 348.48 kHz
- F_{sw-min} is the minimum switching frequency of SN6505B = 363 kHz
- ΔF_{sw} is the spread spectrum frequency spread = 4% of F_{sw} = 4% of 363 kHz = 14.52 kHz

Spread spectrum frequency spread (ΔF_{sw}) is the variation of switching frequency around the average to reduce EMI. Depending on the device, the frequency spreading can have different profiles such as:

- sawtooth
- sinusoidal
- Hershey

- triangular

Spread spectrum clock modulation frequency (F_{SSC}) is the frequency at which frequency spreading (ΔF_{sw}) occurs. 図 11 shows an example triangular frequency spreading profile that explains the parameters of ΔF_{sw} and F_{SSC}.

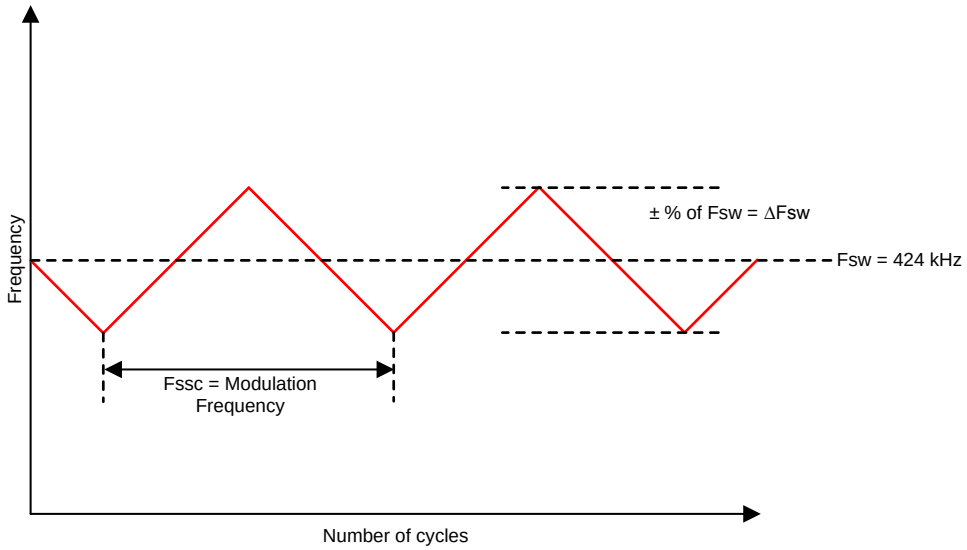


図 11. Modulation Frequency and Spread Spectrum Frequency

2.3.1.4.2 Turns Ratio Calculation

Calculate the turns ratio of the transformer based on the input and output voltage, the output diodes forward drop, and the ON resistance of the input switches. The following calculation assumes the transformers typical efficiency of 97%:

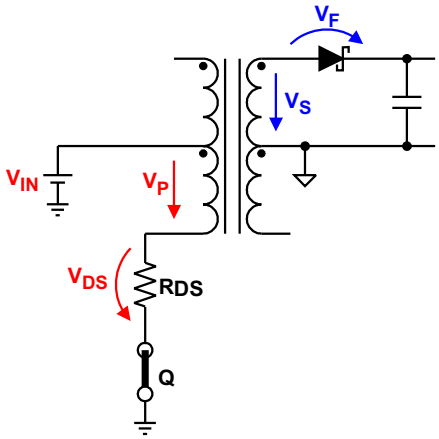


図 12. Establishing Turns Ratio

式 3 provides the output voltage of the converter:

$$V_{OUT\_nom} = V_{S\_nom} - V_f \Rightarrow V_{S\_nom} = V_{OUT\_nom} + V_f \quad (3)$$

- V_f is the forward voltage drop of the rectifier diode
- V_S is the voltage across the top half of the secondary of the transformer

式 4 calculates the voltage across the lower half of the primary coil of the transformer:

$$V_{P\_nom} = V_{IN\_nom} - V_{dsVP\_nom} = V_{IN\_nom} - (I_{P\_nom} \times R_{DS\_on}) \quad (4)$$

- V_{DS} is the voltage drop across the integrated low-side switch in SN6505B
- I_P is the current through the primary
- R_{DSon} is the on resistance of the integrated low-side switch in SN6505B

式 5 determines the turns ratio of the transformer. The factor 0.97 accounts for typical transformer power transfer efficiency.

$$V_{s\_nom} = V_{P\_nom} \times n_{nom} \times 0.97 \Rightarrow n_{nom} = 1.031 \times \frac{V_{S\_nom}}{V_{P\_nom}} \quad (5)$$

式 6 is derived by substituting 式 3 and 式 4 in 式 5. The turns ratio of the transformer is calculated to be 3.5.

$$n_{nom} = 1.031 \times \frac{V_f + V_{OUT\_nom}}{V_{IN\_nom} - I_{P\_nom} \times R_{DS\_on}} = 1.031 \times \frac{0.35 + 17}{5 - (0.1 \times 0.16)} = 3.58 \, nsnp \quad (6)$$

- R_{DSon} = 0.16 Ω is the typical value of the switch ON resistance taken from the SN6505B datasheet (SLLSEP9)
- $I_{P\text{-}nom}$ is calculated at 50% load; $I_{p\text{-}nom} = P_{IN} / V_{IN}$ = 0.5 W / 5 = 0.1 A

A Wurth Electronics transformer, 750342879, is selected for this reference design. 表 4 provides the specifications of this transformer:

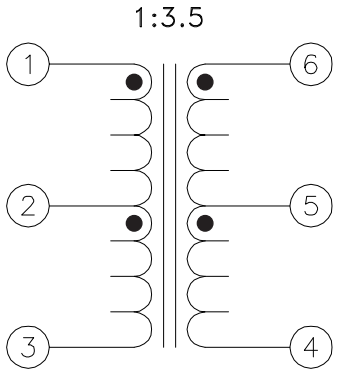


図 13. Push-Pull Transformer—750342879 (Wurth Electronics)

表 4. Selected Transformer Specifications

PARAMETER	SPECIFICATION
Turns ratio (6 – 4):(1 – 3)	3.5:1, ±2%
DC resistance (1 – 3)	0.33 A_{max} at 20°C
DC resistance (6 – 4)	0.75 A_{max} at 20°C
Inductance (1 – 2)	50 µH min at 100 kHz, 10-mV AC
Dielectric (1 – 6)	3000 V_{RMS}, 1 minute
Operating temperature range	–40°C to 125°C
Creepage distance (IEC61800-5-1)	9.2 mm
Clearance distance (IEC61800-2)	8 mm
Transformer dimensions	12.7 mm × 9.14 mm × 7.62 mm (see 図 14)

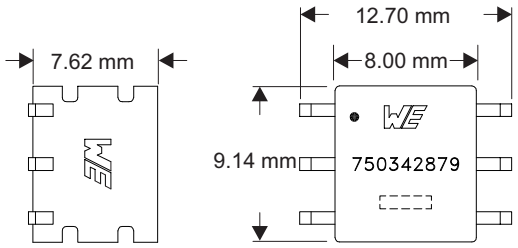


図 14. Transformer Dimensions in mm

2.3.2 Gate Driver Design

表 5 lists the gate driver requirements.

表 5. Gate Driver Specifications

PARAMETER	SPECIFICATION
Primary-side input voltage	3.3 V ± 5%
Secondary-side input voltage	17 V ± 2 V
Source current capacity for gate drive	2.5 A_{max}
Sink current capacity for gate drive	5 A_{max}
Maximum output switching frequency	16 kHz
Maximum secondary-side output power	1 W
Maximum output power to gate	0.85 W
Miller clamp functionality	Yes

注: To operate above 16 kHz, select gate resistors with a higher wattage as per 2.3.2.2.2.

The ISO5451 meets all the requirements in 表 5. 図 15 implements the reinforced isolated gate driver using the ISO5451:

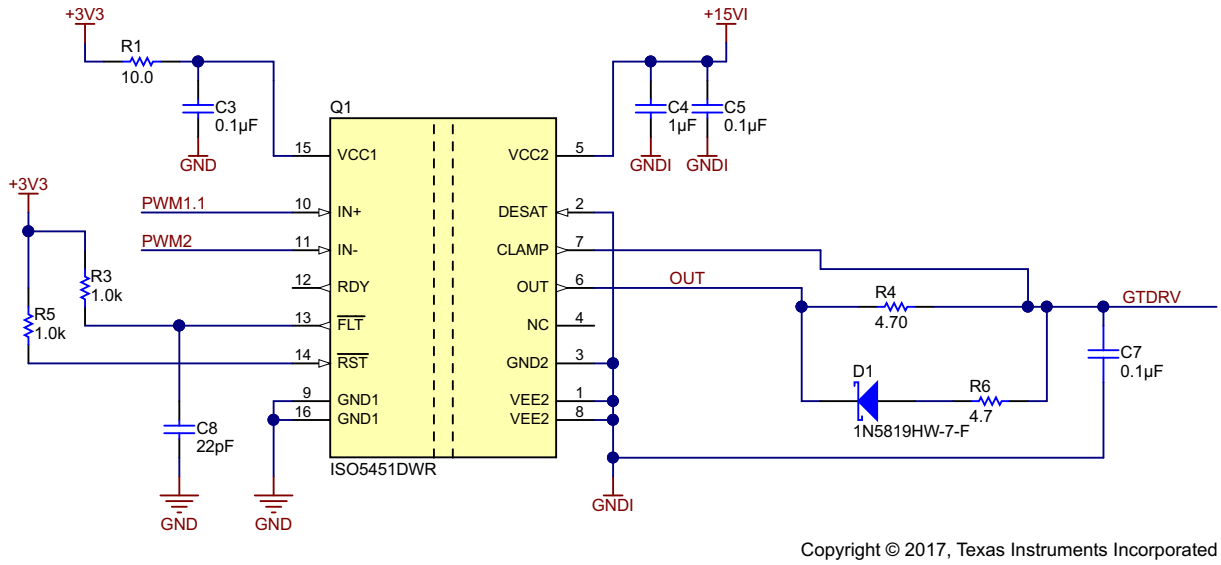


図 15. Isolated Gate Driver Circuit

2.3.2.1 through 2.3.2.5 describe in detail the steps for selecting gate driver components.

2.3.2.1 Power Supply Capacitors

A 3.3-V power supply powers the primary side of the ISO5451. An RC filter filters this 3.3-V rail before connecting to the gate driver power supply.

A 17-V isolated supply rail powers the secondary side of the ISO5451, which is generated from the push-pull power stage described in 2.3.1. A 1-µF bulk capacitor connects beside the VCC2 pin. The gate source current draws from this power pin and the 1-µF bulk capacitor provides large transient current during the switching transient until the power supply capacitors start supplying the current. The design recommends a 0.1-µF high-frequency noise decoupling capacitor on the VCC2 pin.

2.3.2.2 Gate Resistor Selection

When designing gate drivers, selecting the right gate resistor is an important part of the process. The value of the gate resistor affects the following parameters:

- IGBT turnon and turnoff times
- Switching losses
- dv/dt across the IGBT collector to emitter
- di/dt of the IGBT current
- EMI due to IGBT switching

Increasing the value of the gate resistor increases the turnon and turnoff times of the IGBT, which in turn reduces the dv/dt and di/dt, causing reduced EMI. Higher gate resistance also increases switching losses. Decreasing the gate resistance reduces switching losses but increases EMI.

2.3.2.2.1 Gate Resistor Calculation

In this reference design, the gate resistors selected provide a maximum gate source current of 2.5 A_{pk} and a maximum sink current of 5 A_{pk}. The source and sink currents are controlled independently using the gate drive circuit.

図 16 shows the simplified model of the charging phase of the IGBT gate capacitance:

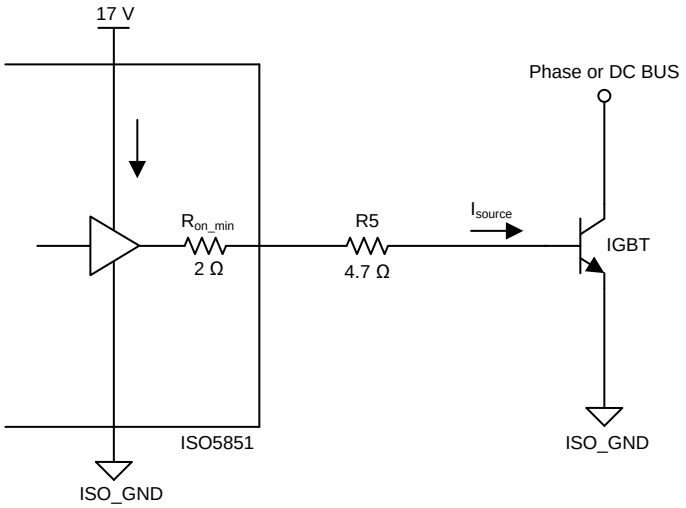


図 16. Simplified Output Model During IGBT Turnon Phase

式 7 calculates the gate resistance required to maintain a peak turnon current of 2.5 A:

$$Rg\_on = ron\_min + R5 = V \, Ipeak\_on = 17 \, V \, 2.5 \, A = 6.8 \, \Omega \, R5 = 6.8 \, \Omega - 2 \, \Omega = 4.8 \, \Omega \quad (7)$$

Select R5 = 4.7.

- Rg_{on} is the gate resistance during IGBT switch on phase
- V is the voltage applied to the gate of the IGBT
- I_{peak_on} is the peak current during turnon
- r_{on_min} is the minimum internal on resistance of the gate driver

図 17 shows the simplified model of the discharging phase of the IGBT gate capacitor:

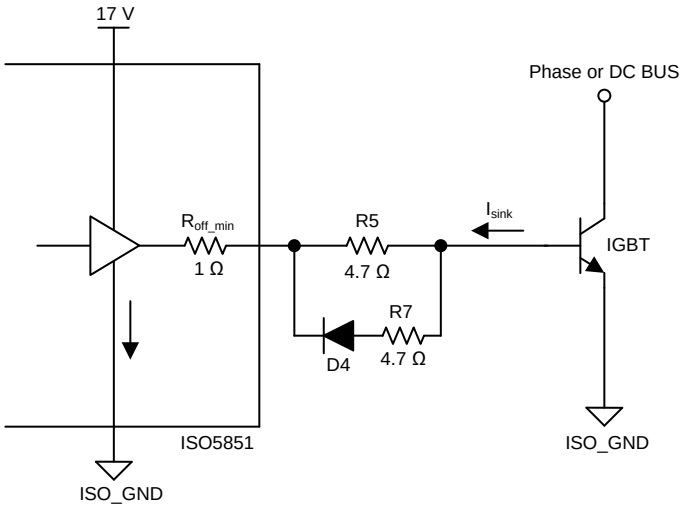


図 17. Simplified Output Model During IGBT Turnoff Phase

式 8 calculates the gate resistance required to maintain a peak turnoff current of 5 A:

$$R_{g\_off} = r_{off\_min} + R5 \;//\; R7 = V_{Ipeak\_off} = 17\,V / 5\,A = 3.4\,\Omega \quad R5 \;//\; R7 = 3.4\,\Omega - 1\,\Omega = 2.4\,\Omega \Rightarrow R7 = 4.9\,\Omega \tag{8}$$

Select R7 = 4.7 Ω.

- R_{goff} is the gate resistance during IGBT switch off phase
- V is the voltage applied to the gate of the IGBT
- I_{peak_off} is the peak current during turnoff
- r_{off_min} is the minimum internal off resistance of the gate driver

2.3.2.2.2 Gate Resistor Dimensioning

式 9 calculates the approximate power required to drive an IGBT gate:

$$P_g = Q_g \times V_g \times f_{SW} \tag{9}$$

- P_g is the gate power required
- Q_g is the gate charge required
- Q_g can be found from the typical gate charge curve of an IGBT module, or if the gate charge curve is not provided in the datasheet, approximately calculate Q_g by multiplying the gate capacitance by the gate voltage swing.
- F_{sw} is the gate switching frequency

This design uses a 100-nF capacitor to simulate the gate emitter capacitance of the IGBT.

式 10 calculates the gate charge:

$$Q_g = C_g \times V_g = 100\,nF \times 17\,V = 1.7\,\mu C \tag{10}$$

式 11 calculates power dissipated:

$$P_g = Q_g \times V \times f_{SW} = 1.7\,\mu C \times 17\,V \times 16\,kHz = 0.4624\,W \tag{11}$$

Assuming symmetrical on and off loses:

- Turnon gate power = 0.2312 W

- Turnoff gate power = 0.2312 W

Referring 図 16, calculate the wattage of R5 during turn-on by 式 12:

$$P_{R5\_on} = Turn\ on\ gate\ power \times \frac{R5}{R5 + r_{on\_min}} = 0.2312 \times \frac{4.7}{4.7 + 2} = 0.1622\ W \quad P_{R5\_on\_peak} = I_{source2} \times R5 = 2.462 \times 4.7 = 28.44 \quad (12)$$

Referring to 図 17, calculate the wattage of R5 and R7 during turnoff by using 式 13:

$$P_{R5\_off} + R7\_off = Turn\ off\ gate\ power \times \frac{R5 \,//\, R7}{R5 \,//\, R7 + r_{off\_min}} = 0.2312 \times \frac{2.35}{2.35 + 1} = 0.1622\ W \quad R_{R5\_off} = P_{R5\_off} + R7\_off2 = 0.081\ W \quad P_{R5\_off\_peak} = I_{sink2} \times R5 = 2.462 \times 4.7 = 28.44\ W \quad (13)$$

P_{R5_off} is the average power dissipated in R5 during IGBT turnoff.

PR5_off_peak is the peak pulse power dissipated in R5 during IGBT turnoff.

$$P_{R7\_off} = P_{R5\_off} + R7\_off2 = 0.081\ W \quad P_{R7\_off\_peak} = I_{sink2} \times R7 = 2.462 \times 4.7 - 28.44\ W \quad P_{R5} = P_{R5\_on} + P_{R5\_off} = 0.1622\ W + 0.081\ W = 0.2432\ W \quad P_{R5\_peak} = P_{R5\_on\_peak} + P_{R5\_off\_peak} = 28.44\ W + 28.44\ W = 56.88\ W \quad (14)$$

The selected resistors must have the capability to handle the average power and the high peak pulse power as calculated in 式 14.

Select R5 = 4.7 Ω, 0.333 W, 1206 package. Select RPC1206JT4R670.

Select R7 = 4.7 Ω, 0.25 W, 0805 package. Select RPC0805JT4R70.

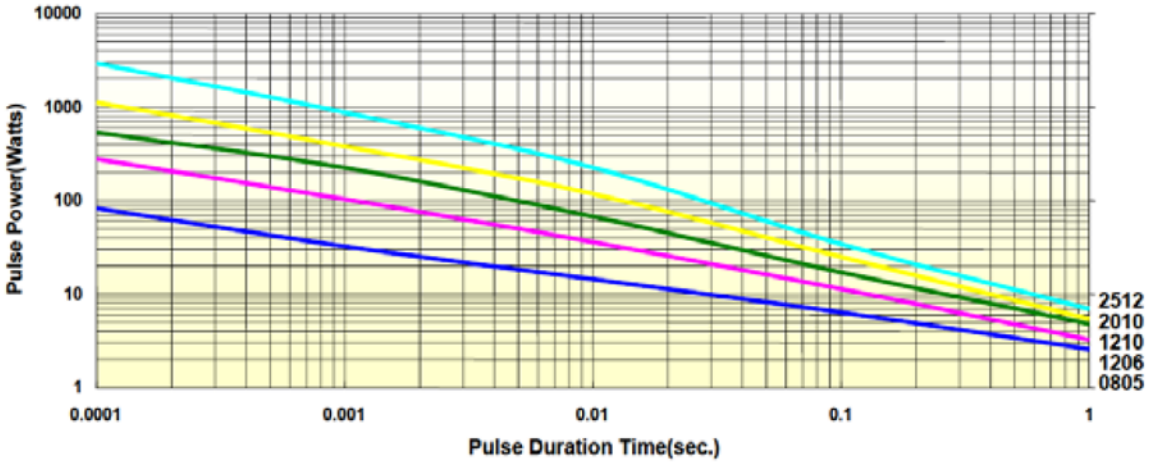


図 18. Peak Power versus Duration of Power Pulse of Selected Resistors

図 18 presents that the 0805 package has a peak power rating of 90 W and the 1206 package has a peak power rating of 300 W for a 100-µs pulse. The continuous pulse load graph in 図 18 is obtained by applying repetitive rectangular pulses where the pulse period is adjusted so that the average power dissipated in the resistor is equal to its rated power at 70°C.

式 15 infers the maximum allowed frequency of operation:

$$P_{avg} = P_{peak} \times duty\ cycle = P_{peak} \times t_{pulse\ width} \times f_{sw} \quad f_{sw} = \frac{P_{avg}}{P_{peak} \times t_{pulse\ width}} \tag{15}$$

- P_{avg} is the rated power of the resistor
- P_{peak} is the peak pulse power dissipated in the resistor
- $t_{pulsewidth}$ is the width of the applied pulse
- F_{sw} is the frequency of operation that is the frequency at which the pulses are repeated

図 19 shows the exponential nature of peak power waveforms for gate drive signals. The exponential waveforms are converted into equivalent rectangular pulses, the width of which is equal to half of RC time constant of the exponential waveform. The gate resistor and the gate capacitance determines the RC time constant of the waveform.

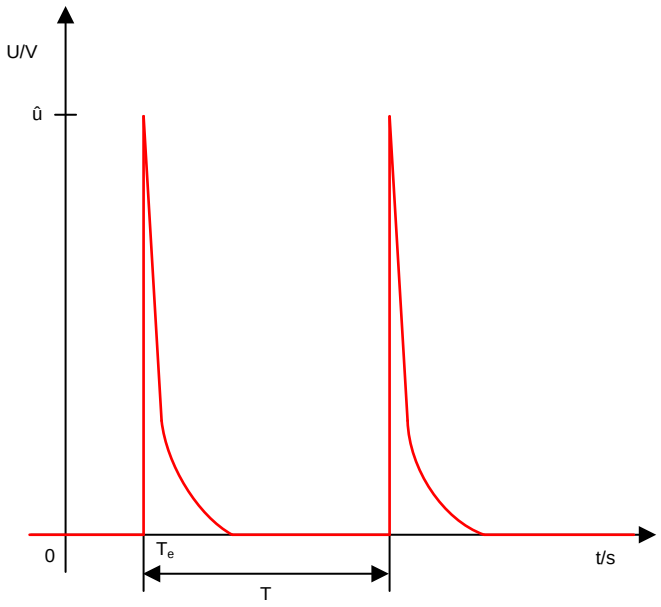


図 19. Exponential Nature of Peak Pulse Power Waveforms

$$\frac{1}{2}\tau_e = \frac{1}{2} R C = \frac{1}{2} \times 4.7\ \Omega \times 0.1\ \mu F = 0.235\ \mu s \tag{16}$$

The pulse width of the equivalent rectangular pulse with amplitude equal to the peak pulse power is 0.235 µs, which has the same power content as the exponential pulse. The values in 図 18 are comparable using this parameter.

For resistor R5 from 図 18, 300 W is the peak pulse power at a 100-µs pulse width, assuming a minimum of 300-W peak pulse power for 0.235 µs.

$$f_{sw} = \frac{0.33\ W}{300\ W \times 0.235\ \mu s} = 4.68\ kHz \tag{17}$$

Resistor R5 can dissipate 300-W pulses of width 0.235 µs at 4.68 kHz. 式 18 calculates the maximum frequency of operation from 56.88-W pulses of the same width.

$$f_{sw} = \frac{0.33\ W}{56.88\ W \times 0.235\ \mu s} = 24.68\ kHz \tag{18}$$

The selected resistor is suitable for operation at 16 kHz.

Similarly for R7 from 図 18, 90 W is the peak pulse power at a 100-µs pulse width, assuming a minimum of 90-W peak pulse power for 0.235 µs.

$$f_{sw} = \frac{0.25\ W}{90\ W \times 0.235\ \mu s} = 11.82\ kHz \tag{19}$$

Resistor R7 can dissipate 90-W pulses of width 0.235 μs at 11.82 kHz. 式 20 calculates the maximum frequency of operation for 28.44-W pulses of the same width.

$$f_{sw} = 0.25\ W \,/\, 28.44\ W \times 0.235\ \mu s = 37.40\ kHz \quad (20)$$

The selected resistor is suitable for operation at 16 kHz.

2.3.2.3 Miller Clamp Circuit

The collector transient voltage can get coupled to the gate of the IGBT through the parasitic Miller capacitance, leading to false turnon of the IGBT if no negative voltage is applied to the gate. Using an active Miller clamp integrated into the ISO5451 resolves this issue. The Miller clamp provides a low-impedance path to ground. The integrated Miller clamp activates when the IGBT is turned off and the gate voltage transitions below 2 V.

A Miller clamp in the gate driver allows the use of a unipolar gate drive supply instead of a bipolar gate drive supply, thus simplifying the power supply design, causing a lower size solution at a reduced cost and smaller board size.

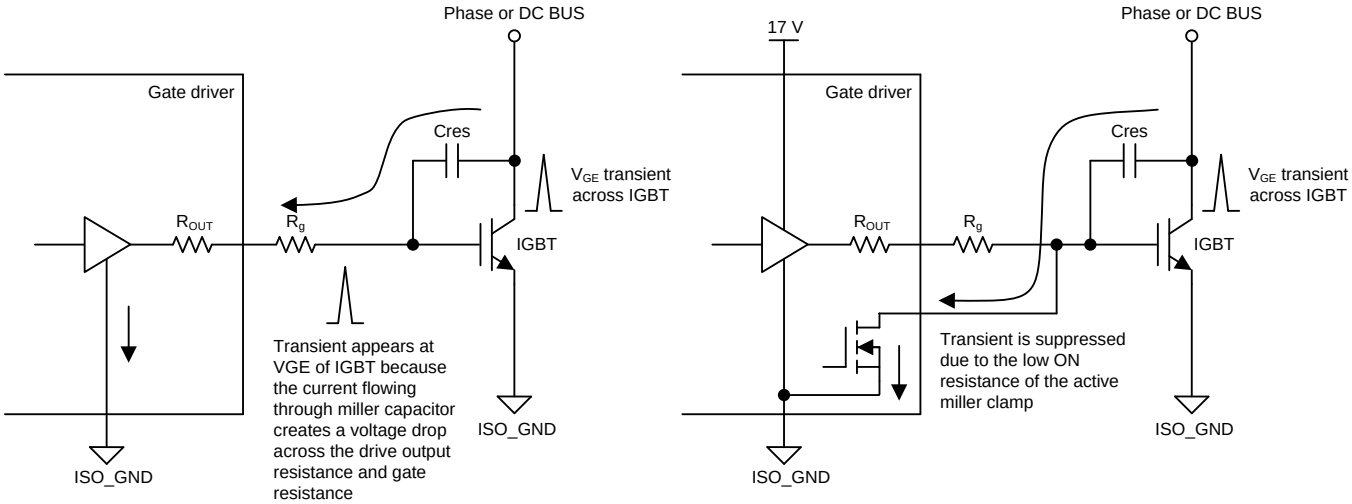


図 20. With and Without Miller Clamp

For the Miller clamp to be effective, the induced current must be less than the Miller clamps current sinking capability. 式 21 calculates the induced current:

$$i = C_{res} \times dV_{CE}/dt \quad (21)$$

Where:

- C_{res} is the reverse transfer capacitance of the IGBT
- dV_{CE}/dt is the rate of change of voltage across the IGBT collector to emitter

2.3.2.4 Control Inputs

The ISO5451 device has two control inputs: the non-inverting and inverting input. The inverting input connects to primary ground and the non-inverting input connects to the microcontroller. Use low-impedance signal sources to avoid unwanted switching of the ISO5451 driver under extreme common-mode transient conditions. Therefore, the control input must be driven by standard CMOS push-pull drivers; avoid passive circuits like open-drain configurations using pull-up resistors. Glitches up to 20 ns on the control inputs are filtered by an on-chip glitch filter.

2.3.2.5 Dynamic Output Power

The maximum allowed total dynamic power consumption PD for ISO5451 is 700 mW at 85°C. This includes the input quiescent power PID, the output quiescent power POD, and the output power under load P_{OL}.

$$PD = PID + POD + POL \quad PID = V_{CC1\_max} \times I_{CC1\_max} = 5.25\,V \times 4.5\,mA = 23.63\,mW \tag{22}$$

- V_{CC1_max} is the maximum input voltage for the primary-side power supply
- I_{CC1max} is the maximum primary-side input quiescent current

$$POD = V_{cc2} - V_{EE2} \times I_{CC2\_max} = 16.5\,V = 0\,V \times 6\,mA = 99\,mW \tag{23}$$

- V_{CC2_max} is the maximum input voltage for the secondary-side power supply
- I_{CC2_max} is the maximum secondary-side input quiescent current

式 24 calculates the power dissipation budget available for the ISO5451 device under load:

$$POL = PD - PID - POD = 700\,mW - 23.63\,mW - 99\,mW = 577\,mW \tag{24}$$

式 25 calculates the worst case actual power loss under load:

$$POL\_WC = 0.5 \times f_{INP} \times Q_g \times V_{CC2} - V_{EE2} \times R_{on\_max} r_{on\_max} + R_{g\_on} + r_{off\_max} r_{off\_max} + R_{g\_off} \tag{25}$$

Where:

- f_{INP} is the signal frequency at the control input
- Q_g is the gate charge of IGBTVCC2 is the positive output supply with respect to secondary ground
- V_{EE2} is the negative output supply with respect to secondary ground
- r_{on_max} is the worst case output resistance of the internal switch in the on-state
- r_{off_max} is the worst case output resistance of the internal switch in the off-state
- R_{gon} is the external gate resistance during the switch-on phase
- R_{goff} is the external gate resistance during the switch-off phase

Verify from 式 24 and 式 25 that $P_{OL} – WC < P_{OL}$.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

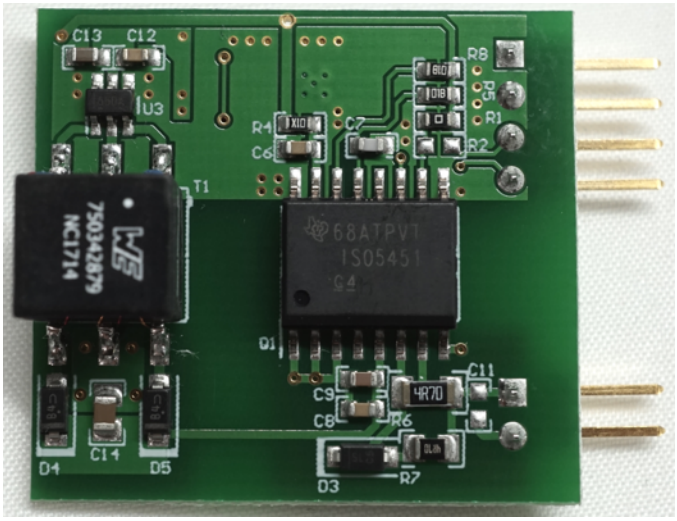


図 21. TIDA-00638 PCB

図 21 shows the full design solution, measuring 1170 mil × 1290 mil (discounting the interface pins). The two main functional elements highlighted in this design are the isolator push-pull power supply on the left of the board as shown, and the isolated gate driver on the right. The power supplies for the 5-V and 3.3-V rails are on the reverse side of the board, but relatively inconsequential to the overall design.

The TIDA-00638 board is designed to interface with the TI C2000™ Solar DC/AC Single Phase Inverter. The interface is a 10-pin header array containing the signals listed in 表 6.

表 6. C2000 Solar DC/AC Single-Phase Inverter Gate Driver Interface

PIN	FUNCTION
1	15-V input
2	GND
3	15-V controllable with jumper resistors R1, R2, R12, and R13
4	PWM
5	GND
6	N/A
7	N/A
8	N/A
9	IGBT gate
10	IGBT emitter

The C2000 Solar DC/AC Inverter EVM uses an opto-isolator based gate driver by default, and as such, has a ULN2003 HV Darlington array, which drains voltage from the low-side of the opto-isolator input. To work around this and have just the required PWM signal input to the ISO5451, resistors R1, R2, R12, and R13, along with U1, are removed from the inverter, and the signals are brought straight to the gate driver interface.

The solar inverter also has gate drive resistor networks on the main board for all IGBTs. To accommodate the drive resistors moving to the card, resistors R8, R9, R10, R11, R17, R18, R19, and R20 are removed. R10, R11, R19, and R20 are then replaced with shorting links. This enables the TIDA-00638 to be inserted into the socket and operate without modification.

All measurements in the following section were captured with a Keysight DSO3024A oscilloscope.

3.1.2 Software

The software used to test the inverter functionality is available with the C2000 Solar DC/AC Single Phase Inverter reference design. The steps from the associated getting started guide were followed to bring up the inverter functionality in an off-grid configuration.

3.2 Testing and Results

3.2.1 Push-Pull Power Supply

For all tests of the push-pull power supply, an external 5-V source is used to isolate any induced ripple to the supply itself.

3.2.1.1 Secondary-Side Output Voltage

The secondary side of the isolated power supply is measured at both no load and full load (1 W). The output is illustrated in 図 22 to 図 26.

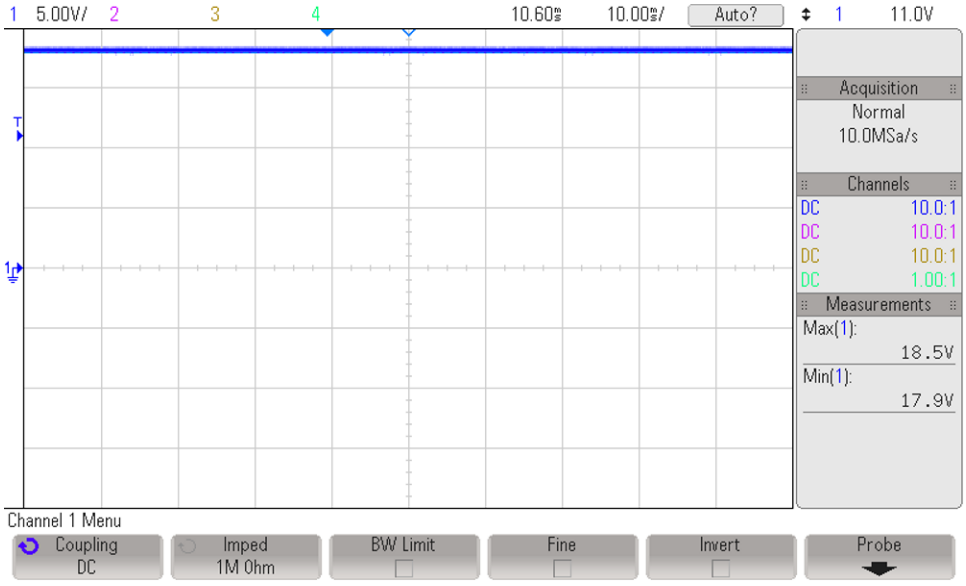


図 22. Output Voltage at No Load

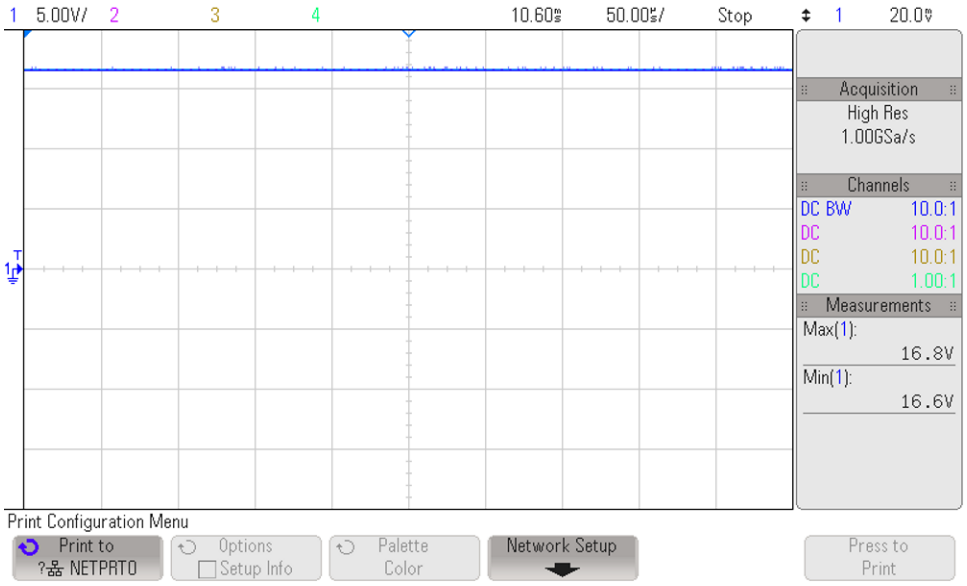


図 23. Output Voltage at Full Load

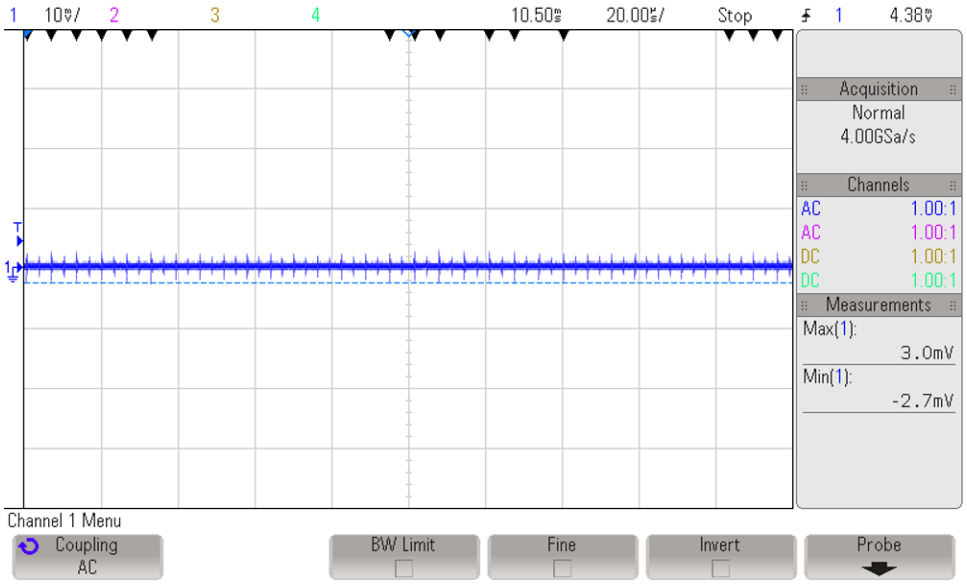


図 24. Output Voltage Ripple at No Load

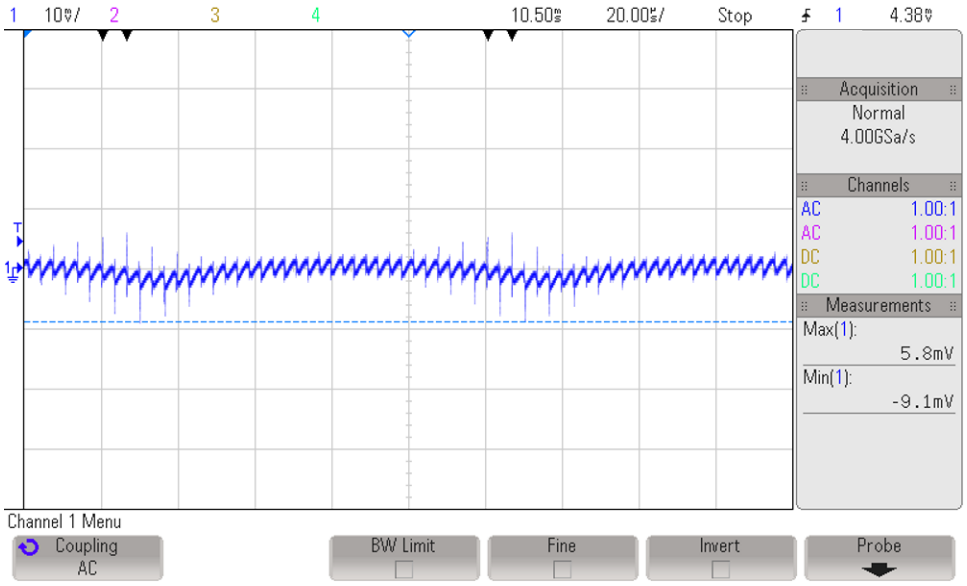


図 25. Output Voltage Ripple at Full Load

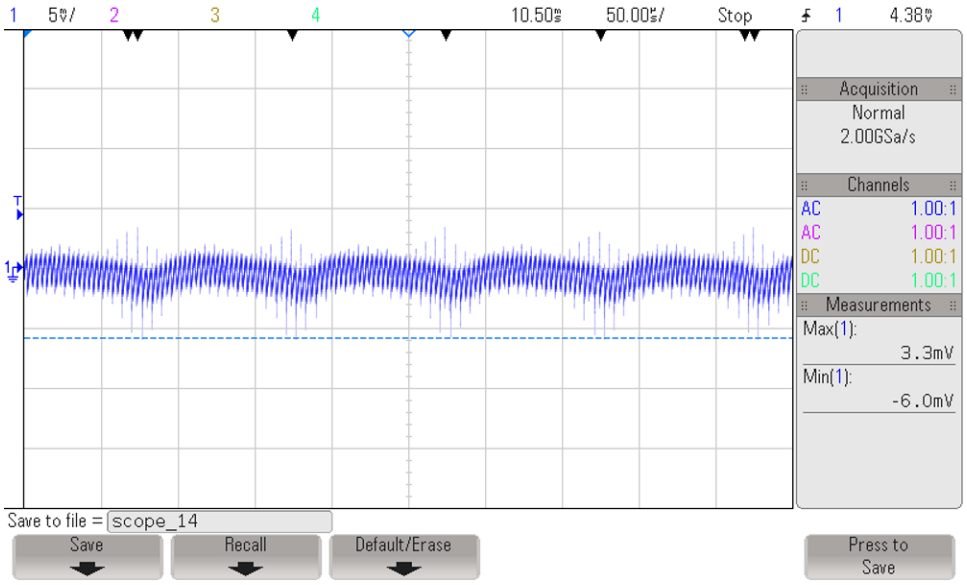


図 26. Output Voltage Ripple Due to Spread Spectrum Modulation at Full Load

3.2.1.2 3.3-V Output of TPS70633

The 3.3-V output of the LDO generating the power for the primary side of the ISO5451 is illustrated in 図 27 and 図 28.

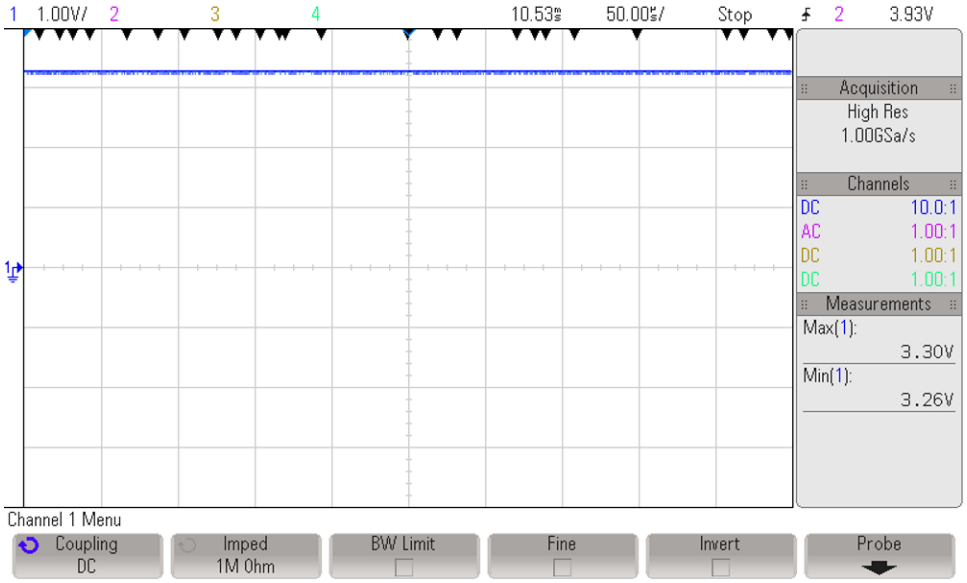


図 27. TPS70633 Output DC Voltage

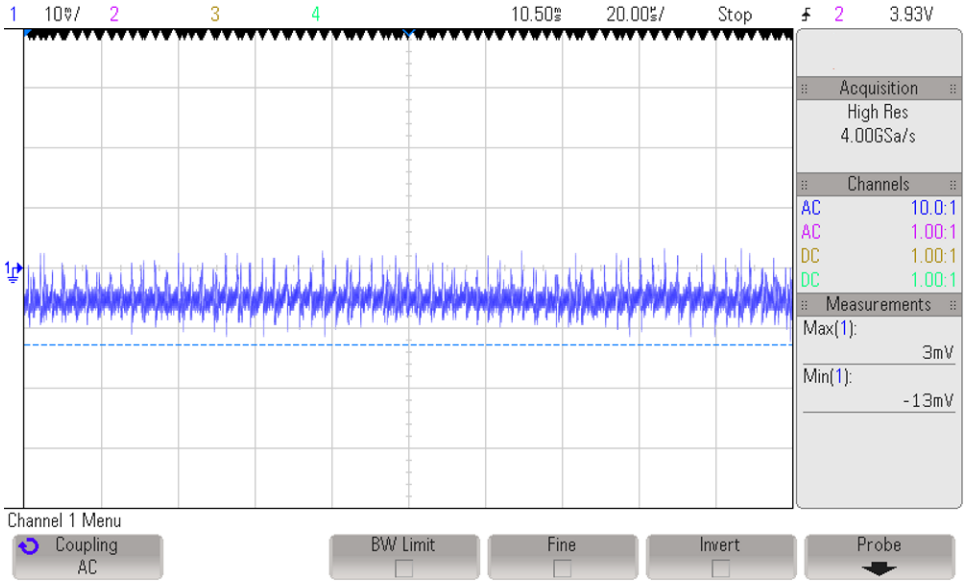


図 28. TPS70633 Output DC Ripple

3.2.1.3 Primary-Side Input Voltage

The 5-V input for testing the push-pull power supply is provided externally to remove any unintended noise and isolate any potential ripple to the design as is. The input was tested with the output both at both no load and full load. The input measurements are shown in 図 29 to 図 33.

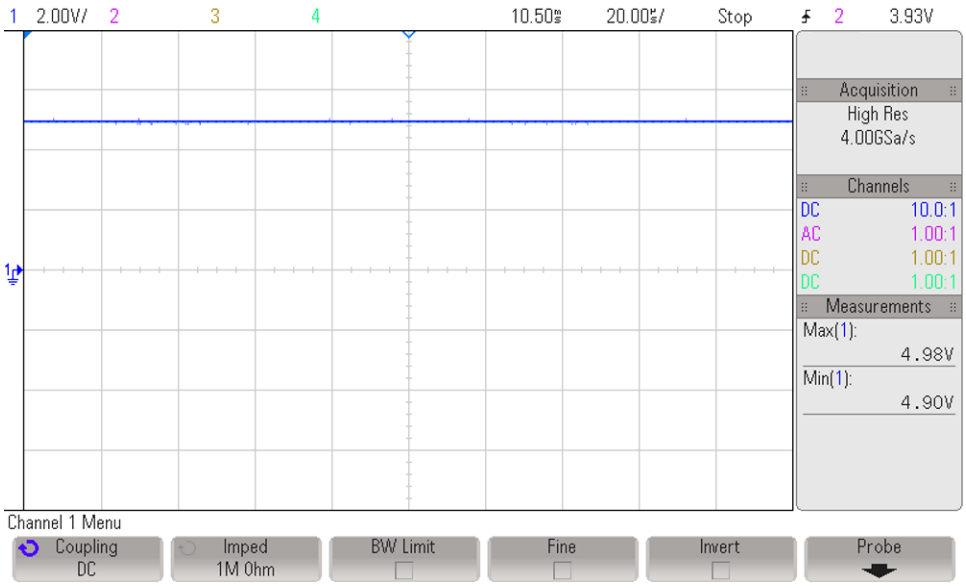


図 29. Primary-Side Input Voltage at No Load

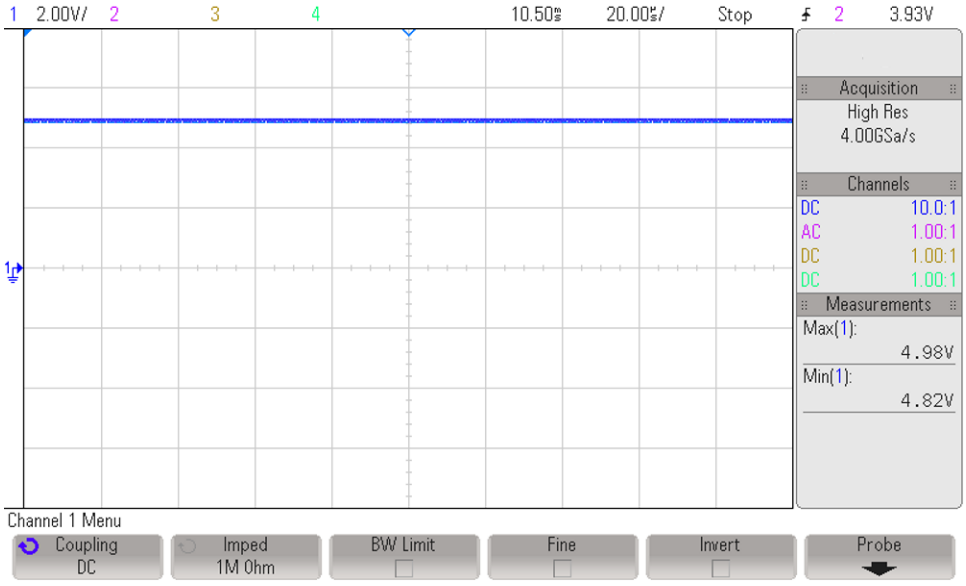


図 30. Primary-Side Input Voltage at Full Load

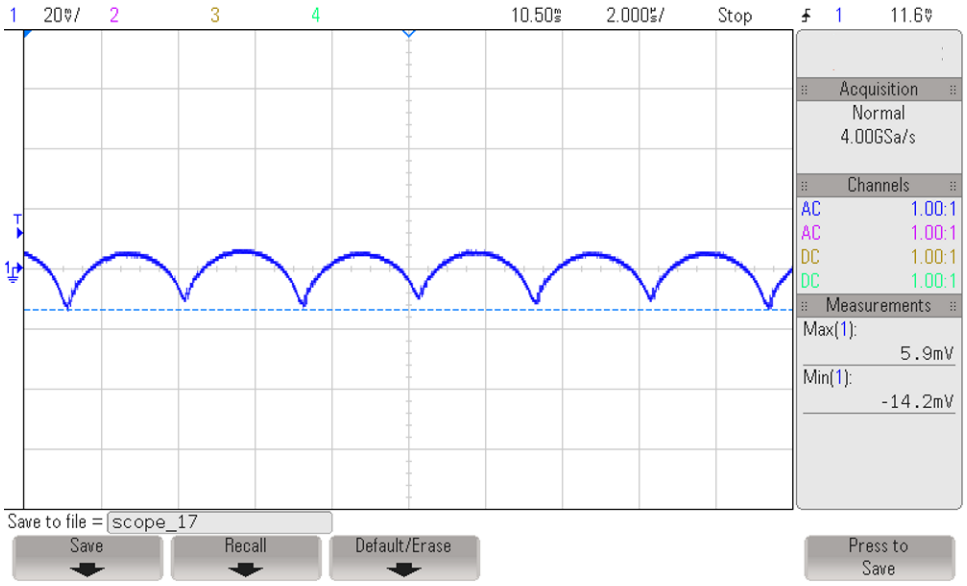


図 31. Primary-Side Input Ripple at No Load

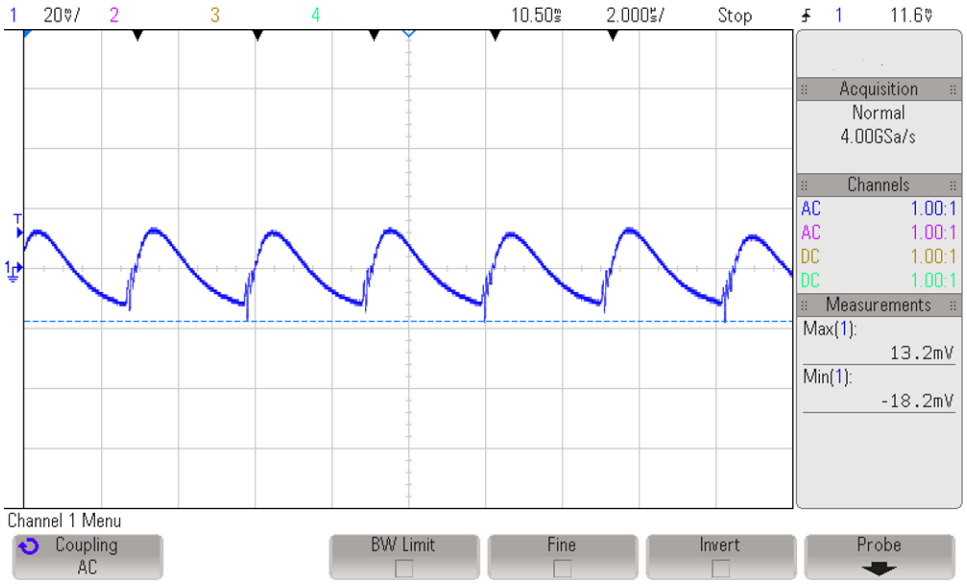


図 32. Primary-Side Input Ripple at Full Load

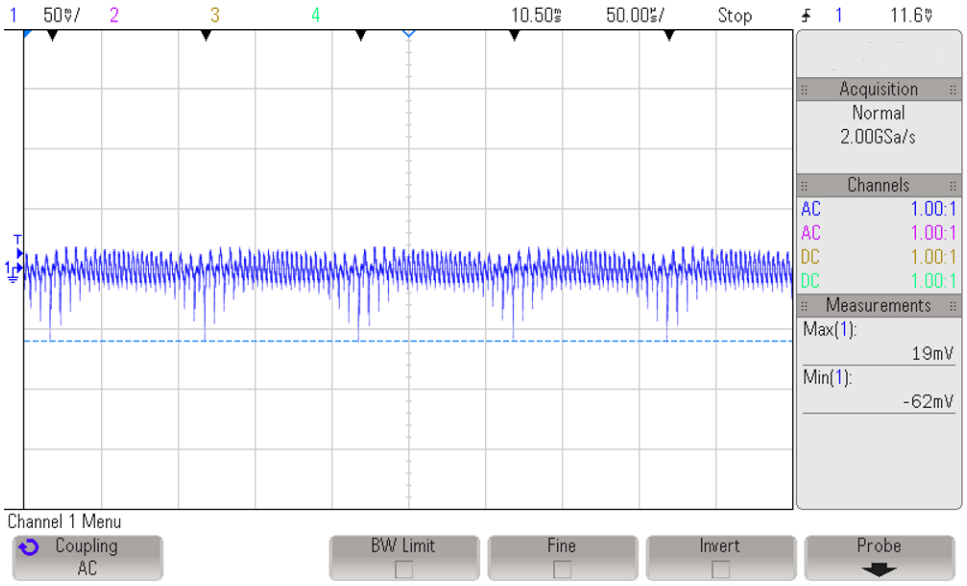


図 33. Primary-Side Input Ripple Due to Spread Spectrum Modulation

3.2.1.4 Switching Waveforms

The following waveforms show the switching waveforms at the transformer terminals. For all primary-side measurements the oscilloscope's channel one is between pins two and three of the transformer, and channel two is between pins one and two. On the secondary-side measurements, channel one is between pins five and six, and channel two is between pins four and five. This is shown in 図 34 to help with correlation.

図 35 to 図 39 show the primary-side winding voltage waveforms.

図 40 to 図 44 show the secondary-side winding voltage waveforms.

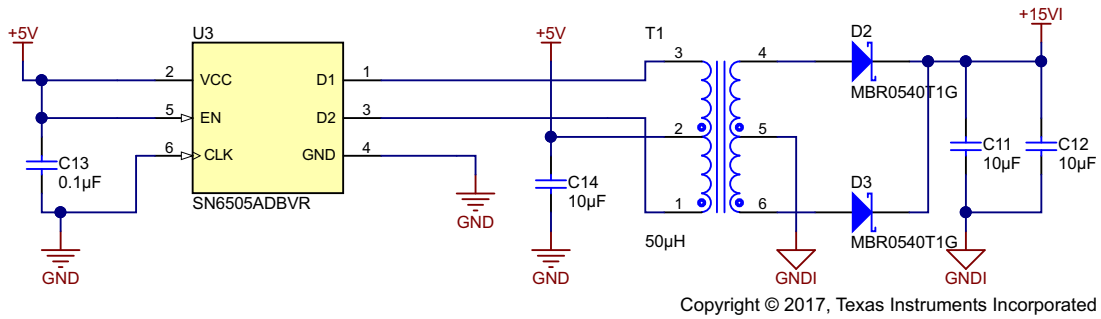


図 34. Transformer Windings Measurement Channels

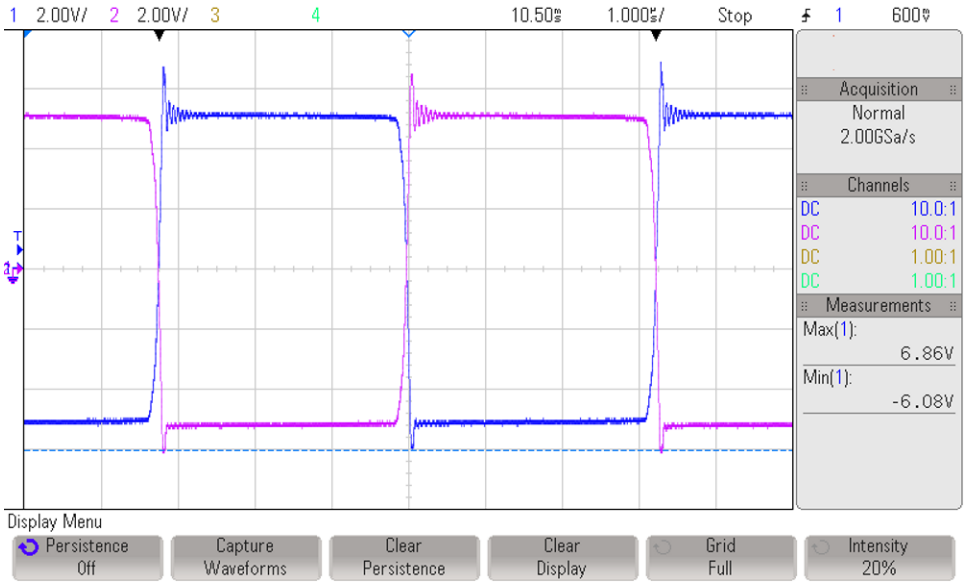


図 35. Primary-Side Winding Waveforms at No Load

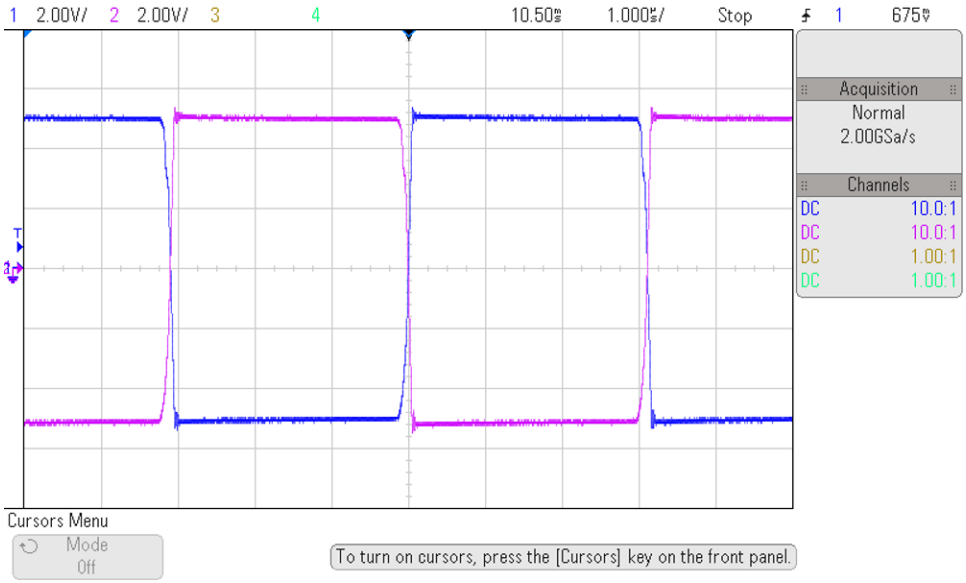


図 36. Primary-Side Winding Waveforms at Full Load

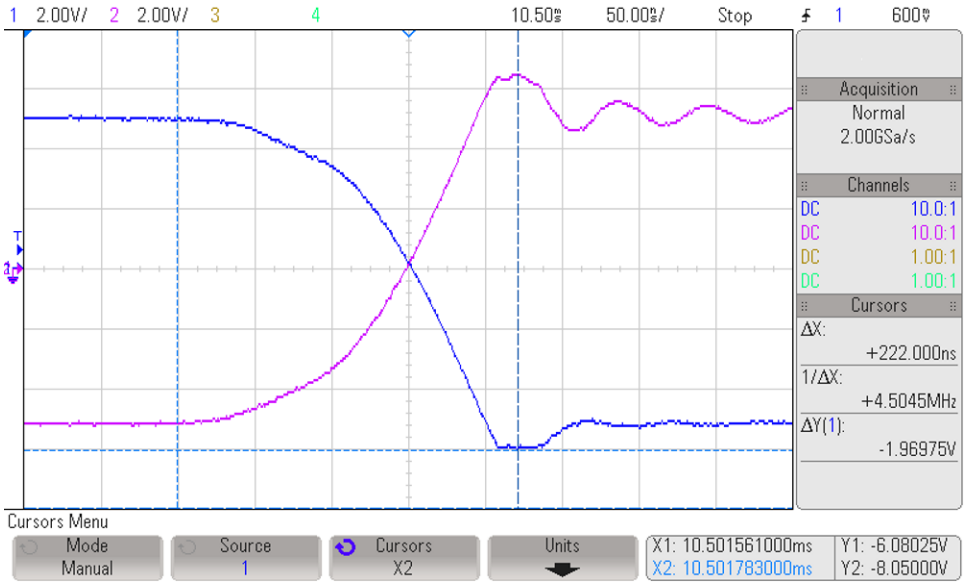


図 37. Primary-Side Winding Rise and Fall Times at No Load

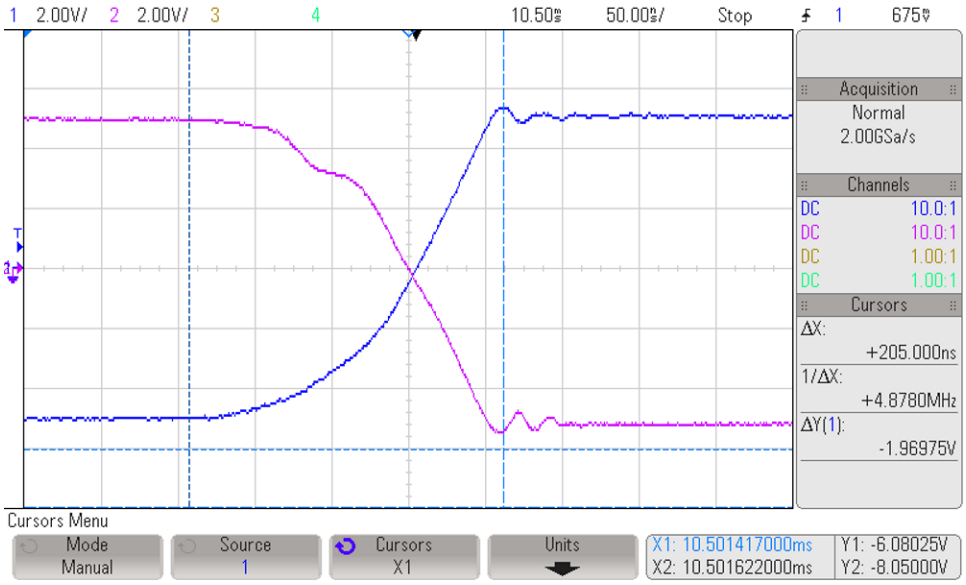


図 38. Primary-Side Winding Rise and Fall Times at Full Load

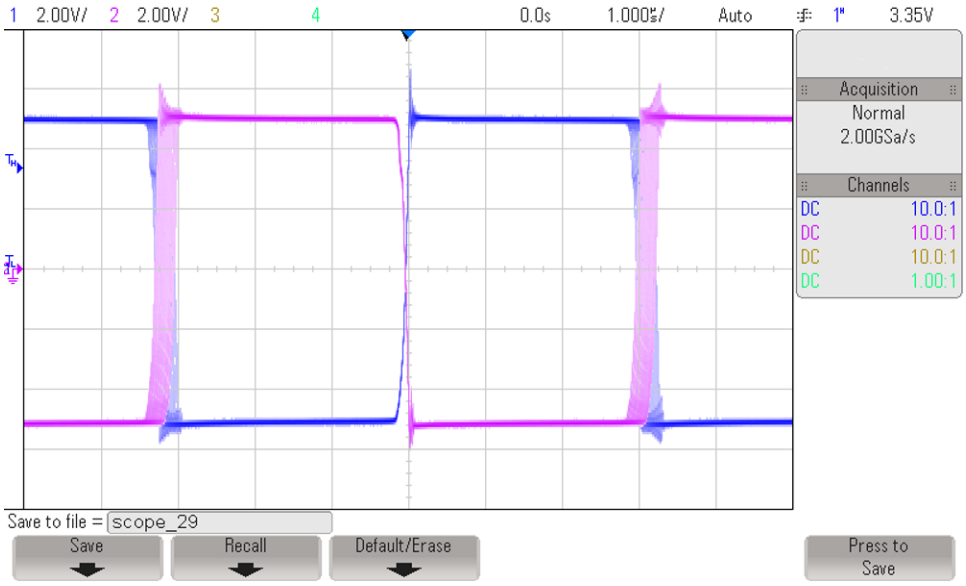


図 39. Primary-Side Winding Spread Spectrum Clocking

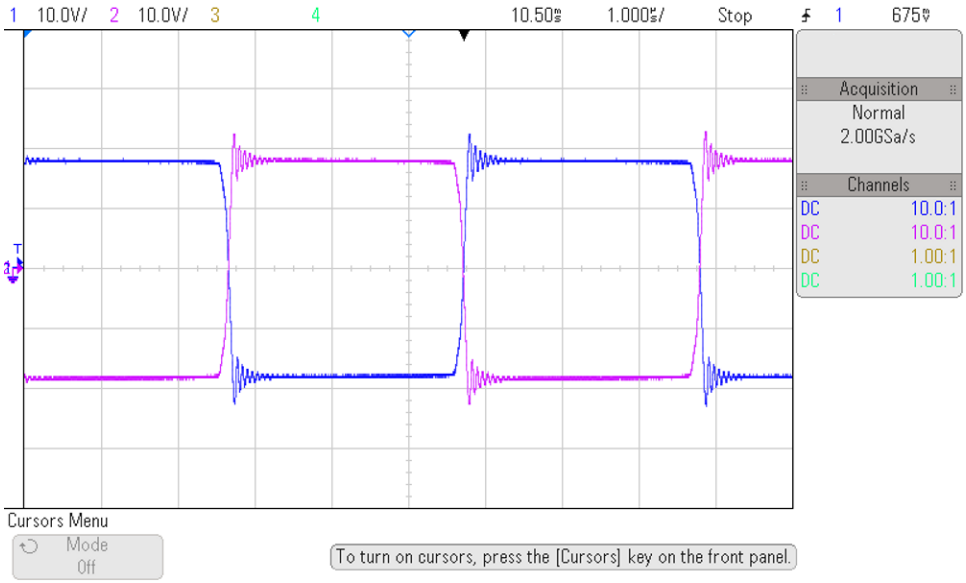


図 40. Secondary-Side Winding Waveforms at No Load

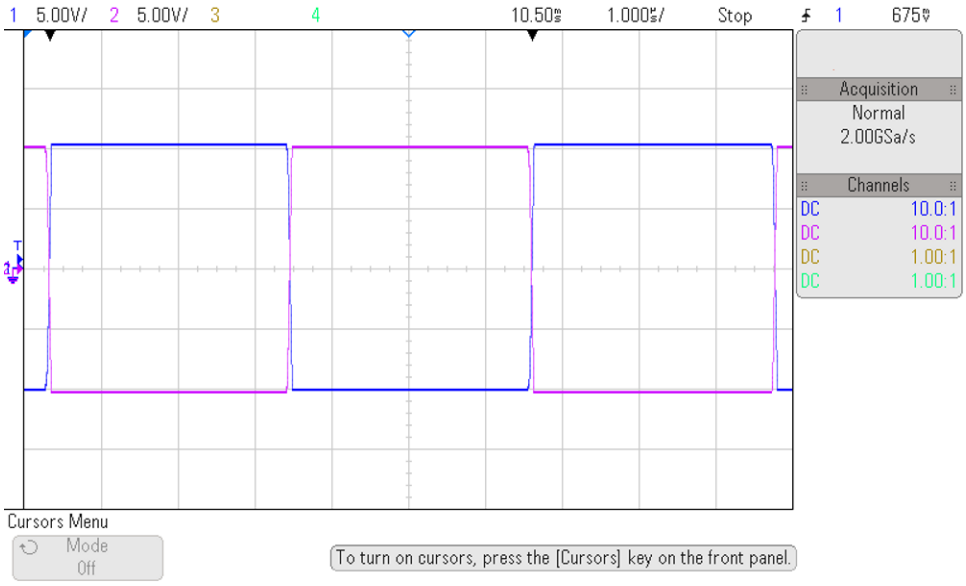


図 41. Secondary-Side Winding Waveforms at Full Load

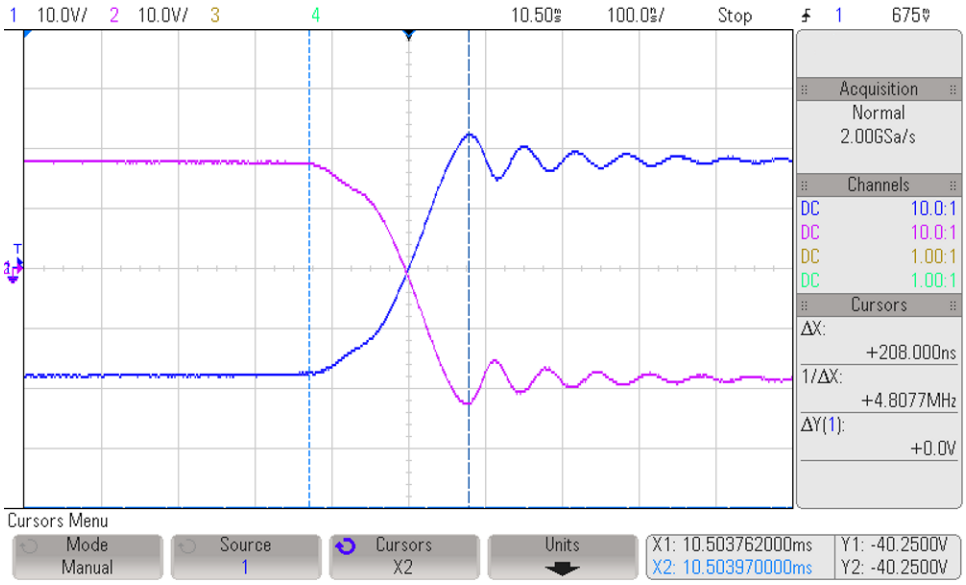


図 42. Secondary-Side Winding Rise and Fall Times at No Load

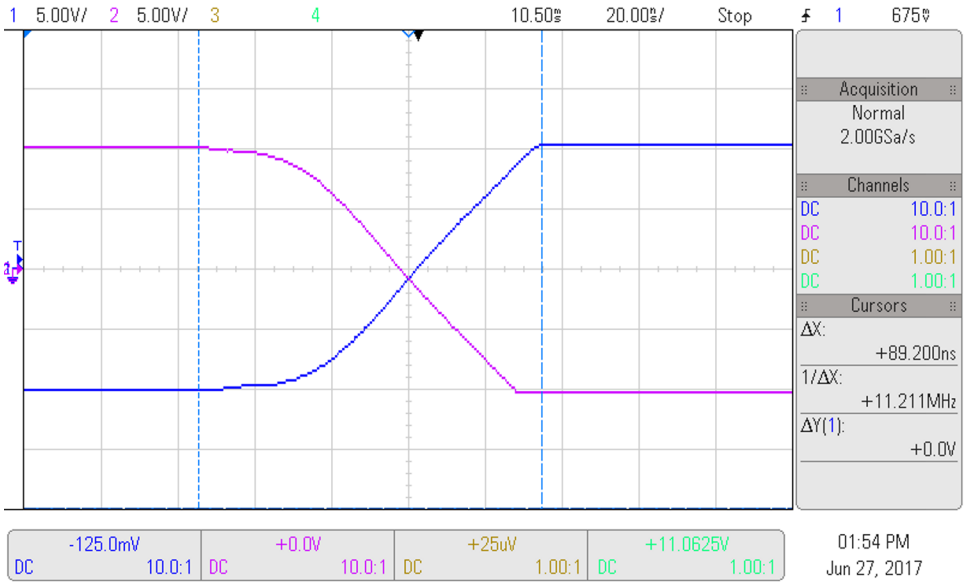


図 43. Secondary-Side Winding Rise and Fall Times at Full Load

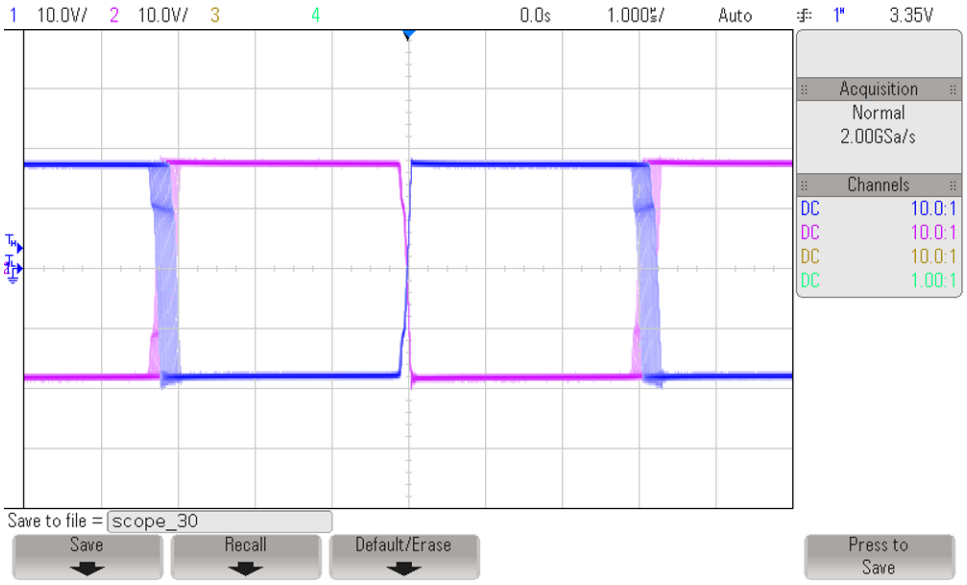


図 44. Secondary-Side Winding Spread Spectrum Clocking

3.2.1.5 Spread Spectrum

The SN6505B has a spread spectrum clocking function. 図 45 shows the effect of this clocking shift on the input windings between pins two and three.

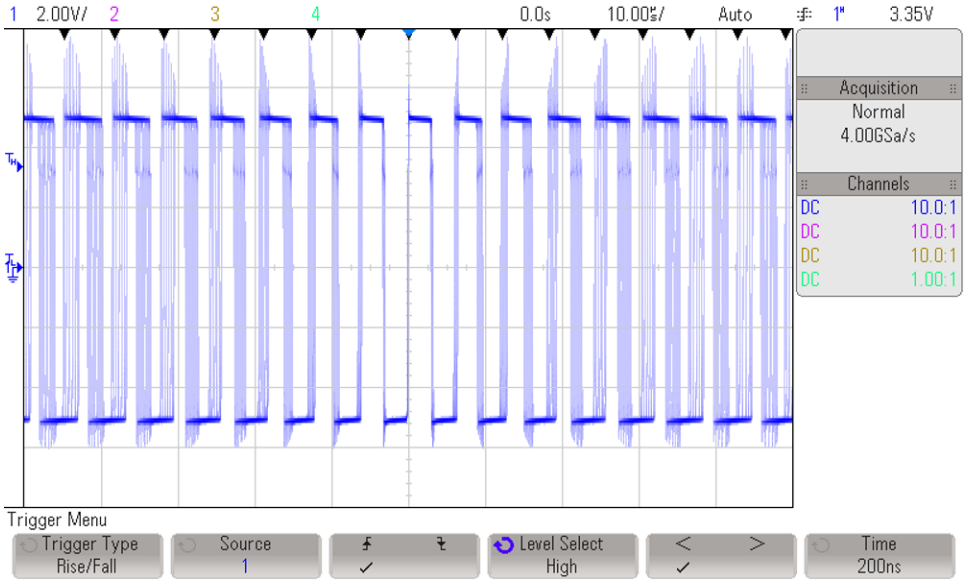


図 45. Effect of Spread Spectrum Clocking

3.2.2 Gate Driver Tests

3.2.2.1 Turnon and Turnoff Delay

The PWM propagation delay from the primary side to the secondary side for both the rising edge and the falling edge is measured in 図 46 to 図 49 at two different switching frequencies. Channel 1 is the PWM input to the gate driver and channel 2 is the gate driver PWM output. Measurement is the delay from 50% to 50% transition of the respective voltages.

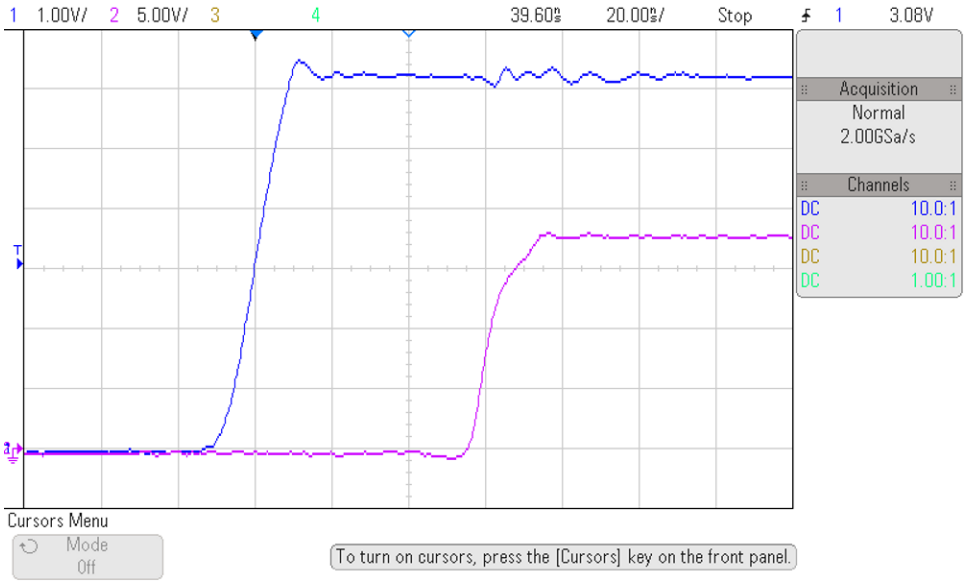


図 46. Turnon Delay at 2 kHz

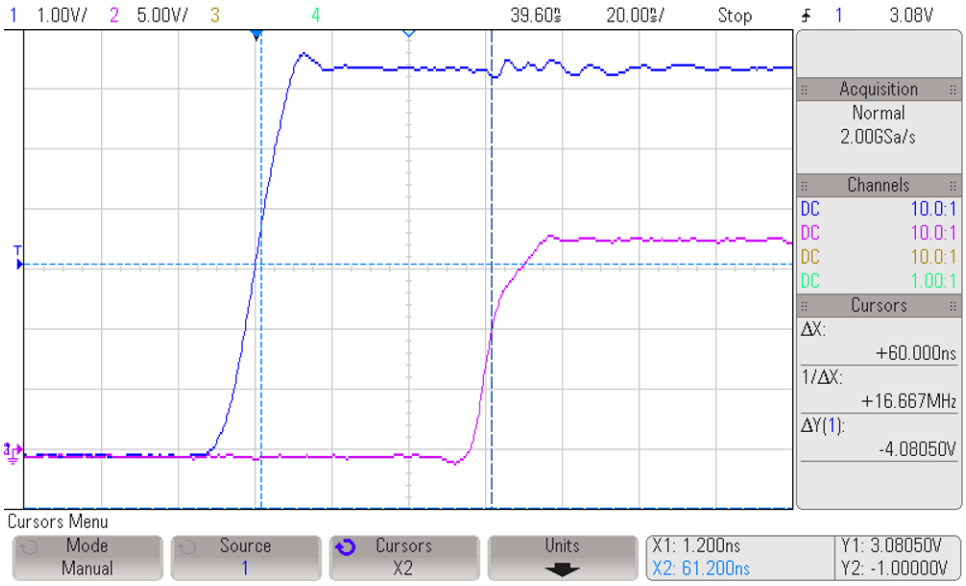


図 47. Turnon Delay at 16 kHz

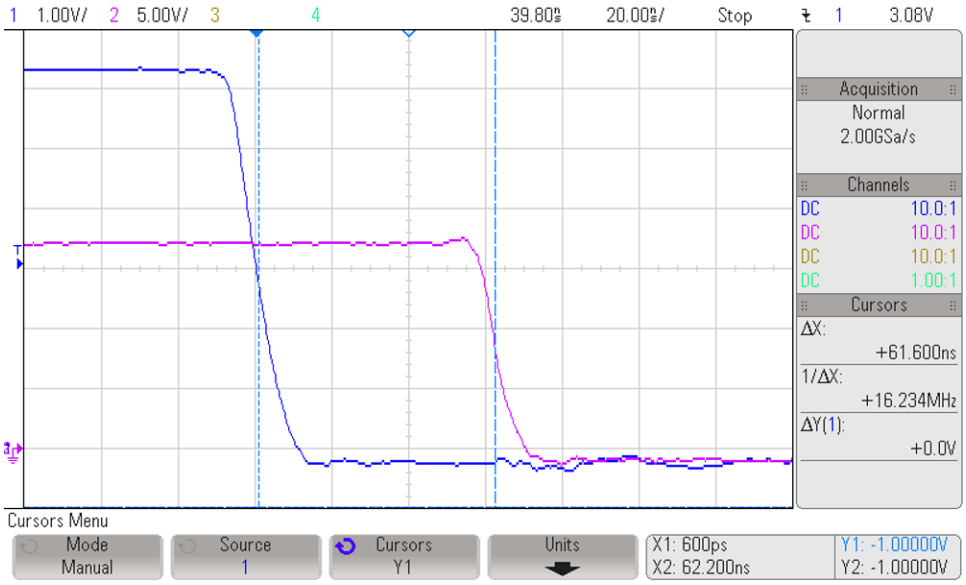


図 48. Turnoff Delay at 2 kHz

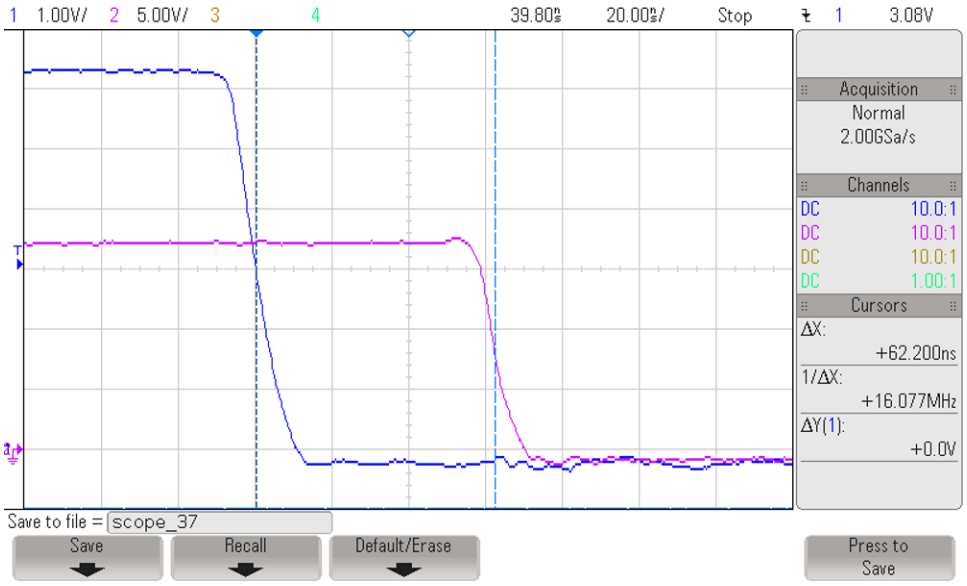


図 49. Turnoff Delay at 16 kHz

3.2.2.2 *Active Miller Clamp Waveforms*

To test the Miller clamp functionality, the TIDA-00638 driver board is installed into the C2000 Solar AC/DC Inverter, and the setup is configured as in the inverter's getting started guide. This included a 400-V DC input and operation of the inverter software on the C2000 control card. The onboard IGBTs under test are IRF IRG4PC30FDPBF-ND.

図 50 and 図 51 show the IGBT gate-emitter voltage (Channel 2) and collector-emitter voltage (Channel 1) with and without the Miller clamp functionality connected.

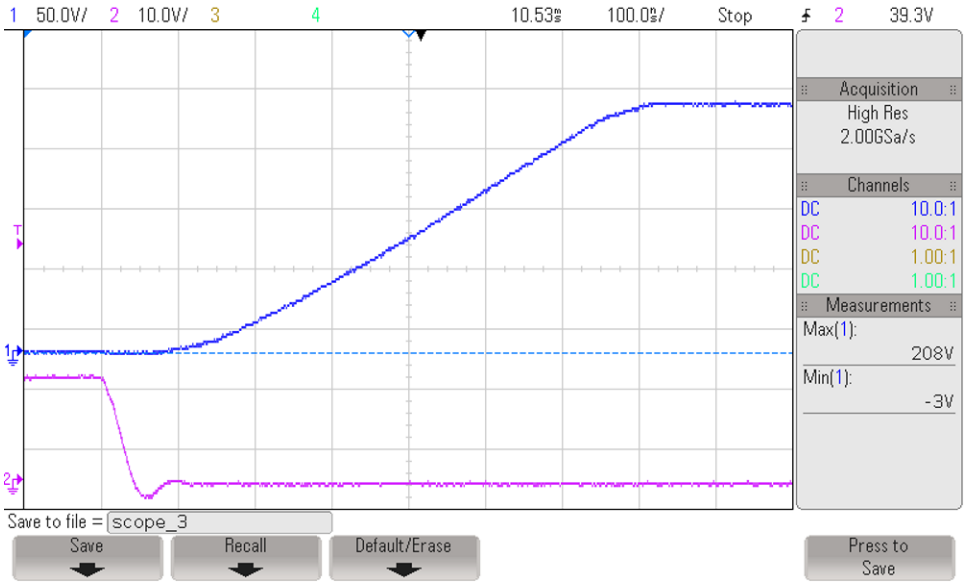


図 50. IGBT Turnoff With Miller Clamp

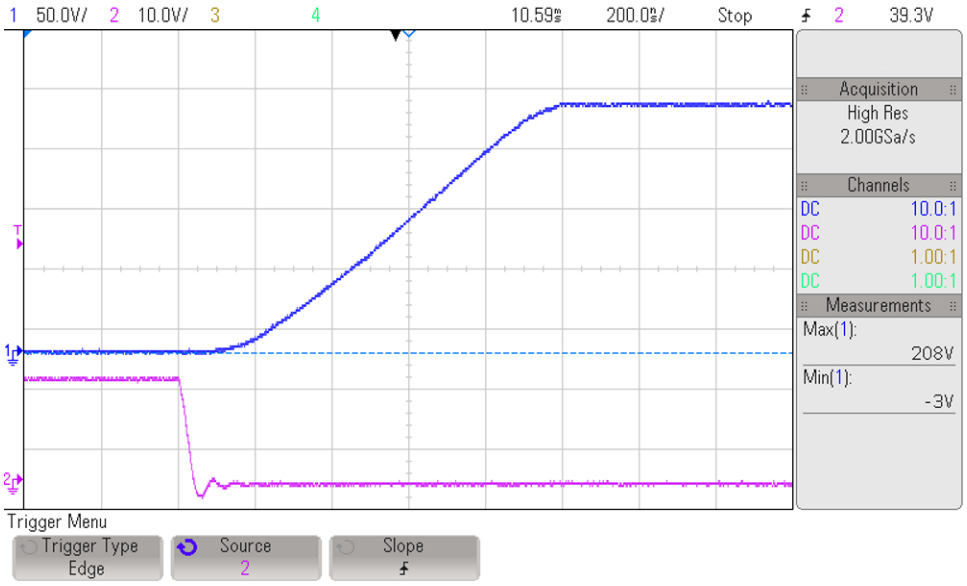


図 51. IGBT Turnon Without Miller Clamp

3.2.2.3 *Inverter Output Validation*

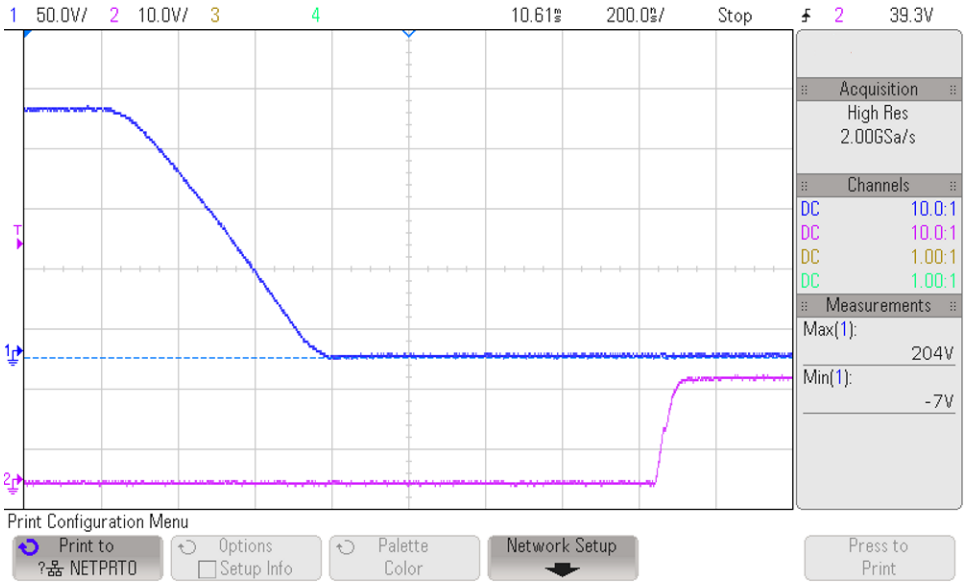


図 52. Inverter IGBT Turnon

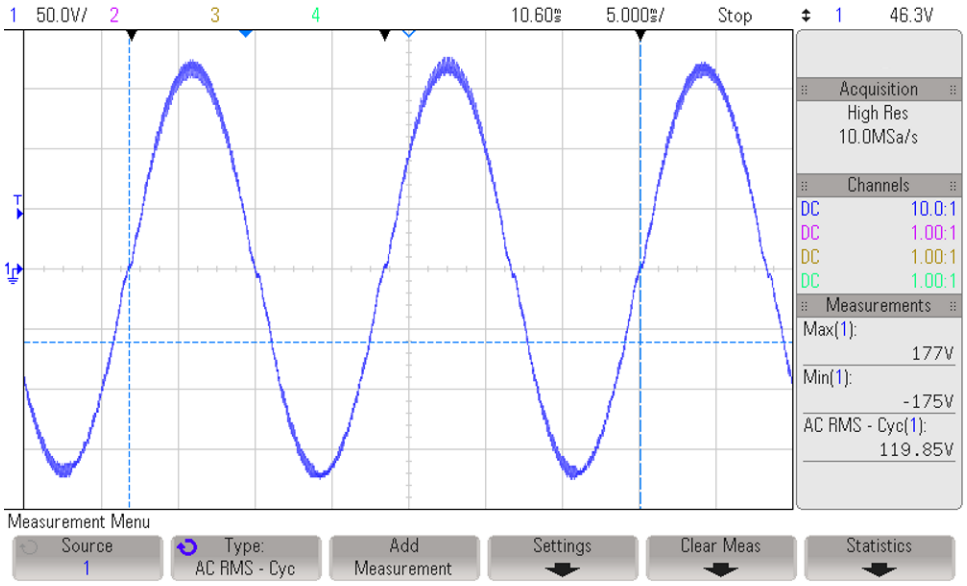


図 53. C2000 Solar AC/DC Inverter AC Output

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00638.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00638.

4.3 PCB Layout Recommendations

4.3.1 Isolated Push-Pull Transformer Supply

SN6505B switches are at 424 kHz. To reduce loop inductance, the switching loops on both the input and output sides must have the minimum area as shown in 図 54 and 図 55. 図 54 shows the primary- and secondary-side switching loops when D3 (pin 1 of SN6505B) is ON, and 図 55 shows the primary- and secondary-side switching loops when D2 (pin 3 of SN6505B) is ON. Both the loop areas are kept minimum to reduce EMI.

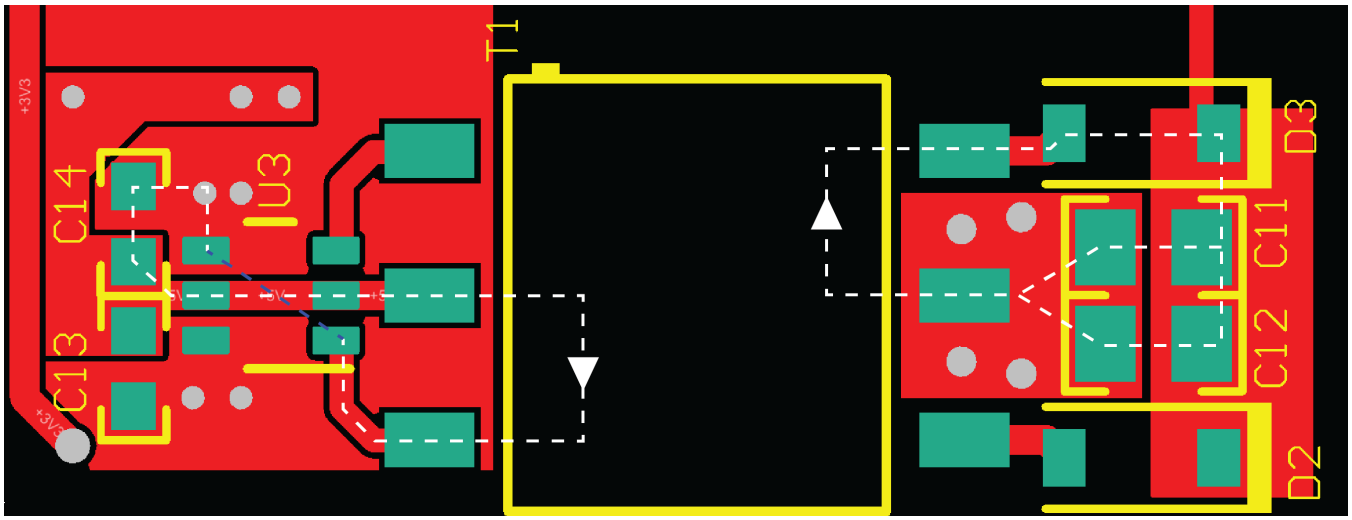


図 54. Switching Loops When D3 is on

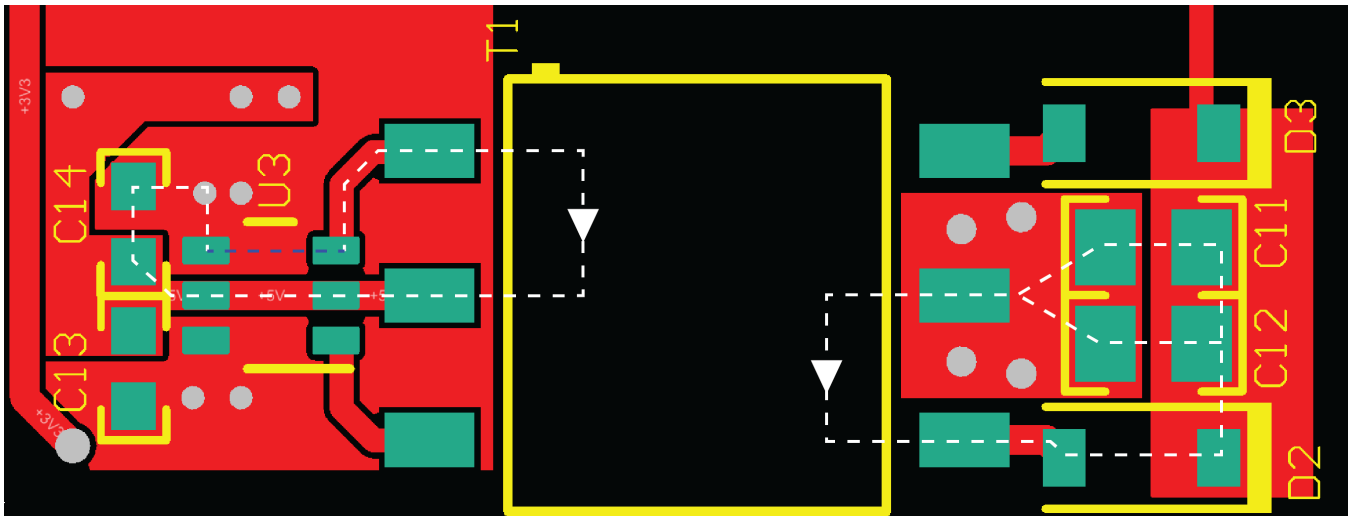


図 55. Switching Loops When D2 is on

- Place the SN6505B device U1 very close to the transformer T1
- Keep the 10-µF bulk capacitor C14 close to the U1 power pin and GND
- Place at least two vias from the output bulk capacitors C11 and C12 to the power planes. This provides a low-inductance connection to the power planes

4.3.2 Gate Driver

- Place the 1-µF bulk capacitor C3 close to the power supply pin of the device
- 図 56 shows the path while sourcing current to the IGBT gate during IGBT turnon. Keep this loop area to a minimum.
- 図 57 shows the path while sinking current from the IGBT gate during IGBT turnoff. Keep this loop area also to a minimum.
- Keep the Miller clamping trace from pin 7 of the IC to the gate of the power switch short or make the trace to reduce the parasitic trace inductance to reduce the induced voltage at the gate of the power switch.

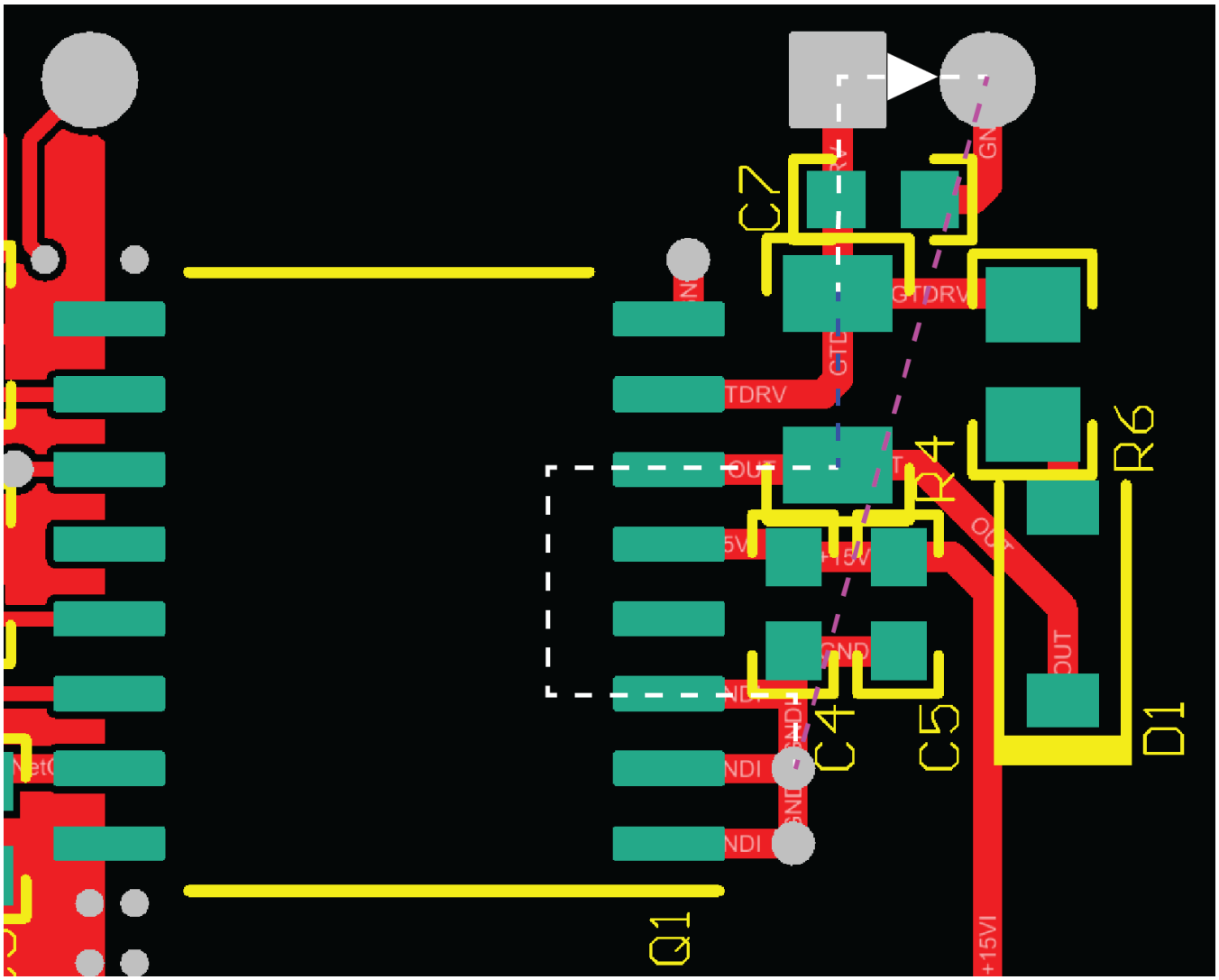


図 56. Gate Source Current Path

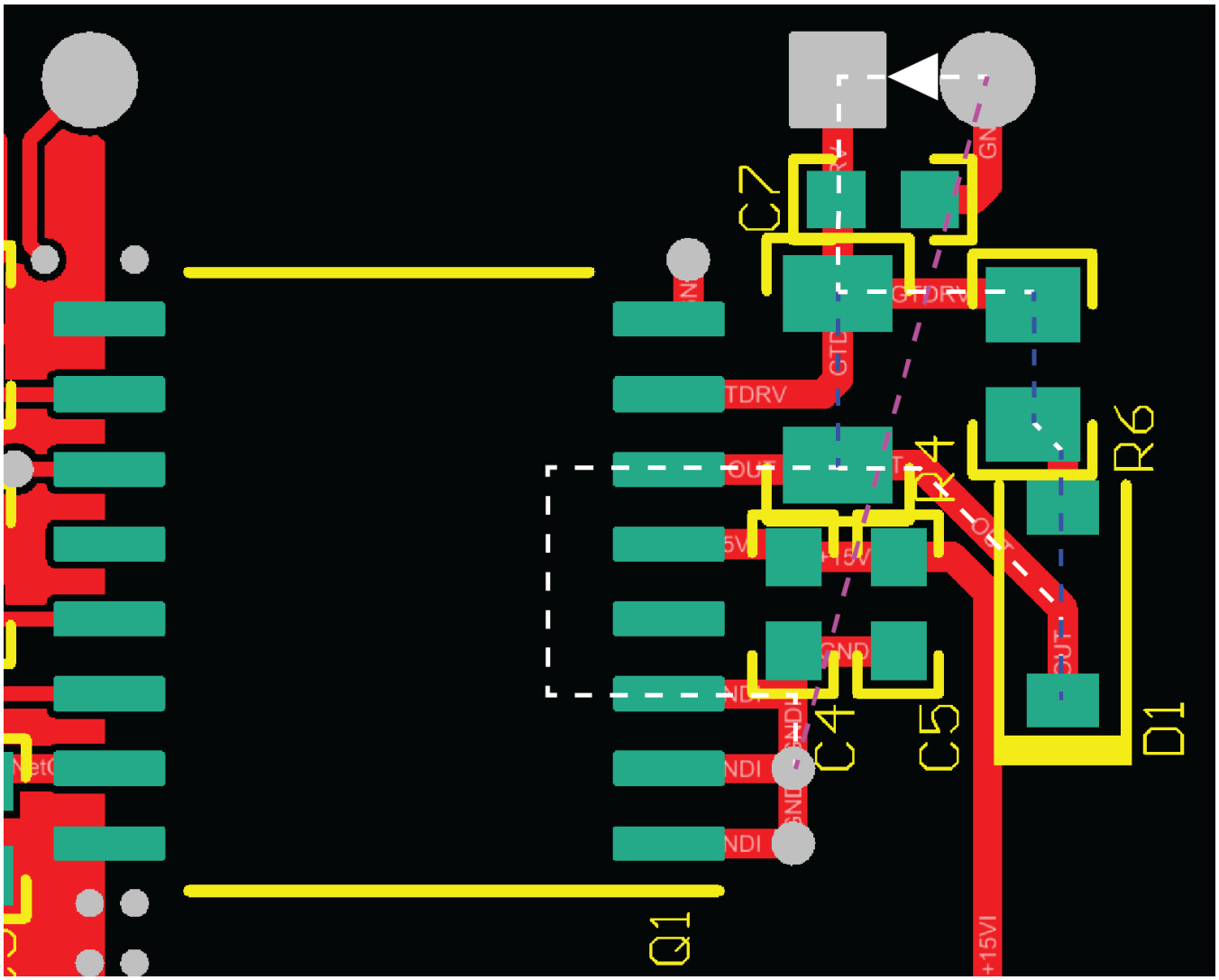


図 57. Gate Sink Current Path

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00638.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00638.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00638.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00638.

5 Related Documentation

1. Texas Instruments, *Compact, Half-Bridge, Reinforced Isolated Gate Drive Reference Design* , TIDA-01159 Design Guide (TIDUCG2)
2. Texas Instruments, *High Voltage Solar Inverter DC-AC Kit User's Guide* (TIDU402)
3. Texas Instruments, *Fundamentals of MOSFET and IGBT Gate Driver Circuits* , Application Report (SLUA618)

5.1 商標

6 About the Author

BART BASILE is a systems architect in the Texas Instruments Grid Infrastructure Solutions Team, focusing on renewable energy and EV infrastructure. Bart works across multiple product families and technologies to leverage the best solutions possible for system level application design. Bart received his bachelors of science in electronic engineering from Texas A&M University.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2015年12月発行のものから更新 **Page**

- 現行のデザイン・ガイド・テンプレートに合わせて 変更 1

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