参考資料

TI Designs: TIDA-01420
産業用ドライブ向けの基本的な絶縁三相、小型電力段のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

この三相小型電力段のリファレンス・デザインは、基本絶縁を持つゲート・ドライバ(UCC53xx)を使用して、デュアル・コントローラを使用するシステムの絶縁要件を満たします。ゲート・ドライバの容量性絶縁により、寿命が長くなるとともに、オプトカプラ上での伝播遅延のマッチングが向上するため、インバータのデッドバンド歪みや損失が最小限に抑えられます。必要に応じて、コントローラ間に別のレベルの基本絶縁を使用することにより、システム・レベルで強化絶縁を達成できます。この手法により、システムの絶縁コストが最適化され、小型化を実現できます。このデザインでは、UCC53xxゲート・ドライバのインターロック機能を使用した、貫通電流に対するIGBTの保護も示されています。このリファレンス・デザインは、F28379D Delfino™制御カードを使用して、PWM信号を生成し、三相インバータを制御しています。

リソース

TIDA-01420	デザイン・フォルダ
UCC5350MCD	プロダクト・フォルダ
UCC5390ECD	プロダクト・フォルダ
LM3480	プロダクト・フォルダ
TLV704	プロダクト・フォルダ
TLV1117-33	プロダクト・フォルダ
SN74LVC1G17	プロダクト・フォルダ
TMDSCNCD28379D	ツール・フォルダ

TI E2E™ Community

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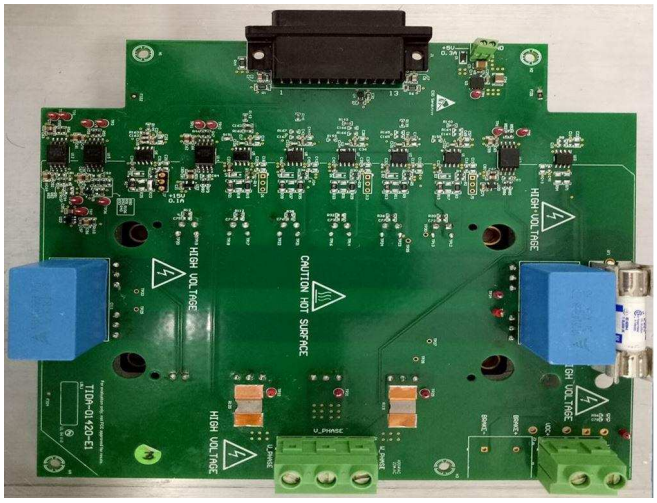
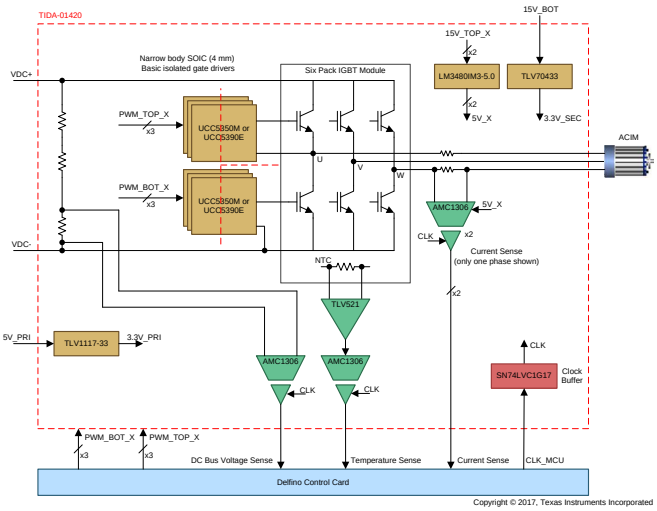
特長

- 基本絶縁された200～480Vの三相電力段と、MCUへの直接PWM CMOSインターフェイスによるホットサイド制御
- ピン数の少ないゲート・ドライバUCC53xxにより、小型のソリューションを実現でき、ゲート・ドライバをより柔軟に配置可能
- 伝播遅延が短く(標準値72ns)、伝播遅延間スキューが非常に小さいことから、デッドバンド歪みと損失が最適化
- ゲート・ドライバは、貫通電流回避のため、PWMインターロック保護オプションをサポート
- ゲート・ドライバの3つのバリエーションを使用するオプション: ミラー・クランプにより寄生ターンオン効果を回避、エミッタ基準のUVLOにより、線形領域での動作に対してIGBTへの堅牢な保護を提供、および分割出力により立ち上がりと立ち下がりの時間を制御
- ハイサイド・ドライバ用の、組み込みのブートストラップ・ベースのユニポーラ電源と、外部のバイポーラ電源レールへの給電オプション
- シンク/ソース電流17Aの高い駆動力を持つゲート・ドライバにより、外部バッファなしに大電流IGBTを駆動可能

アプリケーション

- ACインバータおよびVFドライブ
- 産業用電源
- サーボ・ドライブ
- 太陽光インバータ





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1 System Description

A variable frequency drive (VFD) is a type of motor controller that drives an electric motor by varying the frequency and voltage supplied to the electric motor. As the application changes, the motor speed requirements changes; the VFD can simply increase or reduce the motor speed to meet the speed requirement. In addition, the VFD can reduce the system's average energy consumption. 図 1 shows the block diagram demonstrating a VFD. The basic components of a VFD are:

- Input section, which draws AC electric power from the utility and converts the AC into DC power
- Inverter section, which converts DC back into a controllable AC waveform

In the inverter section, insulated gate bipolar transistors (IGBTs) can be used as semiconductor switches to convert the DC bus voltage to AC. IGBTs have advantages such as high input impedance as the gate is insulated, a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation, and controllability of switching behavior to provide reliable short-circuit protection.

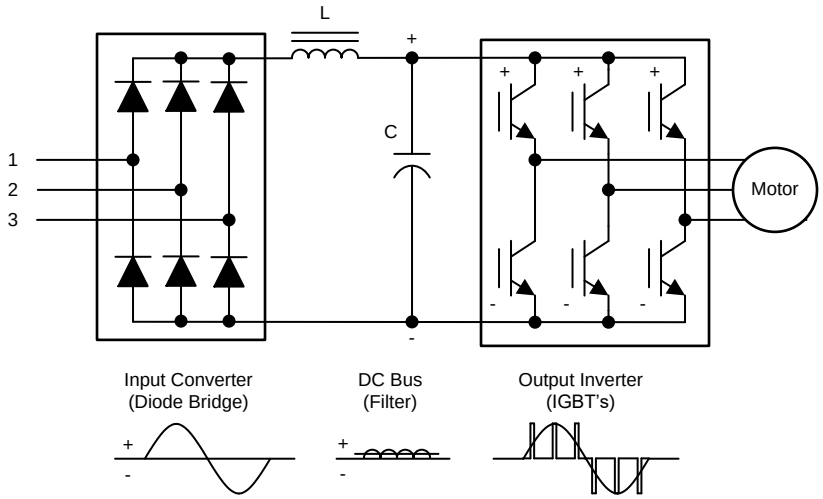

図 1. Block Diagram of VFD

Although various induction motor control techniques are in practice today, the most popular control technique is by generating variable frequency supply, which has a constant voltage to frequency ratio. This technique is popularly known as VF control. VF control is simple to implement and cost effective. The base speed of the induction motor is directly proportional to the supply frequency and the number of poles of the motor. Because the number of poles is fixed by design, the best way to vary the speed of the induction motor is by varying the supply frequency. The torque developed by the induction motor is directly proportional to the ratio of the applied voltage and the frequency of supply. By varying the voltage and the frequency, but keeping their ratio constant, the torque developed can be kept constant throughout the speed range. This is exactly what VF control tries to achieve.

The three-phase induction motor is connected to a three-phase inverter bridge as shown in 図 2.The power inverter has six switches that are controlled to generate three-phase AC output from the DC bus. PWM signals generated from the microcontroller (MCU) control these six switches through an isolated gate driver. The amplitude of phase voltage is determined by the duty cycle of the PWM signals. The switching produces a rectangular shaped output waveform that is rich in harmonics. The inductive nature of the motor's stator windings filters this supplied current to produce a three-phase sine wave with negligible harmonics.

To prevent the DC bus supply from being shorted, the upper and lower switches of the same half bridge must not be switched on at the same time. A dead time is given between switching off one switch and switching on the other. This dead time ensures that both switches are not conductive at the same time as each one change states. The UCC53xx used in this design supports an interlocking function, thereby avoiding shoot-through. For more about this feature, see 2.3.3.

IEC safety standards mandate to isolate the high-voltage inverter section from the low-voltage controller section accessible by the operator to protect from electric shock. Depending upon the system architecture and voltage levels, either basic isolation, reinforced isolation, or a combination of the two are used.

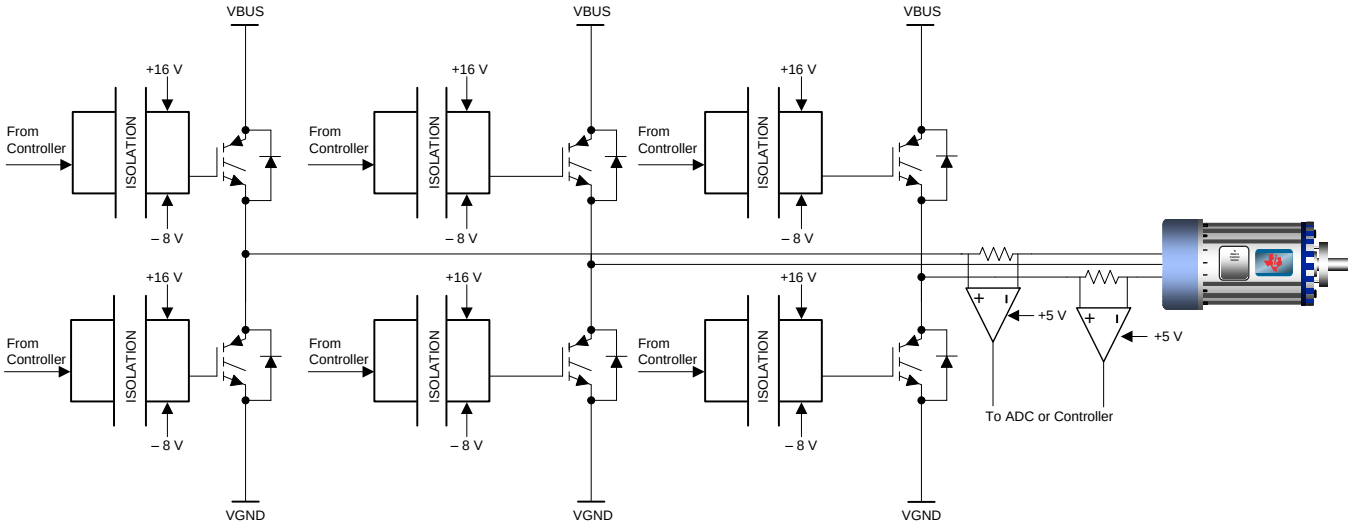

図 2. Three-Phase Power Stage With Isolated Gate Driver

The isolation between the high-voltage side and the low-voltage side MCU can be either basic or reinforced. Basic isolation protects against high voltage as long as the barrier is intact. To protect from and safely withstand high voltage surges that would damage equipment or harm humans, reinforced isolation is required, which is equivalent to two basic isolation in series. Reinforced isolation by itself is sufficient as a safety barrier against high voltage. Reinforced isolation requires a creepage of 8 mm whereas the creepage requirement for basic isolation is 4 mm for systems powered from a 480-V AC grid. A three-phase AC inverter necessitates the use of six gate drivers and a minimum of two current sensors, whose space can be optimized by adopting basic isolation. So the overall PCB area reduces in case of basic isolated gate drivers. To provide a compact and cost-effective solution in the power stage, this reference design uses basic isolation. Another level of basic isolation can be included in the system to obtain reinforced isolation.

This reference design consists of a 3φ power stage using UCC53XXDWV basic isolated gate drivers intended to drive motors for various industrial applications. As shown in 図 3, the UCC53XXDWV is available in three versions:

- The UCC53x0S: This device provides a split output that can be used to control the rise and fall times of the driver.
- The UCC53x0M: This device connects the gate of the transistor to an internal clamp to prevent false turnon caused by Miller current.
- The UCC53x0E: This device has its UVLO2 referenced to GND2, which facilitates bipolar supplies.

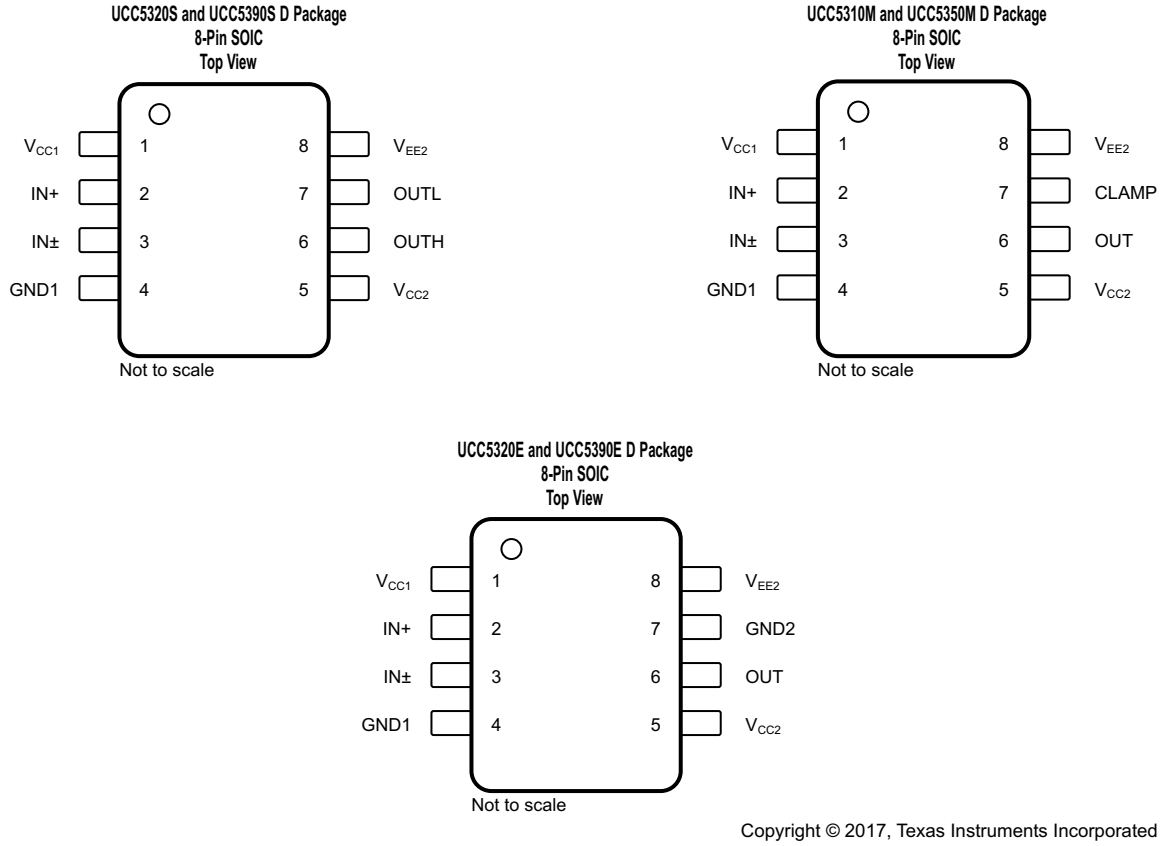

図 3. Pin Diagram of UCC53xx

This reference design characterizes the Miller clamp and UVLO versions of the gate drivers using the UCC5350MCD and UCC5390ECD, respectively. The IGBTs used to test these gate drivers are as follows:

- UCC5350MCD: CM100TX-24S
- UCC5390ECD: 6MI180VB-120-50

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
DC link voltage	280- to 900-V DC	900-V DC max to provide margin for motor regeneration and boost PFC if used. 280- to 680-V DC corresponds to grid voltage of 200- to 480-V AC
IGBT module	6MBI180VB-120-50, 1200-V DC, 150 A	6MBI180VB-120-50 is used with UCC5390E and CM100TX-24S is used with UCC5350M
	CM100TX-24S 1200-V DC, 100 A	
Isolation	Basic	—
Clearance	4 mm	—
Gate driver package	8 pin SOIC(D)	—
Source/sink current rating (Minimum)	UCC5390E: 12 Apk/12 Apk	—
	UCC5350M: 10 Apk/5 Apk	
Switching frequency	4 to 16 kHz	—
Dead time(minimum)	25 ns (gate driver max skew) + dead time for specific IGBT module	Inverter tested with a 1-µs deadband; can be varied as long as there is no overlap between VGE signals of top and bottom IGBT switches
PCB	4 layer, 1-oz copper, high Tg FR4, 1.6 mm thick	—
Primary side supply	5 V ± 5%, 500 mA	—
Secondary side supply	UCC5390E: 15-V / -8 V bipolar	—
	UCC5350M: 15-V unipolar	
PCB size	167 mm × 178 mm	—
PCB thickness	1.6 mm	—
Ambient Temperature	0°C to 55°C	Components selected support the industrial temperature range of 85°C and the reference design can operate outside the mentioned temperature range with sufficient derating. Tested only from 0°C to 55°C
Microcontroller Interface	7 PWM signals, current sense modulator bit streams for two motor phases, DC-link voltage sense modulator bit stream, temperature sense modulator bit stream, clock signal, 5 V for the controller board	—

2 System Overview

The UCC53xx isolated gate driver is available in an 8-pin SOIC (D) package. This package has a creepage and clearance of 4 mm and can support isolation voltage up to 3 kV_{RMS}, which is good for applications where basic isolation is needed. The maximum isolation working voltage (V_{IOWM}) for the UCC53xx is 700 V_{RMS}. The UCC53x0 family has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher common mode transient immunity (CMTI).

2.1 Block Diagram

図 4 shows the system block diagram of the basic isolated three-phase inverter with in-line precision phase current sensing with a shunt resistor. The TIDA-01420 reference design is highlighted with a red dashed box.

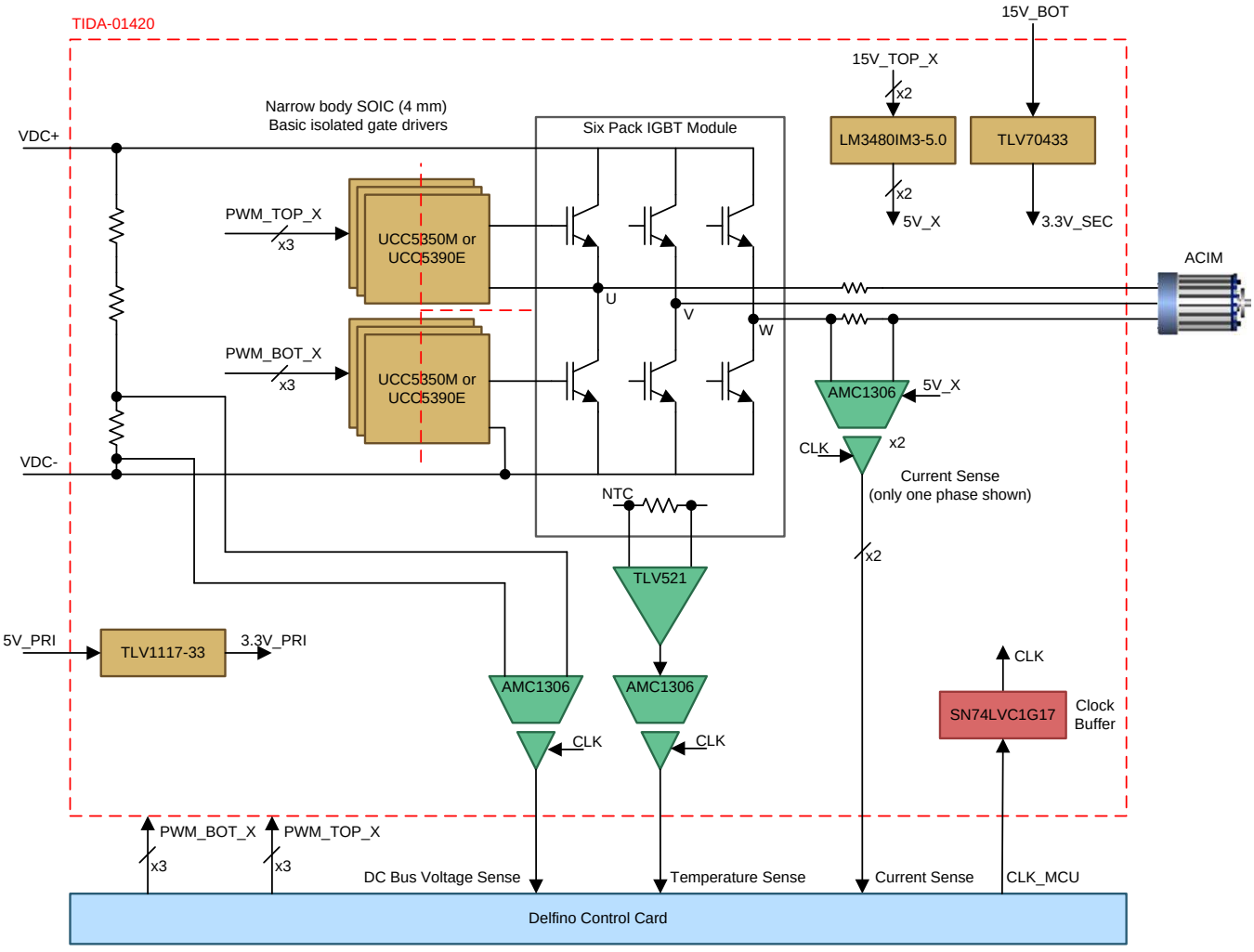

図 4. TIDA-01420 Block Diagram

The inverter section is composed of a six-pack IGBT module that contains three half bridges. Each IGBT of the module is driven by a basic isolated gate driver. Two different PCBs are fabricated to characterize the two versions of the gate driver: the Miller clamp version (UCC5350MCD) and the UVLO version (UCC5390ECD).

The UCC5350MCD uses a unipolar 15-V power supply for driving the IGBT gates. The low-side gate drivers are powered externally using a 15-V supply. The high-side gate drivers are powered up using a bootstrap supply.

The UCC5390ECD uses a bipolar 15-V and –8-V power supply for driving the gates of the IGBTs. The low-side gate drivers are powered externally using a 15-V/–8-V single bipolar supply. The standard method for bootstrapping a positive gate voltage cannot be extended to negative voltages without increasing the complexity. Therefore, in this reference design, the three high-side gate drivers are powered externally using three different power supplies.

A primary-side 3.3-V supply is derived from the 5-V input through the LDO regulator TLV1117-33. The PWM input signals for the gate drivers are routed to a D-SUB 25-pin female connector, which is connected to the Delfino control card TMDSCNCD28379D through an adapter board. Interlocking is present as an optional protection feature in this design at the input of the gate driver. When single gate drivers are used in half-bridge configuration, they usually allow cross conduction instead of preventing it in case of wrong input signals coming from the controller device. This limitation is due to the fact that each driver does not have the possibility to know the status of the input signal of the other companion driver in the same leg. The availability of two input pins with opposite polarity allows implementing an hardware interlocking that prevents cross conduction even in case of wrong input signals generated by the control unit. This can be achieved by making connections as shown in 図 5.

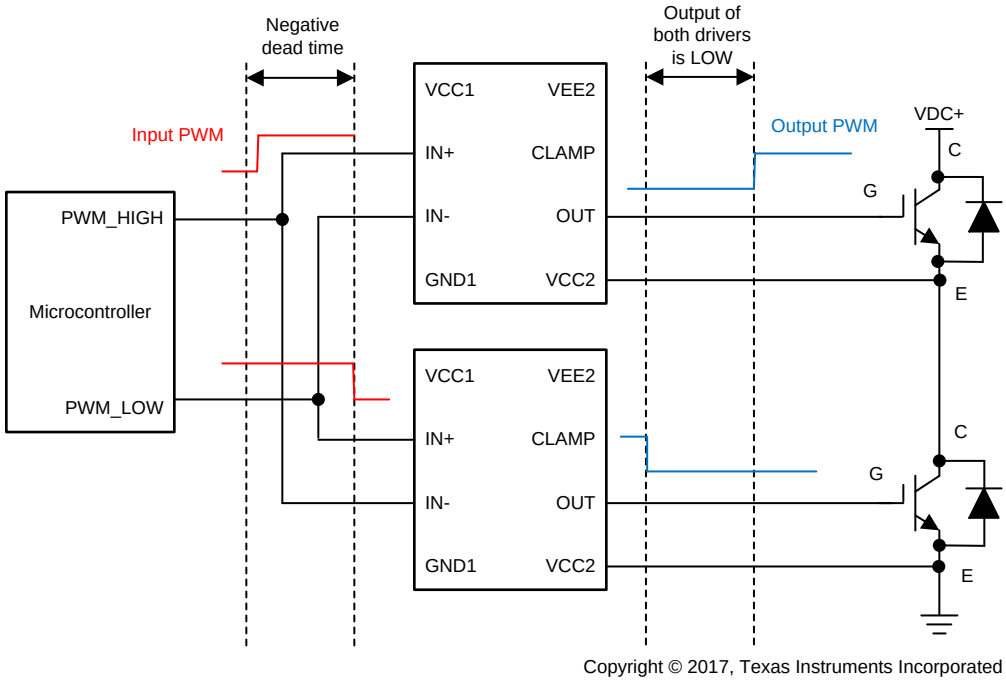

図 5. Hardware Cross-Connection Prevention Using Interlocking

The output of the gate driver is connected to the gate of the IGBT through an external resistor, which can control the source and sink currents provided by the gate driver.

2.2 Highlighted Products

2.2.1 UCC5350M and UCC5390E

The UCC53xx is a family of compact, single-channel, isolated IGBT, SiC and MOSFET gate drivers with superior isolation ratings and includes variants for pinout configuration, drive strength, and package. The UCC53xxMCD option connects the gate to an internal clamp to prevent false turnon caused by Miller current. The UCC53xxECD option has its UVLO2 referenced to GND2; it is recommended to connect this pin to the IGBT emitter. Compared to an optocoupler, the UCC53xx family has superior insulation voltage, lower power consumption, quiescent current, and CMTI. 図 6, 図 7, and 図 8 show the functional block diagrams of UCC5390ECD and UCC5350MCD. 表 2 shows the drive strength capabilities of different gate drivers.

表 2. Drive Strength Capabilities of Different Versions of UCC53xx

PART NUMBER	MINIMUM SOURCE AND SINK CURRENT	DESCRIPTION
UCC5310M	2.4 A and 1.1 A	Miller clamp
UCC5320S	2.4 A and 2.2 A	Split output
UCC5320E	2.4 A and 2.2 A	A UVLO with respect to IGBT emitter
UCC5350M	5 A and 5 A	Miller clamp
UCC5390S	10 A and 10 A	Split output
UCC5390E	10 A and 10 A	A UVLO with respect to IGBT emitter

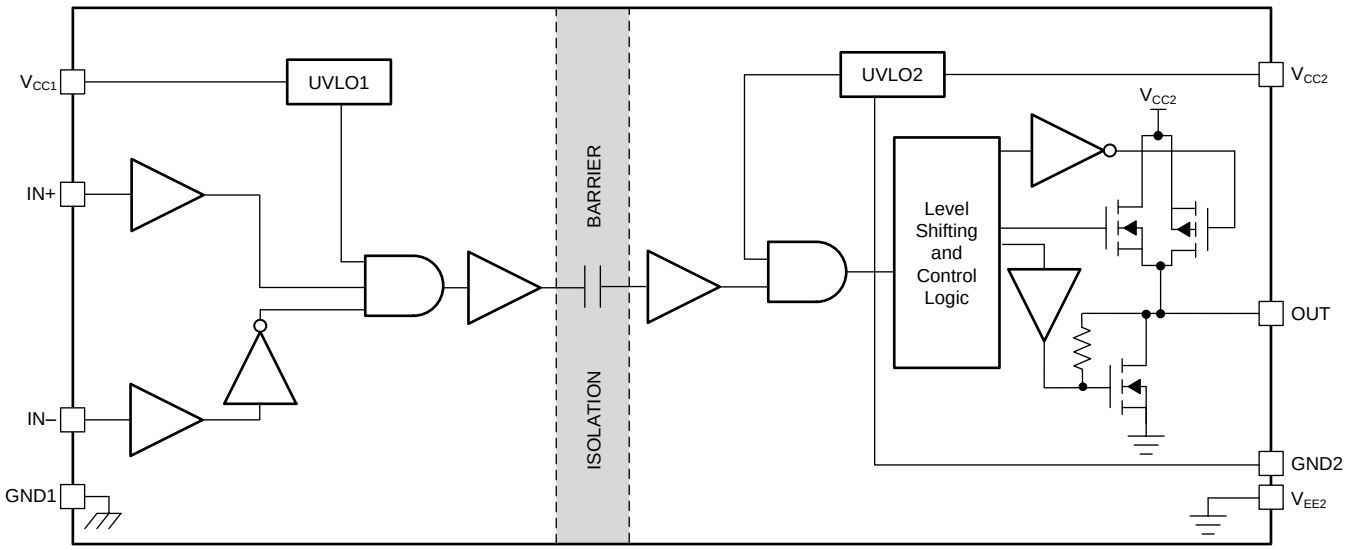

図 6. Functional Block Diagram of UCC5320E and UCC5390E

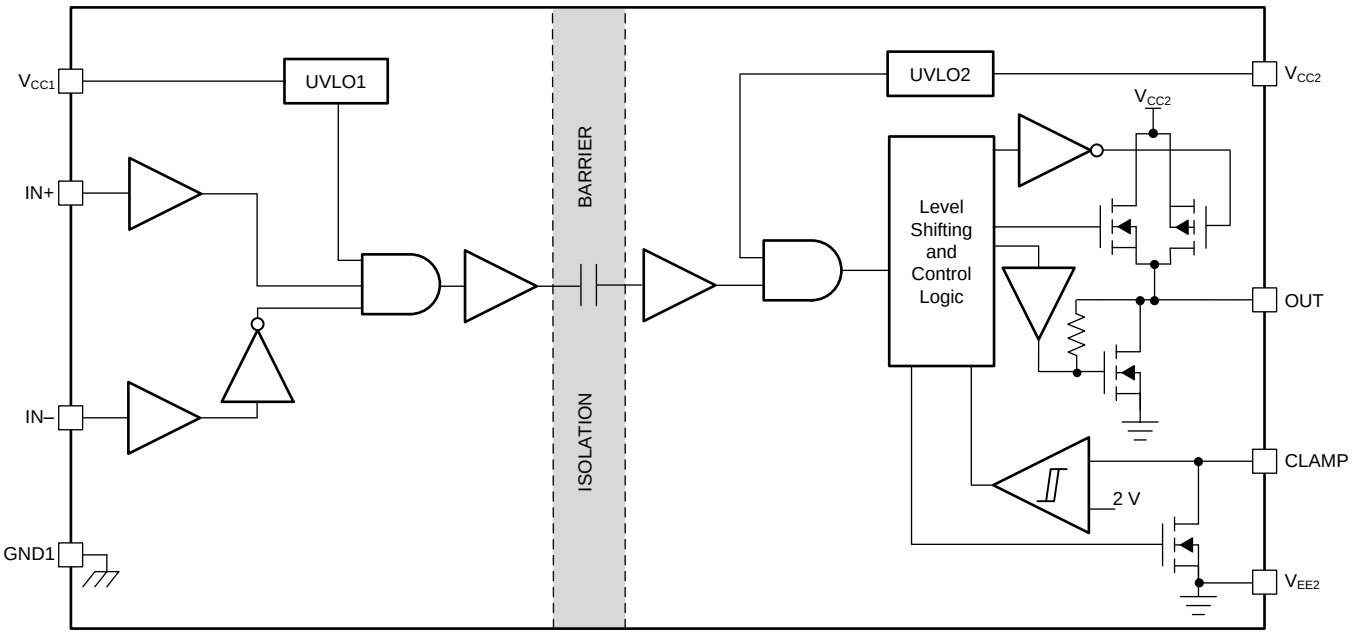

図 7. Functional Block Diagram of UCC5310M and UCC5350M

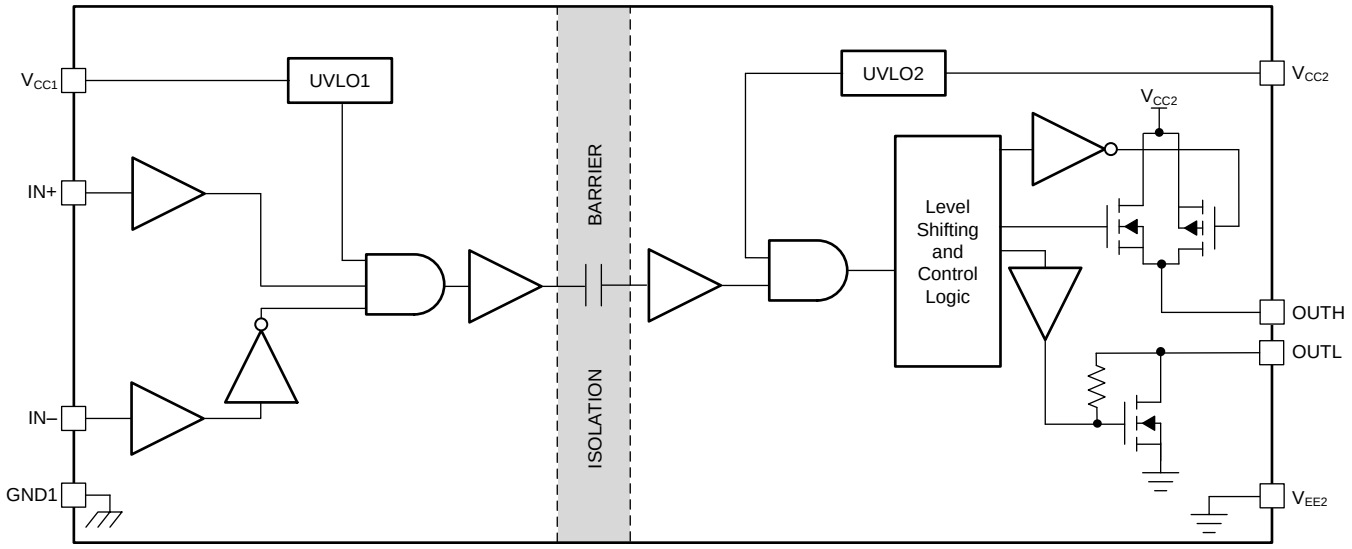

図 8. Functional Block Diagram of UCC5320S and UCC5390S

2.3 System Design Theory

2.3.1 DC to Three-Phase AC Inverter Subsystem

In this reference design, IGBT module CM100TX-24S is used to characterize the UCC5350MCD. The CM100TX-24S is a 1200-V, 100-A IGBT module that has an internal gate resistance of 0 Ω, which allows direct measurement of the Miller induced gate voltage by measuring the voltage drop across the external gate resistor. The IGBT module 6MI180VB-120-50 is used with the UCC5390ECD to convert the DC bus voltage into a three-phase AC. The 6MI180VB-120-50 is a 1200-V, 180-A IGBT with a gate charge of 1500 nC. The typical source/sink currents that can be provided by the UCC5390ECD is 17 A, which can quickly charge the input capacitance of the IGBT.

A schematic of the three-phase inverter stage is shown in 図 9.

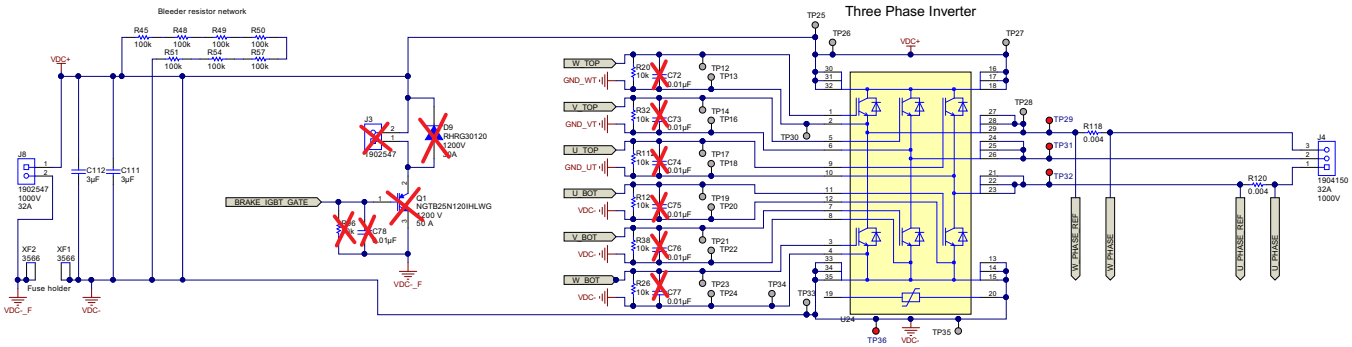

図 9. Schematic of DC to Three-Phase AC Inverter

R20, R32, R112, R12, R38, and R26 are 10-kΩ resistors used to ensure that the IGBTs remain off in case the gate drivers get disconnected due to system malfunction. C72 to C77 are provisions for additional external gate-to-emitter capacitance. R118 and R120 are shunt resistors used for U- and W-phase current sensing. Terminal block J8 is the DC bus voltage input connector. C112 and C111 are localized high-frequency DC bus decoupling capacitors. This reference design uses 3-µF, 1300-V film capacitors. XF2 and XF1 are fuse holders. A 30-A, 1-kV DC cartridge fuse with dimensions of 10.3 mm × 38 mm must be placed within the fuse holders. To facilitate the discharge, bleeder resistors R45, R48, R49, R50, R51, R54, and R57 are added across the DC link capacitors. Provision is given to connect brake resistor to the DC bus. In case of motor regeneration, if the DC bus voltage goes above a specified threshold, the brake chopper can be initiated. J3 is the terminal block used to connect the braking resistor. D9 is the freewheeling diode connected across the braking resistor to prevent overshoots at the collector of brake chopping IGBT power switch Q1.

2.3.2 Gate Driver Power Supply

VCC1 and GND1 are the supply pins for the input side of the UCC53xx. The supply voltage at VCC1 can range from 3 to 15 V with respect to GND1, thus supporting the direct interface to 3.3-V low-power controllers as well as legacy 5-V controllers. A 4.7-µF bulk capacitor C1 is placed close to the IC power supply to provide a stable supply to the primary side of the gate driver. VCC2 and VEE2 are the supply pins for the output side of the UCC5350MCD. A positive V_{GE} of typically 15 V is required to switch the IGBT well into saturation. In this reference design, VCC2 is fed with external 15 V for the low-side gate driver to ensure that IGBT is in full saturation. A bootstrap supply is used to power up the high-side gate driver. 図 10 shows the schematic of the U-phase gate driver, UCC5350MCD.

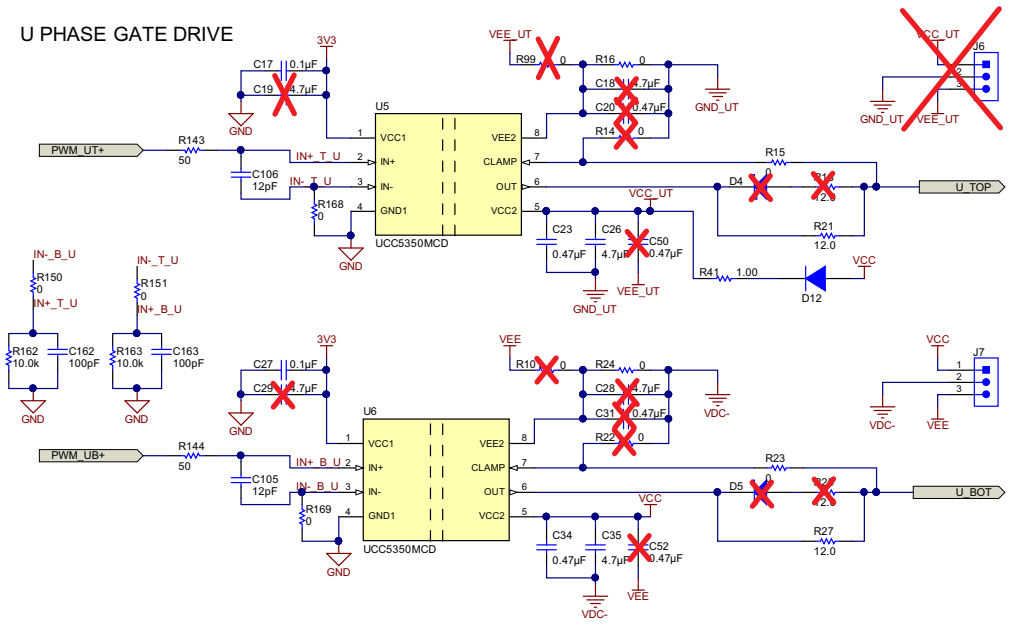

図 10. Schematic of Gate Driver UCC5350MCD

The UCC5390ECD has three power pins on the secondary side: VEE2, VCC2, and GND2. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 13.2 V up to 33 V with respect to VEE2. In this reference design, a bipolar supply of 15 V/–8 V is used to power the UCC5390ECD. 図 11 shows the schematic of the U-phase gate driver, UCC5350ECD.

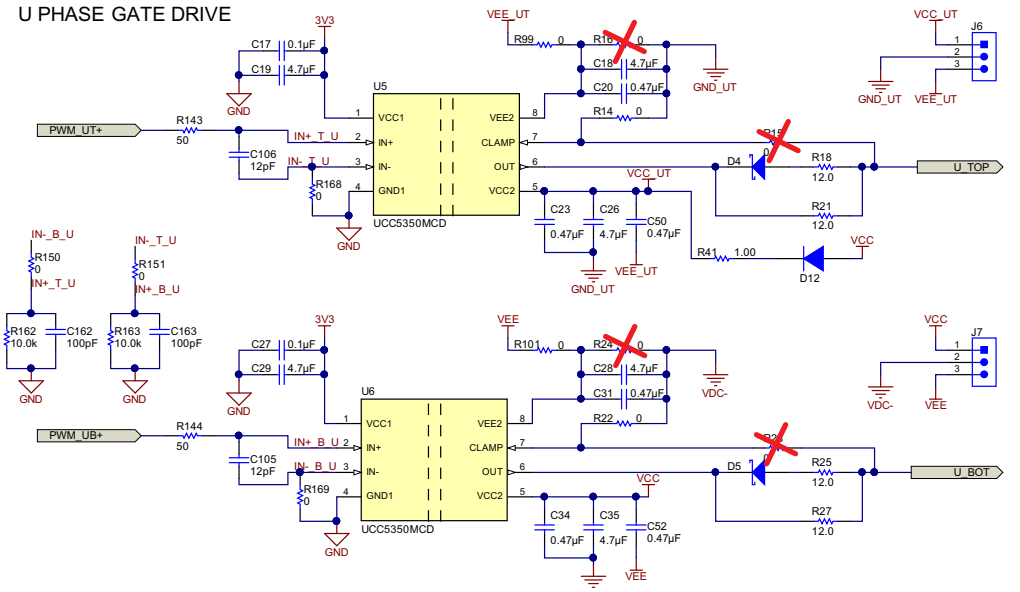

図 11. Schematic of Gate Driver UCC5390ECD

2.3.3 Designing IN+/IN– Input Filter and Interlocking

A small input RIN-CIN filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces. Such a filter must use an RIN in the range of 0 to 100 Ω and a CIN from 10 to 100 pF. In this reference design, an RIN = 50 Ω and a CIN = 12 pF are selected. When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

This reference design also features interlocking between the top and the bottom IGBT gate drivers as shown in 図 12, so that the positive deadband at the input is converted into negative deadband at the output. This safety feature ensures that the high-side and low-side IGBTs do not turn on at the same time. A parallel RC circuit with R = 10k and C = 100 pF is used at the input pin IN+ and IN– of the gate driver to avoid the gate driver from going into an unknown state.

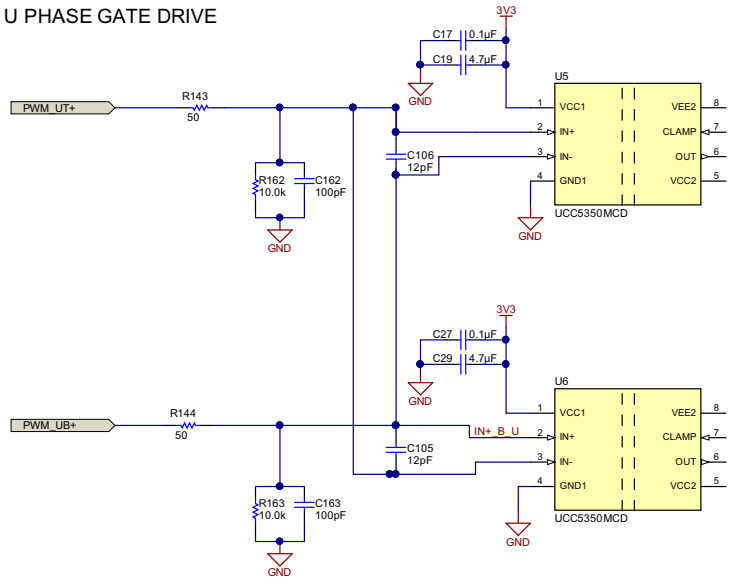

図 12. Schematic of Interlocking Feature

2.3.4 Source and Sink Currents of Gate Driver

To turn on IGBTs and FETs, an initial source peak current must be injected into the gate (up to several amps for larger power devices), and then a holding voltage is required to keep the device on. To turn off, a similar peak sink current opposite the polarity current is required to discharge the gate capacitance, and then a zero or (preferably) negative holding voltage is required to keep the device off.

The source and sink currents of the gate drivers can be controlled by the external gate resistor as shown in 式 1:

$$\text{Peak Gate Current } (I_G) = \frac{V_{G(on)} - V_{G(off)}}{R_G + R_{G(int)}} \quad (1)$$

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 PCB Overview

図 13 shows the top view of the PCB. The DC bus input connector J8 and the three-phase motor output connector J4 are indicated. Provision is given to add a connector J3 for connecting an external brake resistor to the DC bus. J1 is a female 25-pin D-SUB connector for interfacing to the controller. The primary-side 5-V power supply is connected to J2, and the secondary side isolated 15-V power supply is connected to J7. For giving bipolar supply as is required for the UCC5390ECD, connectors J5, J6, and J13 are provided to supply the top three gate drivers with 15 V/–8 V and ground connection. For giving a unipolar supply for the UCC5350MCD, J5, J6, and J13 can be disconnected or left open.

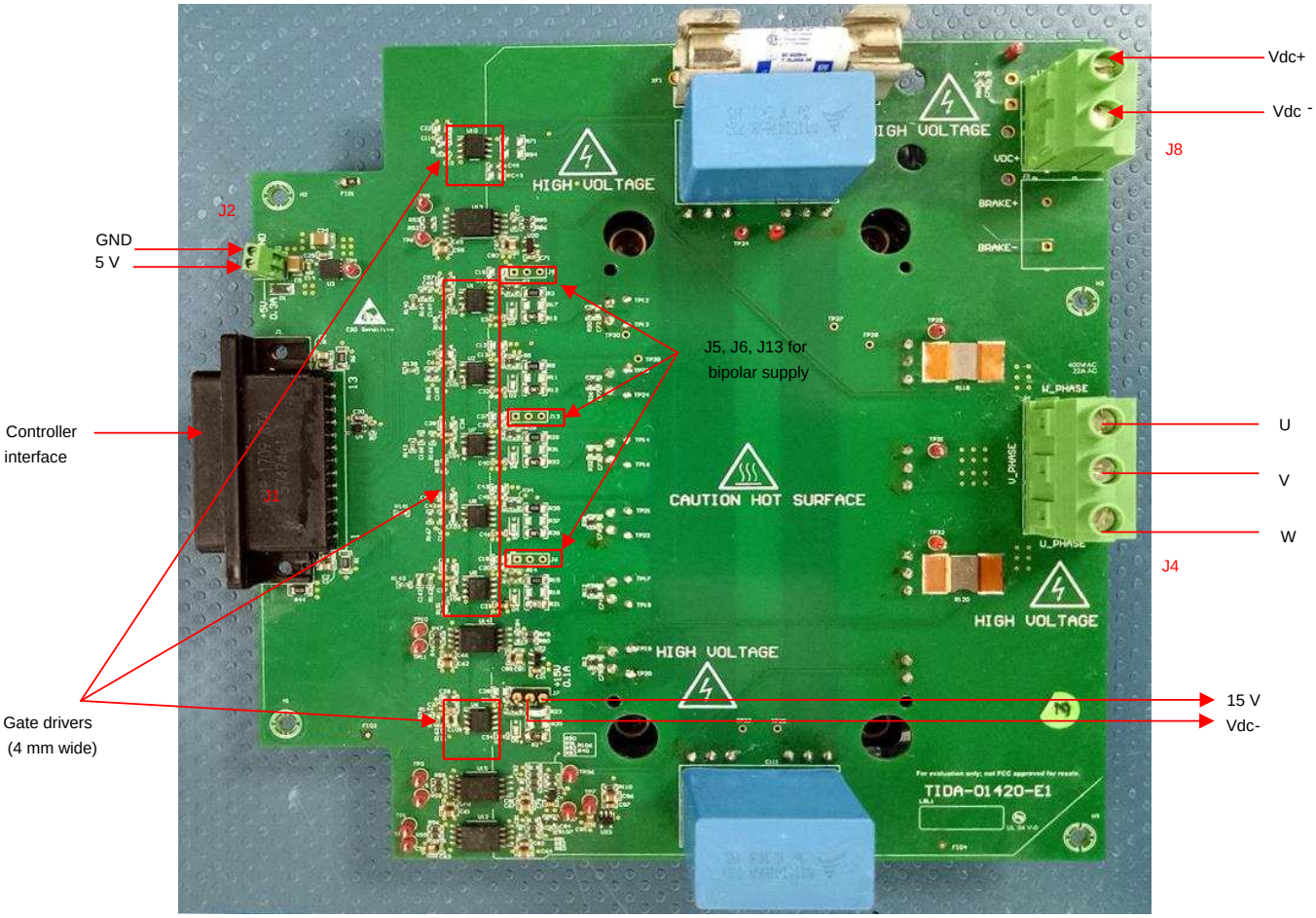

図 13. Top View of TIDA-01420 Board

図 14 indicates the primary low-voltage side, the secondary high-voltage side, and the basic isolation barrier in between.

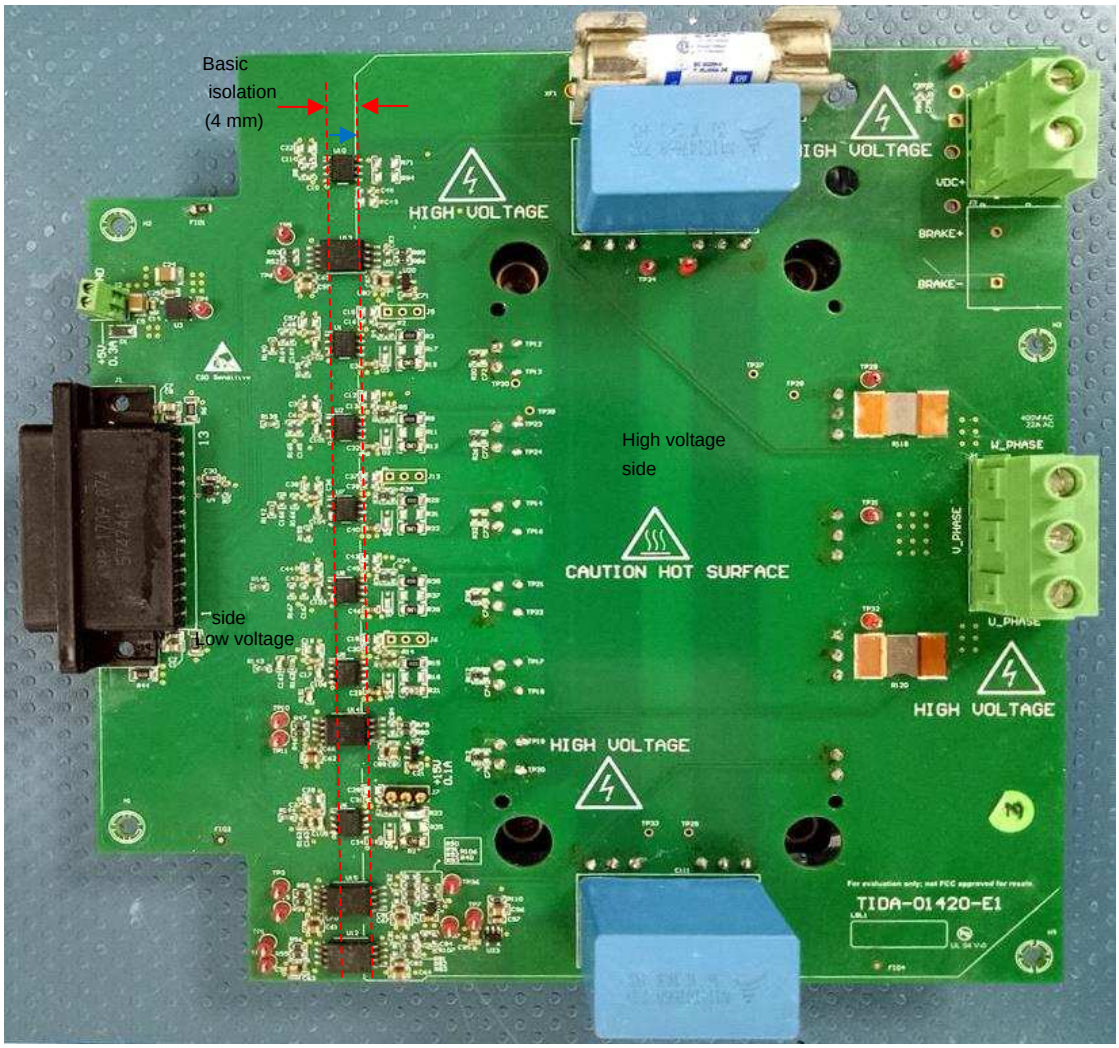

図 14. Primary Side, Secondary Side, and Basic Isolation Barrier

図 15 shows the bottom view of the PCB. Provision is given for adding brake chopper IGBT Q1 and freewheeling diode D9. The pad of the IGBT module must be connected to a heat sink. The thermal compound must be used between the pad and the heat sink, and the module must be rigidly screwed to the heat sink. Choose an appropriate heat sink based on the maximum continuous power to be dissipated.

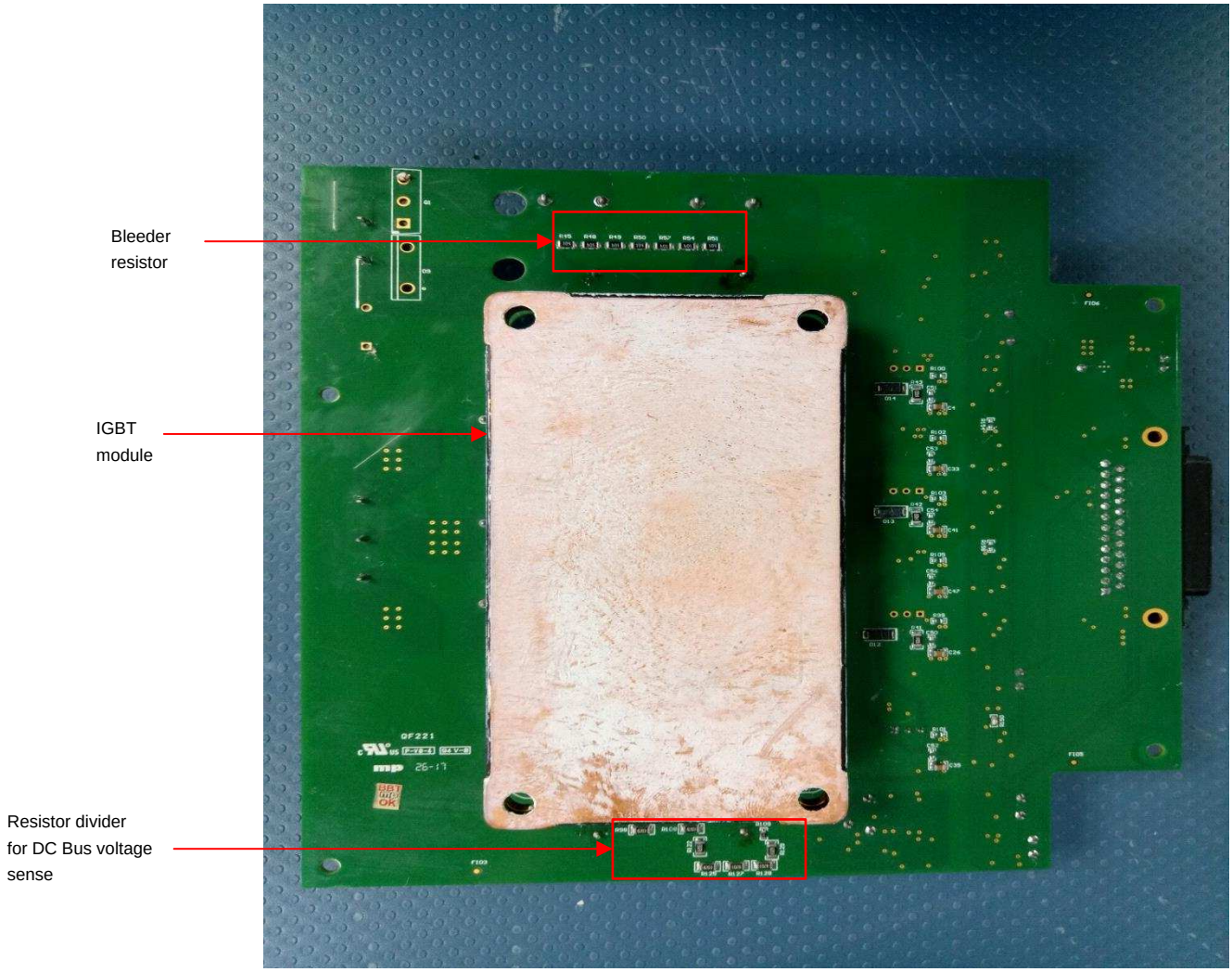

図 15. Bottom View of TIDA-01420 Board

3.1.2 Controller Interface Connector

The Delfino control card is connected to J1 on the TIDA-001420 board through an adaptor PCB as shown in 図 16. A ribbon cable is used to connect the two. The pin functions are described in 表 3.

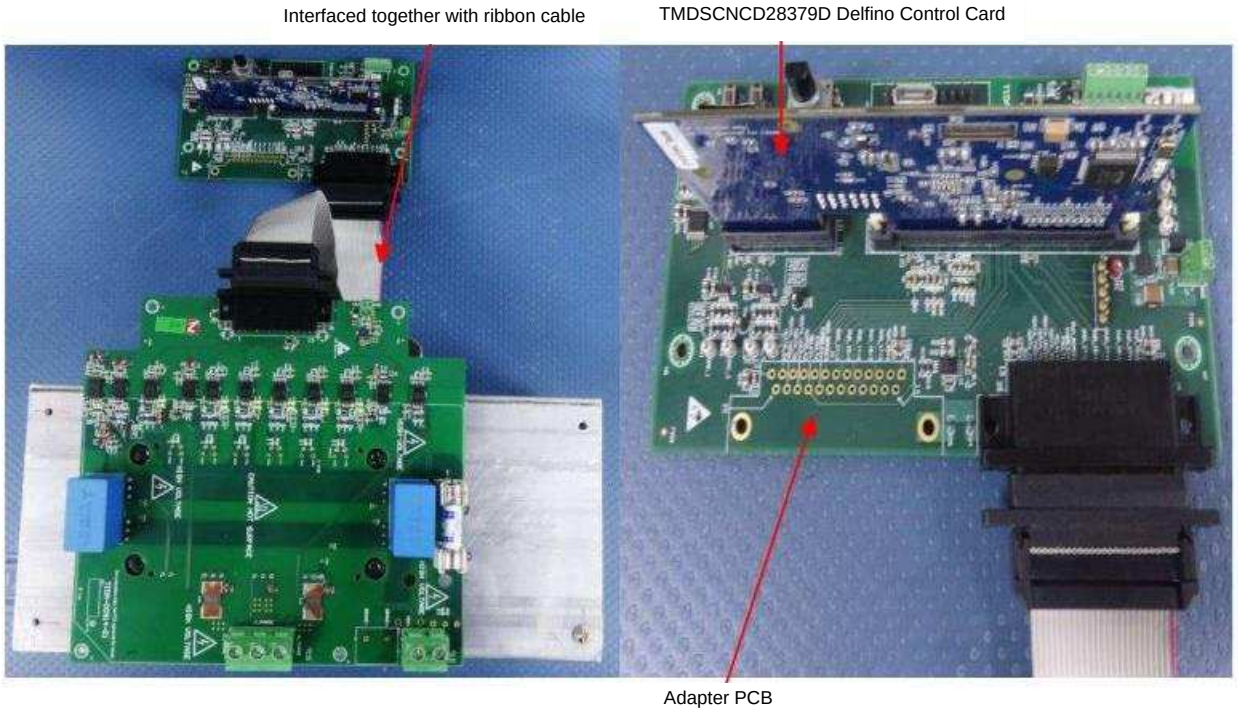

図 16. Interface of TIDA-01420 Board With Control Card

表 3. Connector Pin Description

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	5V0	Power	5-V input to the primary side of the power stage
2	PWM_UB+	3.3-V input	Phase U low-side gate driver PWM input
3	PWM_UT+	3.3-V input	Phase U high-side gate driver PWM input
4	PWM_VB+	3.3-V input	Phase V low-side gate driver PWM input
5	PWM_VT+	3.3-V input	Phase V high-side gate driver PWM input
6	PWM_WB+	3.3-V input	Phase W low-side gate driver PWM input
7	PWM_WT+	3.3-V input	Phase W high-side gate driver PWM input
8	PWM_BRAKE+	3.3-V input	PWM input to brake IGBT gate driver
9	NC	NA	N/A
10	MDATA_U	3.3-V output	U phase current measurement data from ΔΣ modulator
11	NC	NA	N/A
12	MDATA_W	3.3-V output	W phase current measurement data from ΔΣ modulator
13	5V0	Power	5-V input to the primary side of the power stage
14	GND	Power	Primary-side ground
15	GND	Power	Primary-side ground
16	GND	Power	Primary-side ground
17	GND	Power	Primary-side ground
18	GND	Power	Primary-side ground
19	GND	Power	Primary-side ground
20	GND	Power	Primary-side ground
21	NC	NA	N/A
22	CLK	3.3-V input	Clock input to TIDA-01420 from the control card
23	MDATA_VDC	3.3-V output	DC bus voltage measurement data from ΔΣ modulator
24	MDATA_TMP	3.3-V output	Temperature measurement data from ΔΣ modulator
25	GND	Power	Primary-side ground

3.2 Testing and Results

3.2.1 Test Setup

The focus of the tests is to evaluate the functionality and performance of the basic isolated gate drivers UCC5350MCD and UCC5390ECD. The IGBT used for testing UCC5350MCD is CM100TX-24S whereas the IGBT used for testing UCC5390ECD is 6MI180VB-120-50.

3.2.2 Software

This reference design is tested using software modified from the application report *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x*. The incremental build level 2 shown in 図 17 is modified. A switch is added to connect either the OUT signal coming from the RG MACRO or the angle variable to the sine cos block. Connecting OUT enables the design to pump sinusoidal current into the motor. Connecting the angle variable, which is made zero, enables driving DC current into the motor

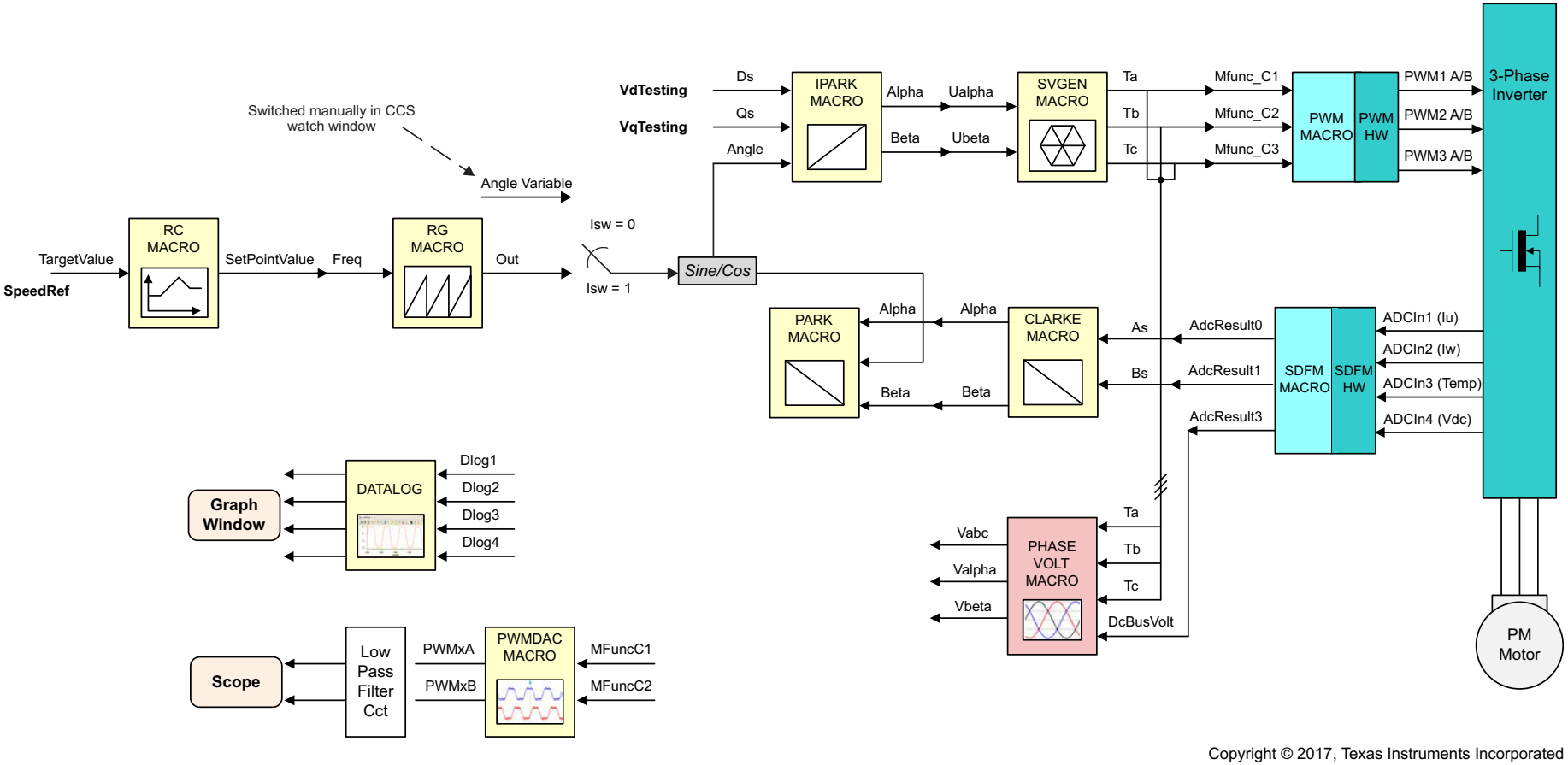

図 17. PWM Control and Current Sense Software

3.2.3 Test Results for UCC5350MCD

3.2.3.1 UVLO Protection

図 18 shows the UVLO protection feature of the gate driver. The IGBT is turned off if the secondary side supply voltage of the UCC5350MCD, VCC2, drops below 11.10 V irrespective of IN+, IN– RST until VCC2 goes above 12.30 V.

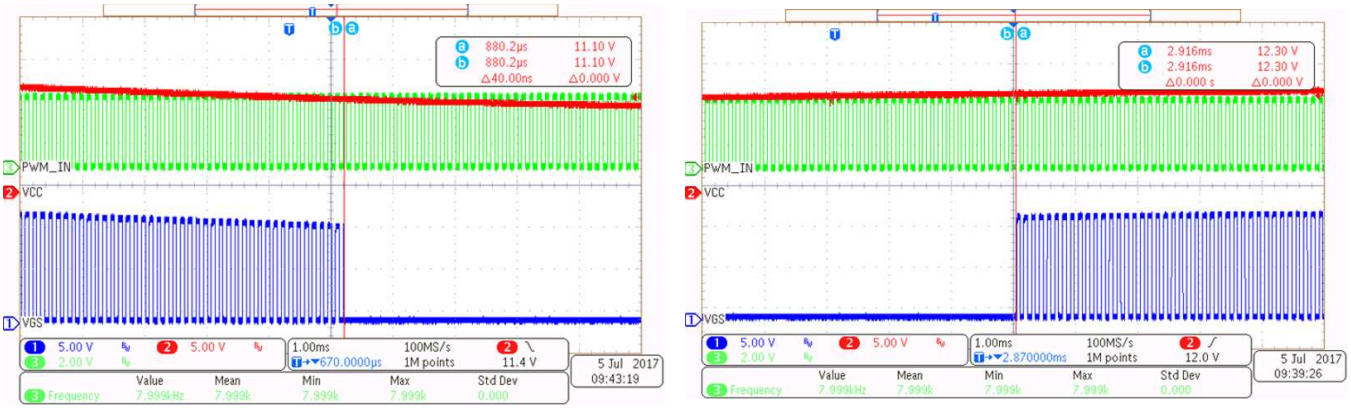

図 18. UVLO Protection Feature of UCC5350MCD Gate Driver

3.2.3.2 Propagation Delay

図 19 shows the line diagram where the measurements are taken for the propagation delay.

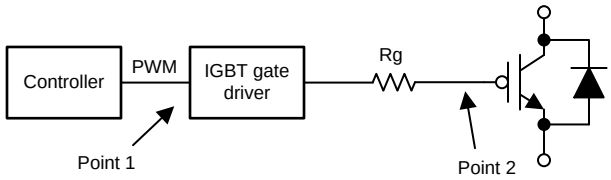

図 19. Propagation Delay Measurement Points

図 20 shows the propagation delays measured for the three low-side gate drivers at rising and falling edges for the UCC5350MCD. 表 4 lists down the propagation delays of the bottom gate drivers. For these figures, the green waveform is the probing point 1, and the blue waveform is the probing point 2. 表 4 summarizes the test results of propagation delay.

表 4. Propagation Delay of Bottom Three Gate Drivers (UCC5350MCD)

PARAMETER	U2	U4	U6
Rising edge (turnon)	70 ns	60 ns	70 ns
Falling edge (turnoff)	60 ns	60 ns	50 ns

Note that the maximum skew between the propagation delay is 10 ns. Low propagation delay allows the design to achieve high switching speeds.

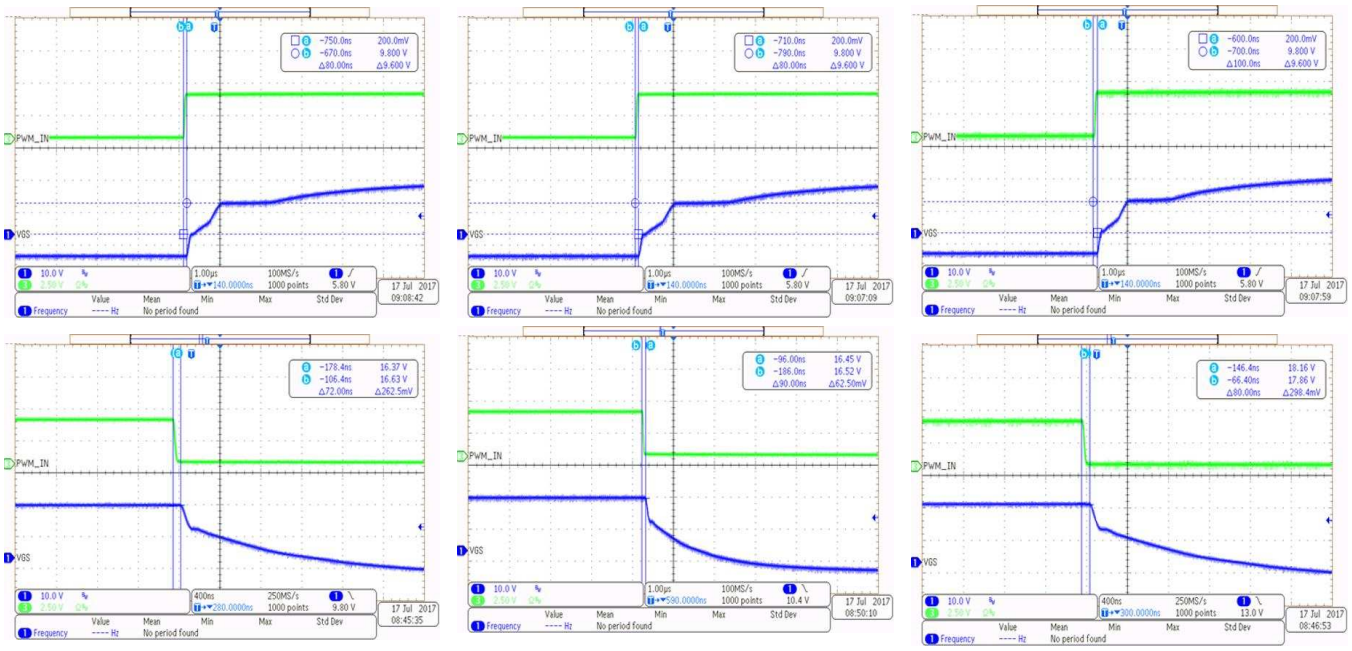

図 20. Propagation Delay of Bottom Gate Drivers (UCC5350MCD)

3.2.3.3 Source/Sink Currents

The source and sink current waveforms have been captured for the bottom IGBTs by measuring the voltage drop across the gate resistors. 図 21 shows the source and sink currents provided by the UCC5350MCD for charging the gate of the IGBT at DC bus voltage of 565 V. The external gate resistor used in this case is 12 Ω, which is in accordance to the recommendation specified in the IGBT datasheet.

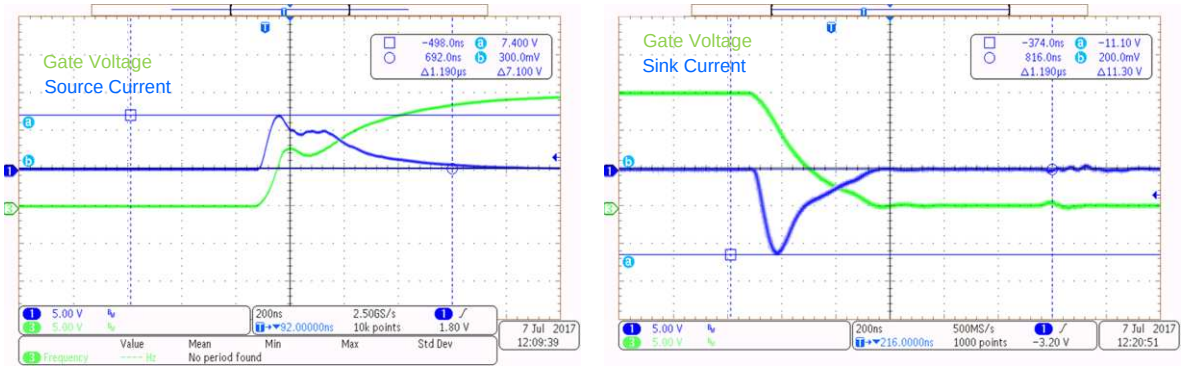

図 21. Source and Sink Currents With IGBT Module at DC Bus Voltage of 565 V With UCC5350MCD

$$\text{Source Current} = \frac{\text{Voltage drop across external resistor during IGBT turnon}}{\text{Value of external resistor}} = \frac{7.1\,\text{V}}{12\,\Omega} = 0.591\,\text{A} \quad (2)$$

$$\text{Sink Current} = \frac{\text{Voltage drop across external resistor during IGBT turnoff}}{\text{Value of external resistor}} = \frac{11.3\,\text{V}}{12\,\Omega} = 0.941\,\text{A} \quad (3)$$

However, the source and sink capabilities of the device is greater than these specified values. The UCC5350MCD can easily drive an IGBT of a high-input capacitance value. This has been verified by replacing the IGBT modules with an external capacitor of 56 nF and measuring the source and sink currents as shown in 図 22. The value of external gate resistor used for making these measurements is 1 Ω with the UCC5350MCD. 式 4. 式 5 shows the sourcing and sinking capability of gate drivers when the external capacitor is used.

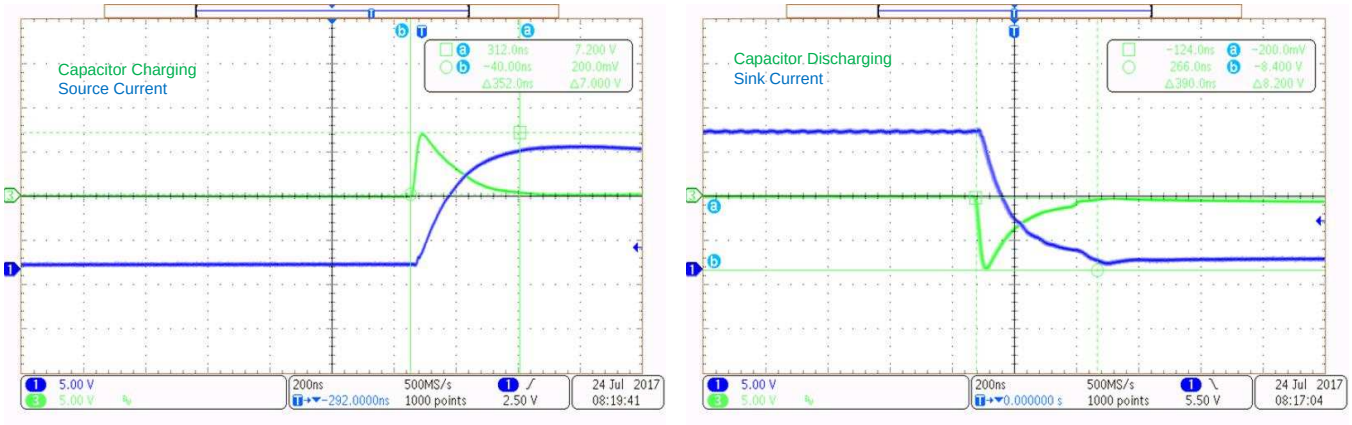

図 22. Source and Sink Currents of UCC5350MCD With 56-nF Capacitor

$$\text{Source Current} = \frac{\text{Voltage drop across external resistor during IGBT turnon}}{\text{Value of external resistor}} = \frac{7\ \text{V}}{1.5\ \Omega} = 4.67\ \text{A} \tag{4}$$

$$\text{Sink Current} = \frac{\text{Voltage drop across external resistor during IGBT turnoff}}{\text{Value of external resistor}} = \frac{8.2\ \text{V}}{1.5\ \Omega} = 5.47\ \text{A} \tag{5}$$

3.2.3.4 *Turn on and Turn off of IGBT*

図 23 and 図 24 show the IGBT turnon and turnoff time intervals. A crude estimate of the IGBT charging and discharging times can be calculated using simplified linear approximations of the gate drive current, drain current, and drain voltage waveforms during periods 2 and 3 of the switching transitions.

式 6 and 式 7 show the charging times:

$$Ig1 + Ig2\_on = \frac{V_{DRV} - 0.5 \times V_{Miller}}{R\_Total} \tag{6}$$

$$t1 + t2\_on = CISS \times \frac{V_{Miller}}{Ig1 + Ig2} \tag{7}$$

式 8 and 式 9 show the discharging times:

$$Ig3\_off = \frac{V_{DRV} - V_{Miller}}{R\_Total} \tag{8}$$

$$t3\_off = CRSS \times \frac{V_{DS,off}}{Ig3} \tag{9}$$

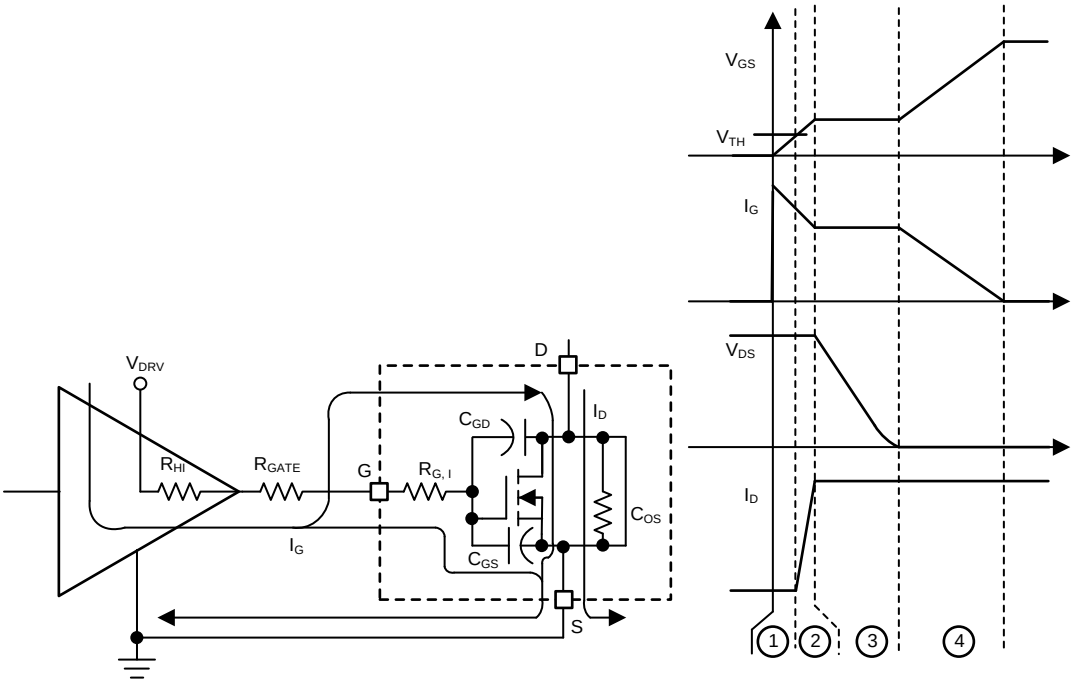

図 23. IGBT Turnon Time Intervals

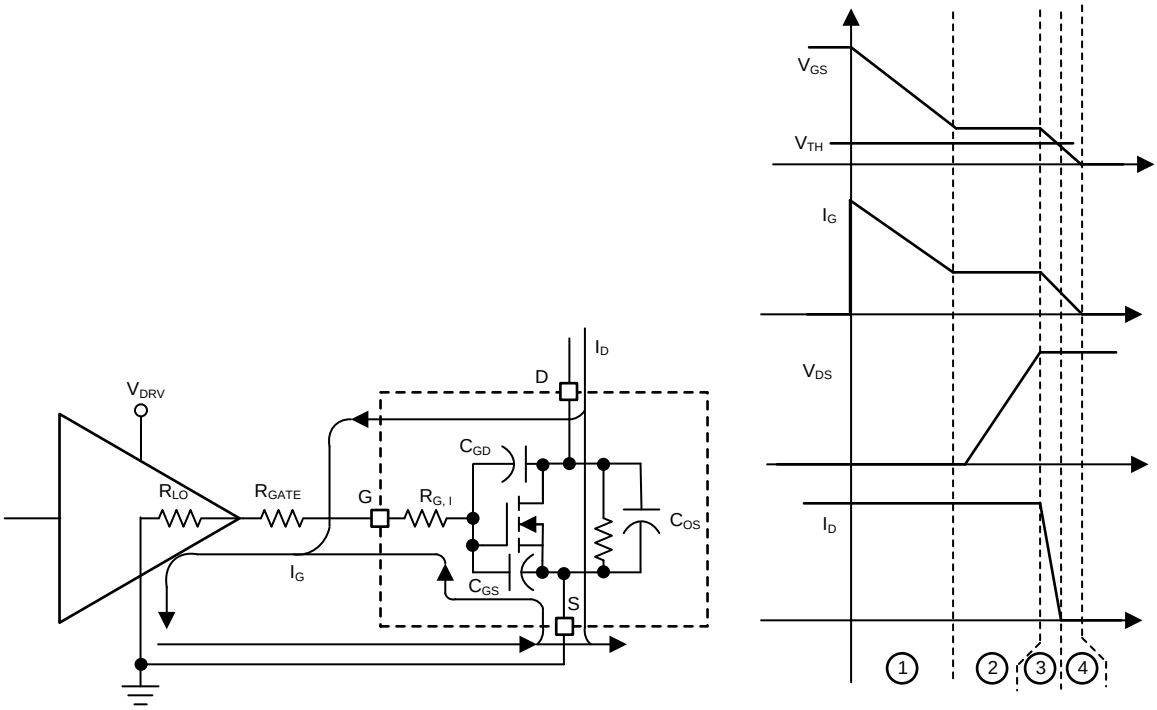

図 24. IGBT Turnoff Time Intervals

表 5 shows the theoretical values of turnon and turnoff times currents at DC bus voltage of 250 V and 565 V as calculated from 式 6 to 式 9:

表 5. Theoretical Values of Turnon and Turnoff Times for UCC5350MCD

PARAMETER	UCC5350MCD (250 V)	UCC5350MCD (565 V)
R_external	12 Ω	12 Ω
R_internal_igbt	0 Ω	0 Ω
R_on_driver	1.36 Ω	1.36 Ω
R_off_driver	0.26 Ω	0.26 Ω
IGBT module used	CM100TX-24S	CM100TX-24S
CISS of IGBT	10 nF	10 nF
CRSS of IGBT	0.1 nF	0.06 nF
Supply voltage VCC2	15 V	15 V
Turnon current (Ig1+Ig2_on)	0.823 A	0.823 A
Turnoff current (Ig2_off)	0.56 A	0.56 A
Turnon time (t1+t2_on)	98.5 ns	98.5 ns
Turnoff time (t2_off)	44.64 ns	60.53ns

図 25 and 図 26 show the experimental values of the corresponding calculated results for the UCC5350MCD. The experiment is carried out for two different sets of DC Bus voltages, 250 V and 565 V:

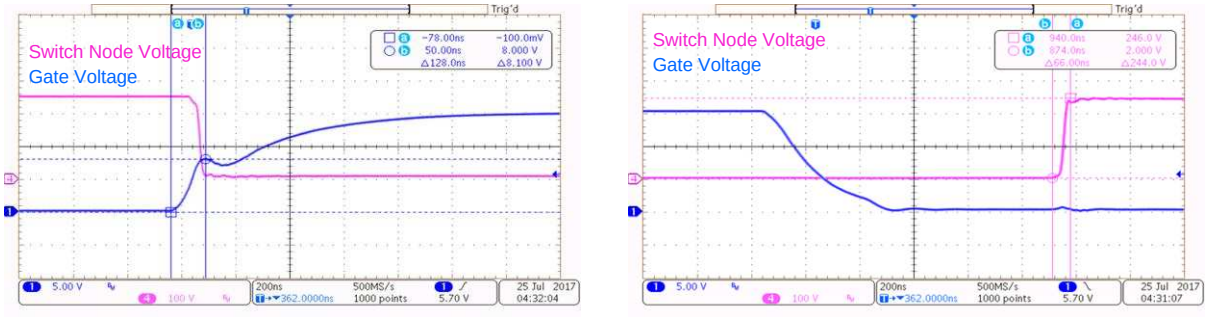

図 25. Turnon and Turnoff Times of IGBT at 250-V Bus Voltage Using IGBT CM100TX-24S With UCC5350MCD

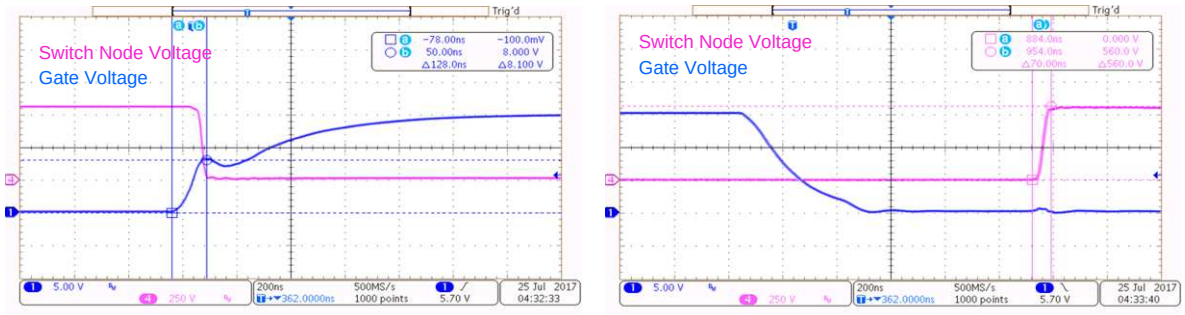

図 26. Turnon and Turnoff Times of IGBT at 565-V Bus Voltage Using IGBT CM100TX-24S With UCC5350MCD

表 6 summarizes the experimental results as follows:

表 6. Experimental Values of Turnon and Turnoff Times of IGBTs

PARAMETER	UCC5350MCD (250 V)	UCC5350MCD (565 V)
IGBT used	CM100TX-24S	CM100TX-24S
Turnon time (t1+t2_on)	128 ns	128 ns
Turnoff time (t2_off)	66 ns	70 ns

3.2.3.5 Suppression of Miller Induced Gate Voltage

The UCC5350M features an active Miller-clamp function that prevents false turnon of the power switches caused by Miller current in applications where unipolar power supply is used. 図 27 and 図 28 show the Miller induced gate voltage when the Miller clamp pin of the UCC5350MCD is disconnected from the circuit.

When dV/dt = 4.79 kV/µs, the induced voltage is 3 V. As dV/dt increases to 8.47 kV/µs, the corresponding induced voltage at the gate goes up to 3.8 V.

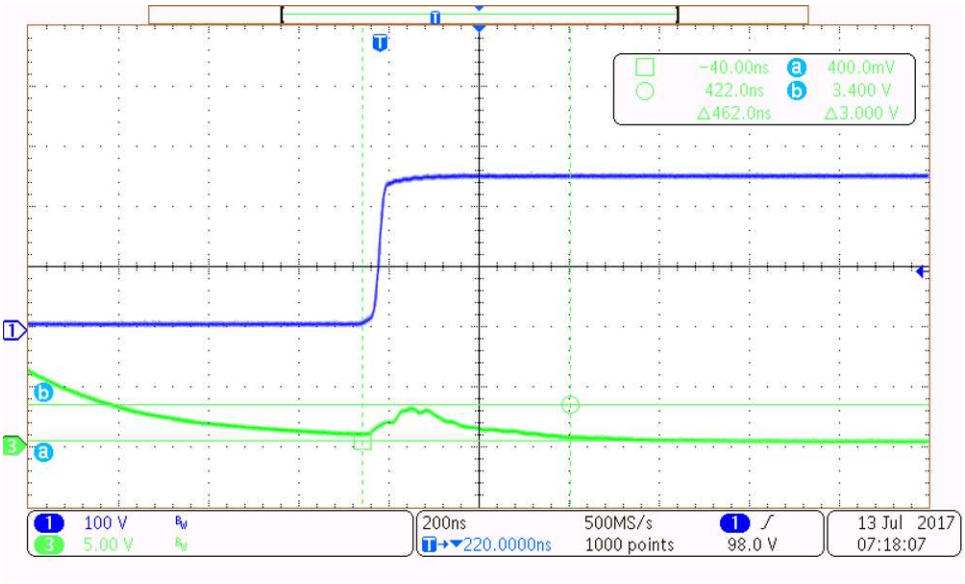

図 27. Miller Induced Gate Voltage of 3.0 V at dV/dt = 4.79 kV/µs With Miller Pin Disconnected

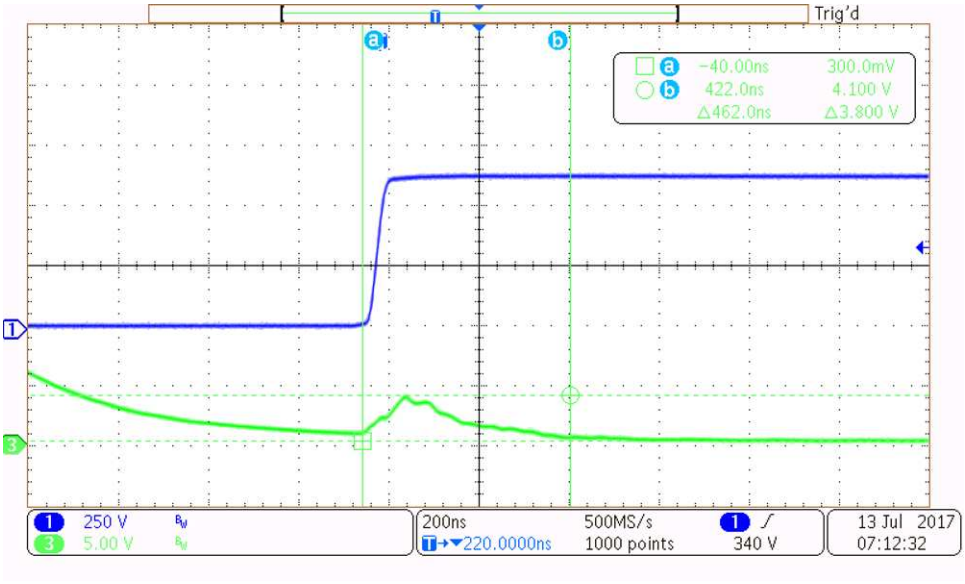

図 28. Miller Induced Gate Voltage of 3.8 V at dV/dt = 8.47 kV/µs With Miller Pin Disconnected

図 29 and 図 30 show the same set of test results when the Miller clamp pin is reconnected to the circuit. The induced voltage is suppressed as the Miller current sinks through the low impedance path between the power switch gate terminal and ground, VEE2.

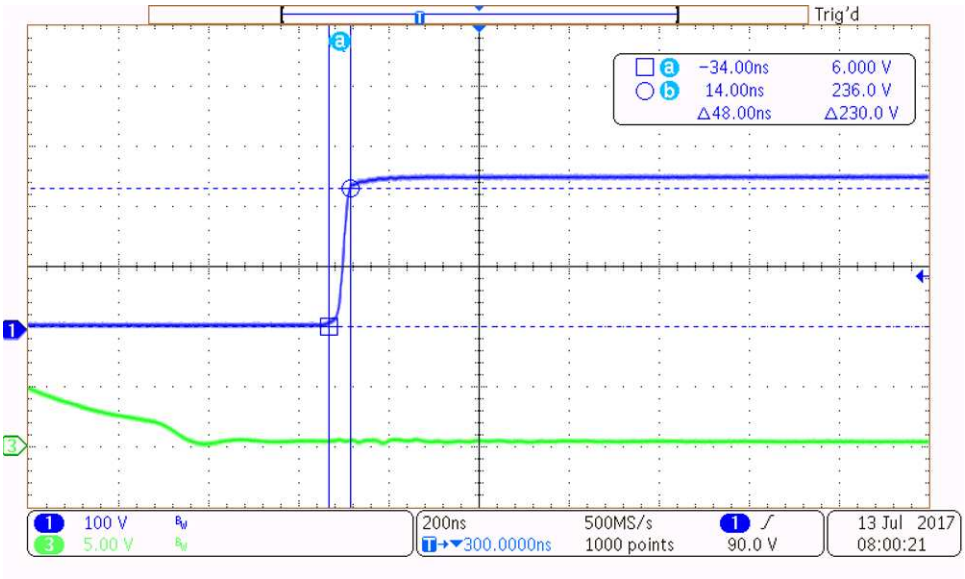

図 29. No Voltage Induced at dV/dt = 4.79 kV/µs With Miller Pin Connected

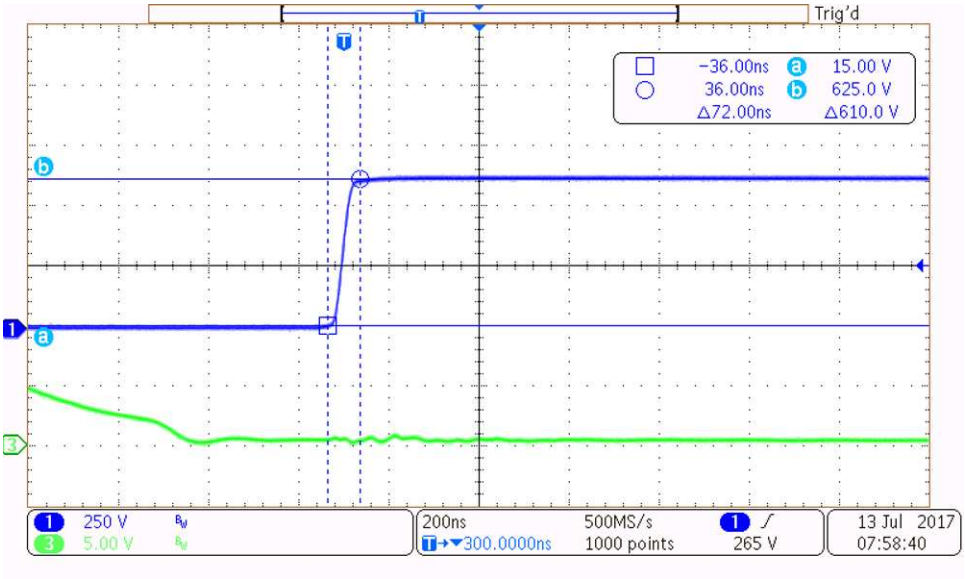

図 30. No Voltage Induced at dV/dt = 8.47 kV/µs With Miller Pin Connected

表 7 summarizes the test results as follows:

表 7. Summary of Miller Induced Gate Voltages at Different dV/dt

MILLER PIN STATUS	dV/dt MILLER INDUCTED (kV/µs)	GATE VOLTAGE (V)
Disconnected	4.8	3.0
Connected	4.8	0
Disconnected	8.5	3.8
Connected	8.5	0

3.2.3.6 Power Supply Rail for High-Side Gate Drivers (Bootstrap Supply)

図 31 shows the ripple on the bootstrap voltage and the switch node voltage. The bus voltage applied while taking these measurements is 50 V. The bus voltage had to be limited to 50 V during the experiment due to the constraint put by the common-mode rejection ratio of the oscilloscope. The duty cycle of the PWM signal is varied to see the variations in the power supply ripple voltage. 表 8 summarizes the results.

表 8. Summary of Variation of Bootstrap Ripple Voltage With Duty Cycle

DUTY CYCLE	RIPPLE VOLTAGE on POWER SUPPLY (mV)
90%	440
50%	840
10%	1320

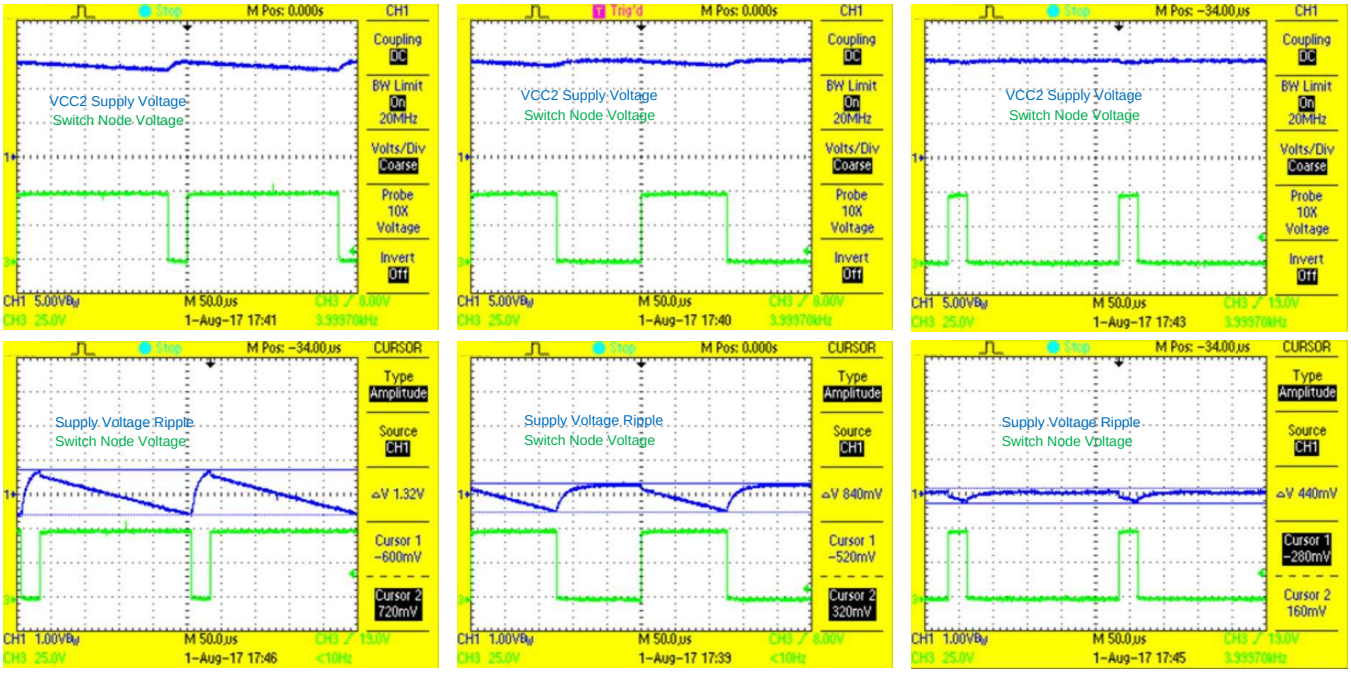

図 31. Variation of Bootstrap Supply Ripple With Change in Duty Cycle

3.2.3.7 Interlocking Functioning

This experiment is done by applying a negative deadband (setting both high-side and low-side PWM signals high for a certain time) at the inputs of the gate drivers. 図 32 shows that because of interlocking, the negative dead time at the input is converted into positive dead band at the output of the gate driver. Thus, this protection feature avoids the possibility of shoot-through.

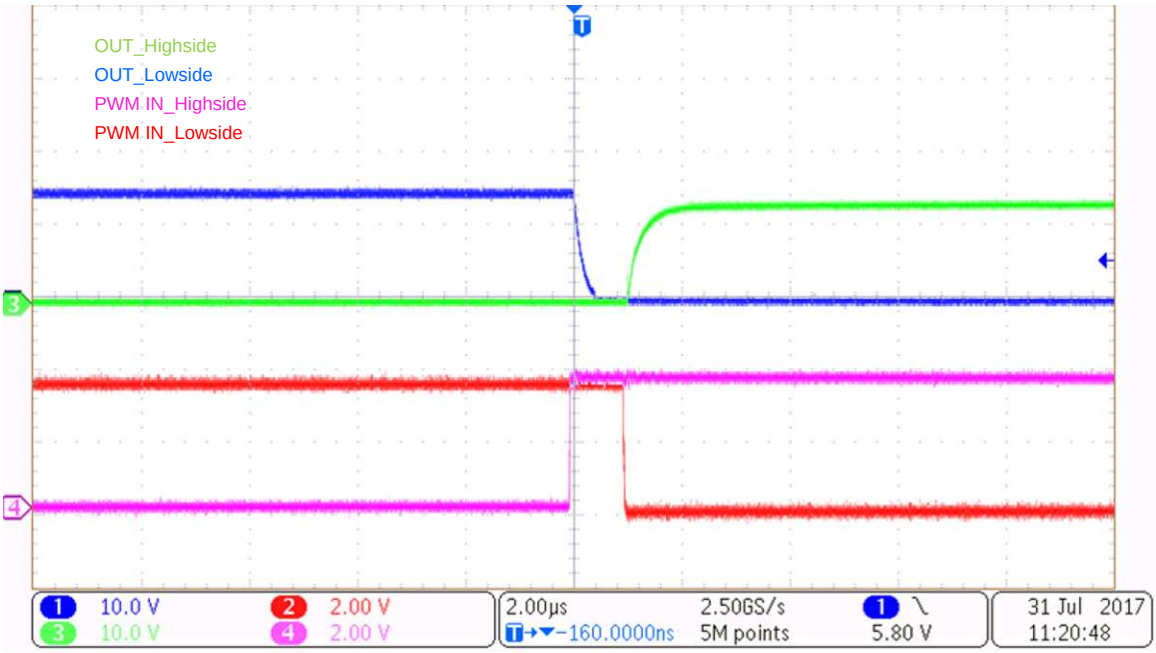

図 32. Interlocking Feature of Design

3.2.3.8 Thermal Image

The thermal image of the board is taken by applying the DC bus voltage of 565 V for a time period of 30 minutes. The switching frequency is kept at 16 kHz. For safety purposes, the board to be tested is kept in a glass chamber and the thermal camera is focused from outside the chamber as shown in 図 33. For more accurate parameters, see the UCC53x0 datasheet (SLLSER8).

図 33. Image of Board Inside High-Voltage Safety Box

図 34 shows the thermal image of the boards UCC5350MCD respectively and the corresponding minimum, maximum, and average temperatures. The ambient temperature while making these measurements is 25°C.

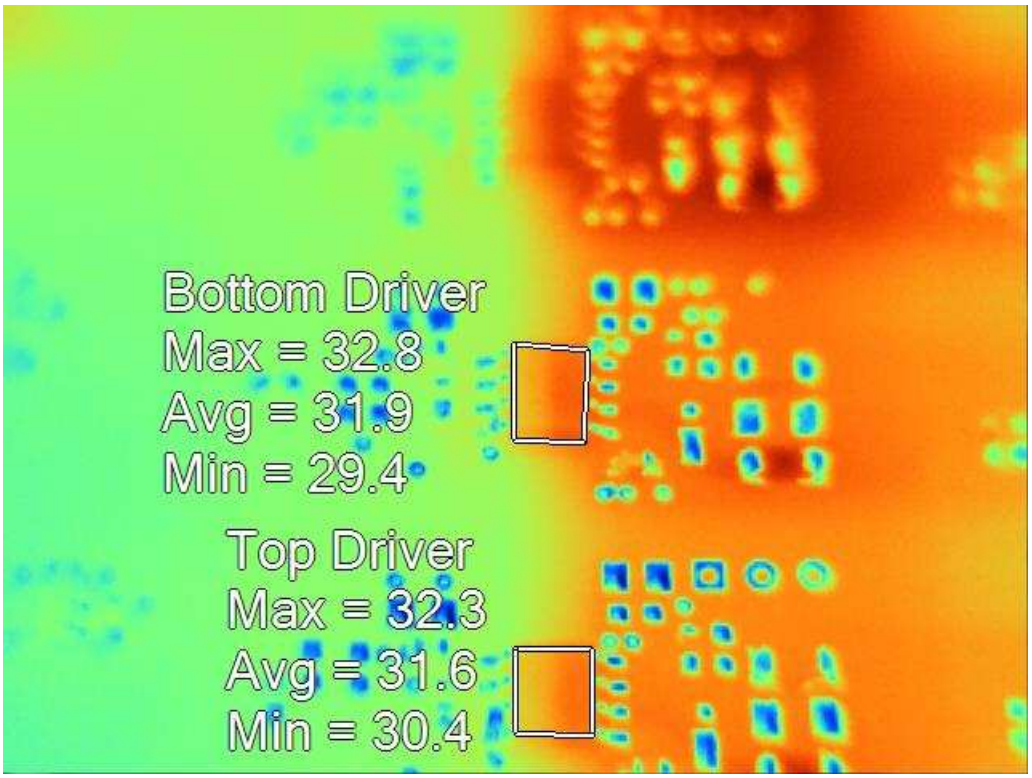

図 34. Thermal Image of Board With Gate Driver UCC5350MCD

3.2.4 Test Results for UCC5390ECD

3.2.4.1 UVLO Protection

The UCC5390ECD has an external pin for UVLO measurement, which is referenced to ground rather than VEE2. As shown in 図 35, IGBT is turned off if the secondary side supply voltage of the UCC5390ECD, VCC2, drops below 11.09 V irrespective of IN+, IN– until VCC2 goes above 12 V.

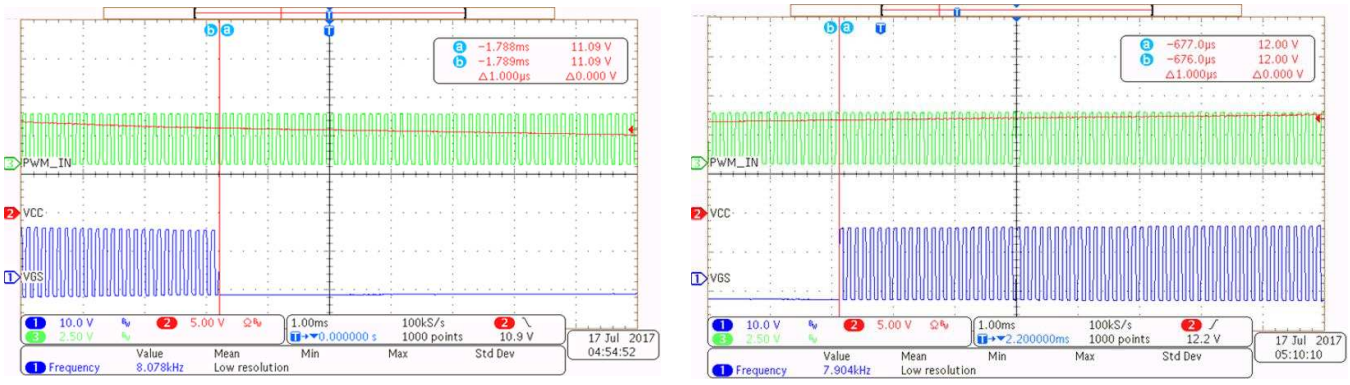

図 35. UVLO Protection Feature of UCC5390ECD Gate Driver

3.2.4.2 Power Consumption by Gate Drivers

In this experiment, the UCC5390ECD is used to drive the IGBT module, 6MI180VB-120-50. The static power loss, P_{GDQ} includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The power supplied by the gate driver can be calculated by measuring the average current consumed by it as shown in 式 10.

$$P_{GDQ} = VCC1 \times ICC1 + VCC2 \times ICC2 \approx VCC2 \times ICC2 \quad (10)$$

表 9 shows the power supplied to the gate driver at 8- and 16-kHz switching frequencies:

表 9. Power Supplied to Bottom Gate Drivers

FREQ SWITCHING	SUPPLY CURRENT (ICC2)	SUPPLY VOLTAGE (VCC2)	POWER SUPPLIED, P_{GDQ} (3 DRIVERS)	POWER SUPPLIED, P_{GDQ} (PER GATE DRIVER)
8 kHz	0.075 A	24 V	1.8 W	0.6 W
16 kHz	0.127 A	24 V	3.048 W	1.016 W

The power lost to drive the gate of the IGBT, that is the switching operation loss, can be calculated as follows:

$$P_{GSW} = Qg \times Vg \times f_{SW} \quad (11)$$

To compare the switching operation loss with the quiescent power loss, P_{GSW} is calculated for two different frequencies- (8 kHz and 16 kHz) and is summarized in 表 10:

表 10. Power Lost to Gate During Switching

FREQ SWITCHING (f_{SW})	Q_g	V_g	P_{GSW}
8 kHz	2000 nC	24 V	0.348 W
16 kHz	2000 nc	24 V	0.768 W

3.2.4.3 Propagation Delay

図 36 shows the propagation delays measured for the three low-side gate drivers at rising and falling edges for the UCC5390ECD.表 11 lists the propagation delays of the bottom gate drivers.

表 11. Propagation Delay of Bottom Three Gate Drivers (UCC5390ECD)

PARAMETER	U2	U4	U6
Rising edge (turnon)	80 ns	80 ns	100 ns
Falling edge (turnoff)	72 ns	90 ns	80 ns

Also note that the maximum skew between the propagation delay is 20 ns.

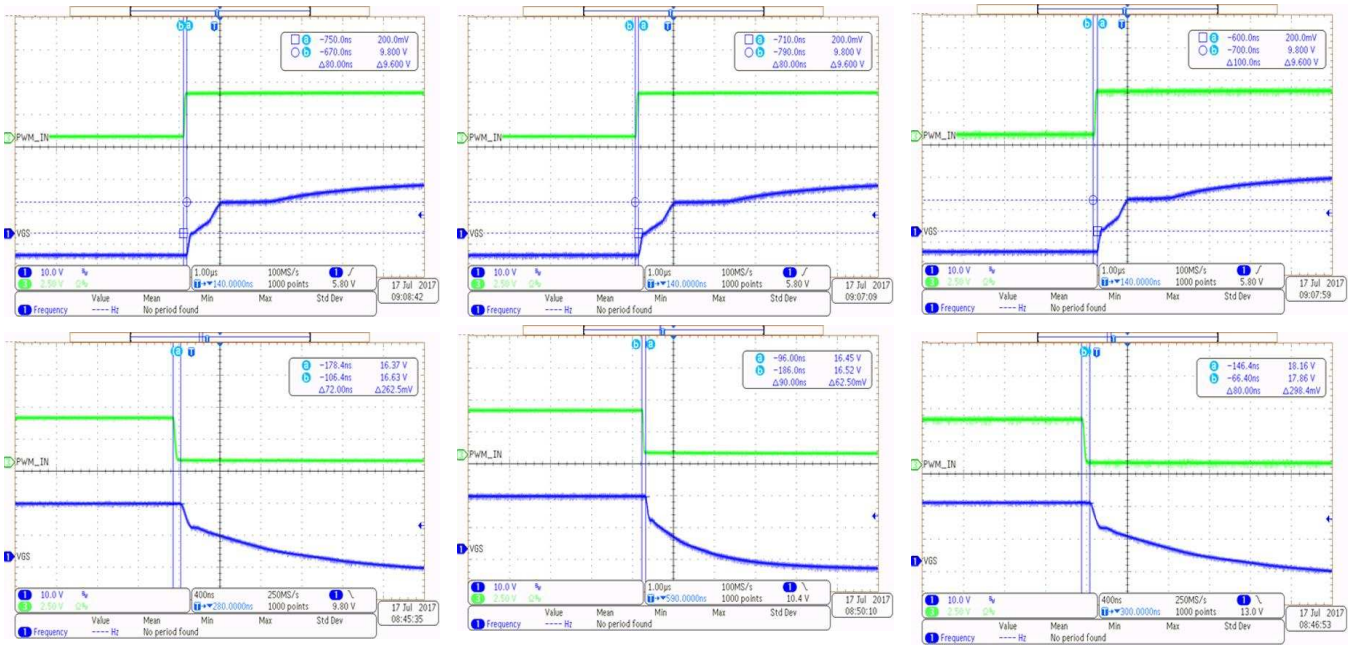

図 36. Propagation Delay of Bottom Gate Drivers (UCC5350ECD)

3.2.4.4 Source-Sink Currents

As in 3.2.3.3, the IGBT module is replaced with an external capacitor of 56 nF and source and sink currents are measured. The value of external gate resistor used for making these measurements is 0.75 Ω. 図 37 shows the sourcing and sinking capability of gate drivers when the external capacitor is used.

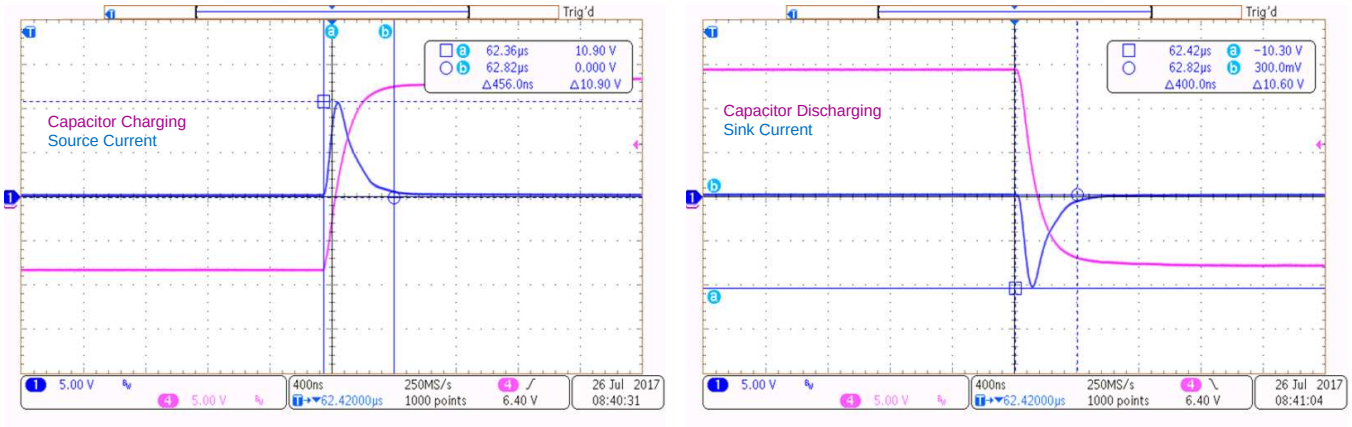

図 37. Source and Sink Currents of UCC5350ECD With 56-nF Capacitor

$$\text{Source Current} = \frac{\text{Voltage drop across external resistor during IGBT turnon}}{\text{Value of external resistor}} = \frac{10.9\ \text{V}}{0.75\ \Omega} = 14.53\ \text{A} \quad (12)$$

$$\text{Sink Current} = \frac{\text{Voltage drop across external resistor during IGBT turnoff}}{\text{Value of external resistor}} = \frac{10.6\ \text{V}}{0.75\ \Omega} = 14.13\ \text{A} \quad (13)$$

3.2.4.5 Turnon and Turnoff Times of IGBT

表 12 shows the theoretical values of turnon and turnoff times.

表 12. Theoretical Values of Turnon and Turnoff Times at 565-V Bus Voltage

PARAMETER	UCC5350ECD (250 V)	UCC5350ECD (565 V)
R_external	0 Ω	0 Ω
R_internal_igbt	3.8 Ω	3.8 Ω
R_on_driver	0.714 Ω	0.714 Ω
R_off_driver	0.13 Ω	0.13 Ω
IGBT module used	6MI180VB-120-50	6MI180VB-120-50
CISS of IGBT	29 nF	29 nF
CRSS of IGBT	0.8 nF	0.8 nF
Supply voltage, VCC2	15V/-8V	15 V/–8 V
Turnon current (Ig1+Ig2_on)	4.18 A	4.18 A
Turnoff current (Ig2_off)	3.51 A	3.51 A
Turnon time (t1+t2_on)	95 ns	95 ns
Turnoff time (t2_off)	50.8 ns	128 ns

図 38 and 図 39 shows the experimental values of the corresponding calculated results for the UCC5350MCD. The experiment is carried out for two different sets of DC Bus voltages: 250 V and 565 V.

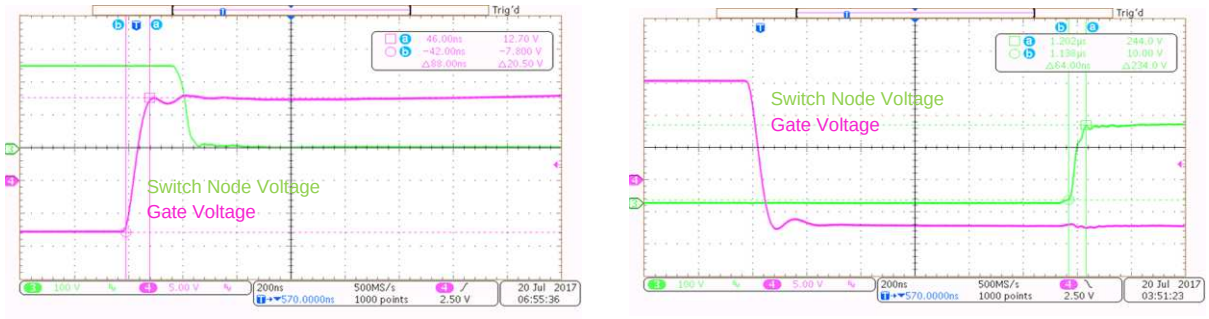

図 38. Turnon and Turnoff Times of IGBT at 250-V Bus Voltage Using IGBT 6MI180VB-120-50 With UCC5390ECD

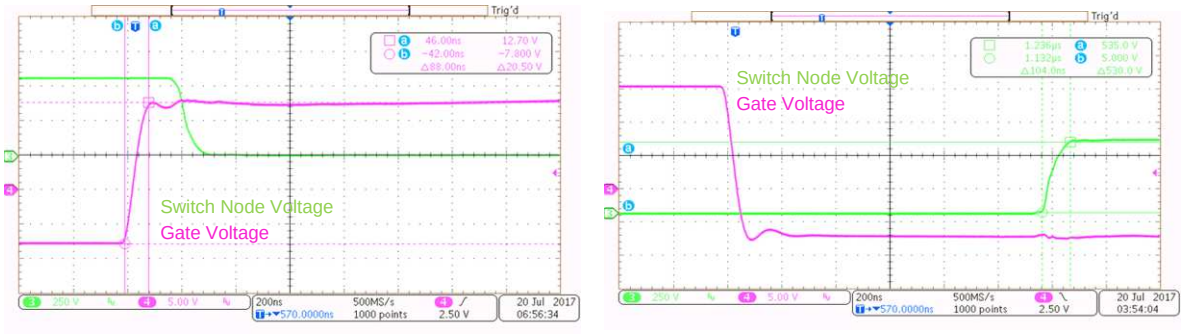

図 39. Turnon and Turnoff Times of IGBT at 565-V Bus Voltage Using IGBT 6MI180VB-120-50 With UCC5390ECD

表 13 summarizes the experimental results as follows:

表 13. Experimental Values of Turnon and Turnoff Times of IGBTs

PARAMETER	UCC5390ECD (250 V)	UCC5390ECD (565 V)
IGBT used	6MI180VB-120-50	6MI180VB-120-50
Turnon time (t1+t2_on)	88 ns	88 ns
Turnoff time (t2_off)	64 ns	104 ns

3.2.4.6 Thermal Image of Board

図 40 shows the thermal image of the boards, UCC5390ECD, and the corresponding minimum, maximum, and average temperatures. The ambient temperature while making these measurements is 25°C.

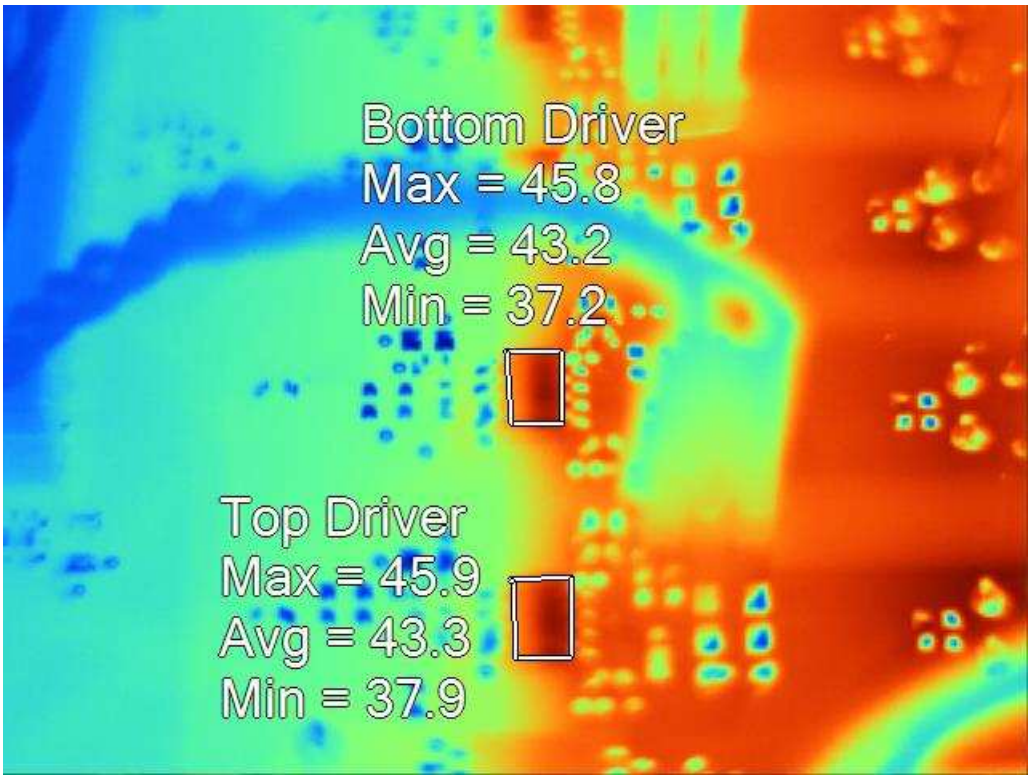

図 40. Thermal Image of Board With Gate Driver UCC5390ECD

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01420 .

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01420.

4.3 PCB Layout Recommendations

図 41 shows the isolation barrier and ground split. The hot-side (high-voltage power side) and the cold-side (low-voltage controller side) copper tracks are separated from each other by a basic isolation barrier. The narrow body package of the gate driver is placed across the isolation barrier. A copper-to-copper creepage spacing of 4 mm is maintained between the hot and cold sides. The low-side gate driver grounds and DC bus negative are common. To avoid noise due to switching currents in the DC bus negative from interfering with the gate driver operation, a split is done in the ground plane and they are connected together at a single point as shown in 図 41.

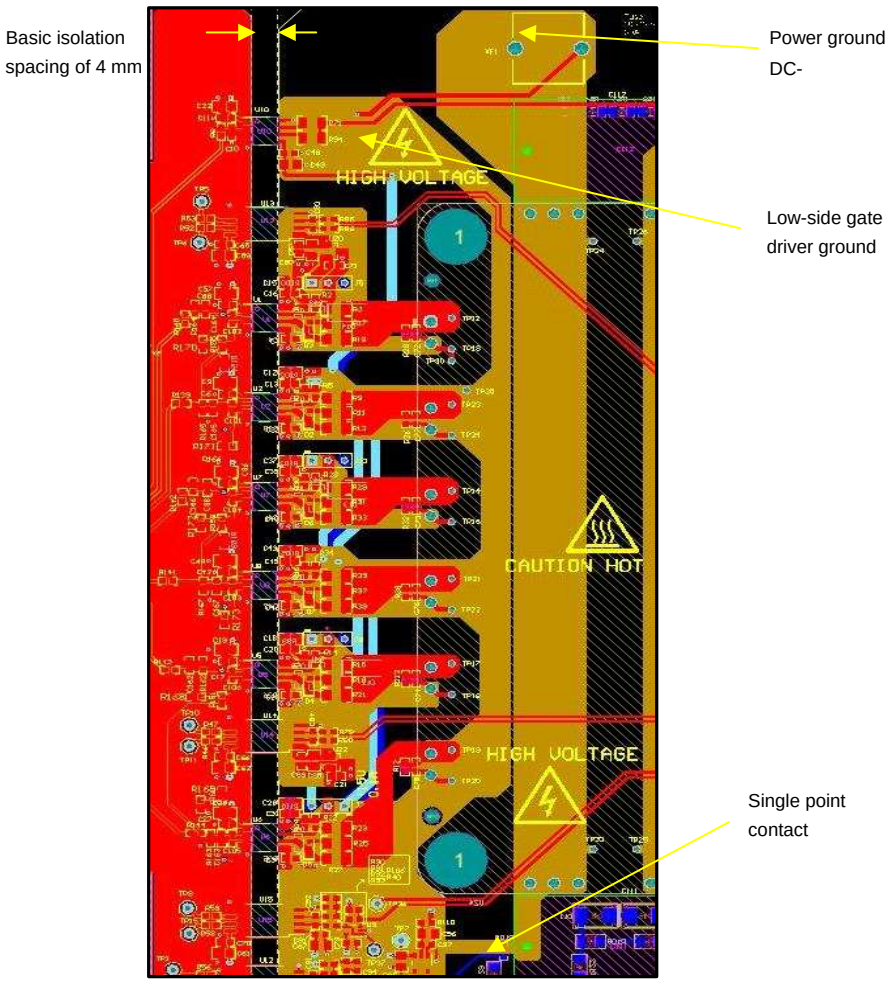

図 41. Basic Isolation Barrier and Ground Split Layout

The shunt resistance of 4 mΩ is in the same range as that of the stray parasitic trace resistances. For accurate shunt-based current sensing, it is important to sense the exact voltage across the shunt resistor only and avoid measuring the drop across the trace and contact parasitic resistance. This is done by implementing a Kelvin connection as shown in図 42. Differential routing is done from the shunt resistor to the ΔΣ modulator. Any noise is common to both the traces and gets cancelled off in the differential input stage of the modulator.

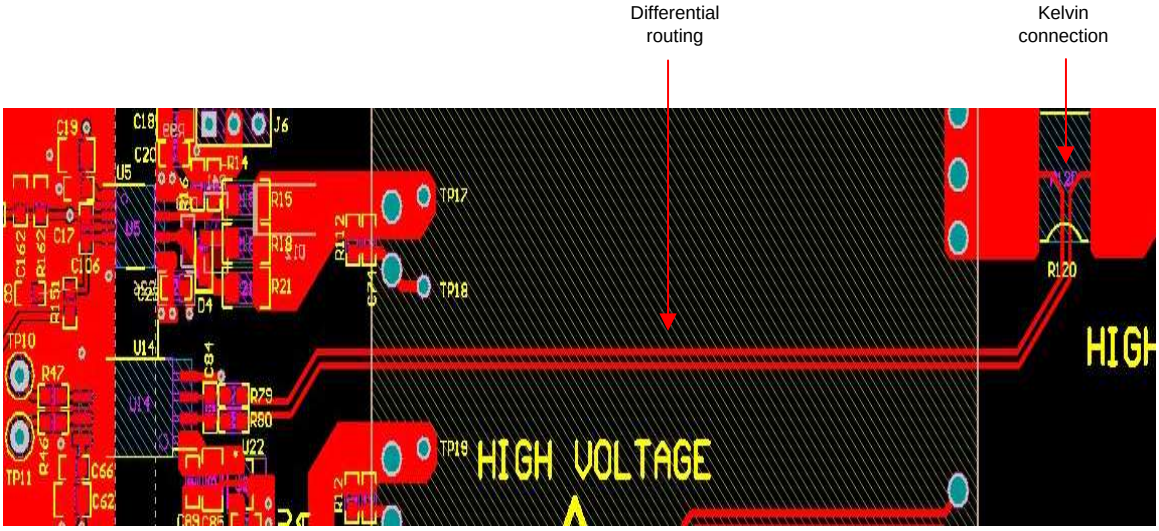

図 42. Shunt Resistor Connection to ΔΣ Modulator Layout

As shown in 図 43, the primary- and secondary-side noise-decoupling capacitors must be connected close to the device between the VCC1 and GND1 pins and between the VCC2 and VEE2 pins to bypass noise and to support high peak currents when turning on the IGBT. It is essential to limit the high peak currents that charge and discharge the IGBT gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the IGBTs. The gate driver must be placed as close as possible to the IGBTs. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device.

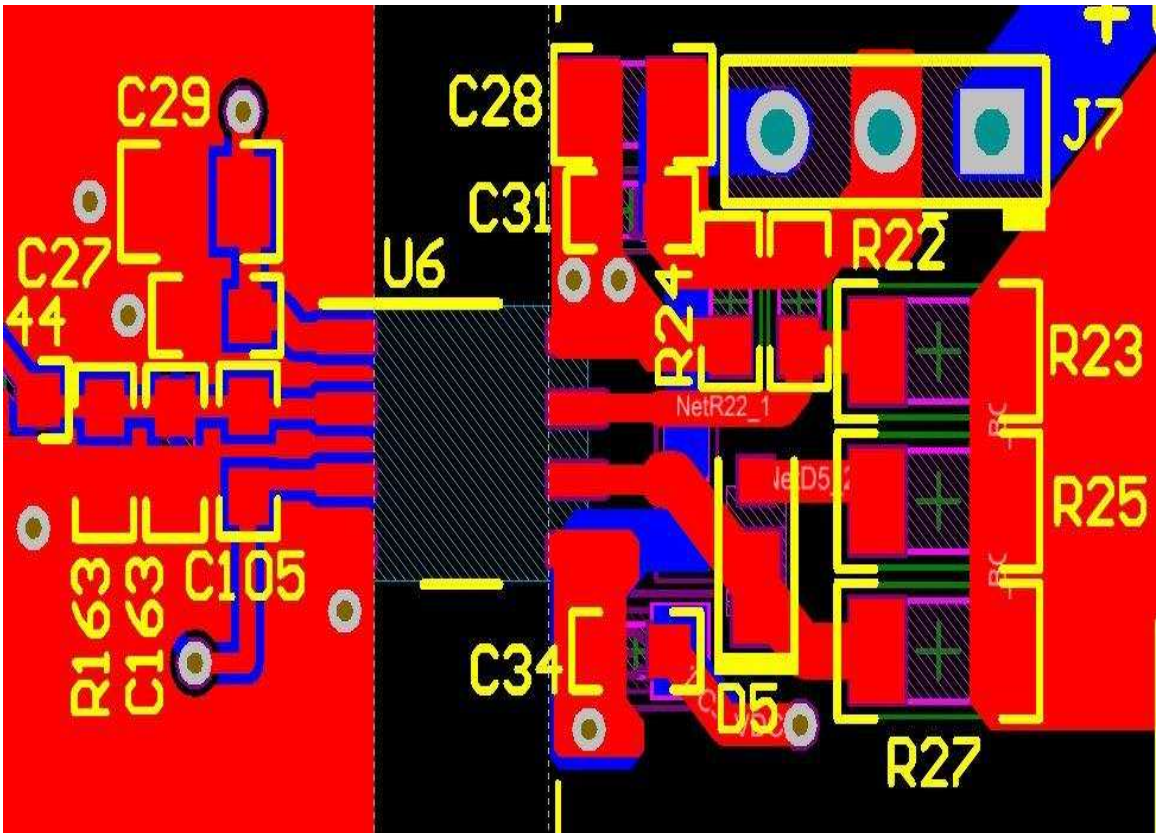

図 43. Low-Side Gate Driver Layout

図 44 shows the DC bus voltage sense circuit. The high-impedance resistor divider network is connected across the pins of the high-voltage DC-link film capacitor C111. The attenuated voltage is sensed by ΔΣ modulator U12. It is important to sense the voltage across the film capacitor for low-noise measurement.

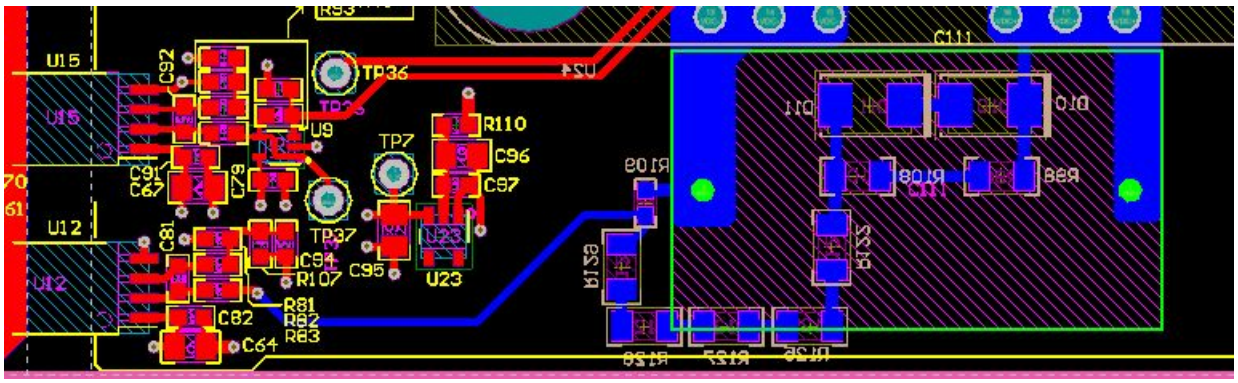

図 44. Connection of DC Bus Voltage Sensing

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01420.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01420.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01420.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01420.

5 Related Documentation

1. Texas Instruments, *Reinforced Isolated Phase Current Sense Reference Design With Small Delta-Sigma Modulators*, TIDA-00914 Design Guide (TIDUD07)
2. Texas Instruments, *Isolated Current Shunt and Voltage Measurement Kit*, TIDA-00171 Design Guide (TIDU499)
3. Texas Instruments, *Isolated Current Shunt and Voltage Measurement for Motor Drives Using AM437x*, TIDA-00209 Design Guide (TIDU755)
4. Texas Instruments, *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x*, Application Report (SPRABQ4)
5. Texas Instruments, *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters*, TIDA-00199 Design Guide (TIDU670)
6. Texas Instruments, *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection*, TIDA-00366 Design Guide (TIDUBX1)

5.1 商標

6 Terminology

IGBT— Insulated gate bipolar transistor

VFD— Variable frequency drive

PWM— Pulse width modulation

UVLO— Undervoltage lockout

DNP— Do not populate

7 About the Authors

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7.1 Recognition

The authors would like to recognize the excellent contributions from **PAWAN NAYAK** and **NELSON ALEXANDER** during the design, test, and documentation phases of the TIDA-01420 reference design.

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