参考資料

TI Designs: TIDA-01054
高性能DAQシステム内のEMIの影響を除去するマルチレール電源のリファレンス・デザイン

概要

このリファレンス・デザインは、LM53635-Q1降圧コンバータを使用し、16ビットを超えるデータ・アクイジション(DAQ)システムでEMIの影響による性能劣化を防ぎます。降圧コンバータにより、設計者は電源ソリューションを不要なノイズ劣化なしに、信号パスと近い場所に配置でき、基板面積を削減できます。このデザインでは、20ビット、1MSPSのSAR ADCを使用し、システムのSNR性能として100.13dBを実現しています。これは、外部の電源を使用した場合のSNR性能である100.14dBとほぼ同等の値です。

リソース

TIDA-01054	デザイン・フォルダ
LM53635-Q1	プロダクト・フォルダ
LM5574、LM46001、TPS7A3001	プロダクト・フォルダ
TPS7A47、LM7705	プロダクト・フォルダ
SN74AHC1G04、SN74AUP1G80	プロダクト・フォルダ
LMK61E2、LMK00804B	プロダクト・フォルダ
OPA827、OPA625、THS4551	プロダクト・フォルダ
REF6041	プロダクト・フォルダ

TI E2E™ Community

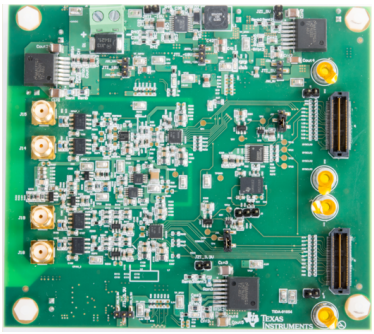
E2E™エキスパートに質問

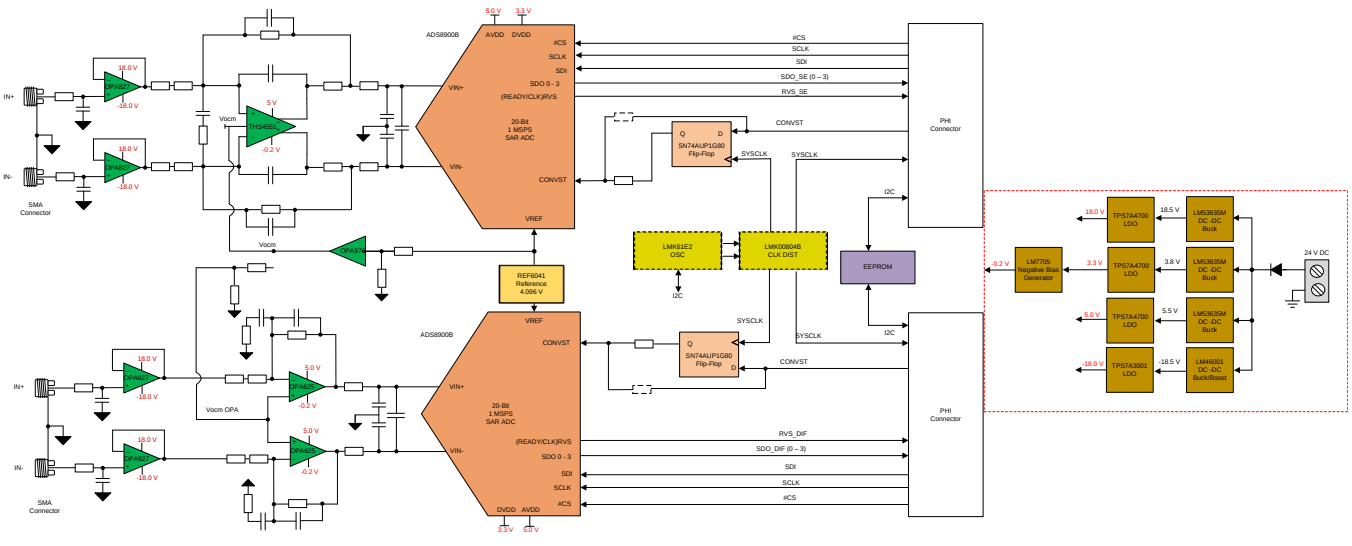
特長

- DC/DCのEMIがシステム性能に及ぼす影響を最小化する電源設計
- 2つの20ビットSAR ADCチャネル
- モジュール形式のフロントエンド・リファレンス・デザインによる、チャネル数が多く、リピート可能なシステム
- 最大±4Vの入力信号($8V_{PP}$差動)

アプリケーション

- データ収集(DAQ)
- 半導体試験用機器
- LCD試験用機器
- ラボ計測機器
- バッテリ試験装置





1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present many design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for applications such as semiconductor test, memory test, LCD test, and battery test. In these systems, sometimes hundreds or even thousands of data channels are required and thus maximizing SNR performance while minimizing power, component count, and cost are all key design criteria. These systems have some type of power generator that typically includes DC-to-DC converters to provide the voltage levels needed to power each device in the analog front end (AFE). These converters have switching components that cause electromagnetic interference (EMI) emission and harm the system performance.

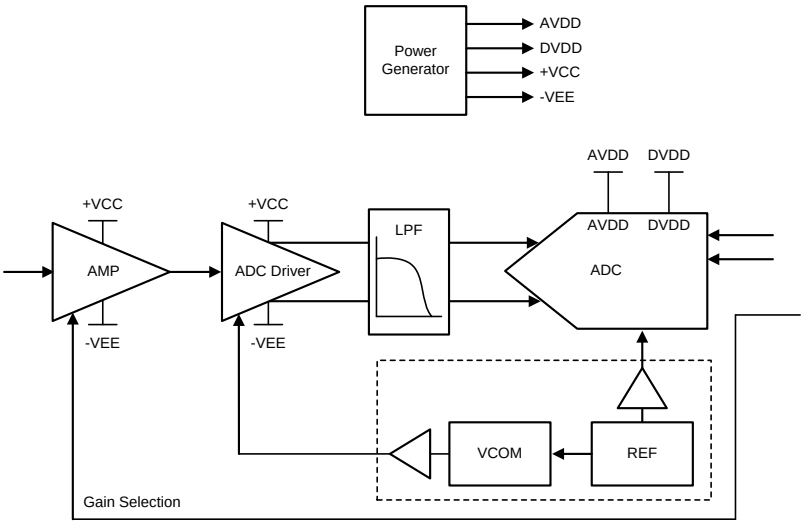


図 1. Generic AFE

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	8-V_{PP} fully differential	8-V_{PP} fully differential
Resolution	20 bits	20 bits
SNR	> 96 dB	100.13 dB
THD	< –120 dB	–123.06 dB
ENOB	> 16 bit	16.32 bits
System power	< 2.5 W	1.92 W
Form factor (L × W)	120 × 100 mm	112.98 × 99.82 mm

2 System Overview

2.1 Block Diagram

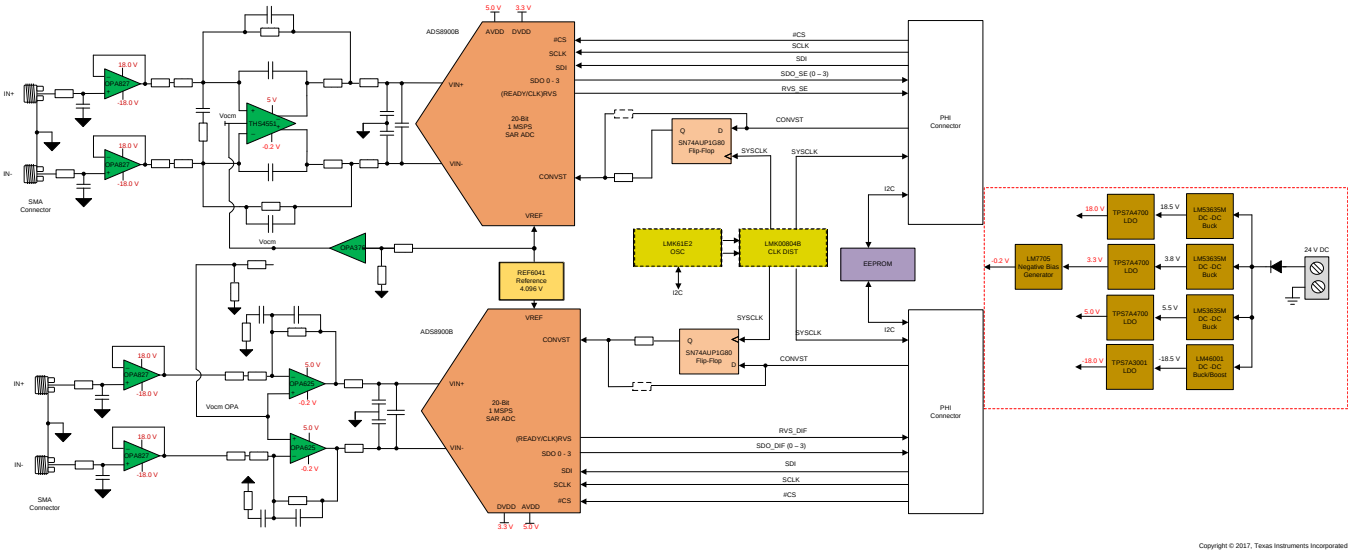


図 2. System Block Diagram

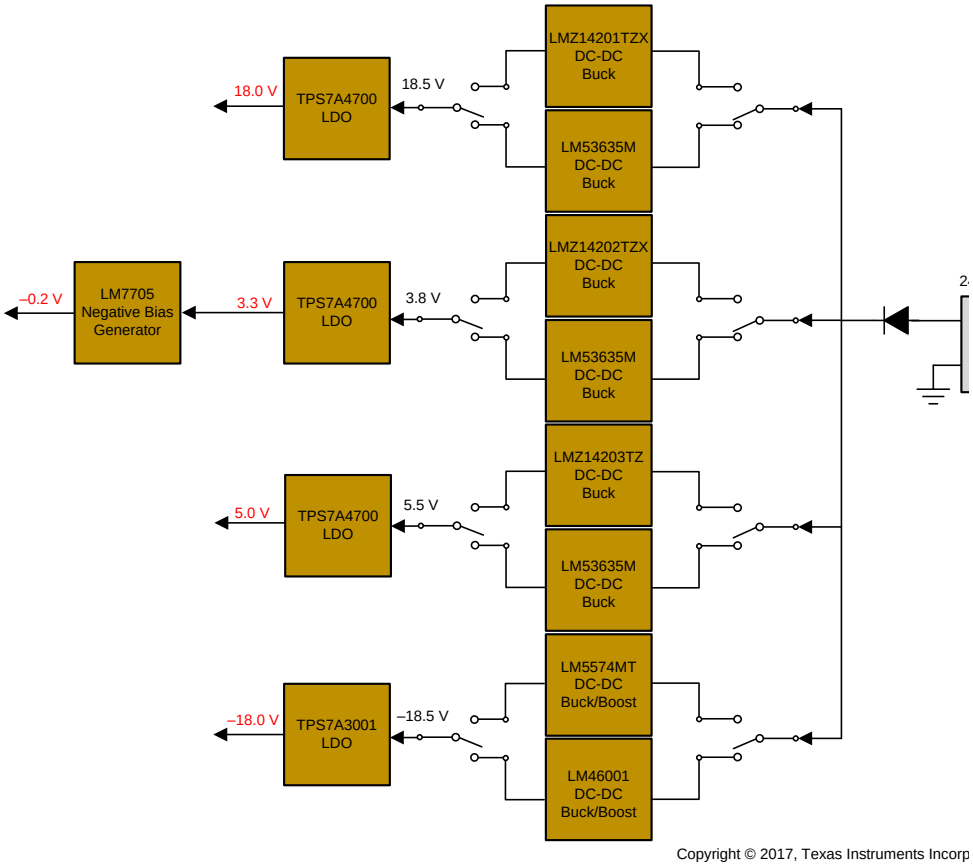


図 3. Power Rail Circuitry

This reference design focuses on reducing the EMI generated from the system's buck converters powering the AFE and successive approximation register (SAR) analog-to-digital converter (ADC). This design has two families of buck converters to show the effects of the EMI and solve the issue. 図 3 shows how the buck converters can be switched and used in different combinations. The –18-V rail has two different buck converters with the LM5574 included for testing purposes only and has no emphasis on the main goal of this reference design: eliminating EMI.

2.2 Highlighted Products

2.2.1 LM53635-Q1

The LM53635M is used in this design to bring the 24-V input voltage down to 3.8 V, 5.5 V, and 18.5 V in a highly efficient manner. This part is selected based on its excellent EMI performance and compact PCB layout. The automotive-qualified HotRod™ QFN package reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering EMI. Seamless transition between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) modes and low quiescent current (only 15 µA for the 3.3-V option) ensures high efficiency and superior transient responses at all loads.

2.3 System Design Theory

High-performance DAQ systems use high-precision ADC to get the most accurate and precise measurements. These high-resolution ADCs have low-noise floors, which make them more susceptible to the EMI being emitted by DC-to-DC converters. This EMI harms the system performance with spurs that show up throughout the frequency spectrum.

The following sections detail the design challenges for reducing the EMI effects on the SAR ADC performance, including theory, calculations, simulations, PCB layout design, and measurement results. The measurement results outline the difference between the low-EMI LM53635-Q1 buck converter and the easy-to-use LMZ1420x.

2.3.1 AFE and SAR ADC

This reference design consists of an AFE with two channels. Both channels are similar with the exception of the ADC driver architecture. The first channel uses the THS4551, a fully differential amplifier specifically designed to be used with high-performance SAR ADCs. The second channel uses dual OPA625 amplifiers wired to work as a fully differential amplifier. These amplifiers are driving the ADS8900B SAR ADC, a 20-bit high-precision and high-speed data converter. The AFE and SAR ADC are key aspects of this design aimed at DAQ systems; however, these devices are not the main focus of this design. To learn more about the design theory of the AFE and SAR ADC, see the TIDA-01052 reference design.

2.3.2 Power Structure

This system requires a wide variety of voltage rails to meet the specification of the reference design. The input voltage required for the system is 24-V DC. The power tree in 図 4 highlights the distribution of the power into the different required rails. To create these rails, this design contains the LM53635-Q1 low-EMI buck converter and the LMZ1420x buck converter. These solutions are compared to show the improvement the low-EMI converter has over the popular, easy-to-use LMZ1420x. Using two-pin and three-pin headers allow the user to customize easily which solution to use. See 表 2 for details on using the jumpers. The data gathered for each combination can be found in 3.2.

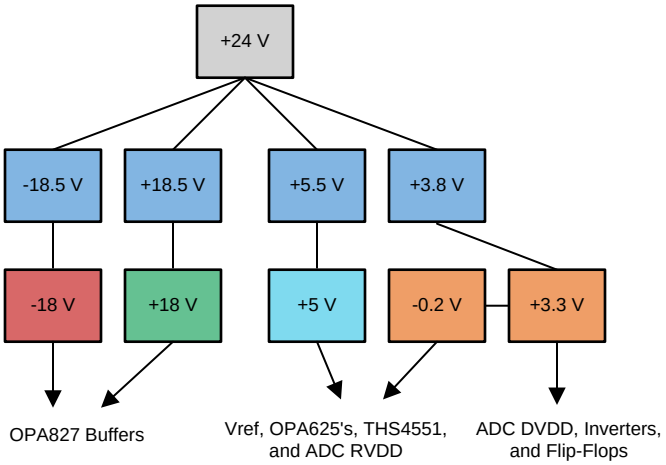


図 4. System Power Tree

2.3.2.1 LM53635-Q1 and LMZ1420x Circuitry

図 5 displays the 18-V rail circuitry with the LM53635-Q1, but each rail is structured the same way with the only difference coming from different passive component values. The input of the buck is connected to the 24-V supply by a two-pin header. This header allows the user to leave unused bucks powered off, which is critical to the testing performed on the reference design. The buck converter is followed by an LDO to remove the switching noise. The input of the LDO is connected to a three-pin header. The other two pins of this header are connected to the outputs of both buck converter options. This header is used in conjunction with the two-pin header to properly connect the buck intended to be used with the LDO. Not only does the three-pin header allow for only one LDO to be used for each rail improving space efficiency, but it also helps with certain aspects of testing and debugging. To get a better visual of the functionality the headers provide, see 図 3.

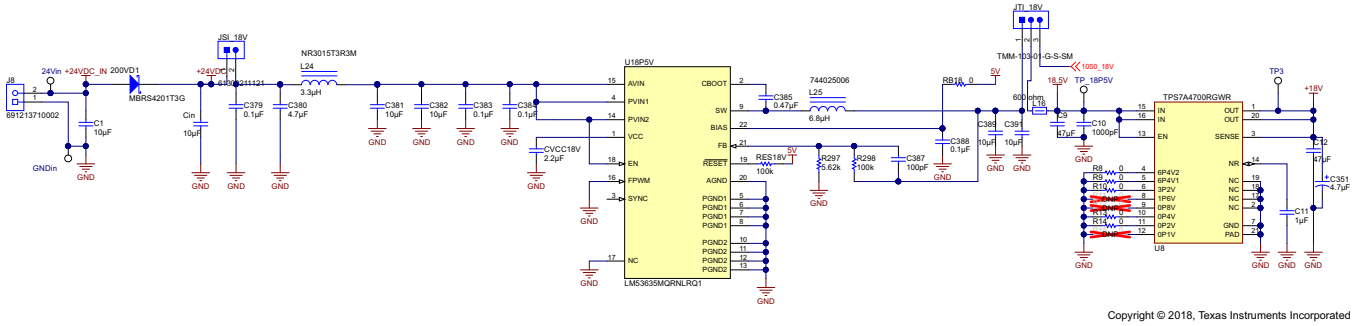


図 5. LM53635-Q1 Schematic

図 6 displays the LMZ1420x circuitry for the 18-V rail. Again, the structure is the same for each rail. The output goes into an off-page connecter, which is connected to the three-pin header discussed previously. The LMZ1420x buck converters are modules, so they do not require a lot of additional passive components. See 4.1 for the schematic downloads to view all of the power circuitry.

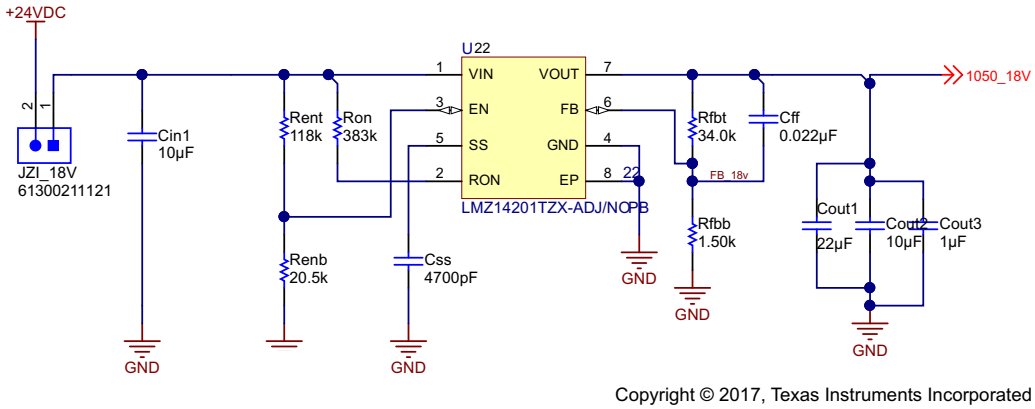


図 6. LMZ1420x Schematic

2.3.3 LM53635-Q1 Switching Noise

Buck converters switching components produce output voltage ripple, which is referred to as switching noise. The amplitude of this ripple is determined by many different factors involved with the switching regulator and can be high enough to cause issues with devices being powered by that buck converter. When it comes to noise sensitive devices like the 20-bit ADC used in this reference design, a high-voltage ripple can have a very detrimental effect on signal integrity. To circumvent this, an LDO is placed at the output of the switching regulator to remove the switching noise.

The following calculations and simulations illustrate the importance of having the LDO remove the switching frequency. The output voltage ripple for the buck in the 5-V rail (the rail powering the RVDD of the ADC) is calculated to be roughly 30 mV using 式 1:

$$\Delta V = \frac{I_L \times (\Delta I - I_L)^2}{C \times f_S \times \Delta I^2} \quad (1)$$

式 1 is used for bucks in discontinuous conduction mode (DCM). The LM53635-Q1 switches from continuous conduction mode (CCM) to DCM when the load current is lower than the 148-mA threshold. The load current (I_L) is measured to be 22 mA, which is why the 式 1 is used. Because the buck is configured to be in auto mode in this design, the buck switches to PFM from PWM for light load conditions. This switch means that the buck adjusts its switching frequency to regulate the output. Therefore, the switching frequency is much lower than the typical 2.1 MHz found in the LM53635-Q1 datasheet. The switching frequency (f_S) is measured to be 15.708 kHz. The buck is designed to output 5.5 V just above the dropout of the LDO to minimize the efficiency loss. A TINA-TI™ simulation model is created for the TPS7A4700 LDO with a step input of 5.5 V and a sine wave input of 30 mVpk-pk (simulating the output of the buck with ripple). A steady-state analysis gave the output of the LDO, which is displayed in 図 7.

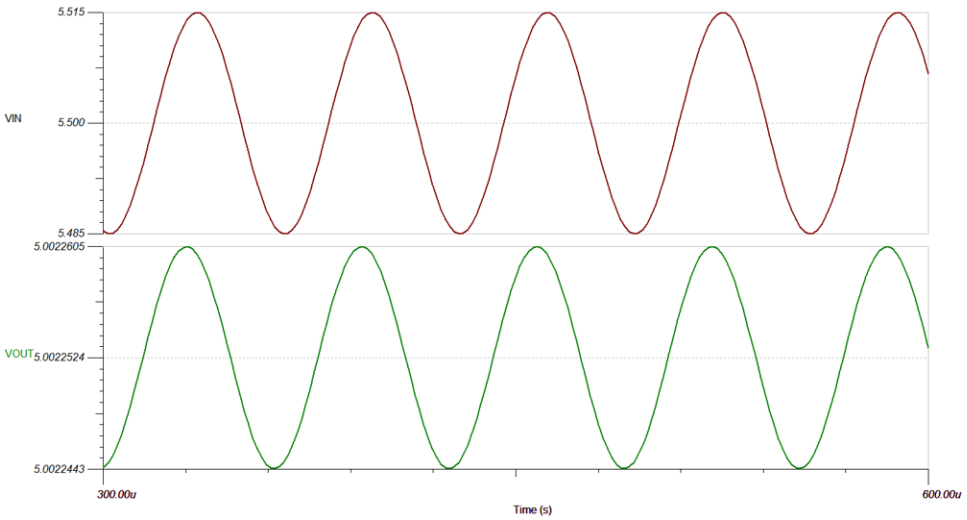


図 7. TPS7A47 LDO Simulation for 5-V Rail

After the LDO, the peak-to-peak amplitude of the switching noise is 16.2 µV. The LDO effectively reduced the switching ripple noise by a factor of 1850. Further calculations are made to see the noise present at the ADC using the output voltage ripple of the LM53635-Q1. This result is compared to the result of using the output voltage ripple of the TPS7A4700 in the same calculations. This ripple voltage without the LDO goes to both the OPA625 and the THS4551. The THS4551 has a PSRR of 110 dB at 15.708 kHz and a gain of 1. PSRR is equal to:

$$\mathrm{PSSR(dB)} = -20\log_{10}\left(\frac{\Delta V_{OS}}{\Delta V_{SUPPLY}}\right) \quad (2)$$

Because this system has a gain of 1, the total noise gain on the non-inverting terminal is 1 + 1. This is a gain of 6 dB. The total PSRR for the THS4551 is approximately 104 dB for this system. This value is equal to 0.00000631 V/V. The amount of power supply noise coupled to the ADC data lines is calculated using 式 3:

$$30\ \mathrm{mV} \times 0.00000631 = 189.3\ \mathrm{nV} \quad (3)$$

This noise value is then compared to the LSB value of the ADC to observe the effect it has on signal integrity. The value of 1 LSB for a differential input, 20-bit ADC with 4.096 V as a reference voltage is found using 式 4 and 式 5:

$$\frac{2 \times 4.096}{2^{20}} = 7.812\ \mu\mathrm{V} \quad (4)$$

$$\frac{189.3\ \mathrm{nV}}{7.812\ \mu\mathrm{V}} \times 100 = 2.42\%\ \mathrm{LSB} \quad (5)$$

The OPA625 has a power supply rejection ratio of 86 dB at 15.708 kHz. At a gain of 1, the PSRR is equal to 80 dB. This value is equivalent to 0.0001 V/V. The power supply noise present at the ADC driven by the OPA625 is:

$$30\ \mathrm{mV} \times 0.0001 = 3\ \mu\mathrm{V} \quad (6)$$

$$\frac{3\ \mu\mathrm{V}}{7.812\ \mu\mathrm{V}} \times 100 = 38.4\%\ \mathrm{LSB} \quad (7)$$

With 2.42% LSB present at the ADC, the THS4551 signal chain is not greatly impacted by excluding the LDO. However, the OPA625 signal chain has a little less than 50% LSB of power supply noise present at the ADC without the LDO. Thus, it can have a negative impact on the output data of the ADC. Using the LDO's output ripple of 16.2 µV and the same equations, the amount of power supply noise coupled to the ADC data lines for the ADC driven by the THS4551 is:

$$16.2\ \mu V \times 0.00000631 = 102.2\ pV \quad (8)$$

$$\frac{102.2\ pV}{7.812\ \mu V} \times 100 = 0.0013\%\ LSB \quad (9)$$

This highlights that the amount of noise on the 5-V rail is much less than 1% of the LSB value of the ADC. The amount of power supply noise present at the ADC of the OPA625 is:

$$16.2\ \mu V \times 0.0001 = 1.62\ nV \quad (10)$$

$$\frac{1.62\ nV}{7.812\ \mu V} \times 100 = 0.021\%\ LSB \quad (11)$$

When using the LDO, both the THS4551 and OPA625 signal chain ADCs have much less than 1% LSB of noise present at their power supply inputs. This guarantees that there is no negative impact on signal integrity with the LDO present in the system. This concludes that the LDO is necessary in the power rail circuits to overall remove any system performance degradation due to switching noise.

2.3.4 LM53635-Q1 EMI

One of the goals for this design is to eliminate any system performance degradation due to EMI for high-performance DAQ systems. Because buck converters have harsh switching components, they are the main culprit in producing unwanted spurs throughout the spectrum. The LM53635-Q1 is a great solution for this problem with its many features focused on reducing EMI.

2.3.4.1 HotRod Packaging

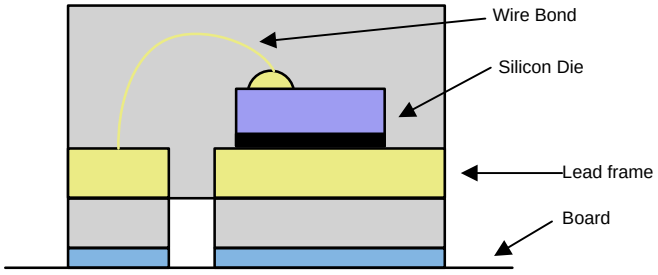


図 8. Standard Wire Bond QFN

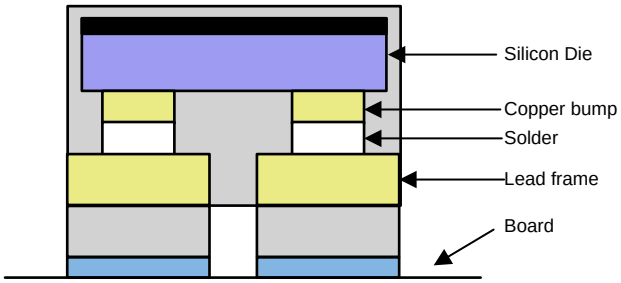


図 9. HotRod FCOL QFN

The biggest factor that helps the LM53635-Q1 reduce EMI is the HotRod FCOL packaging illustrated in 図 9. This package style flips the die over and uses copper bumps to connect directly to the leads, removing the need for a wire bond seen in 図 8. By removing this wire bond, the parasitics are reduced, which dramatically lowers the switch node ringing. This ringing is a major source of EMI for buck converters using the standard wire bond packaging.

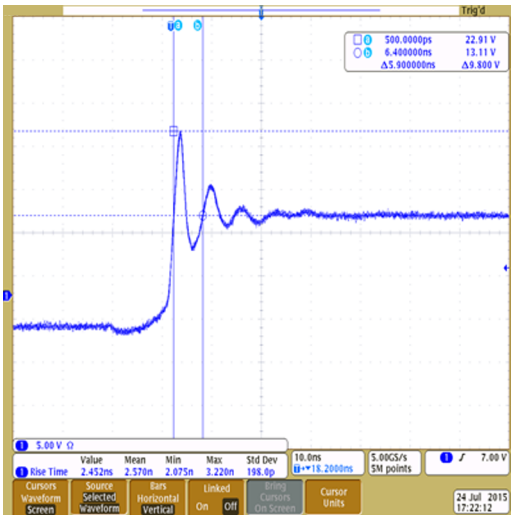


図 10. LM53603 TSSOP

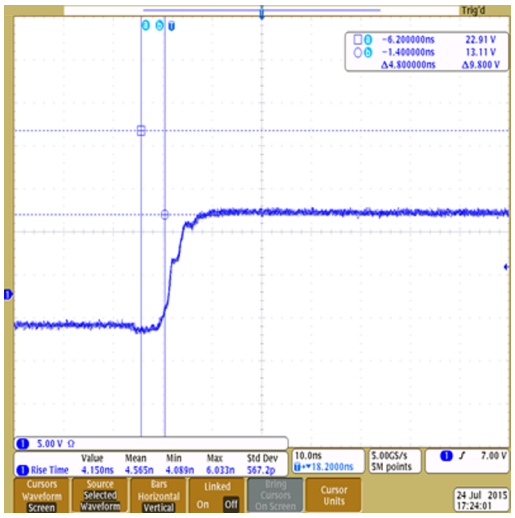


図 11. LM53635-Q1 FCOL

The difference between switch node ringing for a wire bond package and a HotRod package is illustrated in 図 10 and 図 11. The ringing overshoot is reduced from 9 V to 0 V, lowering the overall EMI and noise. Not only does the HotRod packaging help reduce EMI, but it also allows for a smaller size and reduced R_{DS_ON}, improving efficiency.

2.3.4.2 Spread Spectrum

The LM53635-Q1 has an option with spread spectrum capabilities, which is used in this reference design. Spread spectrum is a means of reducing EMI by dithering the switching regulator frequency. This causes the noise power to spread over a wider frequency band and reduces the fundamental energy. Most systems containing the LM53635-Q1 device can easily filter low-frequency conducted emissions from the first few harmonics of the switching frequency. A more difficult design criterion is reducing emissions at higher harmonics, which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LM53635-Q1 device uses a ±3% spread of frequencies, which spreads energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency. Peak emissions at the switching frequency of the LM53635-Q1 are only reduced by slightly less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB, which can be seen in 図 12 and 図 13.

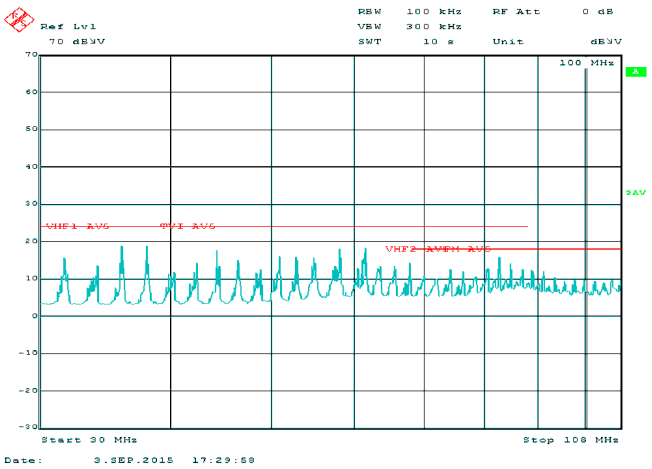


図 12. 30 to 108 MHz Without Spread Spectrum

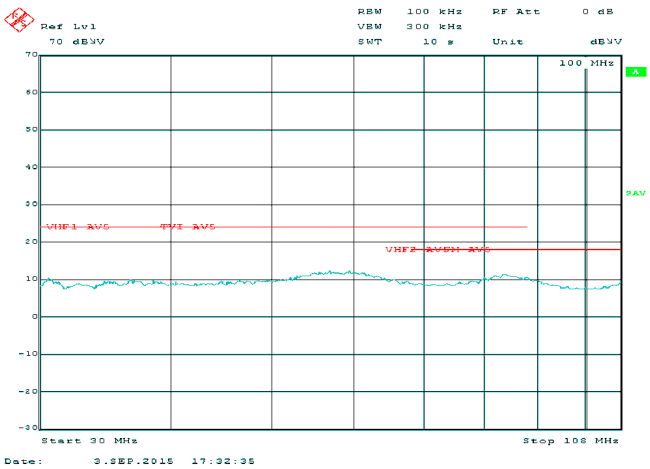


図 13. 30 to 108 MHz With Spread Spectrum

The LM53635-Q1 uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register. An intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats by approximately 8 Hz, which is below the audio band.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

The ensuing section outlines the information for getting the board up and running as fast as possible. To learn about the PHI board or the onboard clocking and jitter cleaner, see the TIDA-01050 reference design. Take care when moving jumper pins to avoid possible damage to the components.

3.1.1 Jumper Configuration

This system has several configurable power options. These options are selectable through using two-pin and three-pin jumpers. 表 2 highlights the purpose of each jumper and assists in changing the configuration to fit the needs of the user.

表 2. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
JSI_18V	Power to LM53635-Q1 18-V rail	—	Short
JTI_18V	Connects LM53635-Q1 to TPS7A700 for 18-V rail	Connects LMZ14201 to TPS7A700 for 18-V rail	Short pins 1 and 2
JSI_5V	Power to LM53635-Q1 5-V rail	—	Short
JTI_5V	Connects LM53635-Q1 to TPS7A700 for 5-V rail	Connects LMZ14203 to TPS7A700 for 5-V rail	Short pins 1 and 2
JSI_3.3V	Power to LM53635-Q1 3.3-V rail	—	Short
JTI_3.3V	Connects LM53635-Q1 to TPS7A700 for 3.3-V rail	Connects LMZ14202 to TPS7A700 for 3.3-V rail	Short pins 1 and 2
JPRI_–18V	Power to LM46001 –18-V rail	—	Short
JTI_–18V	Connects LM46001 to TPS7A3001 for –18-V rail	Connects LM5574 to TPS7A3001 for –18-V rail	Short pins 1 and 2
JMTI_–18V	Power to LM5574 –18-V rail	—	Open
JZI_18V	Power to LMZ14201 18-V rail	—	Open
JZI_3.3V	Power to LMZ14202 3.3-V rail	—	Open
JZI_5V	Power to LMZ14203 5-V rail	—	Open
J39	Connects –0.2-V rail to OPA 625 and THS4551	Shorts –0.2-V rail to ground	Short pins 1 and 2

3.2 Testing and Results

An Audio Precision 2700 series signal generator is used as the signal source to test the AFE and ADC performance. The noise and THD of the AP2700 have adequate performance and do not limit measurements or system performance. A generic DC power supply is used to generate the 24-V DC input voltage.

A PHI controller board is used to connect the TIDA-01054 board to the host PC, where the ADS8900B EVM GUI is being run. This software allows for measuring SNR, THD, SFDR, SINAD, and ENOB for the ADC by running a spectral analysis. The AP2700 is set to output a 2-kHz 8-Vpk-pk sinusoid. 2 kHz is chosen because it is the standard frequency when measuring noise and THD, and 8-Vpk-pk grants full range on the THS4551 or OPA625, thus granting full range of 0 to VREF for the ADC.

3.2.1 EMI Matters

This reference design focuses on how EMI generated by switching regulators affects the system performance of high-performance DAQs. To illustrate this, a test is run to demonstrate the effects of EMI using two TIDA-01054 boards: one connected to the PC and AP2700 and the other providing power. 図 14 displays the physical setup.

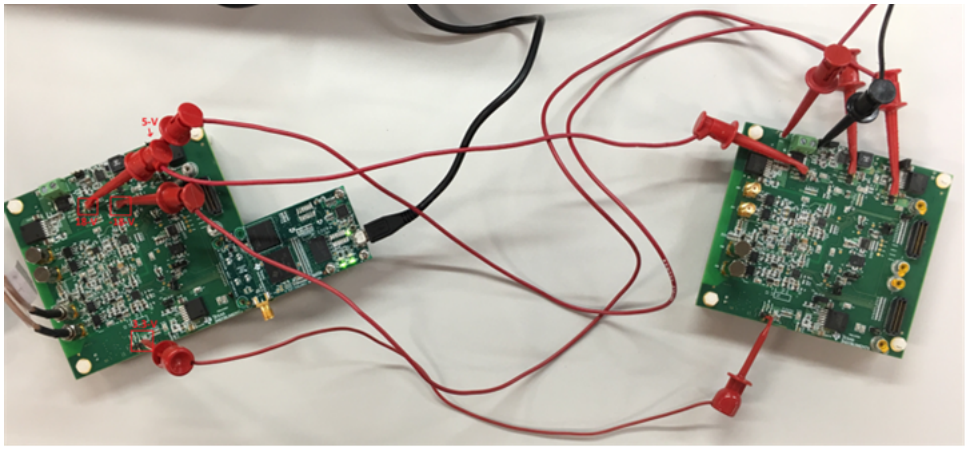


図 14. Physical Setup for EMI Testing

The board on the left of 図 14 is the board under test and on the right is the board providing power. The power board is set up to use all LMZ1420x and LM46001 buck converters because it is the theoretical worst case scenario. The outputs of these bucks are being connected to the inputs of the LDOs on the board under test. Thus, whenever an external source is referenced, it is coming from this board. 図 15 and 図 16 illustrate the performance difference between using the external power board and the onboard LMZ1420x and LM46001 buck converters.

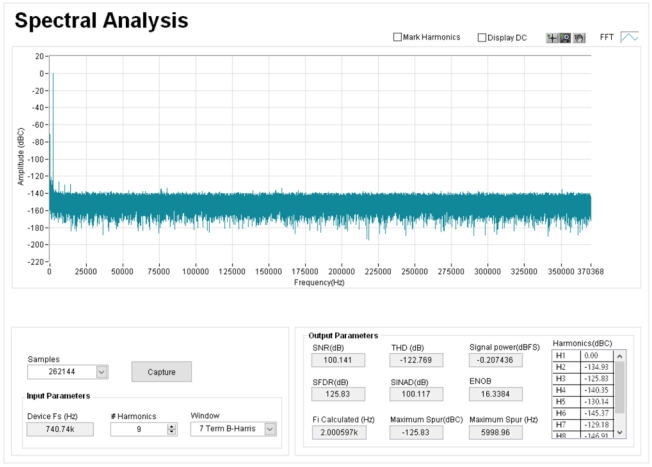


図 15. EMI Test With External Power

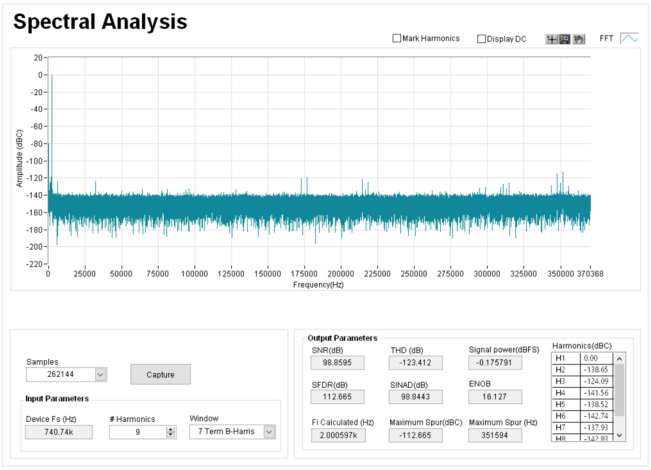


図 16. EMI Test With Onboard Power

The measured results are taken from the top channel of the design. It is very apparent looking at the spectrum plot that the system performance degrades when using onboard power. Spurs show up at multiple frequencies with some having an amplitude up to –112 dBC. These spurs are narrow so they do not affect the SNR as much as the SFDR, but both decrease considerably with the SFDR dropping roughly 13 dB. Because both boards are using the same buck converters, the conclusion can be made that EMI is the cause of the poor performance. With roughly one foot of space between the board under test and the power board, the radiated EMI from the switching components of the bucks are not introduced into the input signal.

3.2.2 Proximity and ΔV Factor in EMI Degradation

The proximity and ΔV of the buck converter are major factors in the EMI impact on system performance. However, these factors are mitigated with the LM53635-Q1. To prove this, the LM53635-Q1 outputting 3.8 V (making it the highest ΔV) is swapped with the LM53635-Q1 outputting 18.5 V to change the proximity to both channels. 図 17 and 図 19 are diagrams to simplify this process. With the highest ΔV buck placed close to the differential channel, the system performance is measured to observe the effects.

図 18 displays the spectrum results of the differential channel when the two bucks are in their original positions, referred to as position 1. Compared the results of position 2 in 図 20, the system performance stayed the same. With no degradation in system performance, the LM53635-Q1 effectively eliminates EMI and presents no concern with the proximity of this buck, even with high ΔV.

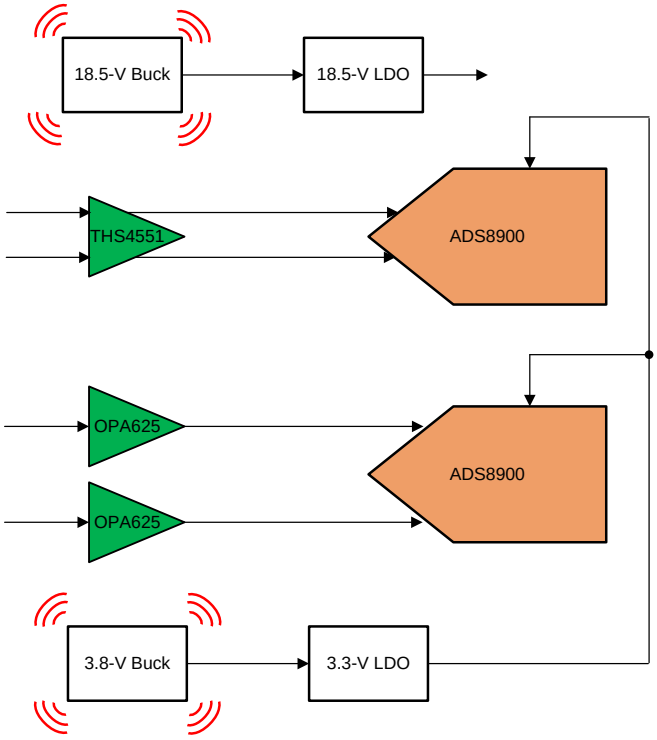


図 17. Position 1

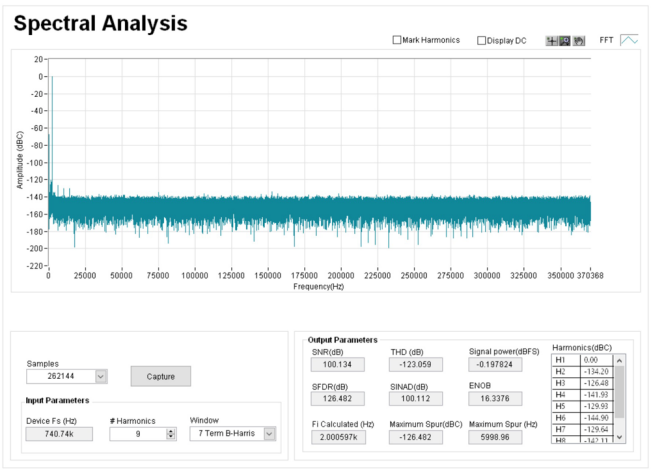


図 18. Spectrum Results for Position 1

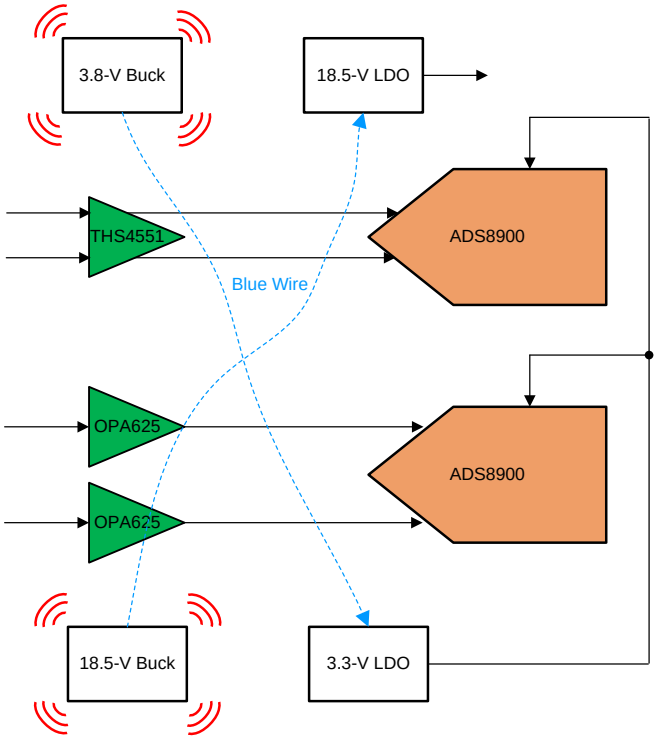


図 19. Position 2

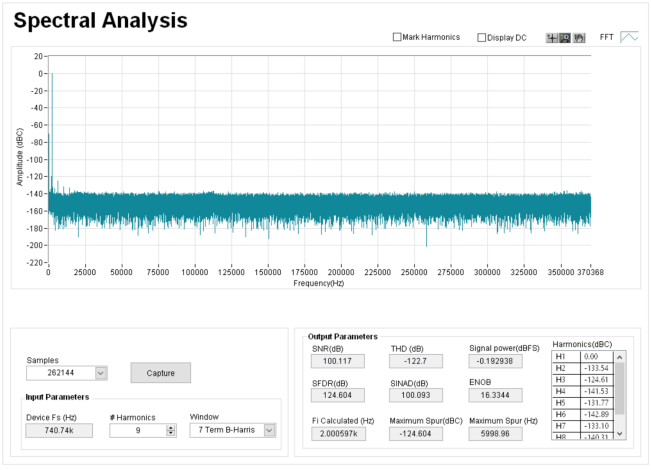


図 20. Spectrum Results for Position 2

3.2.3 Buck Converter and ADC Driver Comparison

This reference design contains two options for power and for driving the ADC. These options allow for a comparison of performance to see which option is better overall. It is expected that the THS4551 ampfilier, used in the differential channel, is a better ADC driver over the dual OPA625 amplifiers, used in the single-ended channel, because the system's bandwidth is limited to the frequency range, where its noise performance is superior. It is also expected that the LM53635-Q1 grants better performance over the LMZ1420x due to its emphasis on low EMI and HotRod packaging. To perform the tests, measurements are taken from each channel separately while also alternating the LM53635-Q1 and LMZ1420x buck converters to power the rails. The results are highlighted in 表 3.

表 3. Summary of Measured Results

3.8-V BUCK POSITION	VOLTAGE SOURCE	ADC CHANNEL	SNR (dB)	SINAD (dB)	THD (dB)	SFDR (dB)	ENOB (bits)
Position 1	LMZ1420x	Differential	98.86	98.84	–123.41	112.67	16.13
Position 1	LM53635-Q1	Differential	100.13	100.11	–123.06	126.48	16.34
Position 2	LM53635-Q1	Differential	100.12	100.09	–122.70	124.60	16.33
—	External	Differential	100.14	100.12	–122.77	126.55	16.34
Position 1	LM53635-Q1	Single-ended	98.57	98.56	–129.55	131.98	16.08
Position 2	LM53635-Q1	Single-ended	98.82	98.82	–129.10	131.61	16.12
—	External	Single-ended	99.45	99.45	–129.70	132.22	16.23

When comparing the differential channel (THS4551) and the dual single-ended channel (OPA625), external power sources are used to isolate performance specifically to the devices themselves. As expected, the THS4551 outperformed the OPA625 by almost 1 dB in SNR. With that, most of the results are taken from the differential channel to get the best overall performance with the buck converters. When using the LM53635-Q1 devices over the LMZ1420x, the SNR performance improved slightly over 1 dB. The SFDR improved by roughly 14 dB because the spurs caused by EMI are very narrow so they do not have a major impact on the total noise even though they have high amplitudes. The single-ended results are added in 表 3 to emphasize the better rejection to EMI noise the THS4551 has over the two OPA625 amplifiers. The column named "3.8-V Buck Position" refers to the testing done in 3.2.2.

All the tests performed help solidify that EMI, with impacting factors of ΔV and proximity, does matter in high-performance DAQ systems. The lower noise floor of a 20-bit SAR ADC makes the spurs caused by the switching components of the buck converters more prominent. With the LM53635-Q1 achieving low EMI, this issue is solved and the system performance degradation is greatly reduced, which is illustrated in 図 21 and 図 22. The LMZ1420x is a widely used buck converter because of its ease of use, but the LM53635-Q1 is a far superior option if the user wants to design a system with a high-resolution ADC. With this option, the user can include power on the same board as the sensitive signal chain with no concern to proximity and still get the same performance as with an external power source.

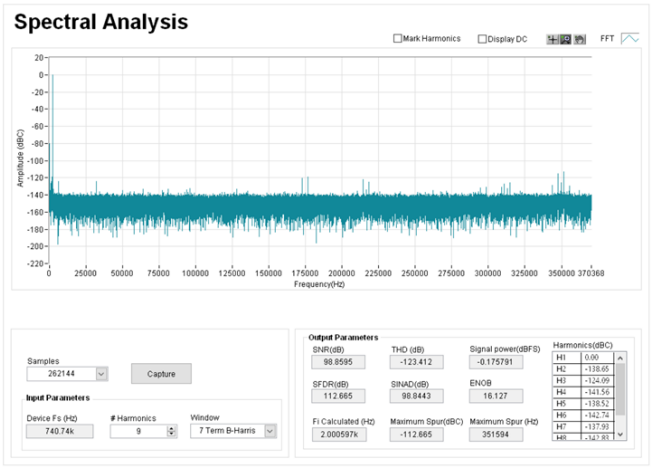


図 21. Spectral Results for LMZ1420x

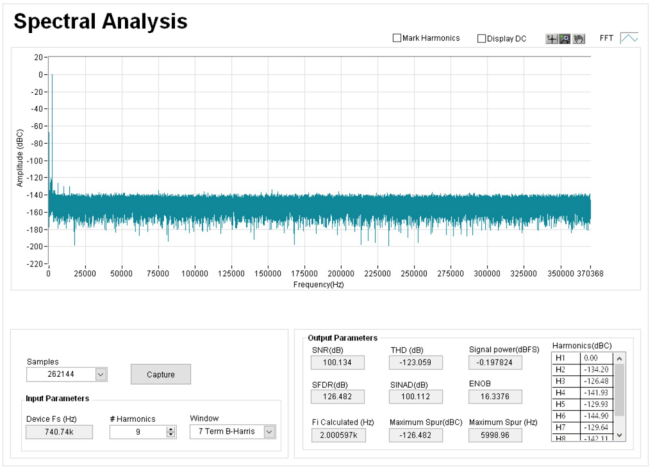


図 22. Spectral Results for LM53635-Q1

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01054.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01054.

4.3 PCB Layout Recommendations

The LM53635-Q1 has certain layout guidelines that help it cut down on EMI. 図 23 illustrates how the LM53635-Q1 and its additional components must be placed in the layout.

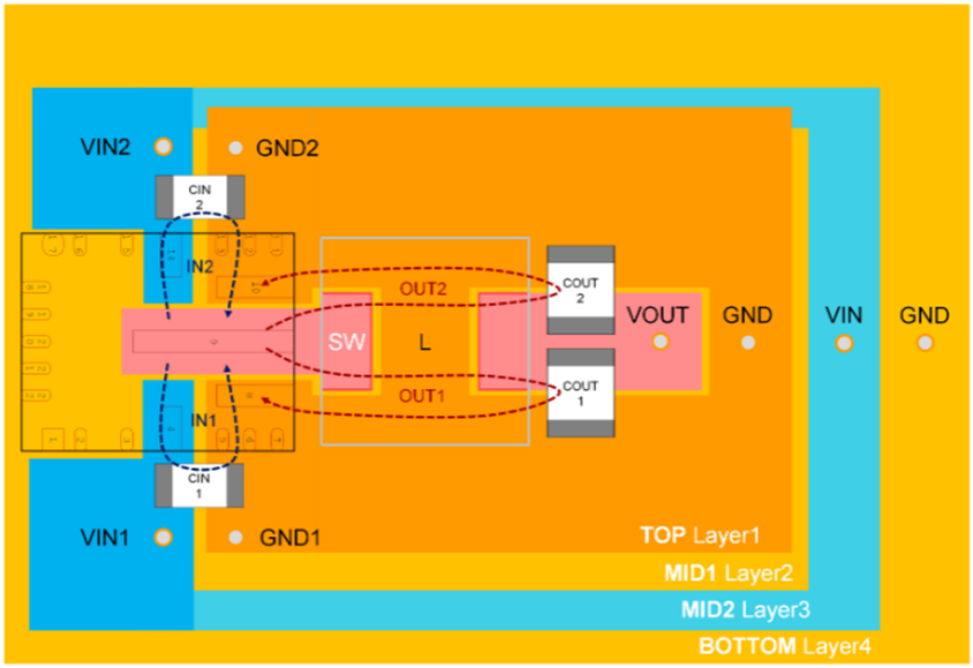


図 23. LM53635-Q1 Layout Guidelines

Putting the input and output capacitors in this configuration creates parallel capacitance loops, minimizing the inductance. This placement then reduces the switch node ringing and overall lowers the EMI emissions. Another recommendation is to leave the ground plane unbroken under the device. This provides the shortest return path possible, minimizing EMI generated by the loop. For more layout recommendations regarding the AFE or SAR ADC, see the TIDA-01050 reference design.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01054.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01054.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01054.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01054.

5 Software Files

To download the software files, see the design files at TIDA-01054.

6 Related Documentation

1. Texas Instruments, *TIDA-01052 ADC Driver Reference Design Improving Full Scale THD Using Negative Supply Design Guide*

6.1 商標

7 About the Authors

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年9月発行のものから更新 **Page**

- Corrected LM53635 part number in Figure 5: *LM53635-Q1 Schematic* 5
- Updated Equation 4 7
- Updated Equation 5 7
- Updated Equation 7 7
- the amount of LSB present at the ADC from 4.85% to 2.42% 変更 8
- the amount of noise the OPA625 has at the ADC from 1 LSB to 50% 変更 8
- Updated Equation 9 8
- Updated Equation 11 8

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