参考資料

TI Designs: TIDA-01371
超音波システム用のプログラム可能な±100V、大電流、フローティング・リニア・レギュレータのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

超音波発信機には、送信時に大電流を圧電トランスデューサへ送り込むため、安定したプログラム可能なDC電源が必要です。このリファレンス・デザインでは、±2.5～±100Vの範囲の出力電圧を供給できる、正および負のリニア・レギュレータを紹介します。外付けの制御電圧を使用して、プログラム可能性(DACからの制御を想定)が実装されています。低ノイズ特性を実現しているため、既製の低ノイズの正および負のLDOレギュレータや、レギュレータの接地をフローティングさせる回路により、パッシブおよびアクティブ・ノイズ・フィルタの置き換えが可能です。さらに、外部のパワーMOSFETを使用してレギュレータの電流能力をスケーリングし、剪断弾性波(エラストグラフィ)モードなどの特殊な画像処理モードをサポートします。トランスデューサへ非常に大きな電流を供給するために、大容量の入力コンデンサが1msにわたって高エネルギーを供給でき、この電源から流れ出る平均電流を極めて低い量に抑えます。このデザインは、高電圧DC/DC昇圧段であるTIDA-01352デザインと組み合わせて使用できます。

リソース

TIDA-01371	デザイン・フォルダ
TIDA-01352	デザイン・フォルダ
TPS7A47	プロダクト・フォルダ
TPS7A33	プロダクト・フォルダ
TLV171	プロダクト・フォルダ
TLV2171	プロダクト・フォルダ
CSD19533KCS	プロダクト・フォルダ

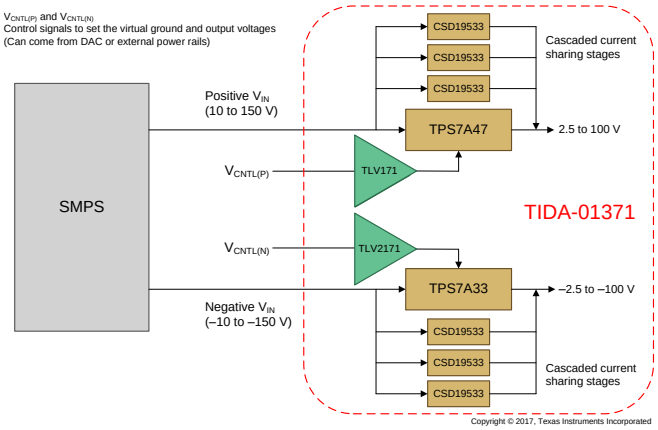
特長

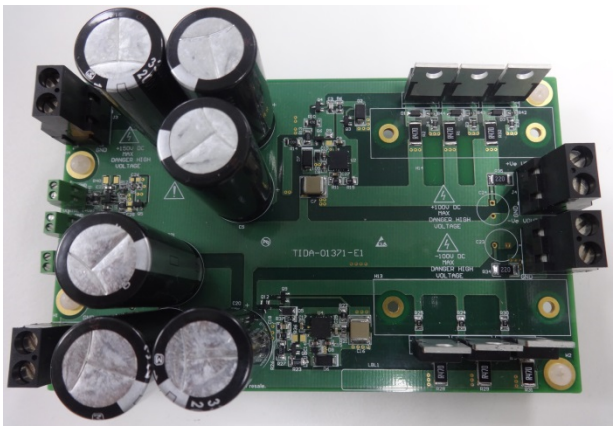
- フローティングおよびトラッキング・レギュレータでパッシブおよびアクティブのノイズ・フィルタを代替、既製のLDOレギュレータで±1.5%以上の負荷レギュレーションを実現
- 革新的なカレントシェア方式に、クラス最高の低$R_{DS(ON)}$を実現したTIのCSDシリーズのパワーMOSFETと、低インピーダンスのドライバ回路を使用し、過渡応答を改善
- DACからの制御信号を使用して、出力電圧を±2.5～±100Vにプログラム可能
- 1msパルス(最大±20Aでテスト済み)について出力電流がスケーラブルで、特殊な画像処理モードをサポート
- 正と負の電圧電源が別々に独立しているため、超音波送信回路へ柔軟に電力を供給可能

アプリケーション

- 医療用超音波スキャナ
- ソナー・イメージング機器
- 非破壊検査機器

TI E2E™ Community　E2Eエキスパートに質問





1 System Description

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. When initiating an imaging, a pulse is generated and transmitted from multiple transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1 to 15 MHz.

1.1 Key System Specifications

表 1 shows the key specifications for this TI Design.

表 1. Key System Specifications

PARAMETER		SPECIFICATIONS	DETAILS
Positive regulator	Off-the-shelf regulator TPS7A4701	36 V, 1 A	2.5.1
	Voltage scaling	Test up to V_{IN} = 120 V	2.5.1
	Current scaling	Test up to I_{OUT} = 20 A pulsed for 1 ms every 1 second	2.5.1
Negative regulator	Off-the-shelf regulator TPS7A3301	–36 V, –1 A	2.5.2
	Voltage scaling	Test up to V_{IN} = –120 V	2.5.2
	Current scaling	Test up to I_{OUT} = –20 A pulsed for 1 ms every 1 second	2.5.2

2 System Overview

A medical ultrasound application requires high-voltage pulses to be transmitted inside a human body to get information about blood, organs, tissues, and so on. These pulses are bipolar in nature and are transmitted by pulsers.

There are two modes in general:

1. Pulse (Brightness or B) mode where high-voltage pulses (–100 and 100 V) are transmitted for a particular short time only.
2. Continuous (CW) mode where low-voltage (±2.5 to ±10 V) pulses are continuously transmitted.

Note that the same power supply is used for both the modes meaning the output of power supply is ranging from ±2.5 to ±100 V. Such a powering scheme is typically implemented using a switched mode power supply (SMPS) followed by regulators as shown in 図 1. The voltage noise on the output signal is very important when CW mode is used because the signal amplitudes are low. Within Pulse mode, there is a special mode called Elastography (or Shear wave) mode. The current requirements are huge (sometimes more than 100 A) for a short period of time (may be tens of microseconds). Delivering such a high current at high voltages without dropping the output voltage is a challenge. To cover for the droop in output voltage, the high value of capacitors is also used at the output of SMPS.

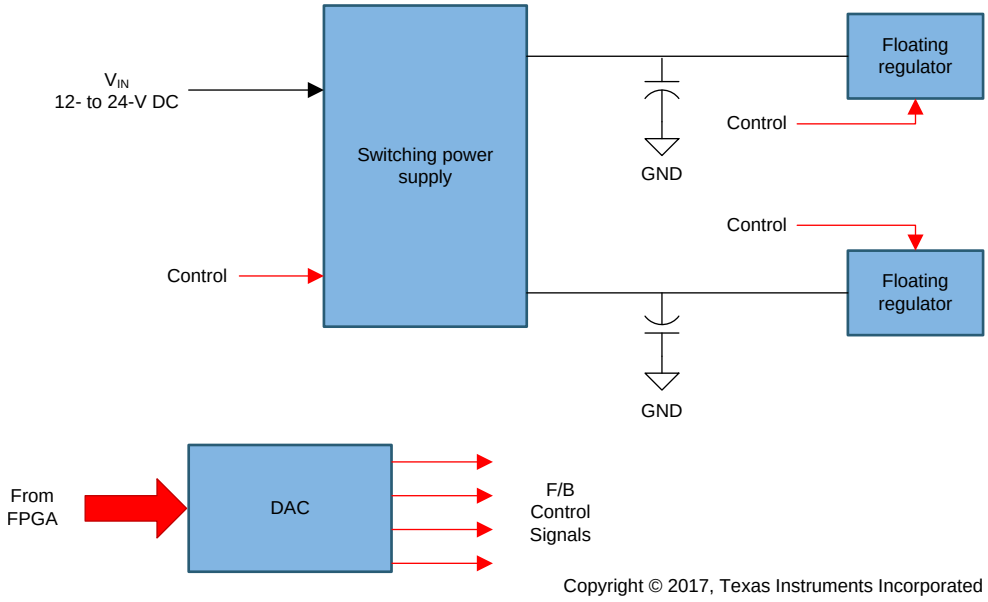


図 1. Typical Power Supply Scheme in Medical Ultrasound Application

2.1 Example of Power Calculations—Standard Imaging Mode

The following is an example of pulse mode for medical imaging. The standard mode has a driving waveform as shown in 図 2.

Assume the following nomenclatures:

- ton = total on-time
- toff = total off-time
- f = operating frequency of the probe
- n = number of pulses
- c = capacitance of the probe at operating frequency f

- N = number of transducers

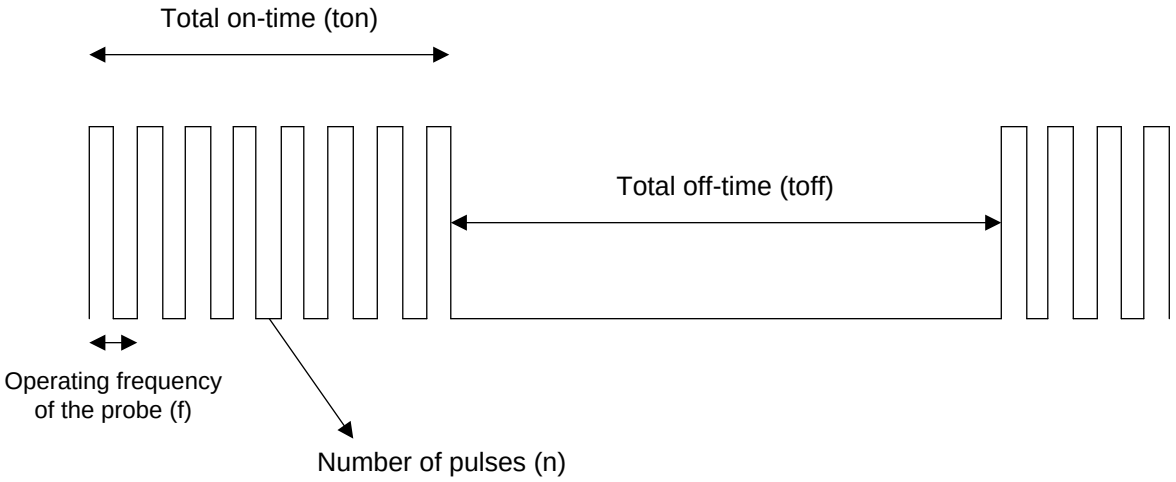


図 2. Standard Driving Waveform for Ultrasound Transducers

For a 128-channel transducer ultrasound system, N = 128.

For the next example, consider a probe with the following specifications:

- C = 470 pF
- f = 7.5 MHz
- Total number of pulses n = 10
- toff = 300 µs
- ton = 1.3 µs (calculated using n = 10 and f = 7.5 MHz)
- Voltage for transition is from –100 to 0 V or 0 to 100 V

$$\text{Peak power consumption} = 4 \times 128 \times 470\text{p} \times 100^2 \times 7.5\text{M} = 18\ \text{kW} \quad (1)$$

$$\text{Peak output current} = \frac{18\ \text{kW}}{100} = 180\ \text{A} \quad (2)$$

$$\text{Average power consumption} = \frac{18\ \text{kW}}{300} \times 1.3 = 78\ \text{W} \quad (3)$$

For a 20-V dip on the output capacitor of SMPS (that is, input capacitor of floating regulators):

$$C_{OUT} > \frac{I_{OUT} \times \text{ton}}{20} > \frac{180 \times 1.3\ \mu}{20} > 11.7\ \mu\text{F} \quad (4)$$

This means that with an output capacitor of SMPS = 470 µF, the dip on the output voltage (of the SMPS) is 0.49 V. In such a case, there is no need to use the floating regulator. The output capacitor of the SMPS is enough to provide the required ability to drive the transducers.

However, there are some special imaging modes like Elastography where the requirements are different.

2.2 Example of Power Calculations—Special Imaging Mode (Elastography)

The special imaging mode Elastography has a driving waveform as shown in 図 3. Considering the same nomenclature as explained in 2.1:

- n = 5 pulses
- ton = 55 ms
- toff = 2 seconds

$$P_{AVG} = P_C \times \frac{1}{11} \times \frac{55}{2055} = 43.7\ W \quad (5)$$

式 6 shows that average power needed for Elastography is less than the standard imaging mode.

Assuming the same voltage dip of 20 V:

$$C_{OUT} > \frac{I_{OUT} \times ton}{V_{dip}} > \frac{180 \times 1\,m}{20} > 9000\ \mu F \quad (6)$$

However, this needs to be replenished in time periods of 10 ms between the two 1-ms pulses as shown in 図 3.

If the SMPS is a 80-W rated power supply, the system would be current limited to 80/100 = 0.8 A only. The charging current needed in such case is:

$$I_{charge} = \frac{20 \times 9000\ \mu}{10\ m} = 18\ A \quad (7)$$

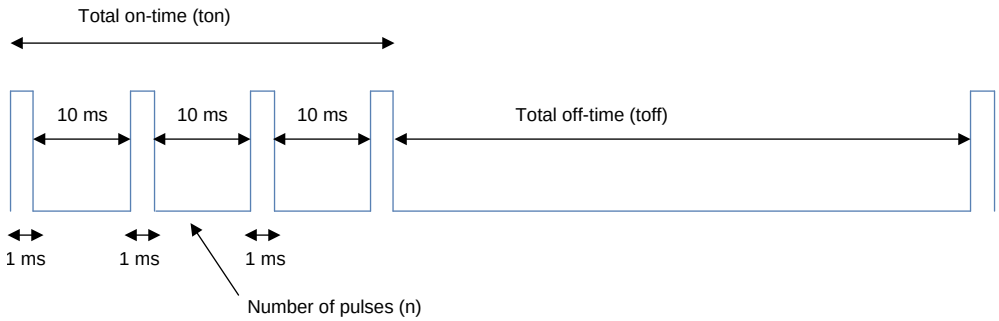


図 3. Elastography—Driving Waveform for Ultrasound Transducers

2.3 Block Diagram

図 4 shows the system level block diagram for the TIDA-01371 design. The design has two sections: positive regulator and negative regulator. Both the regulators are floating, trackable, and scalable in terms of output voltage and output current. The positive and negative inputs (±10 to ±120 V) for this TI Design are taken from a standard SMPS.

The positive floating regulator uses an off-the-shelf linear regulator TPS7A4701 from Texas Instruments. It is a 36-V ultra-low noise (4-μV_{RMS}) low-dropout linear regulator capable of sourcing a 1-A load. The ground of this regulator is floated using a DC amplifier made using the TLV171. The voltage scaling is achieved using a BJT at the input and current scaling is achieved using external N-channel MOSFETs CSD19533 from Texas Instruments. The design has three stages connected in parallel for the current scaling feature. More stages can be used for higher current requirements.

The negative floating regulator uses an off-the-shelf linear regulator TPS7A3301 from Texas Instruments. It is a –36-V ultra-low noise (16-μV_{RMS}) low-dropout linear regulator capable of sinking a 1-A load. The ground of this regulator is floated using a DC amplifier made using the TLV2171. The voltage scaling is achieved using a BJT at the input and current scaling is achieved using external N-channel MOSFETs CSD19533 from Texas Instruments. The design has three stages connected in parallel for the current scaling feature. More stages can be used for higher current requirements.

The DC amplifiers for setting the floating (or virtual) grounds are controlled using control voltages $V_{CNTL(P)}$ and $V_{CNTL(N)}$. These signals can come from DACs or external power supplies. Because the transient response is important for medical ultrasound applications, low-impedance drive circuits using diodes and NPN-PNP transistors are used for driving the current scaling MOSFETs.

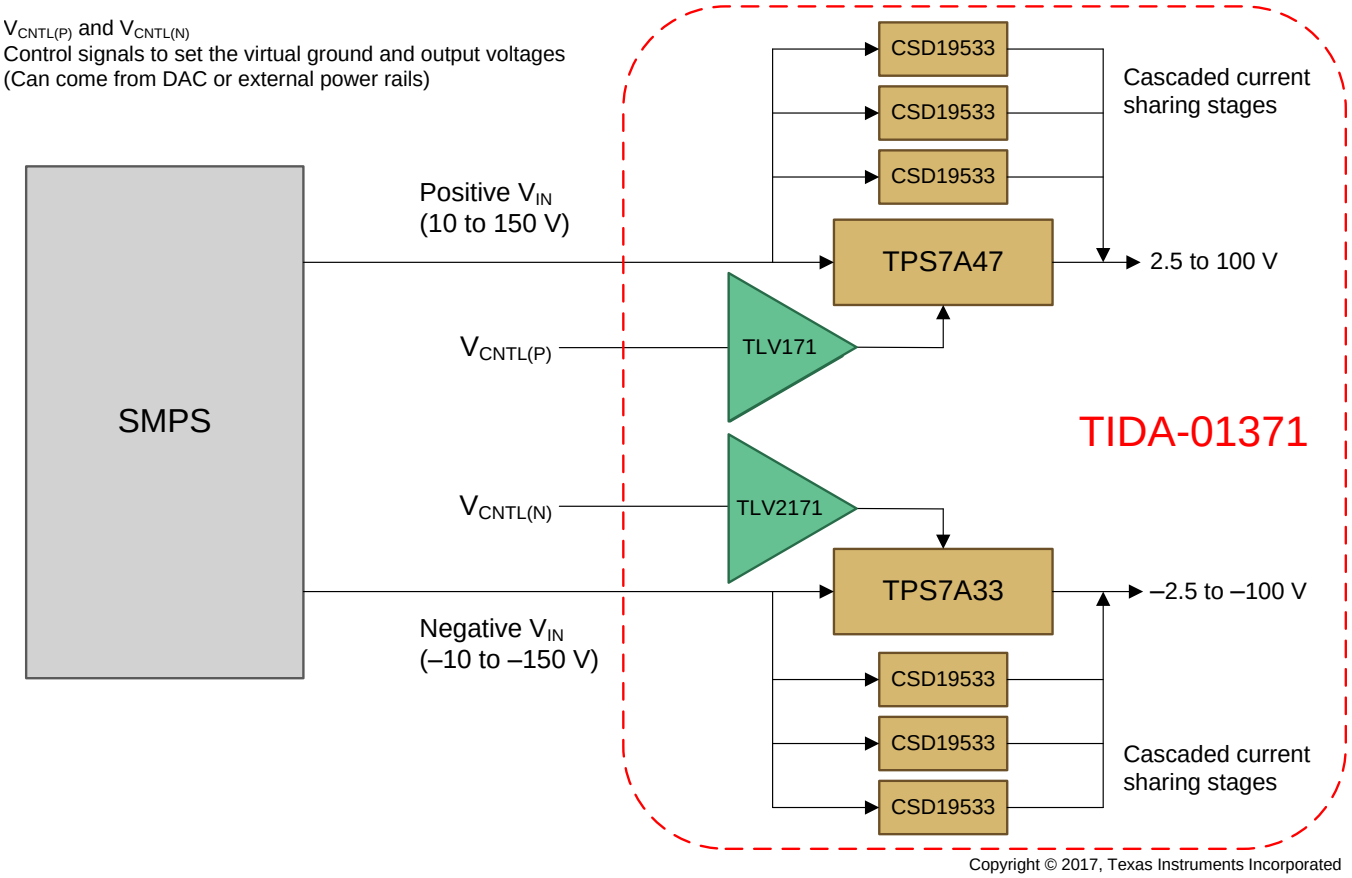


図 4. System Block Diagram

2.4 Highlighted Products

This design has two sections: one is a positive regulator and other is a negative regulator. Both the sections use off-the-shelf low dropout (LDO) regulators from Texas Instruments along with N-channel MOSFETs and op amps.

2.4.1 TPS7A47

The TPS7A47 device is a 36-V ultra-low noise (4-μV_{RMS}) LDO linear regulator capable of sourcing a 1-A load and providing a positive output voltage. The output voltage for the TPS7A47 can be configured with external feedback resistors. The device is designed with bipolar technology primarily for high-accuracy, high-precision applications where clean voltage rails are critical to maximize system performance. This feature makes it ideal for powering high-performance analog circuitry in critical applications such as medical. The device is also ideal for post DC-DC converter regulation.

2.4.2 TPS7A33

The TPS7A33 device is a –36-V ultra-low noise (16-μV_{RMS}, 72-dB PSRR) LDO linear regulator capable of sinking a 1-A load and providing a negative output voltage. The output voltage for the TPS7A33 can be configured with external feedback resistors. The device is designed with bipolar technology primarily for high-accuracy, high-precision applications where clean voltage rails are critical to maximize system performance. This feature makes it ideal for powering high-performance analog circuitry in critical applications such as medical. The device is also ideal for post DC-DC converter regulation.

2.4.3 CSD19533KCS

The CSD19533KCS device is a 100-V, 8.7-mΩ, TO-220 NexFET™ power MOSFET. With a pulsed drain current limit of 207 A (at 25°C) at pulse durations ≤ 100 μs and duty cycle ≤1%, it makes it ideal for the pulsed current output applications like medical ultrasound.

2.4.4 TLVx171

The 36-V TLVx171 family provides a low-power option for cost-conscious industrial systems requiring an electromagnetic interference (EMI)-hardened, low-noise, single-supply operational amplifier (op amp) that operates on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The single-channel TLV171, dual-channel TLV2171, and quad-channel TLV4171 provide low offset, drift, quiescent current balanced with high bandwidth for the power. This series of op amps are rail-to-rail input as well as output.

2.5 System Design Theory

This section explains the theory, component selection, and design details for both the positive and negative regulator sections.

2.5.1 Positive Floating Regulator

The positive regulator section uses a 36-V off-the-shelf positive LDO regulator and floats the ground of regulator with a DC amplifier (using low-voltage op amp and transistor).

2.5.1.1 Floating or Virtual Ground for Positive Regulator

The ground of a regulator can be floated using multiple methods and tricks. For this application, the ground of regulator is floated using a DC amplifier. Any positive regulator has some current flowing into the GND pin, which is termed as I(GND) in its datasheet. For the TPS7A4701, it is specified as 6.1 mA typical when the output current is 1 A.

Taking this current as a worst case, the user can put is as current source in the TINA simulation shown in 図 5. Regulator I(GND) is the current from the GND pin. This current is divided into two paths: one through an NPN BJT and other through a resistor voltage divider. Op amp U1 is operated as an integrator in open-loop configuration and drives the BJT through a series resistance of 2.2 kΩ. The op-amp is supplied with a 12-V supply VCC. *The V_{CNTRL} input decides the value of virtual ground voltage by using 式 8.*

$$\text{Virtual GND} = \left(\frac{379\text{k} + 20\text{k}}{20\text{k}} \times V_{CNTL}\right) \approx 20 \times V_{CNTL} \tag{8}$$

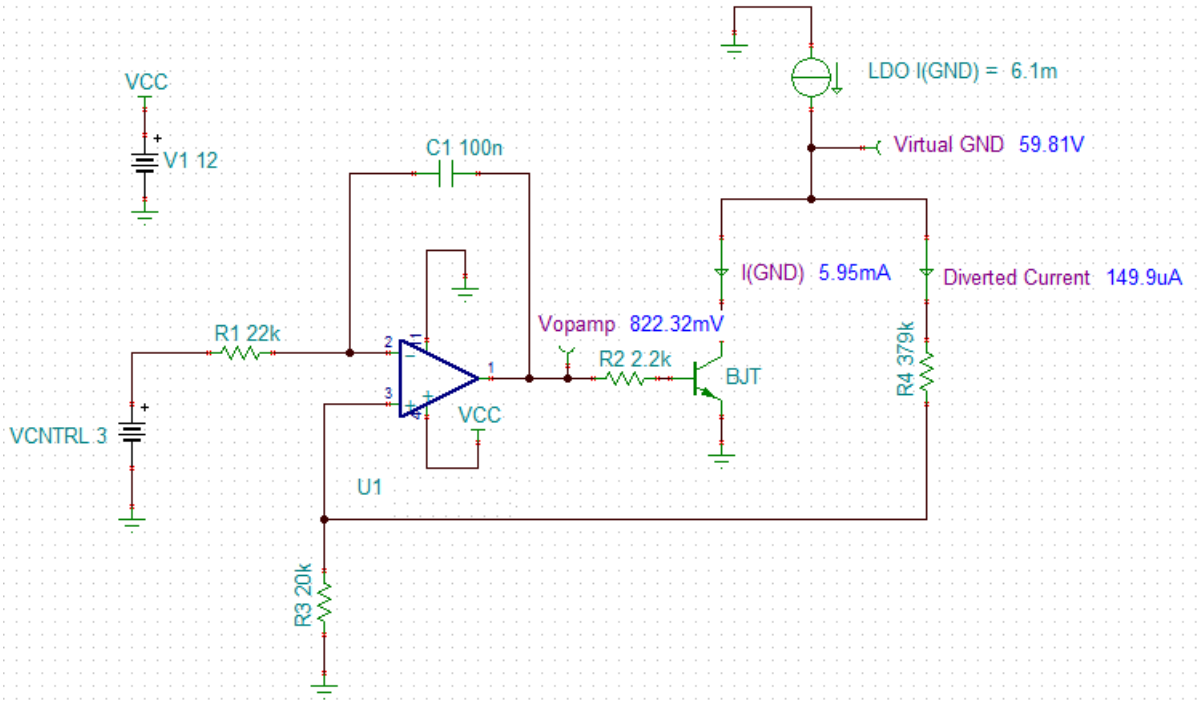


図 5. TINA Simulation for DC Amplifier for Floating Regulator Ground (Positive Regulator)

To understand the relationship between the control voltage and virtual ground signal, the graph shown in 図 6 is useful.

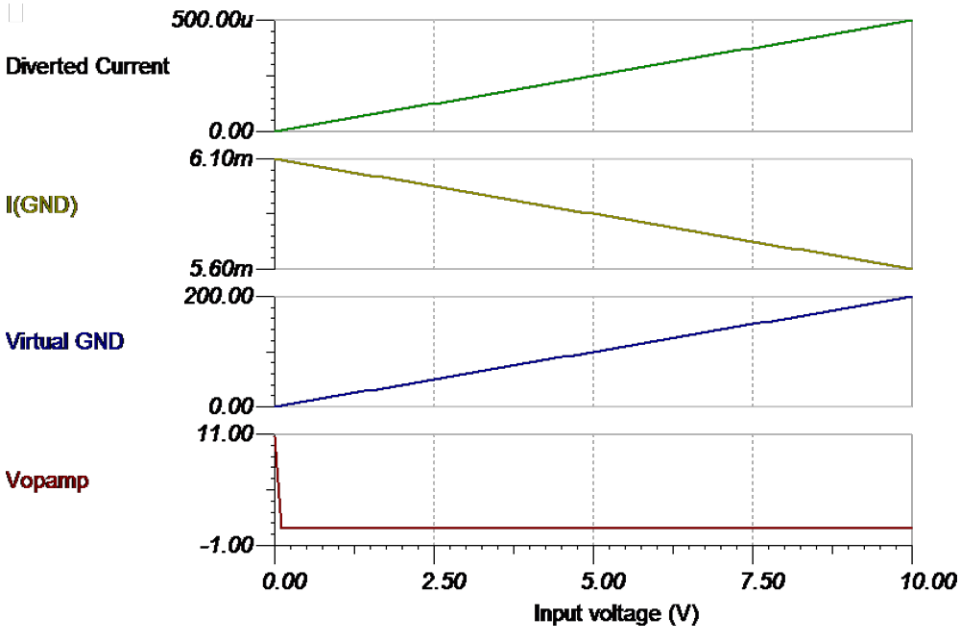


図 6. DC Transfer Characteristics: Control Voltage versus Virtual Ground

Based on the TINA circuit simulation, the TLV171 is used as an op amp for generating virtual ground using control voltage. The schematic for this section is shown in 図 7.

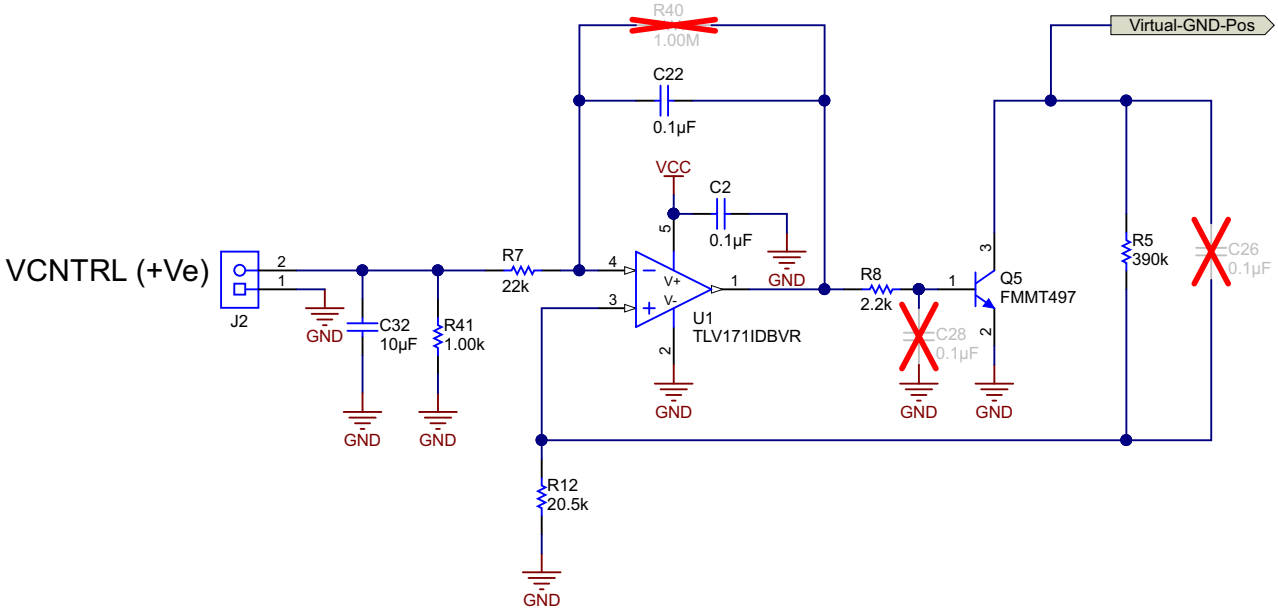


図 7. DC Amplifier to Generate Virtual Ground (Positive Regulator)

2.5.1.2 Voltage Scaling Circuit

The scalability in terms of voltage is implemented using voltage sharing circuit at the input of the regulator. Referring to 図 9, the resistors R13 and R14 along with BJT Q6 are used for implementing voltage sharing circuit.

Assuming the input voltage V_{IN} is 120-V DC and virtual ground (say V_{VG}) is set at 90 V, the R13 and R14 resistors generate a mid-point voltage = (V_{IN} + V_{VG}) / 2 = (120 + 90) / 2 = 105 V. This signal at the base of the BJT (= 105 V) keeps the emitter of BJT at 104.3 V approximately (depending on the BJT used; this can vary). This means the voltage going to the regulator is $V_{EMITTER}$ – V_{VG} = 104.5 – 90 = 14.5 V. This is true for any value of V_{IN} and V_{VG} (for example, V_{IN} = 100 V, V_{VG} = 60 V, V_{BASE} = 80 V, $V_{EMITTER}$ = 79.3 V, and regulator input voltage = 19.3 V).

This functionality helps in keeping a safe voltage at the input of the regulator by setting V_{IN} and V_{VG}. 図 8 shows the TINA simulation for voltage scaling circuit at different V_{IN} and VVG values.

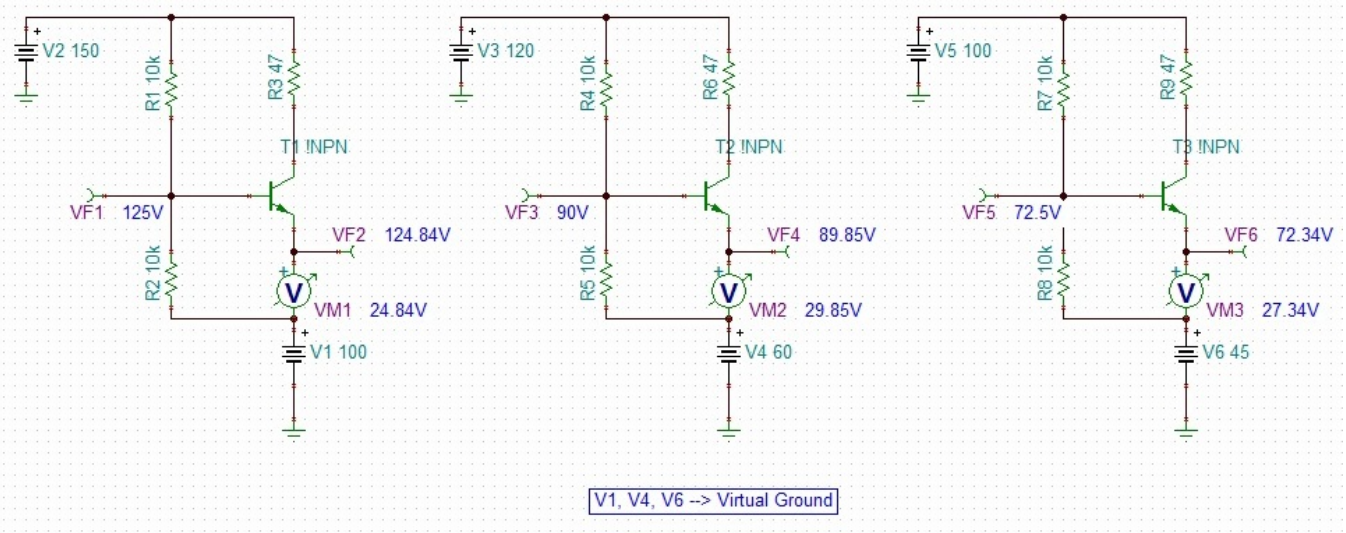


図 8. Voltage Scaling Circuit Simulation at Different V_{IN} and V_{VG} Values

2.5.1.3 Positive Regulator Circuit Using Virtual Ground

図 9 shows the positive regulator circuit using the TPS7A4701. The input capacitor C10 and output capacitor C8 are recommended values from the datasheet of the TPS7A4701. The output of the regulator with respect to virtual ground is 3.3 V set using feedback resistors R11 and R15.

D9 (36-V TVS) and D7 (20-V Zener diode) are used as protection devices for the regulator. The Zobel network (R35 and C24) are used to reduce the effect of inductive wires connected at the output.

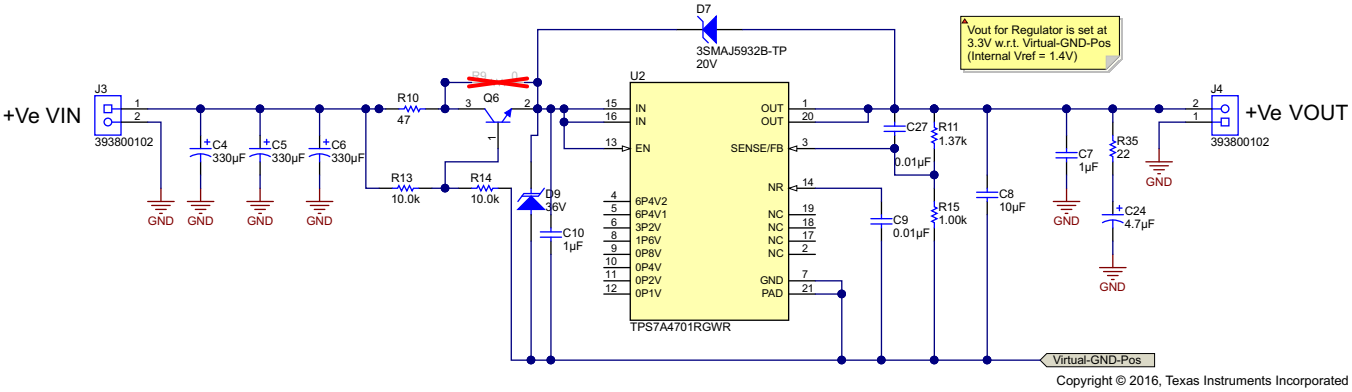


図 9. Positive Regulator Using TPS7A4701 and Virtual Ground

2.5.1.4 Current Scaling Using External MOSFETs

The current scalability is implemented using N-channel MOSFETs as shown in 図 10. Once current starts flowing through the input path of the regulator, it generates a voltage drop across 47 Ω, which is in series with the BJT Q6. Because it is placed across the base and emitter of PNP transistor Q4, the voltage drop across this resistor always remains 0.6 to 0.7 V (depending upon the BJT), limiting the current flowing through the regulator at 0.7 V/47 Ω = 15 mA approximately. Any load current higher than 15 mA passes through the parallel MOSFET paths. Because the transient response is important for the application, a low-impedance drive circuit using a diode and PNP transistor is used for driving the MOSFET. The currents flowing through each MOSFET is also equalized by series resistors of 0.47 Ω.

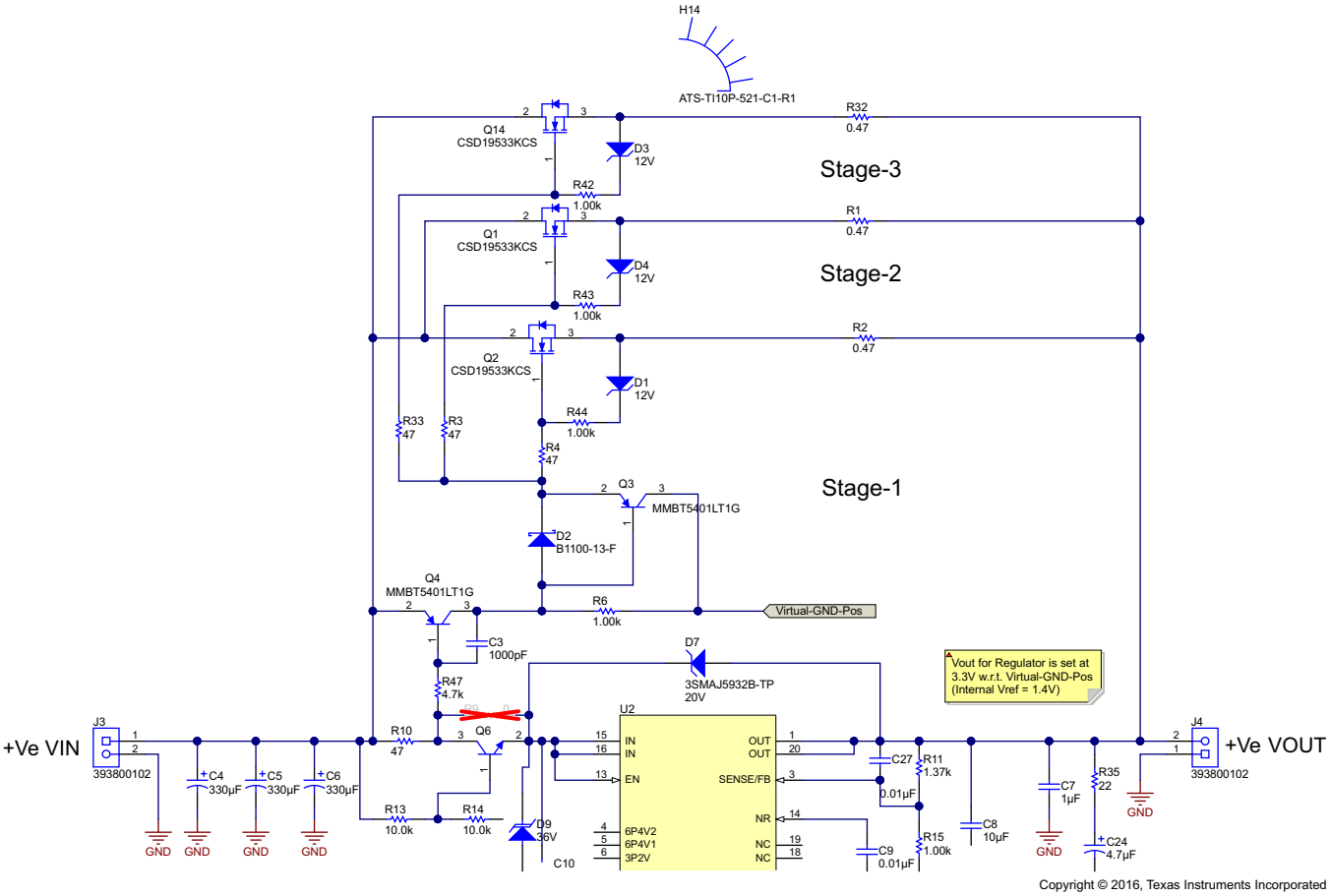


図 10. Current Scaling Using N-Channel MOSFETs (Positive Regulator)

The TINA simulation for the current sharing is shown in 図 11. The output current is set at 6-A DC and each of the N-channel MOSFETs shares 2 A. The current flowing through the 47-Ω resistor is only 15.68 mA, which is governed by voltage set by PNP transistor. The transient waveforms for the current sharing are shown in 図 12.

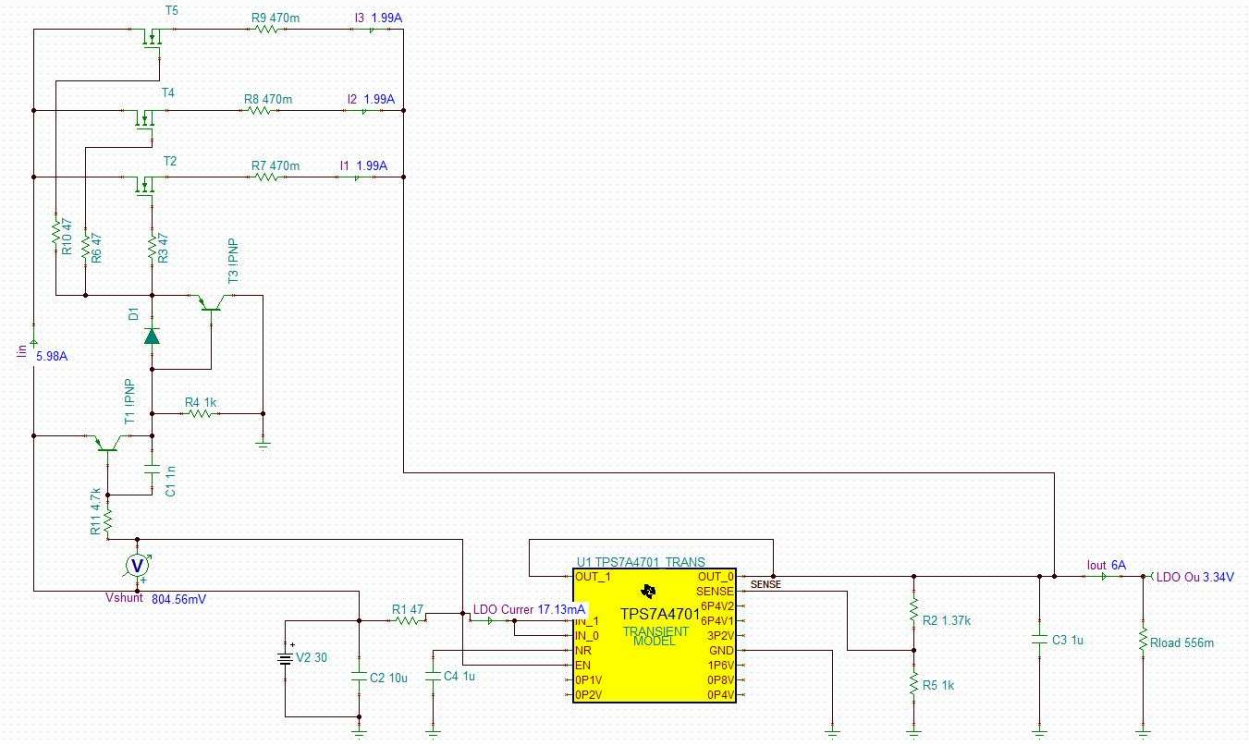


図 11. TINA Simulation for Current Sharing

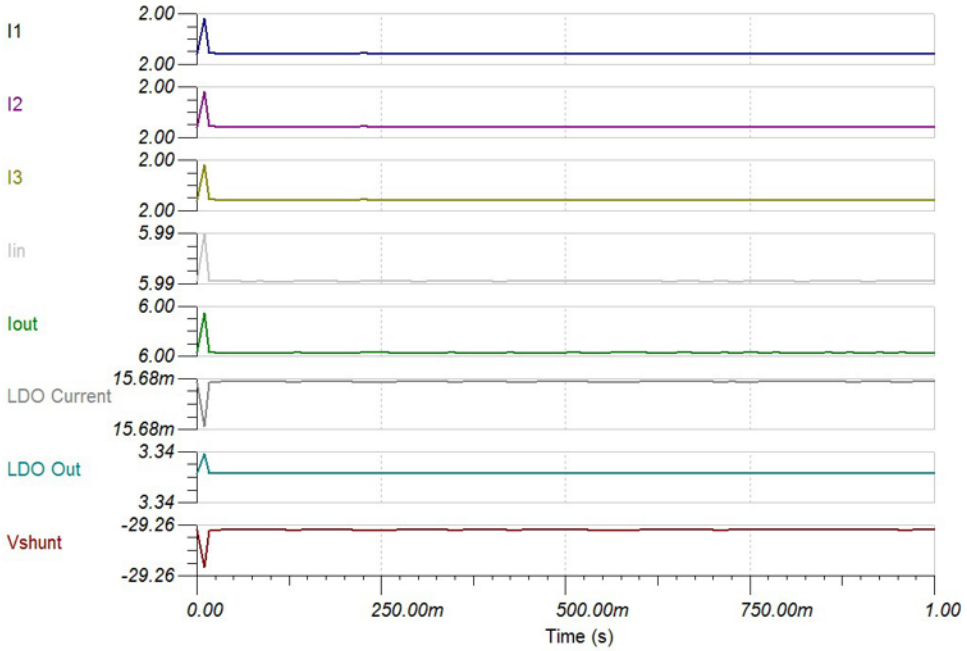


図 12. Transient Current Sharing (Positive Regulator)

2.5.2 Negative Floating Regulator

The negative regulator section uses a –36-V off-the-shelf positive LDO regulator and floats the ground of regulator with a DC amplifier (using two low-voltage op-amps and transistor).

2.5.2.1 Floating or Virtual Ground for Negative Regulator

For this section, the ground of regulator is floated using a DC amplifier as shown in 図 13. Any negative regulator has a specification termed as I(GND) in the LDO datasheet. For the TPS7A3301, it is specified as 5 mA typical when the output current is 500 mA. This current is diverted using a PNP BJT. Two op amps form a DC amplifier. The first stage converts the negative output voltage to a positive value. The second op amp is an error amplifier and the system has a stable point where the negative Input becomes equal to the positive input of this second op amp. If the output goes too negative the PNP transistor (at the output of second op amp) is driven and this shifts the virtual ground towards zero. The V_{CNTL} input decides the value of the output voltage by using 式 9:

$$VNEG(out) \approx 21 \times V_{CNTL} \quad (9)$$

As shown in 図 13, the output of the first op amp locks at V_{CNTL} voltage (= 1 V) and sets the negative output voltage at –21.32 V and virtual ground at –18.02 V. The relationship between the control voltage, negative output voltage, and virtual ground is shown in 図 14.

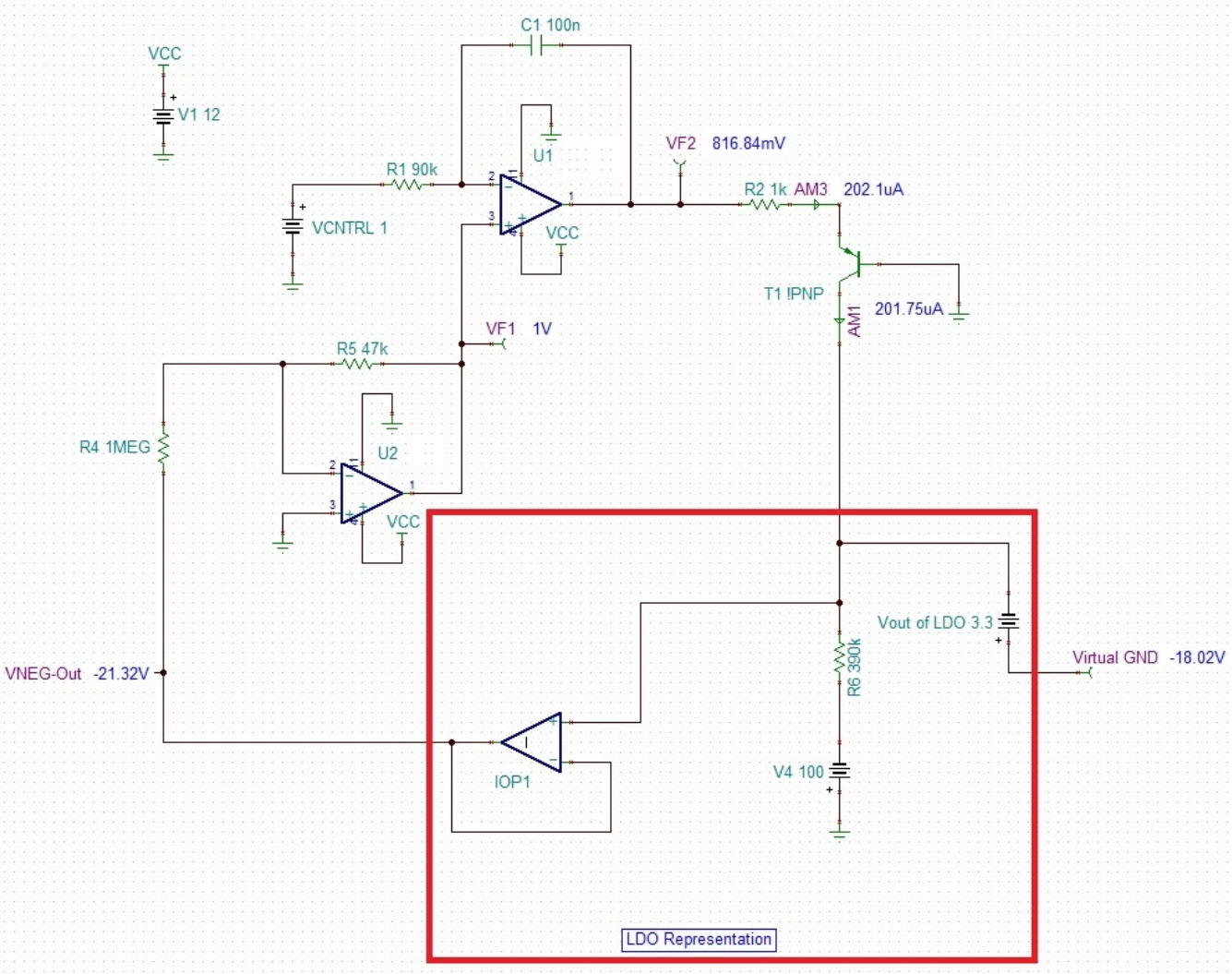


図 13. TINA Simulation for DC Amplifier for Floating Regulator Ground (Negative Regulator)

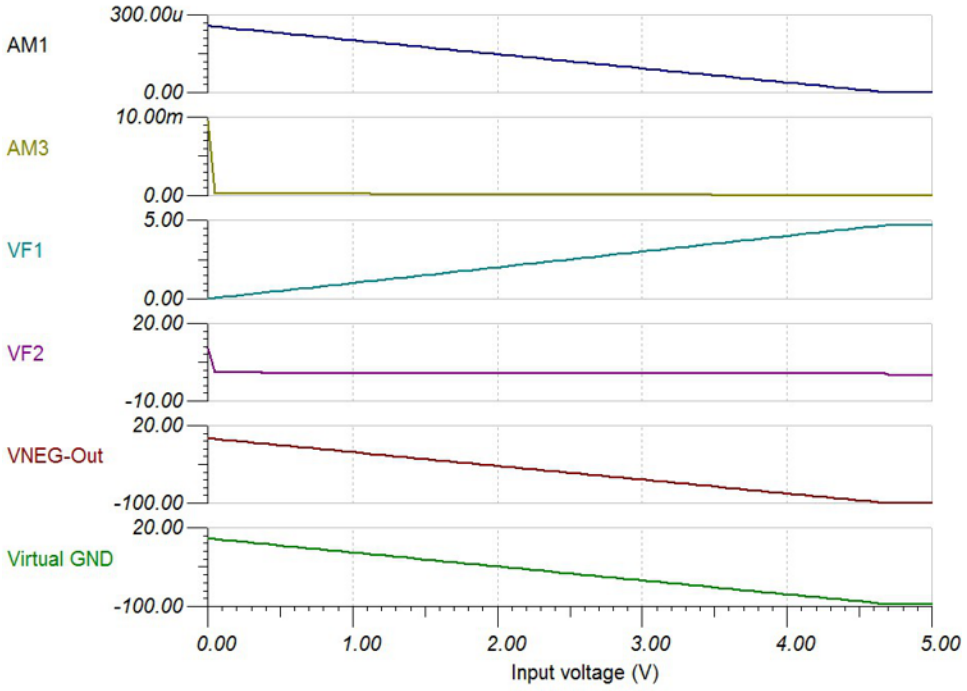


図 14. DC Transfer Characteristics: Control Voltage versus Negative V_{OUT} and Virtual Ground

Based on the TINA circuit simulation, the TLV2171 is used as an op amp for generating virtual ground using control voltage. The schematic of this section is shown in 図 15.

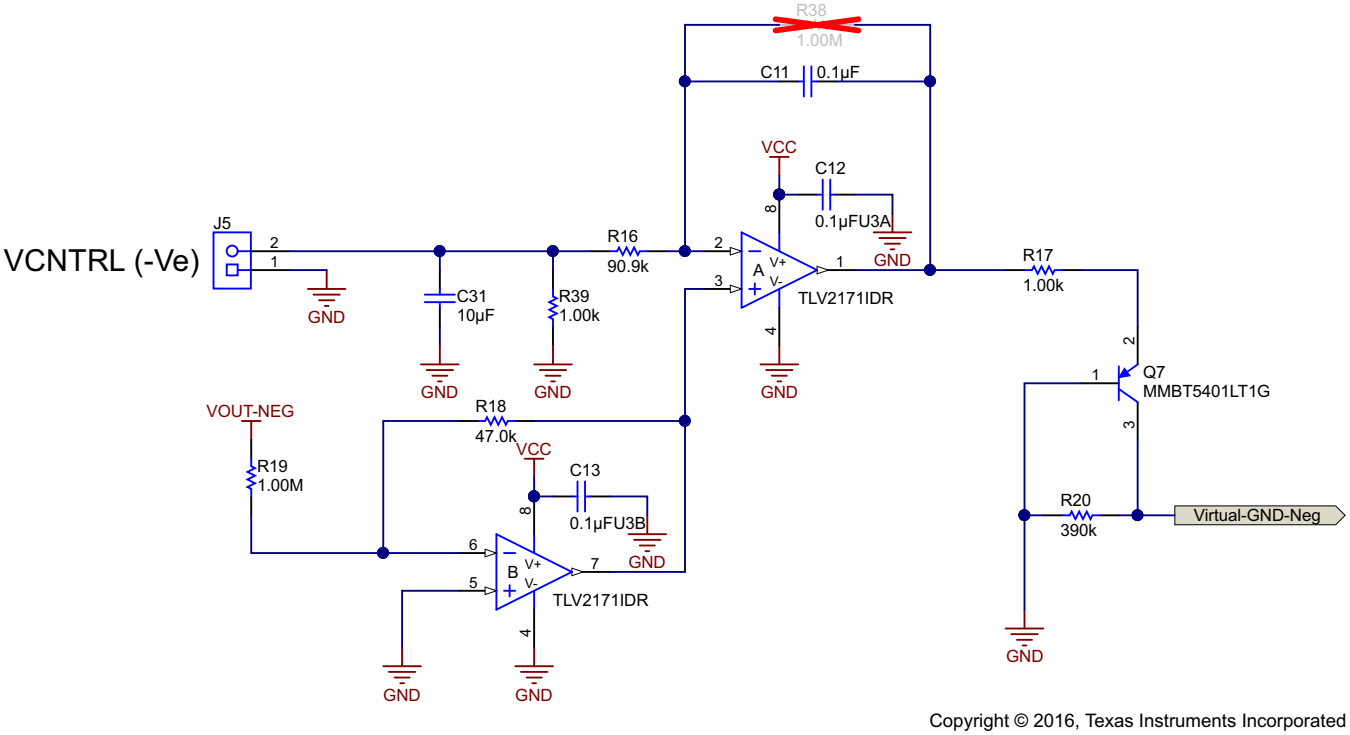


図 15. DC Amplifier to Generate Virtual Ground (Negative Regulator)

2.5.2.2 Voltage Scaling Circuit

Referring to 図 16, the scalability in terms of voltage is implemented using a voltage sharing circuit at the input of the regulator. Resistors R27 and R23 along with BJT Q8 are used for implementing voltage sharing circuit. The operation is similar to the circuit explained in 2.5.1.2 for positive regulator input voltage scaling.

2.5.2.3 Negative Regulator Circuit Using Virtual Ground

図 16 shows the negative regulator circuit using the TPS7A3301. Input capacitor C14 and output capacitor C15 are recommended values from the TPS7A3301 datasheet. The output of the regulator with respect to virtual ground is 3.3 V set using feedback resistors R21 and R22.

D8 (36-V TVS) and D6 (20-V Zener diode) are used as protection devices for the regulator.

Note that the peak detector circuit is used before feeding the input to the regulator. Capacitor C30 and diode D5 along with R27 (= 10 kΩ) are used as the peak detector circuit. This helps in improving the output voltage because during the loaded condition, the input voltage across the bulk capacitors (C19, C20, and C21) will start drooping. The peak detector circuit holds the charge until the time constant value of 10 µs × 10k = 0.1 seconds.

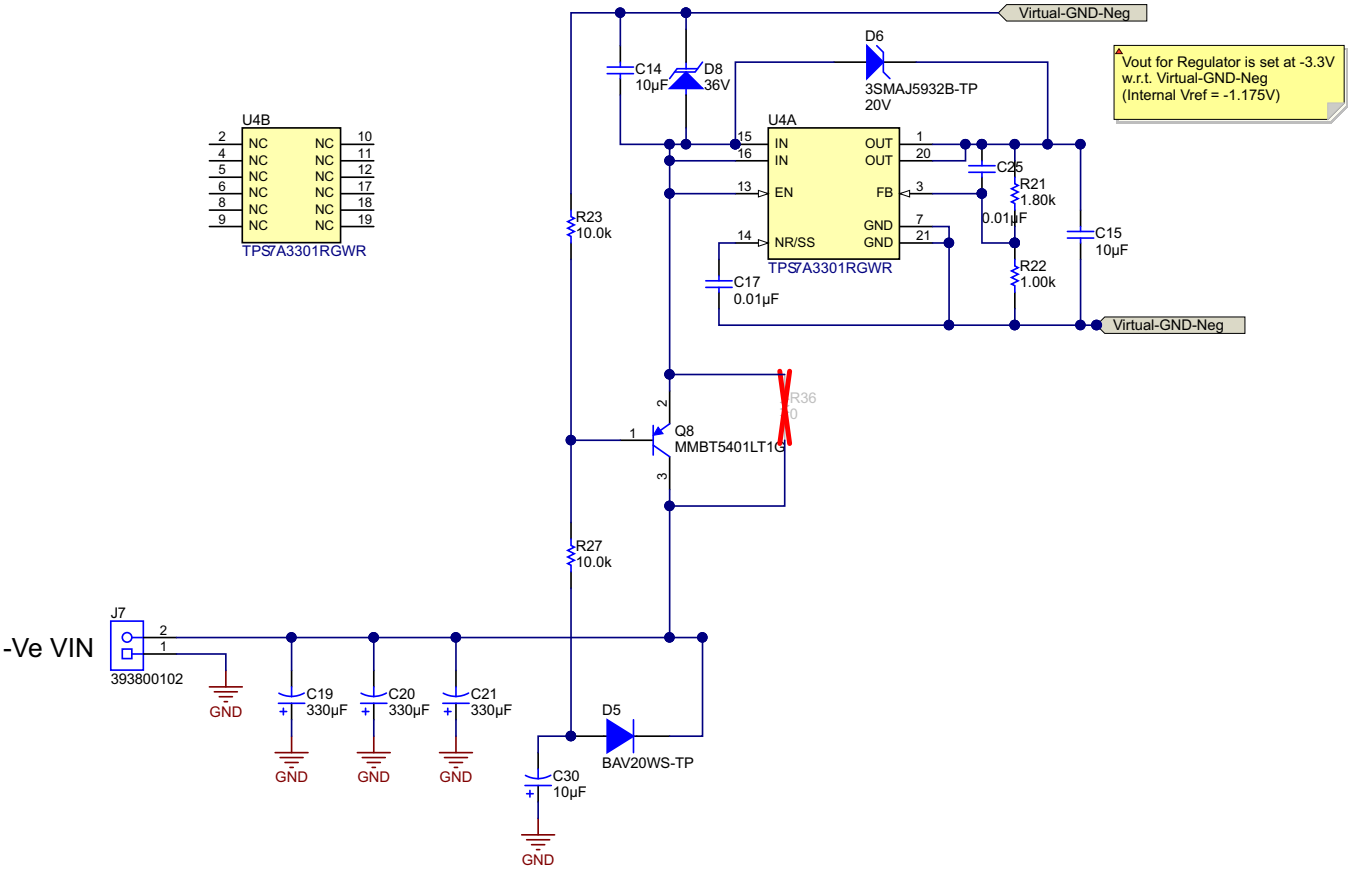


図 16. Negative Regulator Using TPS7A3301 and Virtual Ground

2.5.2.4 Current Scaling Using External MOSFETs

The current scalability is implemented using N-channel MOSFETs as shown in 図 17. Once current starts flowing through the regulator, it generates a voltage drop across 47 Ω, which is in series with the regulator output. The voltage drop across this resistor always remains 0.6 to 0.7 V (depending upon the BJT), limiting the current flowing through the regulator at 0.7 V/47 Ω = 15 mA approximately. Any load current higher than 15 mA passes through the parallel MOSFET paths. Because the transient response is important for the application, a low-impedance drive circuit using a buffer (made using NPN and PNP transistors) is used to drive the MOSFET. The current buffer is decoupled using a 47–Ω resistor (R46) and a 2.2-µF capacitor (C29). The sense signal across R37 generates a current to be flown through R26. The voltage drop across R26 is used for generating Vgs to drive the MOSFETs. The currents flowing through each MOSFET is also equalized by series resistors of 0.47 Ω.

Note that the output is always affected by the voltage drop across R37, which can be in the range of 0.6 to 0.7 V (depending on the BJT used). This should be considered while setting up the output voltage, especially in lower voltage conditions.

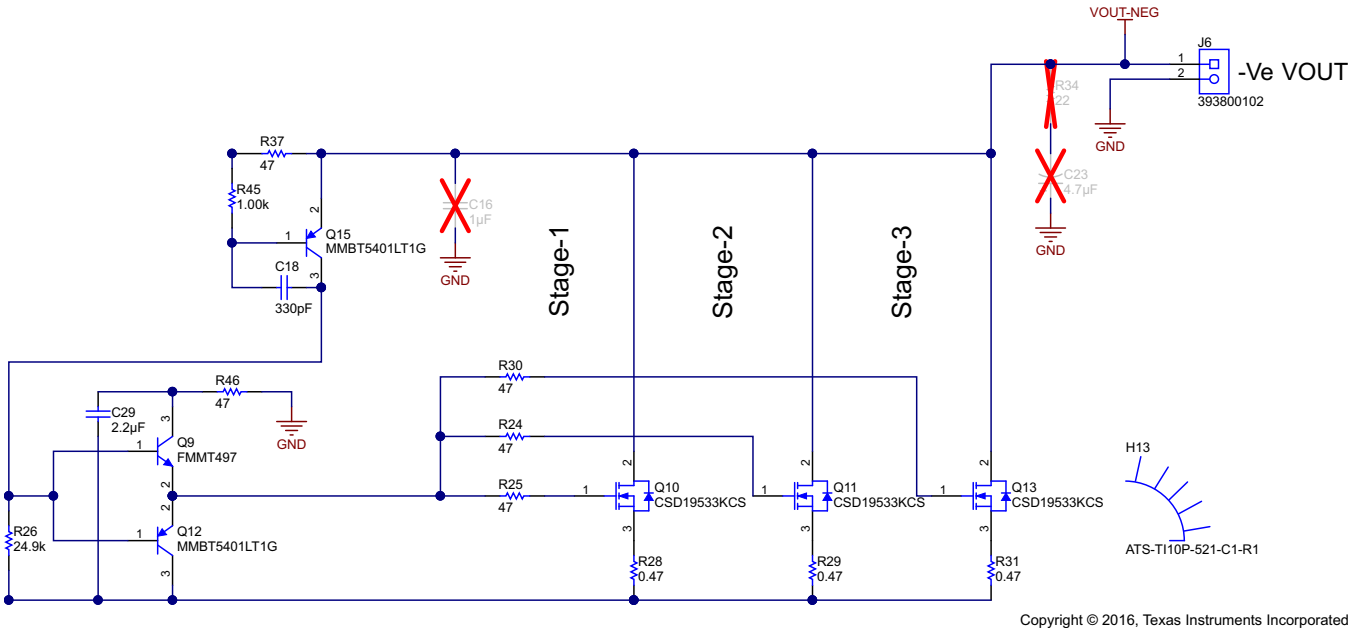


図 17. Current Scaling Using N-Channel MOSFETs (Negative Regulator)

The TINA simulation for the current sharing is shown in 図 18. The output current is set at –6-A DC and each of the N-channel MOSFETs shares –2 A. The current flowing through the 47-Ω resistor is only –14.24 mA, which is governed by voltage set by the PNP transistor across 47 Ω. The transient waveforms for the current sharing are shown in 図 19.

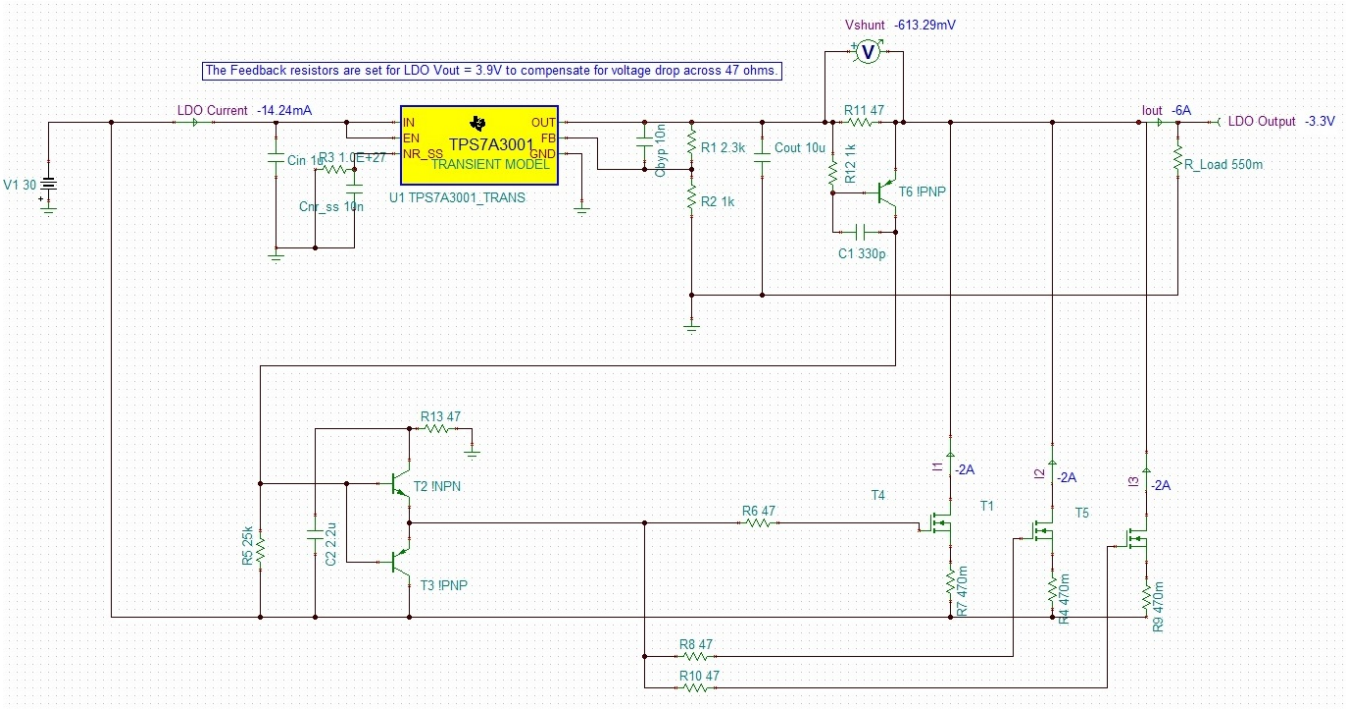


図 18. TINA Simulation for Current Sharing

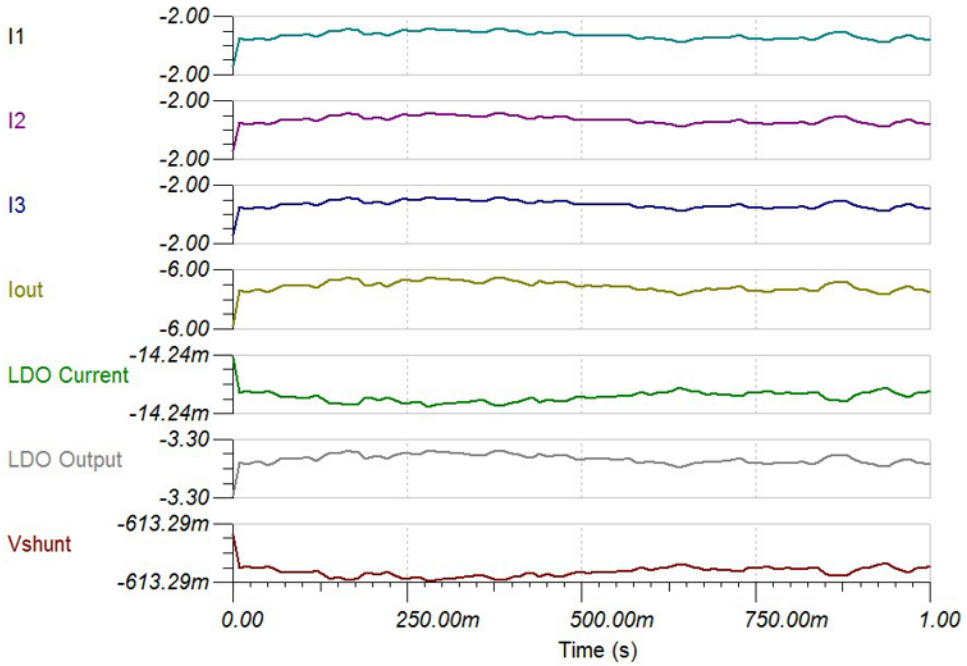


図 19. Transient Current Sharing (Negative Regulator)

2.5.3 Selecting Power MOSFETs

The output current delivering ability of the regulator depends on a few parameters.

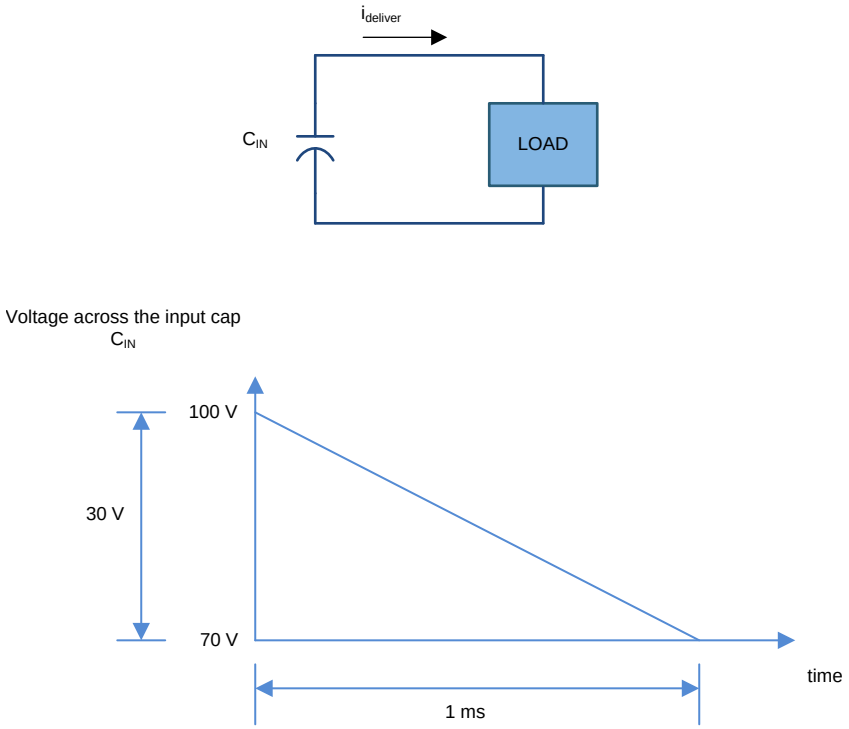


図 20. Current Delivering Ability of Input Capacitor

As shown in 図 20, the deliverable current is calculated as 式 10:

$$I_{DELIVER} = \frac{V_{DIP} \times C_{IN}}{t} \quad (10)$$

V_{dip} is dependent on the regulator's maximum input to output difference allowable (as mentioned in the regulator's datasheet). For the TIDA-01371, both regulators have the maximum allowable input to output difference of 36 V. Also, due to input voltage scaling circuit, that maximum can be doubled. In summary, the TIDA-01371 can support a voltage dip on input capacitor of 72 V approximately.

Using the example shown in 図 20, assume the voltage across input capacitor is dropping from 100 V to 70 V in a time period of 1 ms. Because it is dropping in a linear fashion, the actual voltage seen by the MOSFETs is an average of the same, which is 15 V.

Now look at the MOSFET datasheet for the SOA graph. This graph defines the instantaneous V-I product of the MOSFET. The SOA graph for CSD19533KCS is shown in 図 21.

At VDS = 15 V and a pulse of 1 ms, the maximum drain to source current supported by CSD19533KCS is ≈ 15 A.

As the voltage dip across input capacitor goes bigger, the current capability of the MOSFET (based on the SOA graph) will reduce.

The MOSFETs are selected based on the following parameters:

1. Current to be delivered
2. Voltage dip on the input capacitor
3. Pulse duration for which MOSFET is turned on
4. Package of MOSFET

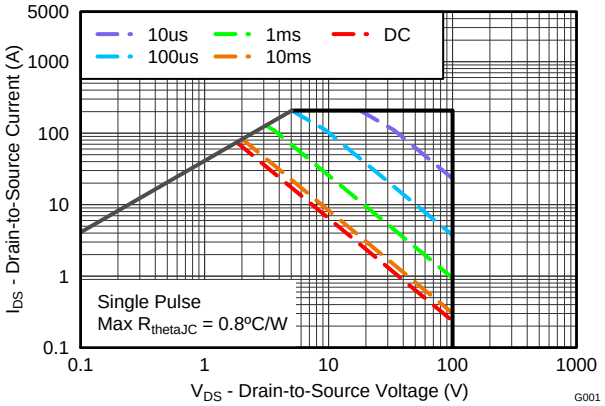


図 21. SOA Graph for CSD19533KCS

3 Hardware, Testing Requirements, and Test Results

This section explains the test setup required to test the TIDA-01371 design.

3.1 Test Setup

図 22 shows the top view of the TIDA-01371 board. Note that heat sinks are not shown in the board image; however, two heat sinks are required (one for positive current sharing circuit and one for negative current sharing circuit) to test this circuit.

The board has a total of seven connectors:

- J1 = VCC for virtual ground generation circuit
- J2 = Control voltage for positive regulator
- J3 = Positive input connector (10 to 120 V)
- J4 = Positive output connector (2.5 to 100 V)
- J5 = Control voltage for negative regulator
- J6 = Negative output connector (–2.5 to –100 V)
- J7 = Negative input connector (10 to 120 V)

WARNING

The user must have experience in handling high-voltage circuits while testing this board.

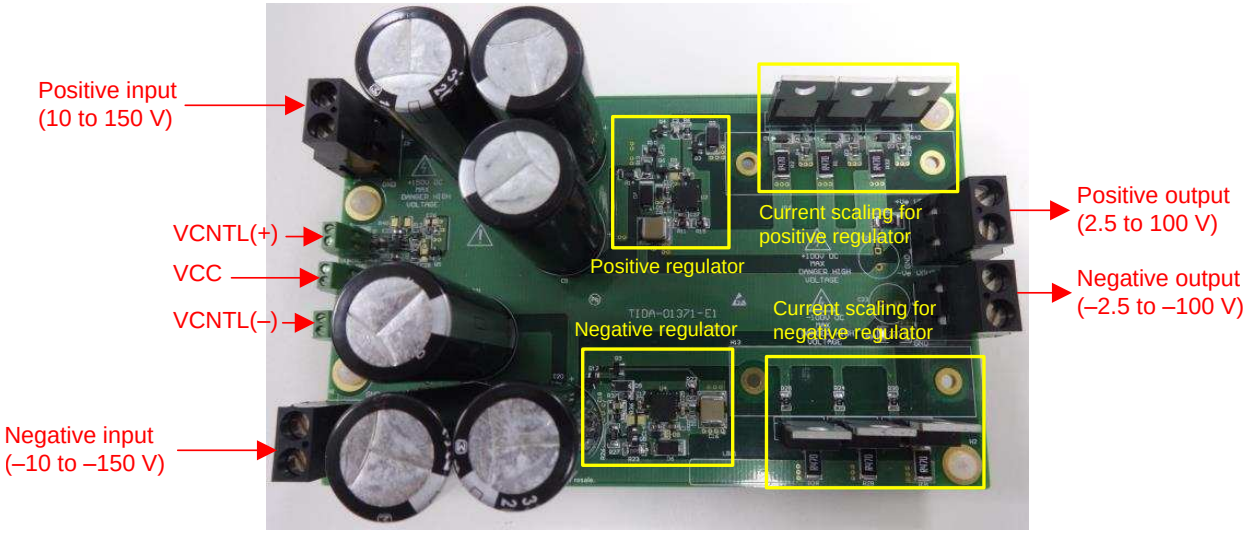


図 22. Top View of TIDA-01371 Board

The block diagram shown in 図 23 highlights the test setup required to test the TIDA-01371 board for load regulation tests. The load regulation is required to have 1-ms pulses generated for very high currents (±20 A) to be connected at J4 and J6. Also, the current limits typically set by the SMPS circuits is the average current limit. To see the actual droop across the input bulk capacitors of the TIDA-01371, special current limit circuits are built and used for testing purposes.

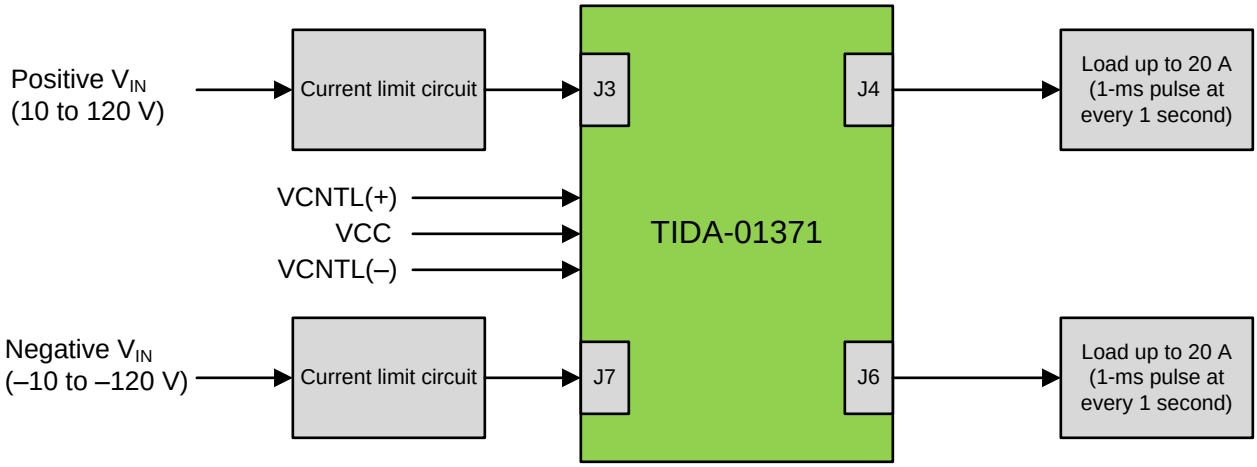


図 23. Test Setup

3.2 Testing and Results

This section shows the test results for the TIDA-01371 design.

3.2.1 Transfer Characteristics

The positive regulator section is operating with respect to a virtual ground. This virtual ground is set using an external control voltage $V_{CNTL(P)}$. 図 24 shows the transfer characteristics for a positive regulator with respect to the control voltage.

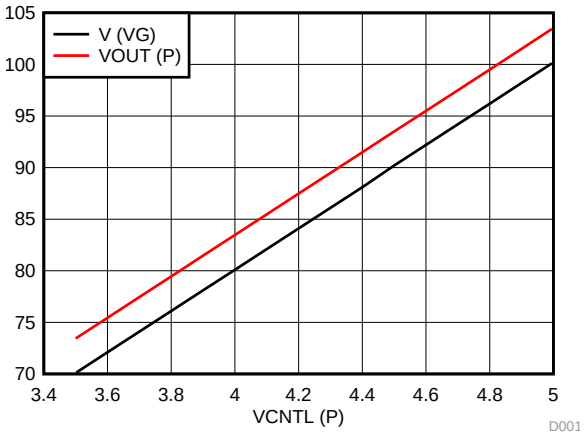


図 24. Transfer Characteristics for Positive Regulator (at Input Voltage of 110 V)

The negative regulator section is operating with respect to a virtual ground. This virtual ground and ultimately the negative output voltage is set using an external control voltage $V_{CNTL(N)}$. 図 25 shows the transfer characteristics for a negative regulator with respect to the control voltage.

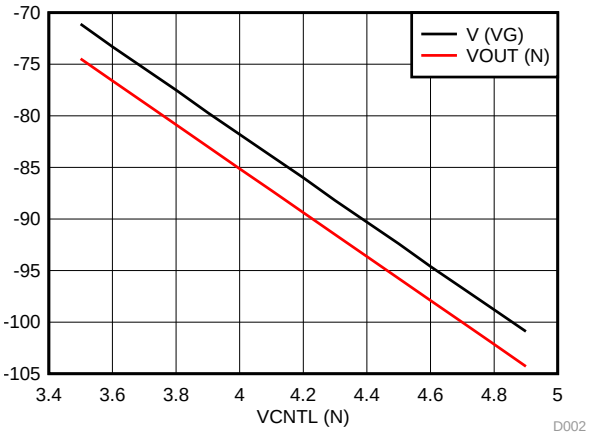


図 25. Transfer Characteristics for Negative Regulator (at Input Voltage of –110 V)

3.2.2 Load Regulation with Pulsed Load

図 26 shows the load regulation waveform for a positive regulator. It shows that the output voltage is constant during the 19-A load step for a 1-ms period. The voltage across input capacitors is falling by 13.5 V, but the output is constant throughout the pulse.

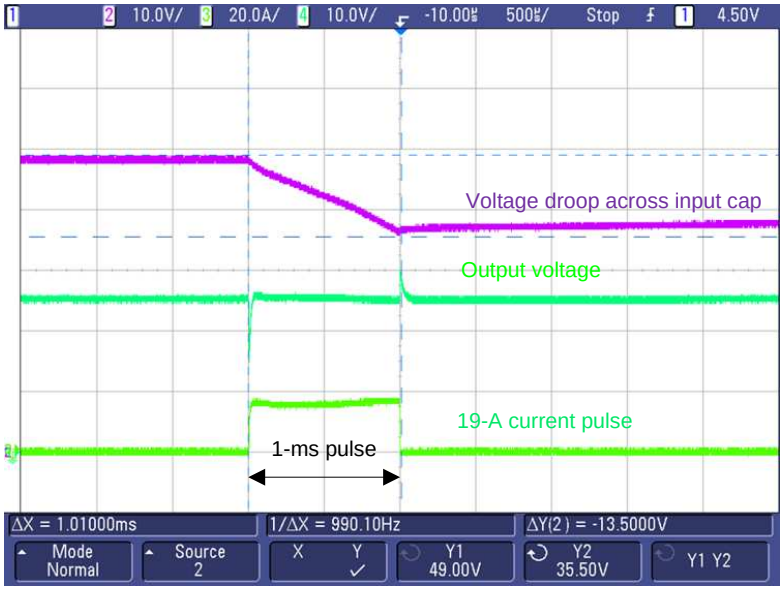


図 26. Load Regulation for Positive Regulator

図 27 shows the load regulation waveform for a negative regulator. It shows that the output voltage is constant during the –20-A load step for a 1-ms period. The voltage across input capacitors is falling by –15 V, but the output is constant throughout the pulse.

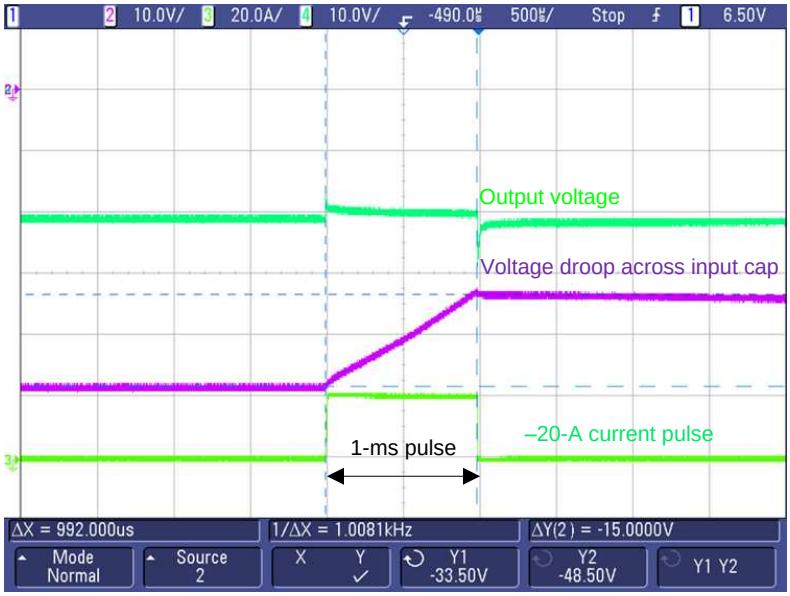


図 27. Load Regulation for Negative Regulator

3.2.3 Load Regulation with Constant Load

図 28 shows the load regulation for the positive and negative regulator together.

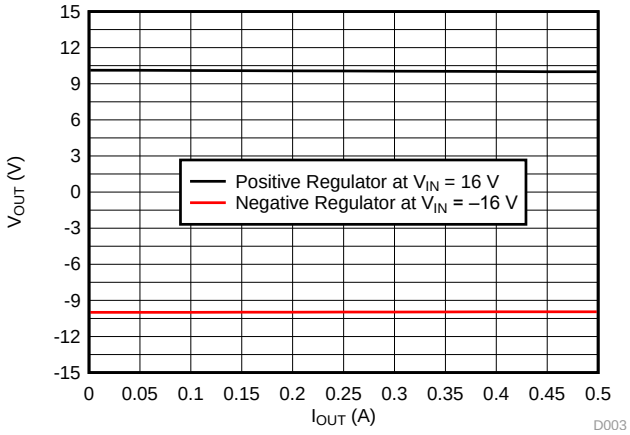


図 28. Load Regulation With Constant Load

3.2.4 Thermal Performance

The CW mode needs a continuous current flow through both the regulator sections at the same time. The TIDA-01371 board is tested for thermal performance with the following conditions:

- $+V_{IN}$ = 15 V
- $+V_{OUT}$ = 10 V at 500 mA
- $–V_{IN}$ = –15 V
- $–V_{OUT}$ = –10 V at 500 mA
- Ambient temperature = 22°C
- Forced cooling = No
- Time after which thermal image is taken (using thermal camera) = 30 minutes

The thermal image for the TIDA-01371 is shown in 図 29.

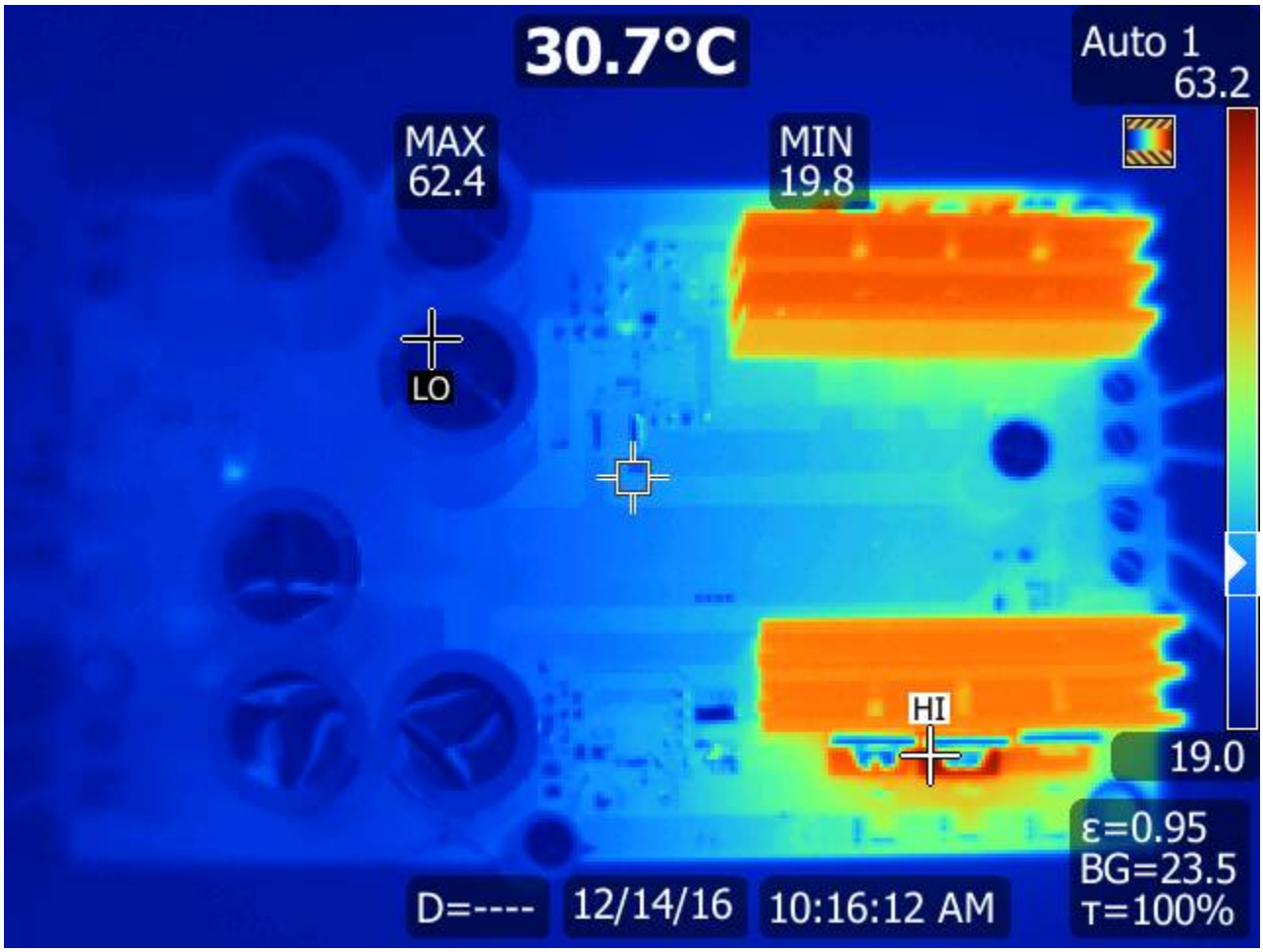


図 29. Thermal Image for TIDA-01371

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01371.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01371.

4.3 PCB Layout Recommendations

Because the design supports high current and high voltage conditions, it is required to have a proper layout. The TIDA-01371 board has four layers: Top, GND, PWR, and bottom.

図 30 and 図 31 show the placement of components near to the two regulators TPS7A4701 and TPS7A3301, respectively. Note the placements of input capacitors, output capacitors, noise rejection capacitors, and feedback resistors as shown in these layout examples.

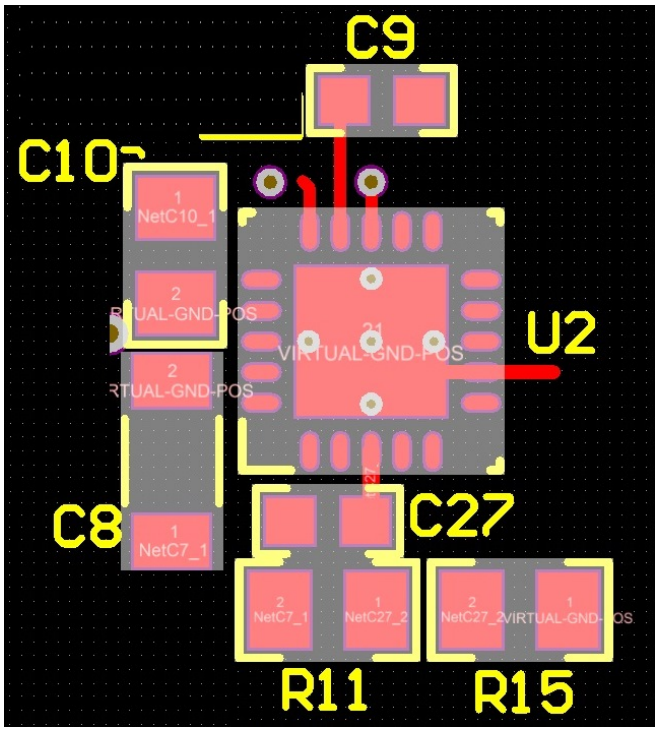


図 30. Placements for TPS7A4701 and Adjacent Components

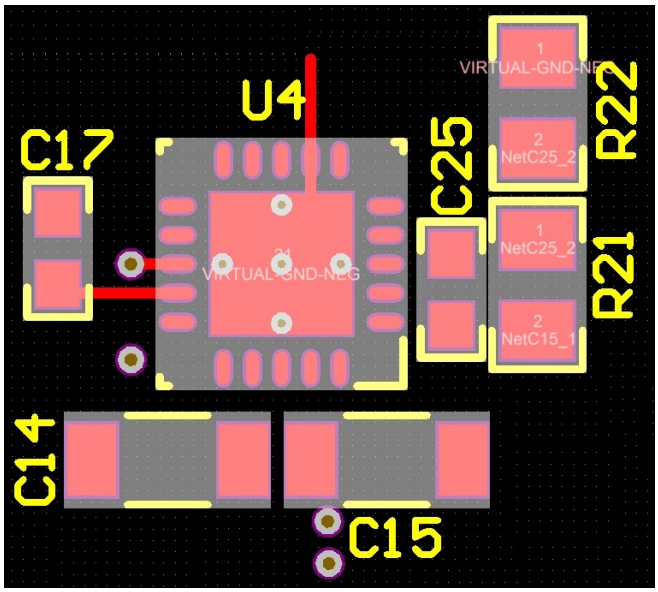


図 31. Placements for TPS7A3301 and Adjacent Components

図 32 and 図 33 show the placement of power MOSFETs and corresponding components like gate resistor, current equalization resistors, and clamping Zener diodes.

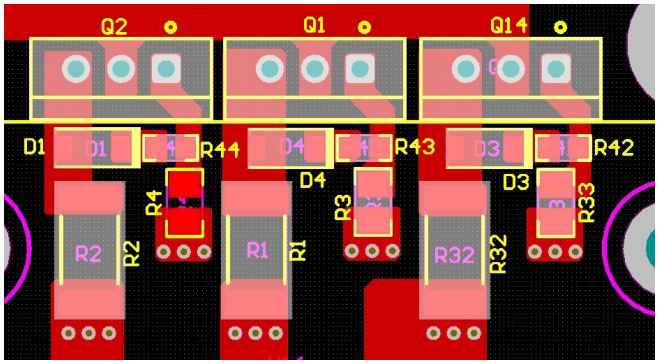


図 32. Placements for MOSFETs and Adjacent Circuits for Positive Regulator

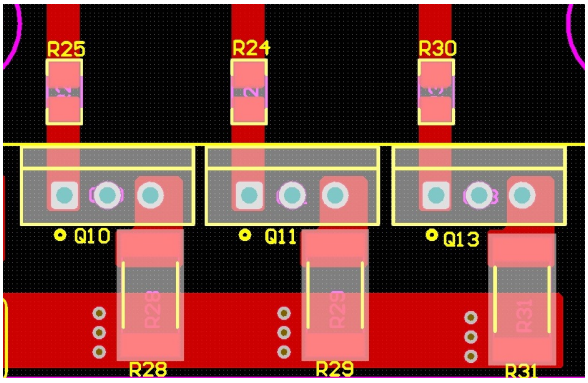


図 33. Placements for MOSFETs and Adjacent Circuits for Negative Regulator

図 34 and 図 35 show the direction of current flow and the layout done according to these directions.

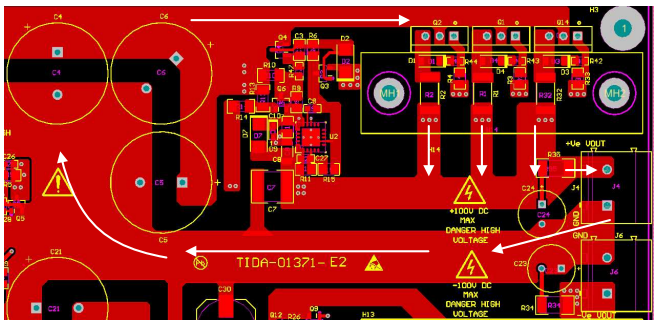


図 34. Current Path for Positive Regulator

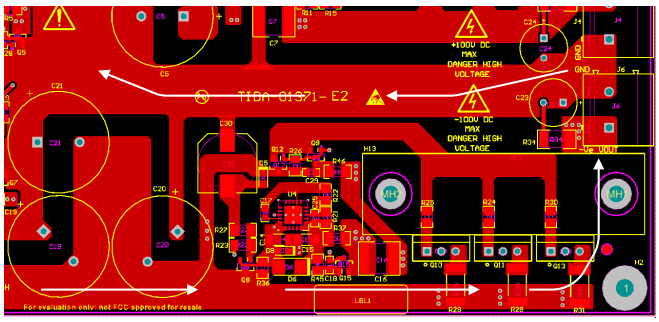


図 35. Current Path for Negative Regulator

図 36 shows how positive input voltage (+VIN) is laid as a plane on all four layers.

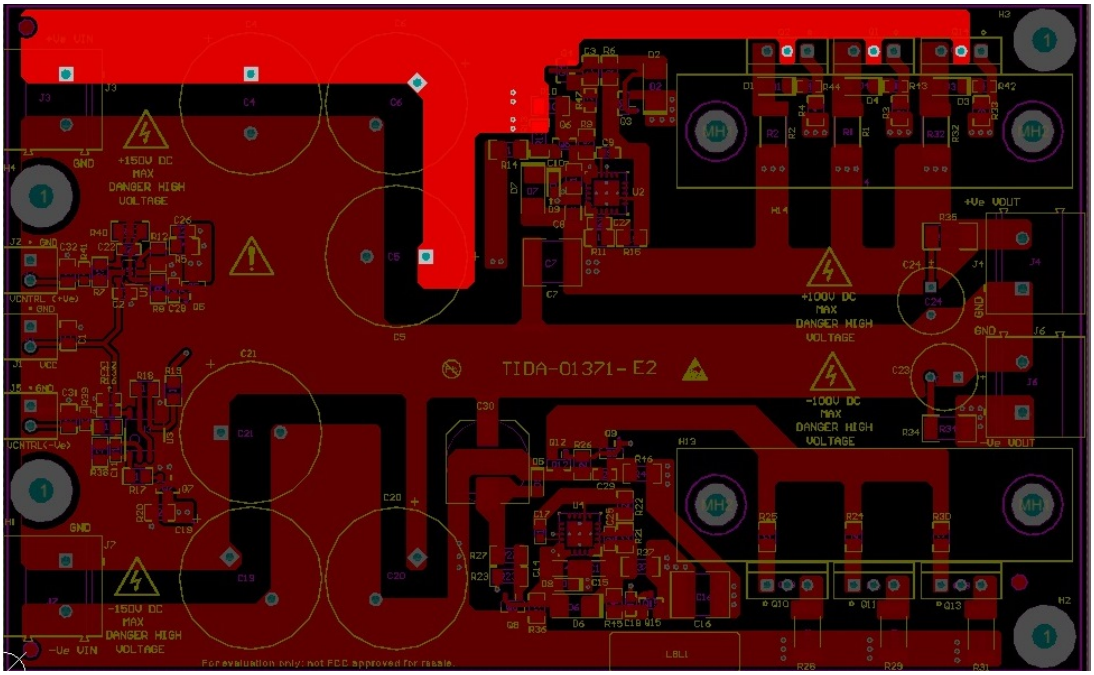


図 36. Layout Showing +VIN Plane

図 37 shows how ground is laid as a plane on all four layers.

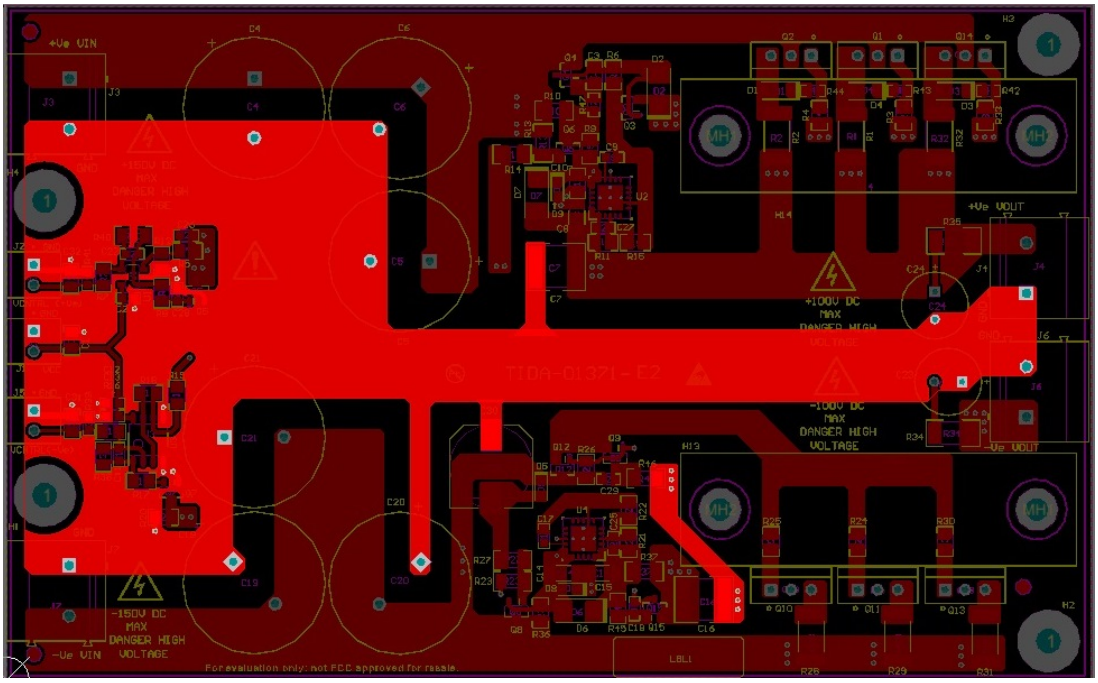


図 37. Layout Showing GND Plane

図 38 shows how negative input voltage (–VIN) is laid as a plane on all four layers.

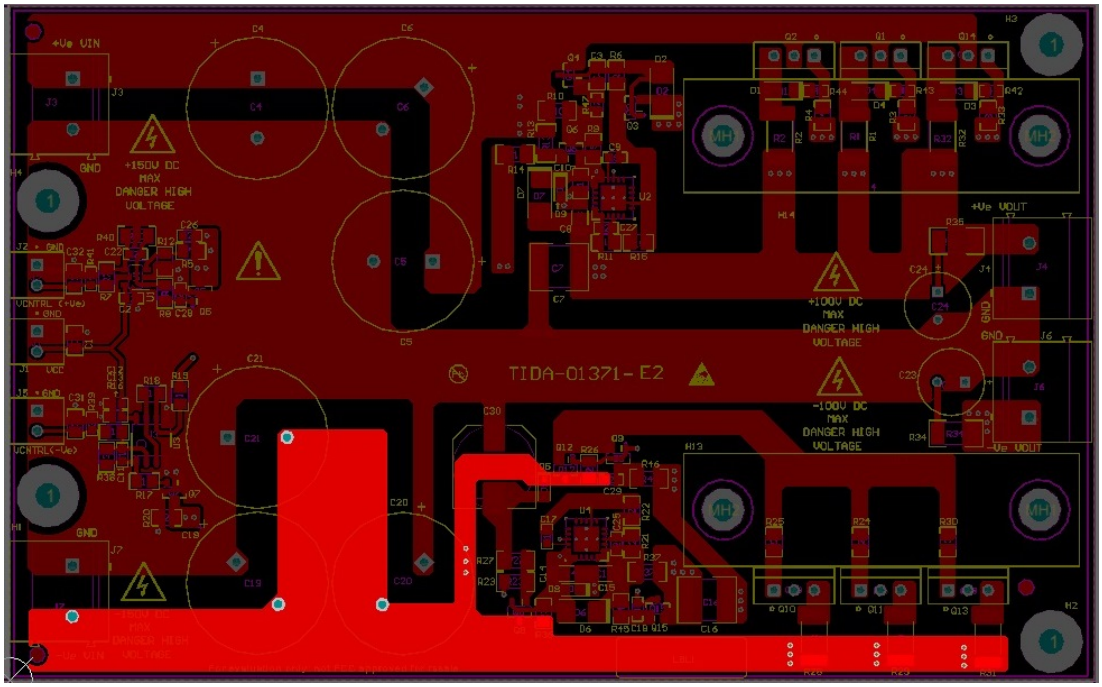


図 38. Layout Showing –VIN Plane

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01371.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01371.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01371.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01371.

5 Related Documentation

1. Texas Instruments, TINA TI Simulation Software (http://www.ti.com/tina-ti)

5.1 商標

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6 Terminology

DAC— Digital-to-analog converter

LDO— Low dropout

SOA— Safe operating area

7 About the Authors

SANJAY PITHADIA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Medical Healthcare and Fitness sector. Sanjay has been with TI since 2008 and has been involved in designing products related to Energy, Smart Grid, Industrial Motor Drives, and Medical Imaging. Sanjay brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Sanjay earned his bachelor of technology in electronics engineering at VJTI, Mumbai.

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年2月発行のものから更新 **Page**

- 現行のデザイン・ガイドのテンプレートに合わせてレイアウトを 変更 1
- 「リソース」にTIDA-01352を 追加 1
- denominator in the C_{OUT} equation from "300" to "20" 変更 4
- title from *Circuit Design* to *System Design Theory* 変更 9
- BJT in *Current Scaling Using External MOSFETs* from Q5 to Q6 変更 12
- *TINA Simulation for Current Sharing* figure 変更 14
- Software Files section 削除 31

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