参考資料

TI Designs: TIDA-01429
CAN向けに前昇圧と後降圧を行う車載用ディスクリートSBCのリファレンス・デザイン

TEXAS INSTRUMENTS

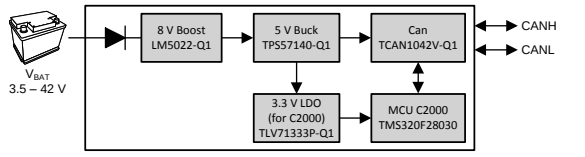
概要

TIDA-01429リファレンス・デザインは、広い入力電圧範囲の昇圧回路を持ち、出力電圧が8Vに設定されているディスクリート・システム・ベース・チップ(SBC)を実装します。昇圧回路の後に、広い入力電圧範囲を持ち、出力電圧が5Vに設定されている降圧コンバータが続き、C2000™マイクロコントローラ(MCU)へ電力を供給するための小型の3.3V固定リニア・ドロップアウト(LDO)レギュレータや、コントローラ・エリア・ネットワーク(CAN)トランシーバなどの駆動に使用されます。このデザインは、500KBPSで動作するCAN通信について、電波暗室(ALSE)法を使用したCISPR 25の放射性エミッション、電圧法を使用したCISPR 25の伝導性エミッション、およびISO 11452-4に従ったバルク電流注入(BCI)耐性のテスト済みです。これは、CANに対応し、電磁適合性（EMC）を検討した3段構造のパワー・ツリーのリファレンス・デザインであり、入力電圧が最小3.5Vの条件下における動作を必要とする多くの車載用アプリケーションで使用できます。

リソース

TIDA-01429	デザイン・フォルダ
LM5022-Q1	プロダクト・フォルダ
TPS57140-Q1	プロダクト・フォルダ
TLV713P-Q1	プロダクト・フォルダ
TMS320F28030Q	プロダクト・フォルダ
TCAN1042V-Q1	プロダクト・フォルダ
SN74LVC2G06-Q1	プロダクト・フォルダ
SN74AHCT1G04-Q1	プロダクト・フォルダ
CSD17313Q2	プロダクト・フォルダ

TI E2E™ Community　E2Eエキスパートに質問

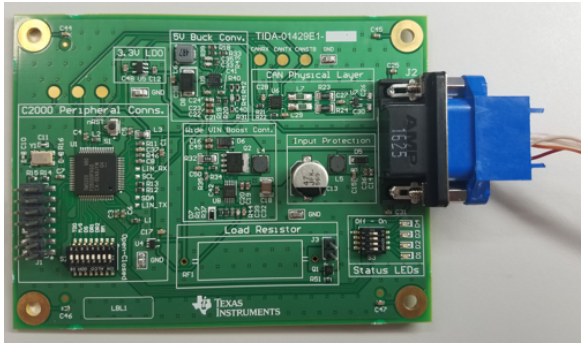


特長

- 広い入力電圧範囲を持つ可変昇圧コントローラ
- 広い入力電圧範囲を持つ可変降圧コントローラ
- 低い入力電圧、3.3V固定のLDO
- 最大5MBPSの柔軟なデータ・レート(FD)に対応できるCANトランシーバ
- ALSE法を使用して、Class 5 CISPR 25の放射性エミッションに合格
- 電圧法を使用して、Class 4 CISPR 25の伝導性エミッションに合格
- ISO 11452-4バルク電流注入に合格
- 最高40Vの負荷ダンプ電圧への耐性
- 最高-40Vのバッテリ逆電圧への耐性
- バッテリ入力電圧が3.5Vまで低下しても、5Vおよび3.3Vのレギュレートされた電源を維持

アプリケーション

- 車載用車両制御モジュール(BCM)
- 車載用フロント・カメラ
- 車載用ヘッド・ユニット



1 System Description

The TIDA-01429 reference design implements a 3-stage power tree. The first stage is a wide-input voltage boost controller with an output voltage set to 8.1 V. When the battery-supplied input voltage is greater than a diode drop above the set output voltage, the boost controller transitions to 0% duty cycle and the input voltage is passed through the high-side Schottky diode. Therefore, the output voltage of the boost controller during regulation will always be 8.1 V or higher. For this reason the second stage 5-V buck converter also needs to be a wide input voltage device. The 5-V supply is used for powering a CAN physical layer interface and a compact, low-input voltage LDO regulator for creating the 3.3-V rail for the C2000 MCU. This design has been tested for CISPR 25 radiated emissions per the ALSE method, CISPR 25 conducted emissions per the voltage method, and for immunity to BCI per ISO 11452-4. All of these EMC tests were performed with CAN communication operating at 500 KBPS. Therefore, this is an EMC-vetted, 3-stage power tree with CAN reference design that can be used in many automotive applications requiring operation with input voltages as low as 3.5 V.

The necessity for multiple regulated supply rails is becoming more and more prevalent in automotive as more MCUs transition from 5 V to 3.3 V. The first-stage boost regulator of this design is strictly used for boosting the input voltage to the buck converter during low-voltage transients for start and stop or cold crank scenarios. During nominal vehicle battery voltages the devices transitions to 0% duty cycle operation and the input voltage is passed to the output through the high-side, Schottky diode. The second stage buck regulator is a 1.5-A wide input voltage buck converter that takes the output from the first stage and regulates it down to 5 V. Lastly, the low-input voltage, 150-mA, fixed 3.3-V LDO is used to supply the MCU.

This reference design is an example implementation of how to create a 8.1-V intermediate supply, a 1.5-A, 5-V supply, and a 150-mA, 3.3-V supply that can handle battery input voltages down to 3.5 V. Example modules where this power topology and CAN interface can be applicable includes BCMs, multi-mode radar modules, front camera modules, and head unit modules. This design passes Class 5 radiated emissions using the ALSE method, Class 4 conducted emissions using the voltage method on both VBATT and GND, and ISO 11452-4 BCI with greater than 106 dBµA of immunity routing VBATT, GND, CANH and CANL through the current injection probe.

An SBC is an integrated circuit (IC) that combines many typical building blocks of a system, which includes transceivers, linear regulators, and switching regulators. While these integrated devices can offer size and cost savings in a number of applications, the integrated devices do not work in every case. For applications where an SBC is not a good fit, it might be beneficial to build a discrete implementation of these aforementioned building blocks thus making a *discrete SBC*.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input power source (VBATT)	Automotive 12-V battery system	2.3.1
Operational input voltage range (VBATT)	3.5 V to 40 V	2.3.2
Survivable input voltage range (VBATT)	-40 V to 40 V	2.3.1

表 **1. Key System Specifications (continued)**

PARAMETER	SPECIFICATIONS	DETAILS
Regulated output voltages	5.0 V and 3.3 V	2.3.2 and 2.3.3
Maximum 5-V load current	1.5 A	2.3.2
Maximum 3.3-V load current	150 mA	2.3.3
Form factor	Rectangular, 4.0" × 3.0" (101.6 mm × 76.2 mm), 2-layer, 1-oz copper foil, printed circuit board (PCB)	3.1.1.1 and 4.3

2 System Overview

2.1 Block Diagram

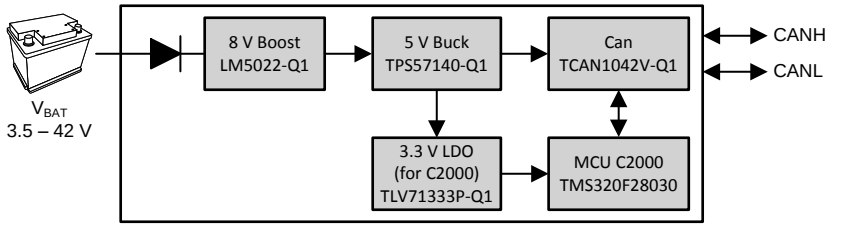


図 1. TIDA-01429 Block Diagram

2.2 Highlighted Products

The TIDA-01429 TI Design features the following eight devices:

1. LM5022-Q1: Automotive, wide-input voltage, non-synchronous, step-up, DC-DC controller
2. TPS57140-Q1: Automotive, wide-input voltage, non-synchronous, step-down, DC-DC converter
3. TLV71333P-Q1: Automotive, low-input voltage, fixed 3.3-V LDO
4. TCAN1042V-Q1: Automotive fault-protected CAN transceiver with CAN FD and IO level shifting
5. TMS320F28030Q: Automotive, high-efficiency 32-bit Piccolo™ MCU
6. SN74LVC2G06-Q1: Automotive, catalog, dual-inverter buffer and driver with open-drain outputs
7. SN74AHCT1G04-Q1: Automotive, 5 V, single inverter gate with transistor-transistor logic (TTL) input thresholds
8. CSD17313Q2: 30-V N-channel, NexFET™ power MOSFET

For more information on each of these devices, see their respective datasheets in 5 or product folders on www.ti.com.

2.2.1 LM5022-Q1

The LM5022-Q1 is a high-voltage, low-side, N-channel MOSFET controller ideal for use in boost and SEPIC regulators. The device contains all of the features needed to implement single-ended primary topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent input voltage feed-forward.

The LM5022-Q1 includes a start-up regulator that operates over a wide-input range of 6 V to 60 V. The pulse width modulation (PWM) controller is designed for high-speed capability, which includes an oscillator frequency range up to 2.2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, line undervoltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, external synchronization capability, and thermal shutdown. The LM5022-Q1 is available in the 10-pin VSSOP package.

図 2 shows a block diagram of the device.

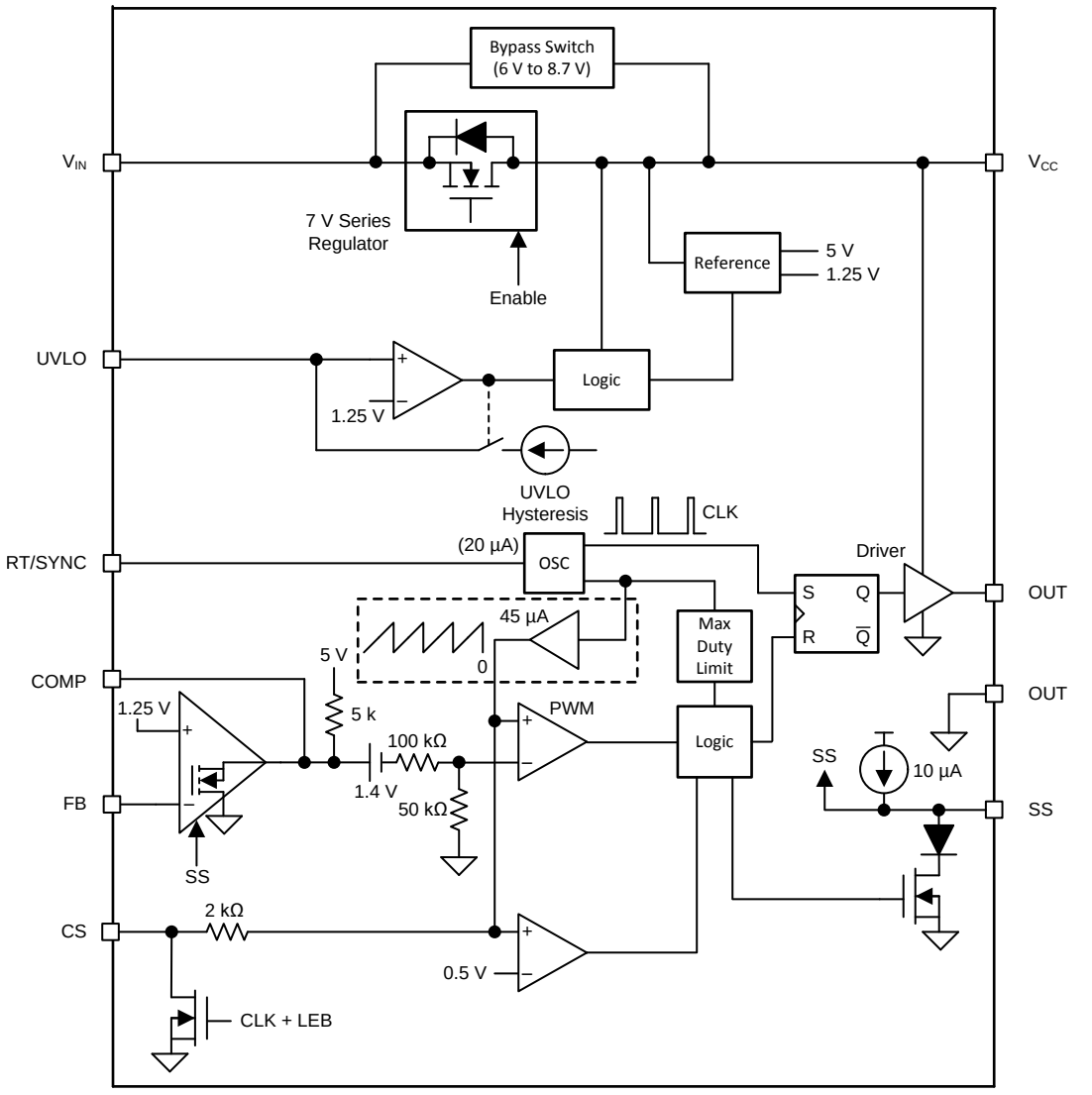


図 2. LM5022-Q1 Block Diagram

Additional features:

- AEC-Q100 grade 1 qualified for automotive applications
- Wide operating input voltage: 6 V to 60 V (down to 3 V after startup)
- 1-A peak MOSFET gate drive current
- Duty cycle limit of 90%
- Single resistor oscillator frequency set
- Adjustable switching frequency up to 2.2 MHz
- External clock synchronization
- Programmable UVLO with hysteresis
- Cycle-by-cycle current limit
- Slope compensation
- Adjustable soft start
- Internal compensation, soft start, current limit, and UVLO
- 10-lead, 3-mm × 3-mm VSSOP Package

2.2.2 TPS57140-Q1

The TPS57140-Q1 device is a 42-V, 1.5-A, step-down regulator with an integrated, high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple, pulse-skip mode reduces the no-load, regulated output supply quiescent current to 116 μA. When the enable pin is in the low state, the shutdown current is reduced to 1.5 μA.

Undervoltage lockout is internally set at 2.5 V but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow-start pin that can also be configured for sequencing or tracking. An open-drain, power-good signal indicates when the output is within 92% to 109% of its nominal voltage. This output can be used for sequencing a second regulator or driving the reset input pin of a MCU.

A wide switching-frequency range allows optimization of efficiency and external component size. Frequency foldback and thermal shutdown protect the part during an overload condition. The TPS57140-Q1 is available in a 10-pin thermally enhanced MSOP-PowerPAD™ package (DGQ) and a 10-pin VSON package (DRC). This design uses the 10-pin leadless VSON package.

図 3 shows a block diagram of the device.

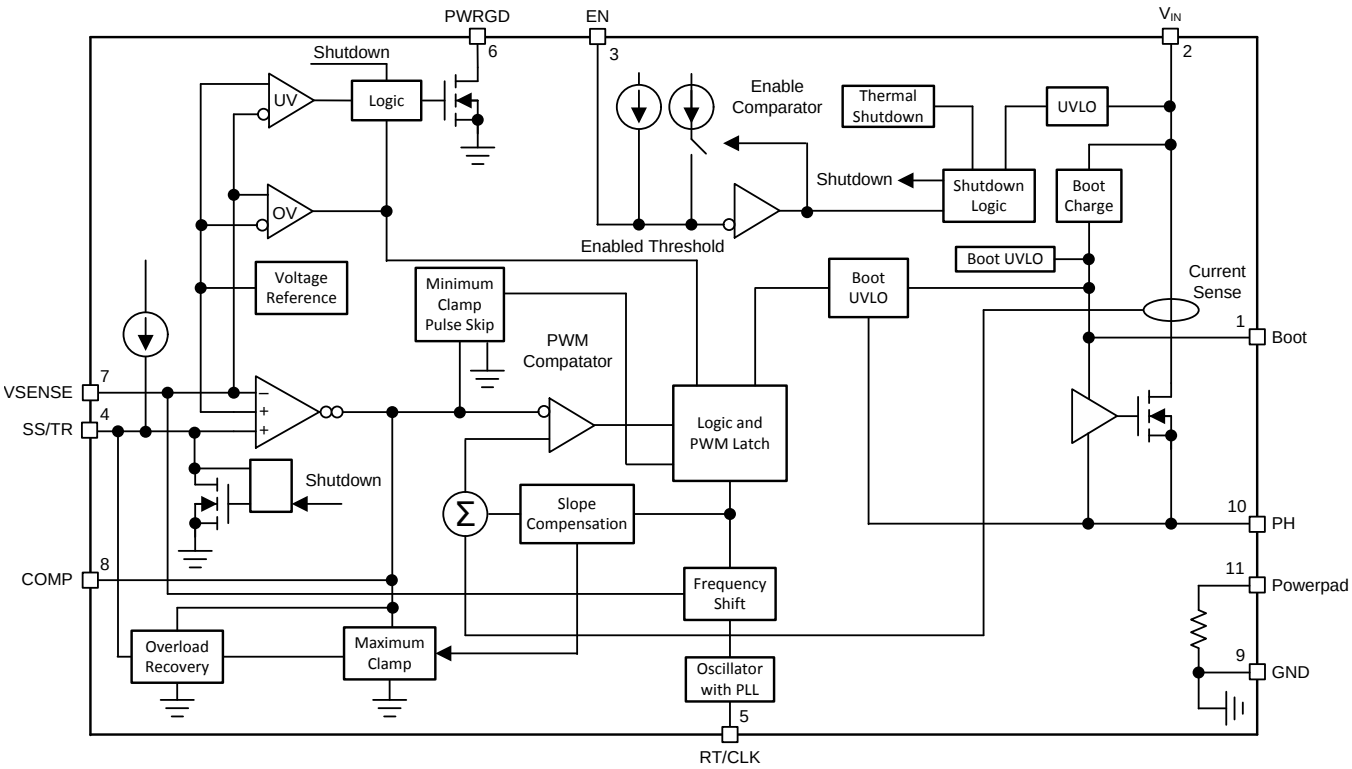


図 3. TPS57140-Q1 Block Diagram

Additional features:

- AEC-Q100 Grade 1 qualified for automotive applications
- 3.5-V to 42-V input voltage range
- 200-mΩ high-side MOSFET
- High efficiency at light loads with pulse-skipping Eco-mode™ control scheme
- 116-μA operating quiescent current
- 1.5-μA shutdown current
- 100-kHz to 2.5-MHz switching frequency
- Synchronizes to external clock
- Adjustable slow start and sequencing
- Undervoltage and overvoltage power-good output
- Adjustable undervoltage lockout voltage and hysteresis
- 0.8-V internal voltage reference
- Available in a 10-pin MSOP-PowerPAD package (DGQ) and a 10-pin VSON package (DRC)

2.2.3 TLV71333P-Q1

The TLV713P-Q1 series of LDO linear regulators are low-quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%. Additionally, the TLV713P-Q1 family of devices are designed to be stable without an output capacitor enabling a very small solution size but remain stable with any output capacitor if one is used.

The TLV713P-Q1 also provides inrush current control during device power-up and enabling. The TLV713P-Q1 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV713P-Q1 series is available in a standard SOT23 5-pin DBV package and provides an active pulldown circuit to quickly discharge output loads. The TLV713P-Q1 is suited for automotive applications with AEC-Q100 grade 1 qualification.

図 4 shows a block diagram of the device.

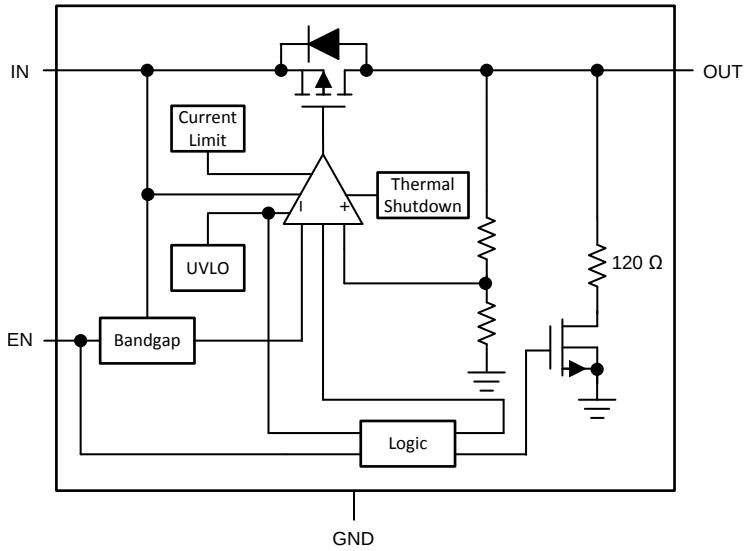


図 4. TLV713P-Q1 Block Diagram

Additional features:

- AEC-Q100 Grade 1 qualified for automotive applications
- Input voltage range up to 5.5 V
- Stable operation with or without capacitors
- Frequency foldback and overcurrent protection
- Very low dropout: 230 mV at 150 mA
- Accuracy: 1%
- Low IQ: 50 µA
- Available in fixed-output voltages from 1 V to 3.3 V
- High PSRR: 65 dB at 1 kHz
- Active output discharge
- Available in a 5-pin SOT-23 package (DBV)

2.2.4 TCAN1042V-Q1

This TCAN1042 family is a CAN transceiver family that meets the ISO11898-2 (2016) high-speed CAN physical layer standard. All devices are designed for use in CAN FD networks up to 2 Mbps . Devices with part numbers that include the *G* suffix are designed for data rates up to 5 Mbps, and versions with the *V* suffix have a secondary power supply input for IO level shifting the input pin thresholds and RXD output level. This family has a low power standby mode with remote wake request feature. Additionally, all devices include protection features to enhance device and network robustness including a TXD dominant state timeout, thermal shutdown, undervoltage lockout, short circuit current limiting, and internal pull ups for critical floating input terminals.

図 5 shows a block diagram of the device.

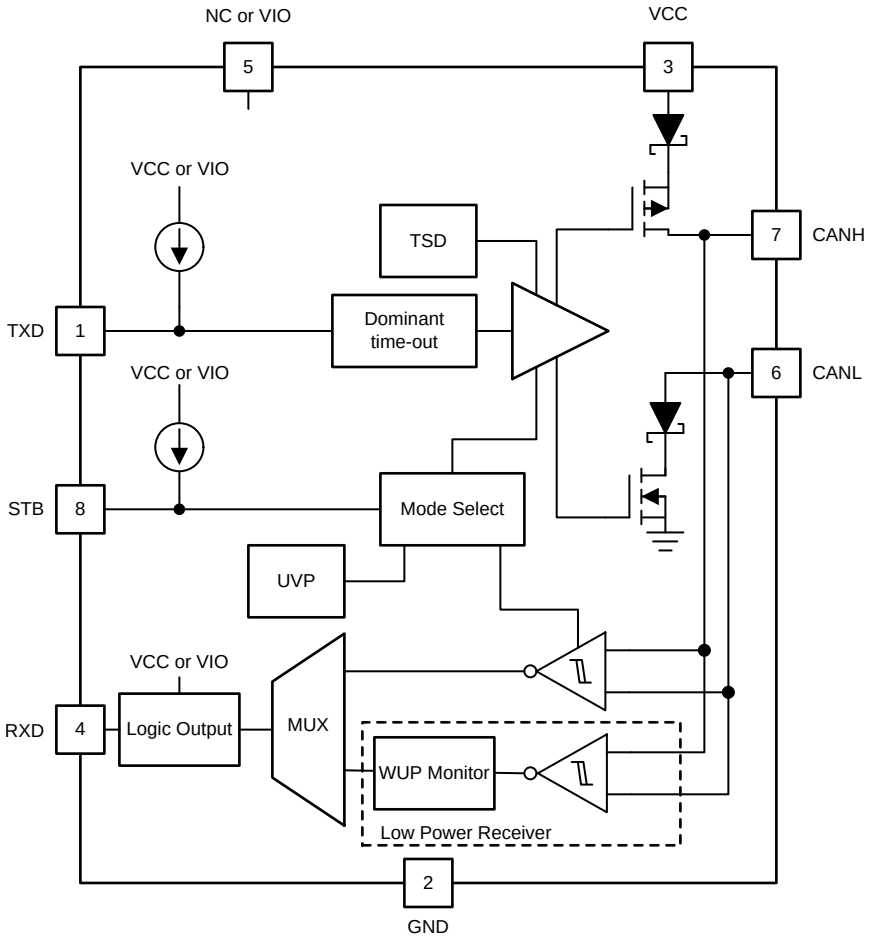


図 5. TCAN1042-Q1 Family Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- All devices support classic CAN and 2 Mbps CAN FD and *G* versions support 5 Mbps
- Short and symmetrical propagation delay times and fast-loop times for enhanced timing margin
- IO voltage range supports 3.3-V and 5-V MCUs
- Ideal passive behavior when unpowered
- IEC ESD protection up to ±15 kV
- Bus fault protection: ±58 V (non-H variants) and ±70 V (H variants)
- Undervoltage protection on V_{CC} and V_{IO} (V variants only) supply terminals
- Driver dominant time out (TXD DTO) supporting data rates down to 10 kbps
- Thermal shutdown protection (TSD)
- Receiver common mode input voltage: ±30 V
- Typical loop delay: 110 ns
- Junction temperatures from –55°C to 150°C

- Available in SOIC(8) package and leadless VSON(8) package (3.0 mm × 3.0 mm) with automated optical inspection (AOI) capability

2.2.5 TMS320F28030PAGQ

The F2803x Piccolo family of MCUs provide the power of the C28x core and control law accelerator (CLA) coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed, full-scale range and supports ratio-metric VREFHI and VREFLO references.

図 6 shows a block diagram of the device.

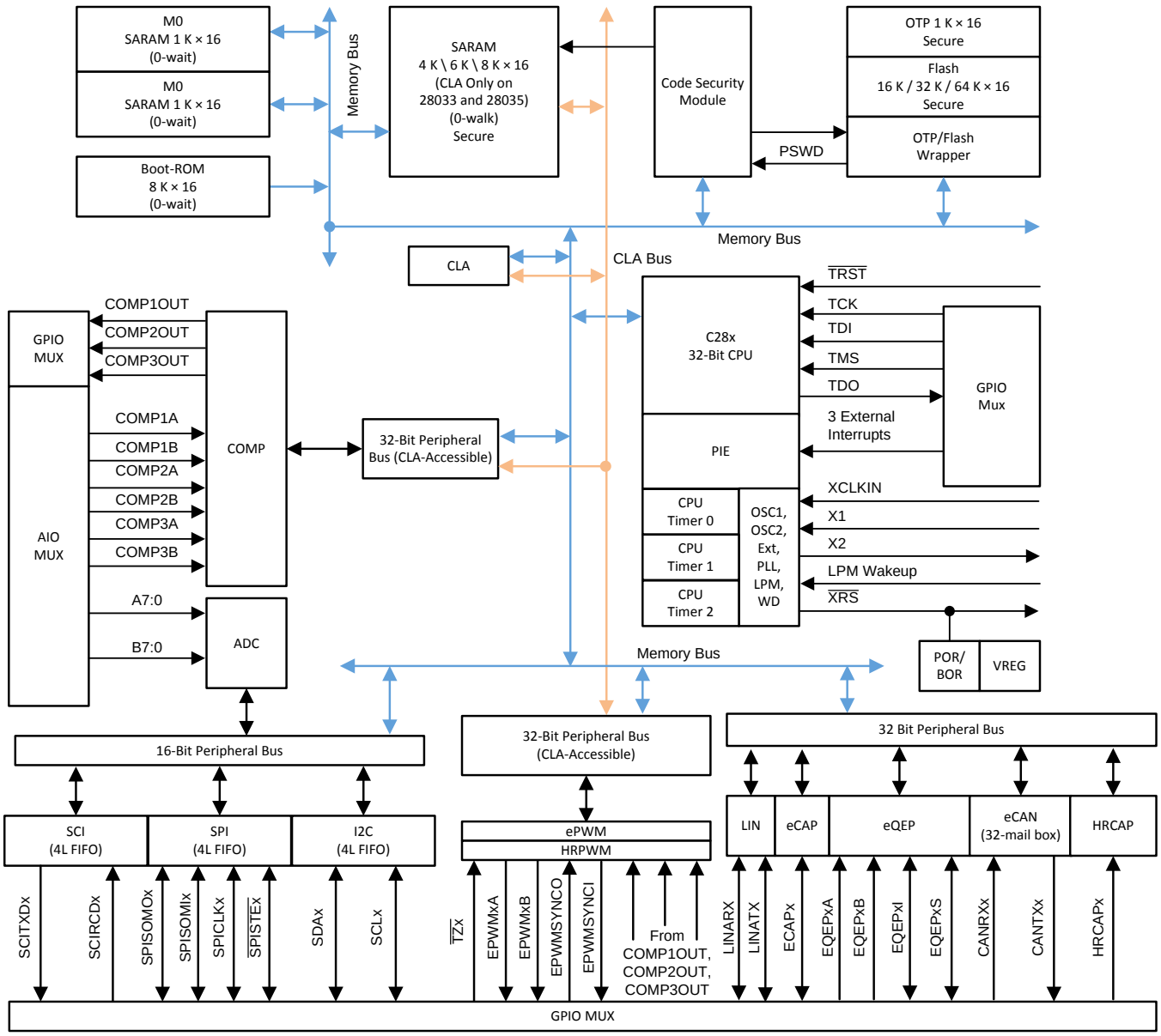


図 6. TMS320F28030PAGQ Block Diagram

- 60 MHz, 32-bit, floating-point, high-efficiency, CPU (TMS320C28x)
- 128-bit security key and lock
- Single, 3.3-V supply with no power sequencing requirement
- Integrated power-on reset and brown-out reset
- Clocking: two internal zero-pin oscillators, on-chip crystal oscillator, and external clock input
- Up to 45 individually programmable, multiplexed GPIO pins with input filtering
- Peripheral interrupt expansion (PIE) block that supports all peripheral interrupts
- Three 32-bit CPU timers and a watchdog timer module
- On-chip Flash, SARAM, OTP, and boot ROM available
- Serial port peripherals:
  - One serial communications interface (SCI) universal asynchronous receiver/transmitter (UART) module
  - Two serial peripheral interface (SPI) modules
  - One inter-integrated-circuit (I2C) module
  - One local interconnect network (LIN) module
  - One enhanced controller area network (eCAN) module
- Enhanced control peripherals
  - ePWM
  - High-resolution PWM (HRPWM)
  - Enhanced capture (eCAP) module
  - High-resolution input capture (HRCAP) module
  - Enhanced quadrature encoder pulse (eQEP) module
  - Analog-to-digital converter (ADC)
  - On-chip temperature sensor
  - On-chip comparator
- Available in 56-pin VQFN, 64-pin TQFP. and 80-pin LQFP packages

2.2.6 SN74LVC2G06-Q1

The SN74LVC2G06-Q1 is a dual-inverter buffer and driver IC that is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC2G06-Q1 device has two open-drain outputs that can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA per output. This device is fully specified for partial-power-down applications using I_{off} circuitry. The I_{off} circuitry disables the outputs preventing damaging backflow current through the device when the device is powered down but voltage remains on the output (or outputs).

図 7 shows a block diagram of the device.

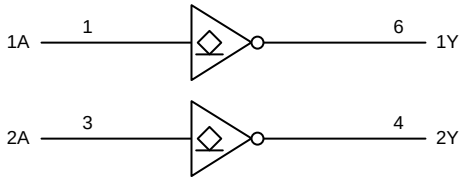


図 7. SN74LVC2G06-Q1 Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- Supports 1.65-V to 5.5-V V_{CC} operation
- Max t_{pd} of 3.4 ns at 3.3 V
- Low power consumption, 10-µA maximum
- ±24 mA output drive at 3.3 V
- Inputs and open-drain outputs accept voltages up to 5.5 V
- ESD Protection exceeds 2-kV human-body model, 200-V machine model, and 1-kV charged-device model

2.2.7 SN74AHCT1G04-Q1

The SN74AHCT1G04-Q1 is an automotive qualified single inverter gate with TTL input threshold that comes in a 5-pin SC70 package.

図 8 shows a block diagram of the device.

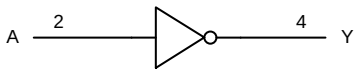


図 8. SN74AHCT1G04-Q1 Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- Operating range of 4.5 V to 5.5 V
- Maximum t_{pd} of 7.5 ns at 5 V
- Low power consumption—10 µA maximum I_{CC}
- ±8-mA output current drive at 5 V
- TTL input thresholds
- Available in a SOT SC-70 package (DCK)

2.2.8 CSD17313Q2

The CSD17313Q2 is a 30-V, 24-mΩ, 2-mm × 2-mm SON package NexFET power MOSFET device designed to minimize losses in power conversion applications. The 2-mm × 2-mm SON offers excellent thermal performance for the size of the package.

図 9 shows a block diagram of the device.

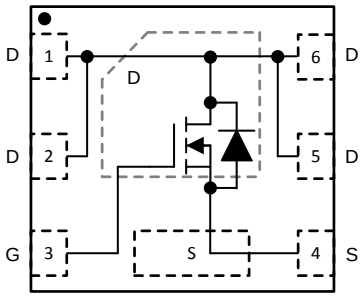


図 9. CSD17313Q2 Block Diagram

Additional features:

- 30 V VDS drain-to-source voltage
- Ultra-low Qg and Qgd
- Low-thermal resistance
- Pb-free, halogen-free, and RoHS compliant
- 1.3-V input threshold voltage
- 31-mΩ drain-to-source on resistance at V_{GS} of 3 V
- SON 2-mm × 2-mm plastic package

2.3 System Design Theory

BCMs, gateway modules, side mirror replacement modules, and head unit modules are all composed of several sub-circuits. This design covers the battery input, voltage regulation, and CAN portions of these applications. The following subsections cover the component selection and device configuration decisions for this design.

2.3.1 Supply Protection and Filtering

図 10 shows the portion of the schematic that has the reverse battery input protection diode, input capacitors, and pi filter components.

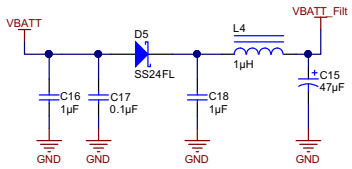


図 10. Supply Protection and Filtering Circuitry

Diode D5 is a 40-V Schottky diode for protection against reverse battery conditions. Due to the wide-input voltage tolerant inputs of the LM5022-Q1 and the TPS57140-Q1 in conjunction with the reverse blocking Schottky diode the design can handle from –40 V to 40 V on the VBATT input supply.

Capacitors C16 and C17 are used for input transient filtering, and the pi filter (composed of C18, L4, and C15) can be used to implement a two-pole, low-pass filter for conducted emissions. Input capacitors C16 and C17, pi filter components C18, and C15 were left unpopulated, and a 0-Ω shunt was placed across the inductor for the evaluation of this design.

Lastly, the VBATT net is directly tied to pin 9 of the external D-subminiature (D-sub) connector J6 as shown in 2.3.6.

図 11 shows a snippet of the battery filtering and reverse voltage protection portion of the PCB.

図 11. Battery Filtering and Protection PCB Snippet

2.3.2 Wide-Input Voltage Boost Controller

図 12 shows the portion of the TIDA-01429 schematic with the LM5022-Q1 and all of its supporting circuitry.

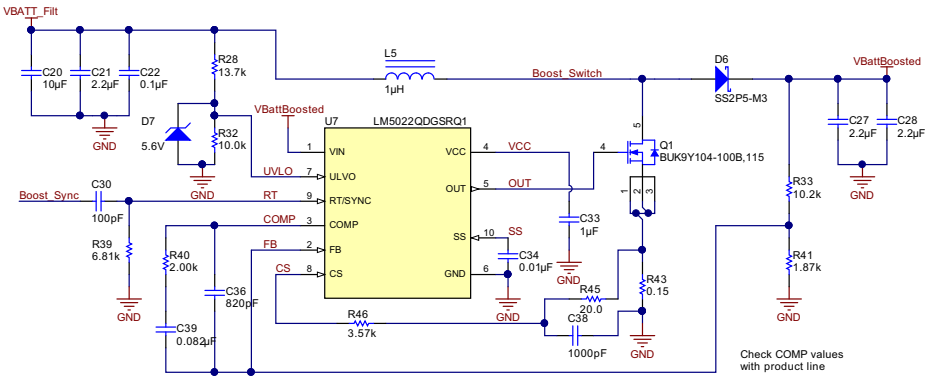


図 12. LM5022-Q1 Non-Synchronous Boost Controller Circuitry

- UVLO pin: The UVLO pin of the LM5022-Q1 is able to handle voltages up 7 V and has a typical shutdown threshold of 1.25 V. Due to the desired wide-input voltage operation of this design (3 V up to 40 V), a voltage divider with an additional Zener diode clamp was implemented. R28 and R32 create a 0.42:1 input voltage ratio, which means the UVLO pin will detect nominally 42% of the VBATT_Filt voltage. Additionally, when the VBATT_Filt voltage rises above 13 V, the Zener diode (D7) begins to clamp this voltage to protect the pin.
- VIN pin: The VIN pin supplies the internal logic of the device and is the source for the internal VCC

regulator, which supplies the integrated gate driver of the device. This pin has nominal UVLO threshold of 5 V. This threshold means that if the VBATT_Filt voltage was fed directly to the VIN pin of the regulator, the device would undervoltage and shut off when VBATT_Filt dropped below 5 V. To enable the device to operate all the way down to 3 V on VBATT_Filt the VIN pin was supplied using the VBATT_Boosted output voltage (nominally 8.1 V). The caveat to this approach is that the device will startup at a diode drop higher voltage (due to D6) later than if the VIN pin was directly supplied by VBATT_Filt. The benefit to this solution that no extra components are needed and the regulator can continue to operate down to input voltages to 3 V instead of just 5 V.

- RT/SYNC pin: External resistor R39 sets the switching frequency of the LM5022-Q1. Using a 6.98-kΩ resistor set the nominal switching frequency to 2.07 MHz, which is above the AM band frequency range. Additionally, C30 can be used to capacitively couple an external clock to this pin for external clock synchronization. This pin can be used if a user desires synchronizing multiple switching supplies to the same frequency, therefore, avoiding beat frequencies due to slightly mismatched regulator switching frequencies. See 2.3.11 for more information on the clock synchronization signal. The design was evaluated with just the 6.98-kΩ resistor to GND setting the switching frequency of the LM5022-Q1.
- FB pin: Resistors R33 and R41 were used to set the output voltage of the LM5022-Q1. The internal error amplifier has a typical threshold voltage of 1.25 V. These resistors result in a nominal output voltage of 8.07 V.
- SS pin: An external capacitor on the SS pin can be used to set the period of time where the power converter gradually turns on. This pin can be used to reduce turn on power surges on the input rail. The pin has a nominal 10-µA current source with a 550-mV input threshold. A capacitor value of 10 nF was used to create a 550-µs soft-start time.
- CS pin: Sense resistor R43, low-pass filter R45 and C38, and series sense resistor R46 are used to set the overcurrent threshold and filtering. A sense resistor value of 150 mΩ was used to set a steady state inductor current limit of 3.3 A.
- Output diode: A low-forward voltage drop Schottky diode was used to limit the power losses in the output diode of the boost regulator. D6 is a 50-V, 2-A diode in a DO-220AA package.
- Input capacitors, output capacitors, compensation network, FET selection, and inductor selection were made using the *Detailed Design Procedure* section of the *LM5022-Q1 2.2MHz, 60 V Low-Side Controller For Boost and SEPIC*[1] datasheet. See 5 for a link to the datasheet.

The LM5022-Q1 is a non-synchronous boost controller with external FET and diode. This enables a scalable design at the tradeoff of a larger solution size. The total PCB solution size on the TIDA-01429 for the LM5022-Q1 and all of its supporting circuitry is 17.78 mm × 20.32 mm (700 mils × 800 mils).

図 13 shows a snippet of the boost controller portion of the PCB.

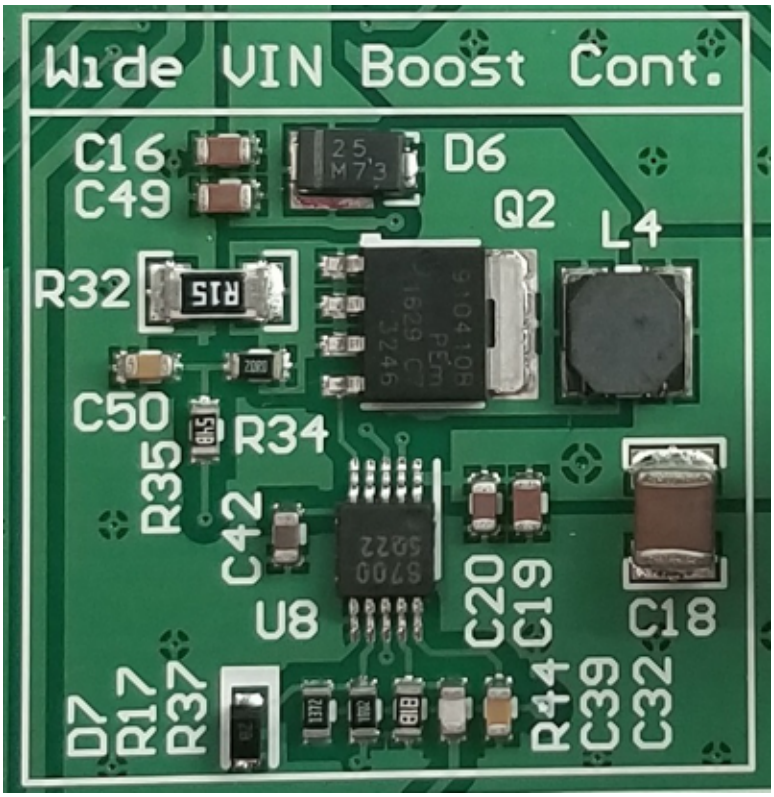


図 13. LM5022-Q1 Boost Controller Circuitry on PCB

Lastly, the LM5022-Q1 is able to handle input voltages as low as 3 V after startup. Due to the series Schottky diode drop on the input battery connection of up to 0.5 V for reverse battery protection, the module is able to handle input voltages as low as 3.5 V after startup and remain in regulation.

2.3.3 Wide Input Voltage Buck Converter

図 14 shows the portion of the TIDA-01429 schematic with the TPS57140-Q1 and all of it's supporting circuitry.

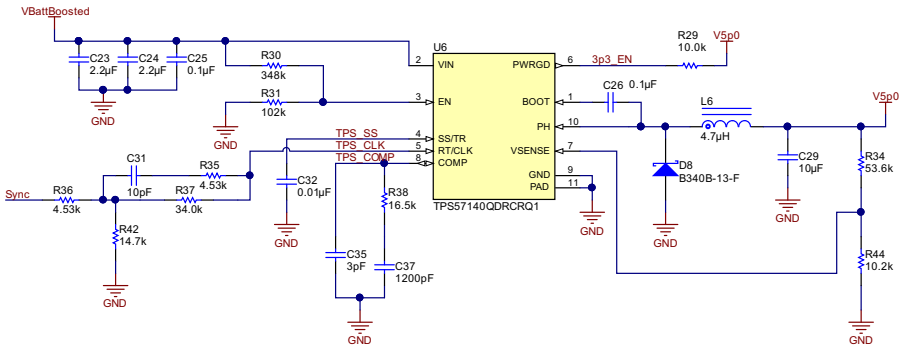


図 14. TPS57140-Q1 Non-Synchronous Buck Converter Circuitry

- EN pin: For low-impedance input voltages the EN pin is only rated for a maximum input voltage of 5 V, but if the input voltage will not source more than 100 µA, the 5-V maximum rating can be exceeded. Therefore, a high-impedance, resistive voltage divider is placed on the EN pin. R30 ensures that the

input current on the EN pin stays below 100 µA for voltages up to 40 V. If a higher load dump voltage is desired, this resistor value can be increased allowing load dump input voltage up to 47 V because the LM5022-Q1 can handle up to 60 V.

- PWRGD pin: The PWRGD pin is used to enable the subsequent 3.3-V LDO that is supplied by the output voltage of the TPS57140-Q1. This pin is an open-drain output that is placed in a high-impedance state when the output voltage is between 94% and 107% of the set output voltage. Resistor R29 is used to pull the output high when the pin is in a high-impedance state.
- SS/TR pin: A capacitor placed between this pin and ground sets the slow start time of the regulator. Once the output capacitance, output voltage, and desired in-rush current is known, a soft-start time can be calculated. For this design a soft-start time of 3 ms was chosen, which results in a 9.38-nF capacitor. This value was rounded up to the standard value of 10 nF.
- VSENSE pin: The pin has a nominal voltage reference value of 0.8 V. External resistors R34 and R44 are used to create a voltage divider with the top node of the divider (output voltage) set to 5 V.
- Output capacitance, inductor, catch diode, and compensation network component selections were made using the formulas found in the *Detailed Design Procedure* section of the *TPS57140-Q1 1.5-A 42-V Step-Down DC-DC Converter With Eco-mode™ Control*[2] datasheet.

The TPS57140-Q1 is a non-synchronous buck converter with integrated, high-side FET, which enables a smaller PCB solution size. The total PCB solution size on the TIDA-01429 for the TPS57140-Q1 and all of its supporting circuitry is 15.75 mm × 17.0 mm (620 mils × 670 mils). 図 15 shows a snippet of the buck converter portion of the PCB.

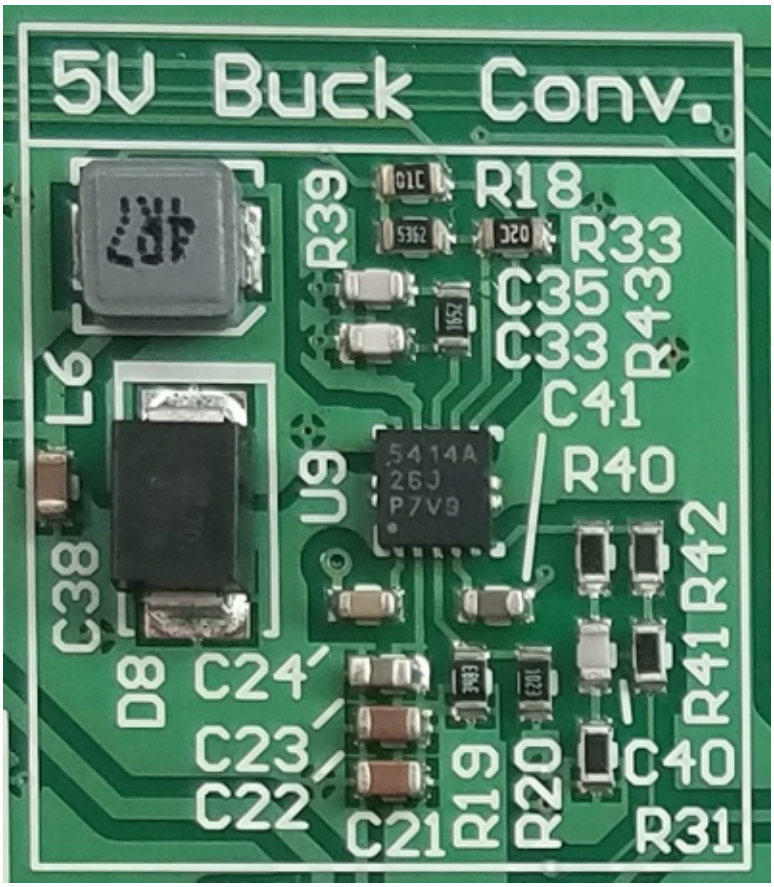


図 15. TPS57140-Q1 Buck Converter Circuitry on PCB

2.3.4 Low-Input, Voltage Fixed 3.3-V LDO

図 16 shows the portion of the schematic with the TL71333P-Q1 and its input and output capacitors.

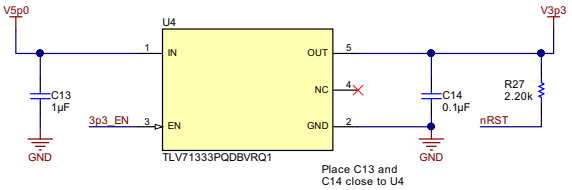


図 16. TLV71333P-Q1 3.3-V LDO Circuitry

Although the TLV713P-Q1 family of LDOs can be used without input and output capacitors, for best transient results a 1-µF capacitor was placed in the input node (C13) and a 0.1-µF capacitor was placed on the output node (C14) per datasheet recommendations.

The TLV71333-Q is a linear drop-out regulator with integrated pass FET enabling a very small solution size. The total PCB solution size on the TIDA-01429 for the TLV71333P-Q1 with the input and output capacitors is 7.75 mm × 3.18 mm (305 mils × 125 mils). 図 17 shows a snippet of the boost controller portion of the PCB.

図 17. TLV71333P-Q1 LDO Circuitry on PCB

2.3.5 CAN Physical Layer

図 18 shows the potion of the schematic with the CAN physical layer, which includes the CAN transceiver, filtering common mode choke (CMC), filtering capacitors, Electro-Static Discharge (ESD) protection IC, and termination components.

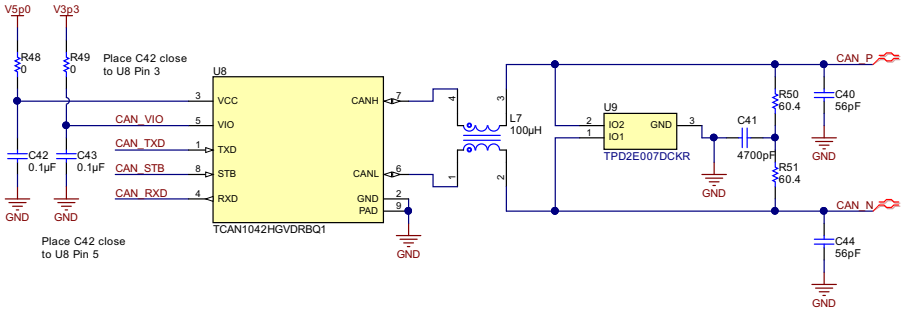


図 18. TCAN1042V-Q1 CAN Physical Layer Circuitry

- Transceiver U8: The TCAN1042 family comes in both an 8-pin, SOIC package and a small 3-mm × 3-mm, leadless, DFN package. For this design, the small DFN package was used.
- CMC L7: A standard CMC footprint was added to the CANH and CANL bus lines, so the design could easily be evaluated with a variety of CMCs. However, the design was evaluated without the CMC, and instead, two series 0-Ω resistors were populated in place of the choke.
- ESD IC U9: A common footprint dual-channel, bidirectional ESD protection IC was placed for optional, additional protection of the CANH and CANL bus lines. However, the design was evaluated with U9 unpopulated.
- Termination components R50, R51, and C41: These components are used for terminating the CAN bus with a split termination. This technique uses two resistors that are equal to one half the characteristic impedance of the cable (typically 120 Ω) with a capacitor placed to ground between the two resistors. This creates two low-pass filters on the CANH bus lines and the CANL bus line for filtering common mode noise. If standard termination is desired, capacitor C41 can be left open.
- Filtering capacitors C40 and C44: These capacitors are place from CANH to GND and CANL to GND to help filter high-frequency transients and noise from getting into or out of the module.

shows a snippet of the CAN physical layer portion of the PCB.

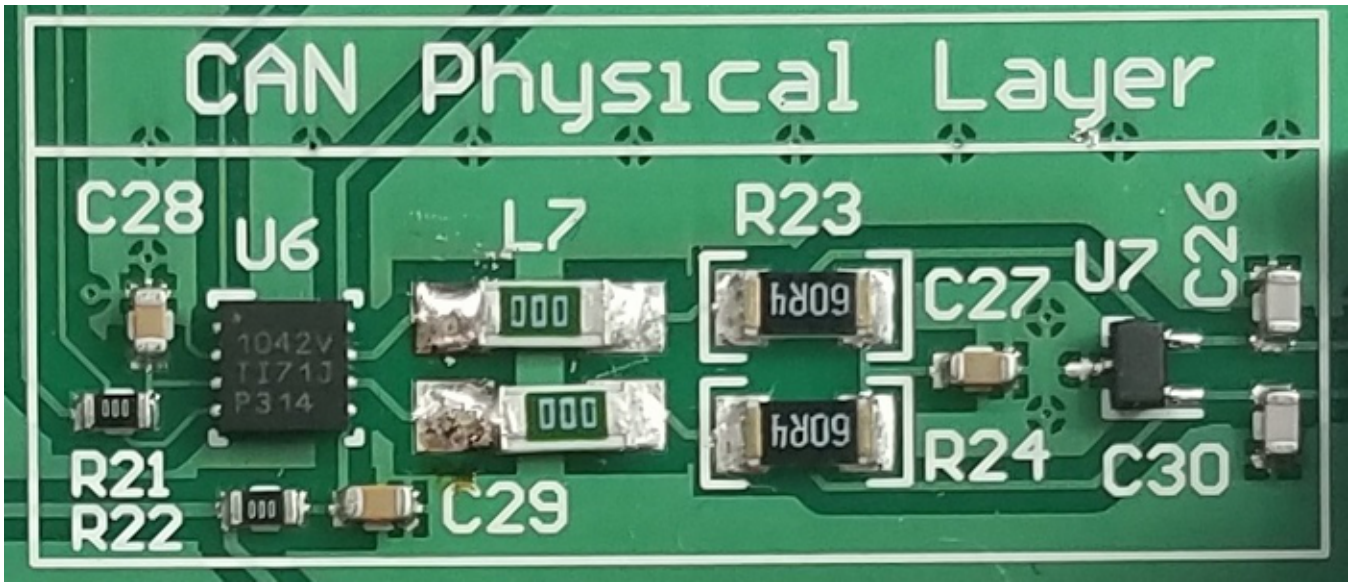


図 19. CAN Physical Layer Circuitry on PCB

2.3.6 External Power and Networking Connections

図 20 shows the external connector which includes the VBATT input, GND connection and the CANH and CANL connections. The pinout used for the D-sub 9 connector is the recommended pinout by CAN in automation (CiA) document DIN 41652. 図 20 shows the pinout for both the female D-sub 9 connectors that were populated on the boards and the male connectors that were used for creating the wire harness.

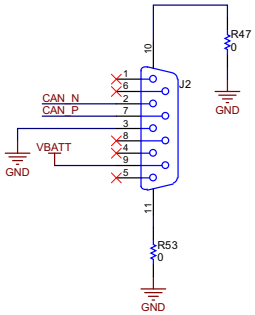


図 20. External Connector Pinout

図 21 shows the external connector on the TIDA-01429 PCB.

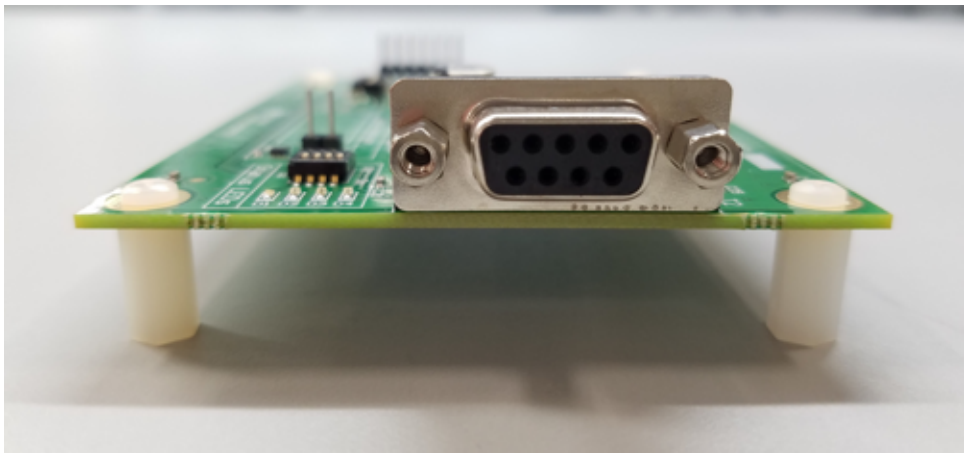


図 21. External Connector for Power and CAN on PCB

2.3.7 Electronically-Controlled Dummy Load

図 22 shows the dummy load resistor and external circuitry that was used to help further evaluate the 5-V buck regulator. A 3-W, 10-Ω resistor was used for the dummy load, which results in an additional load current when active on the buck regulator's output of 500 mA. This was used to evaluate the load step transient response of the TPS57140-Q1 buck converter.

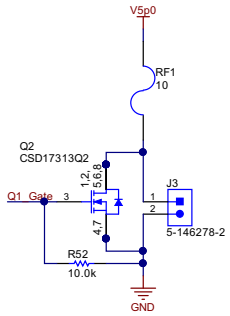


図 22. Dummy Load Circuitry

- J3: The two-pin, 100-mil header can be used for manually enabling and disabling the dummy load by placing a shunt across the pins.
- Q1: Additionally, the dummy load can be electronically controlled via GPIO24 (pin 64) of the TMS320F28030Q device. GPIO24 is tied to the gate connection of Q1 to enable and disable the load. Q1 is a 30-V, N-Channel, NexFET™ power MOSFET.
- R52: Resistor R52 is placed between the gate and source of Q1 ensures that the gate voltage is pulled low when the GPIO24 of the C2000 is in the high-impedance state.

GPIO24 and Q1 were used to evaluate the load-step response oscilloscope shots were taken in 3.2.

図 23 shows the dummy load resistor portion of the PCB.

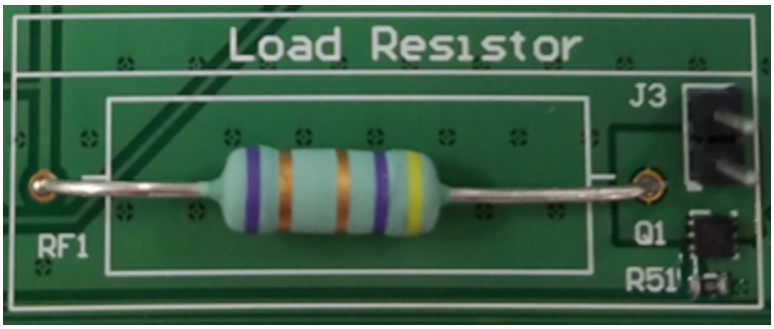


図 23. Dummy Load Resistor Circuitry on PCB

2.3.8 Status LEDs

Four status LEDs have been added to the design for ease of evaluation and monitoring during electro-magnetic compliance (EMC) testing. 図 24 shows the status LED portion of the schematic.

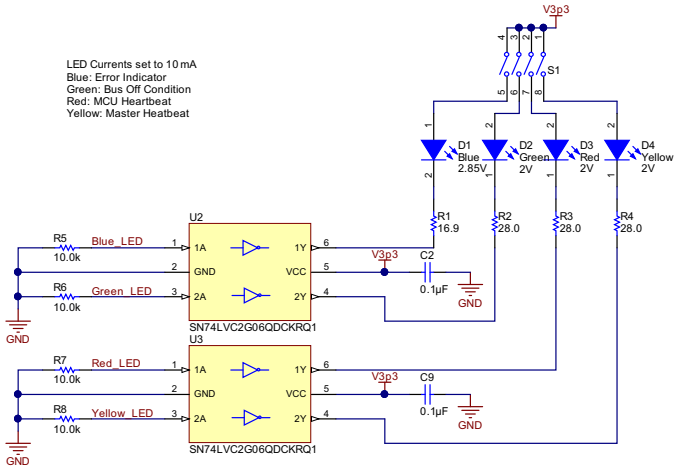


図 24. Status LED Circuitry

To ensure there would be proper drive current for the status LEDs two SN74LVC2G06-Q1 automotive dual-inverter and driver ICs were used for driving the four status LEDs. Additionally, the 3.3-V supply to each LED has been equipped with a single-pole switch that can be opened for disabling the LED, which is useful when taking current consumption measurements on the TIDA-01429 design.

All series resistors for the LEDs have been sized for a nominal 10 mA of LED current. 表 2 shows what status each LED was programmed to indicate.

表 2. Status LED Descriptions

LED COLOR	DESCRIPTION	BEHAVIOR
Blue	Any error status flag set in the CAN controller	Blinks at 1 Hz when any CAN error status flag is set
Green	Bus Off error condition in the CAN controller	Blinks at 1 Hz when the *Bus Off* flag is set
Red	MCU status LED heartbeat	Blinks at 1 Hz to indicate module is functioning properly
Yellow	Master status LED heartbeat	Blinks at 1 Hz to indicate module is configures as the master module and initiates communication

図 25 shows the status LED portion of the PCB. The closed position for each switch is to the right indicated by *On*, and the open position for each switch is to the left.

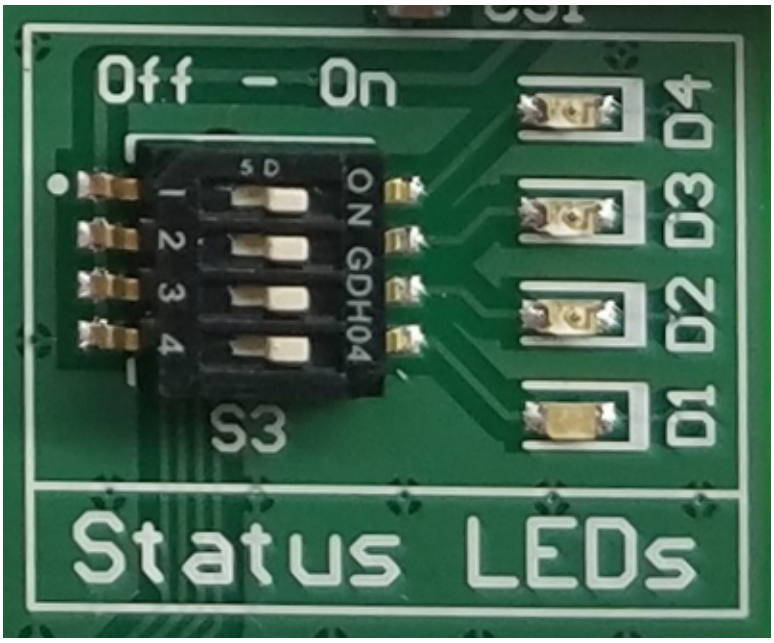


図 25. Status LED Circuitry on PCB

2.3.9 Piccolo™ Input Power Filtering

図 26 shows the power connections circuitry for the TMS320F28030PAGQ device.

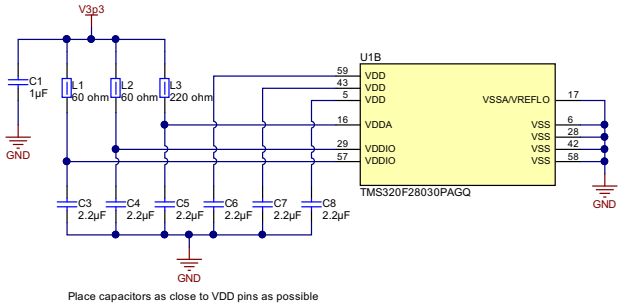


図 26. Input Power Filtering for the Piccolo™ MCU

- Supply decoupling capacitors: It is recommended to place a dedicated 2.2-µF capacitor on each VDDIO, VDDA, and VDD input as close to the device as possible.
- Ferrite beads: Additionally, it is recommended to place a series ferrite on both VDDIO supply input pins and the VDDA supply input pin for additional filtering.

2.3.10 Piccolo™ Mode Selection and Programming Interface

図 27 shows the optional external crystal, the mode selection input circuitry, reset control, and the JTAG programming interface portion of the schematic.

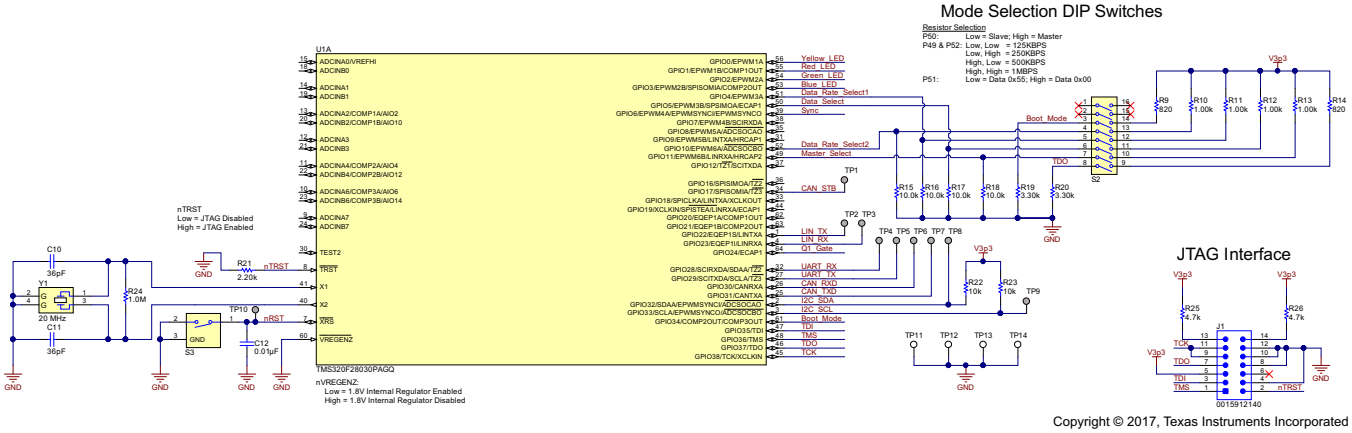


図 27. Mode Selection and Programming Interface Circuitry

- Optional external crystal: The TMS320F28030 has an internal crystal and the option to run off an external crystal. An optional 20-MHz crystal was populated, but the internal crystal was used for evaluation.
- Mode selection circuitry: Five of the general purpose input outputs (GPIOs) were used for mode selection and boot mode control:
  - GPIO11: If this pin is pulled high on startup, the module will be configured as the master node; if the pin is pulled low on startup, the module will be configured as the slave node.
  - GPIO5: The state of this pin on startup dictates what the data field of the CAN messages will be. If the pin is low, the data field will be 0x55555555, and if the pin is low, the data field will be 0x00000000.
  - GPIO10 and GPIO4: The state of these two pins on startup dictates what data rate the CAN interface is configured to:
    - Low, low: 125 KBPS
    - Low, high: 250 KBPS
    - High, low: 500 KBPS
    - High, high: 1000 KBPS
  - GPIO37 and GPIO34: The state of these two pins on startup tells the bootloader software what boot mode to use on power up:
    - Low, low: Parallel IO mode
    - Low, high: SCI mode
    - High, low: Wait mode
    - High, high: GetMode

    The default behavior of GetMode is to boot to flash, and therefore, once the modules were programmed (into flash) after assembly, this is the mode that the modules were configured to for evaluation. For more information on boot modes please see *TMS320F2803x Piccolo Microcontrollers*[5].

- $\overline{\text{XRS}}$ reset input pin: Two connections were made to $\overline{\text{XRS}}$ input pin. The first is a manual push button for restarting the MCU, and the second is the open-drain, $\overline{\text{RESET}}$ output of the LM53601-Q1 device as shown in 図 12. The LM53601-Q1 holds this output low until the 3.3-V supply is in regulation. This ensures that the MCU only begins the boot process once a stable supply has been generated.
- JTAG programming interface: The device was programmed using a 7 × 2, 100-mil, JTAG header using the XDS100V2 JTAG emulator. For more information on JTAG programming please see *TMS320F2803x Piccolo Microcontrollers*[5].

図 28 shows the optional external crystal, the mode selection circuitry, manual reset button, power supply filtering components, and JTAG programming header J1.

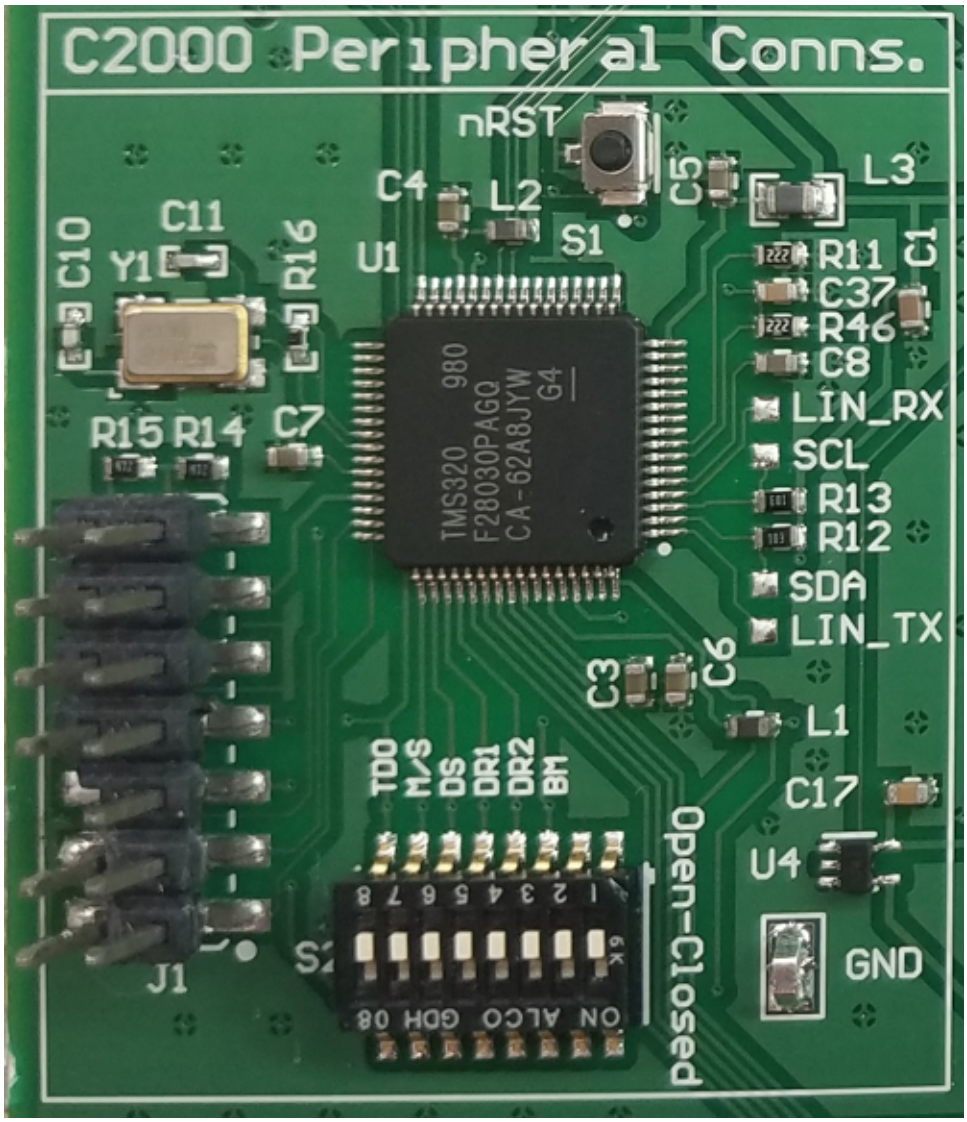


図 28. C2000™ Peripheral Circuitry on the PCB

2.3.11 External Clock Level Shifting

Because the Piccolo C2000 MCU's IO pins are 3.3 V and the LM5022-Q1 RT/SYNC input threshold can be as high as 3.8 V, an single-inverter gate was placed in the design for the option to drive the LM5022-Q1 and TPS57140-Q1 with an external clock signal. 図 29 shows the level shifting portion of the schematic.

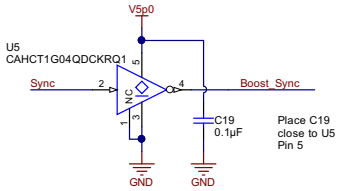


図 29. Clock Level Shifting Circuitry

This SN74AHCT1G04-Q1 was selected because the device has a small SC70 footprint, low-propagation delay, a TTL input threshold, and is automotive qualified. The TTL input threshold allows the device to be supplied by 5 V and have the input signal driven by a 3.3-V MCU IO pin.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Harware and Software

This section provides an overview of the TIDA-01429 board, the external connections on the board, the mode selection switches, and how the design was evaluated.

3.1.1 Hardware

The TIDA-01429 reference design was created to evaluate a 3-stage power tree with a CAN interface. The first stage of the power tree is a wide-input voltage boost controller to an intermediate voltage of 8.1 V when boosting, and the second stage is a wide-input voltage buck converter to 5 V. The third stage is a low-input voltage LDO used to create a 3.3-V supply rail for the C2000 MCU. To evaluate the CAN interface, a pair of modules connected to each other using a 4-wire harness is required.

To set-up and evaluate this design the following three items were used:

1. Two TIDA-0429 PCBs
2. A wire harness with four conductors: One unshielded twisted pair (UTP) cable for CANH and CANL, and another UTP cable for VBATT and GND power connections
3. An XDS100V2 JTAG emulator for programming the TMS320F28030PAGQ Piccolo MCU

All of these items are shown in 図 30.

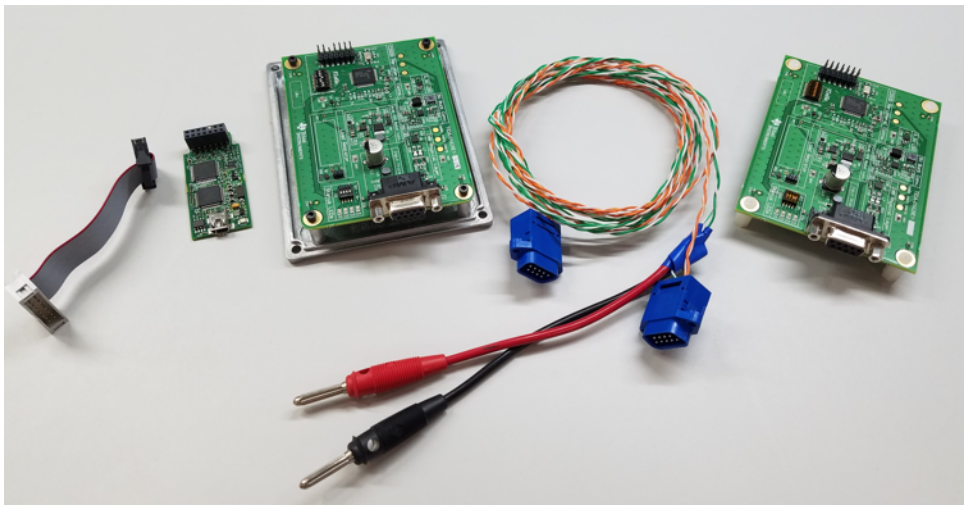


図 30. Getting Started Hardware

3.1.1.1 TIDA-01429 PCB Boards

The PCBs are 101.6 mm × 76.2 mm (4" × 3") and have 1-oz copper foil on both sides. There are two external connectors used to interface with the board:

1. Header J1: This is a 14-pin (7 × 2) ,100-mil header used for programming the TMS320F28030PAGQ device using a JTAG interface using the XDS100v2 JTAG emulator
2. Connector J2: This is a female, 9-pin, D-subminiature (D-sub) connector (DE-9) that has four connections for power, ground, CANH, and CANL

3.1.1.2 Mode Selection

As discussed in 2.3.10, four GPIO pins are used to configure the module on power up. The state of GPIO5 on power up dictates the data field of the CAN messages, the state of GPIO11 dictates whether the node will be configured in master or slave mode, and GPIO11 and GPIO4 dictate which of the four data rates the CAN messages will be transmitted and received at. Note that both modules must be configured to the same data rate to properly communicate. 表 3 shows the 16 possible configurations that are dictated by the states of GPIO4, GPIO 5, GPIO10, and GPIO11 on power up.

表 3. Mode Selection

GPIO5	GPIO11	GPI10	GPIO4	DATA FIELD	MASTER OR SLAVE	DATA RATE (KBPS)
Low	Low	Low	Low	0 x 5555 5555	Slave	125
Low	Low	Low	High	0 x 5555 5555	Slave	250
Low	Low	High	Low	0 x 5555 5555	Slave	500
Low	Low	High	High	0 x 5555 5555	Slave	1000
Low	High	Low	Low	0 x 5555 5555	Master	125
Low	High	Low	High	0 x 5555 5555	Master	250
Low	High	High	Low	0 x 5555 5555	Master	500
Low	High	High	High	0 x 5555 5555	Master	1000
High	Low	Low	Low	0 x 0000 0000	Slave	125
High	Low	Low	High	0 x 0000 0000	Slave	250
High	Low	High	Low	0 x 0000 0000	Slave	500
High	Low	High	High	0 x 0000 0000	Slave	1000
High	High	Low	Low	0 x 0000 0000	Master	125
High	High	Low	High	0 x 0000 0000	Master	250
High	High	High	Low	0 x 0000 0000	Master	500
High	High	High	High	0 x 0000 0000	Master	1000

All of the states for GPIO4, GPIO5, GPIO10, and GPIO11 are controlled by switch S2. If the switch is in the closed position, the input will be pulled high, and if the switch is in the open position, the input will be pulled low. The status of the GPIO pins are only checked one time after power up during initialization. To change the mode of a module, the switch state must be changed and the module must be power cycled.

3.1.1.3 Wire Harness

The wire harness for electrically connecting the two boards together was created using two 1.7-m long, 24-gauge UTP cables with two male 9-pin, D-sub connectors. The pinout used is the recommended pinout by CiA document DIN 41652. 表 4 shows the pinout for the four connections that were used on each D-sub connector.

表 4. Wire Harness Connections

D-SUB CONNECTOR PIN	CONNECTION DESCRIPTION
Pin 2	CANL: Low-level CAN bus IO line
Pin 3	Ground power connection
Pin 7	CANH: High-level CAN bus IO line
Pin 9	Battery input power connection

Additionally, two banana plug pigtail power connections were added to one side of the harness for connecting to a lead-acid battery or alternate power supply.

図 31 shows an image of assembled wire harness that was used for evaluation.

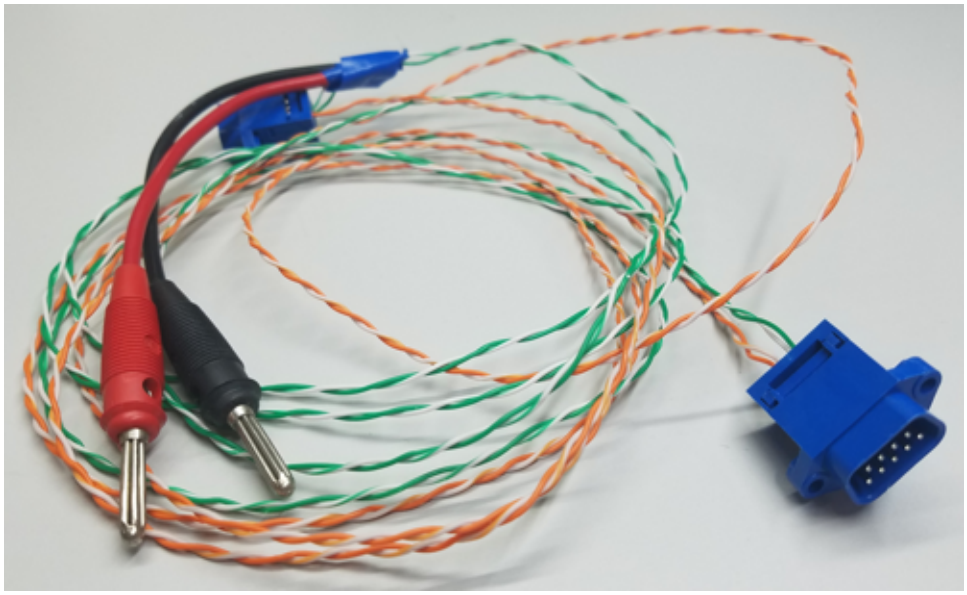


図 31. Assembled Wire Harness

3.1.1.4 Power Supply Connection

The modules are powered through the banana plug pigtails that were added to the wire harness as shown in 図 31. The VBATT net is red and GND net is black. These two connections are shared between both ends of the wire harness, therefore, the supply connection is only required to be made on the one end of the harness to power both modules. The recommended supply voltage range is from 3.5 V to 40 V.

3.1.1.5 XDS100V2 JTAG Emulator

The XDS100V2 JTAG emulator is an emulator made by Spectrum Digital Incorporated that can be used to program a variety of MCUs using JTAG. This emulator plugs into a computer using a USB and connects to the target using a standard, 14-pin, JTAG interface. 図 32 shows an image of the XDS100V2.

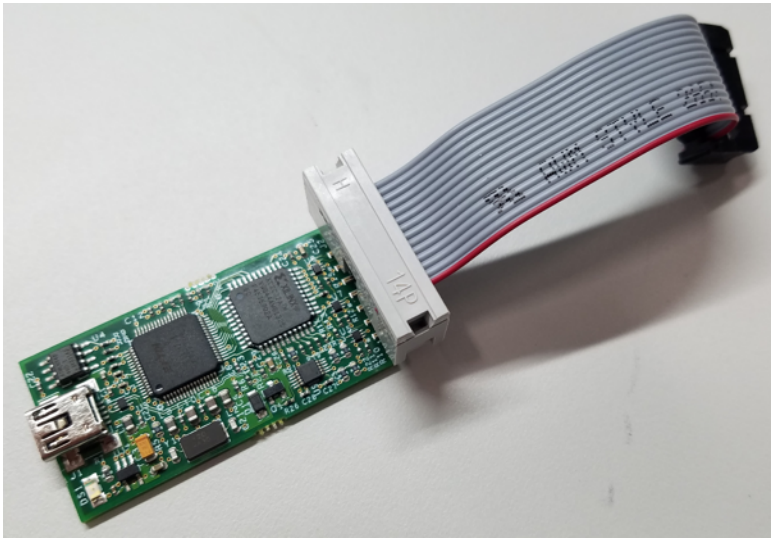


図 32. XDS100V2 JTAG Emulator

Once the modules are programmed in flash and the boot mode switches for GPIO34 and GPIO37 are both set to high, the modules can be power cycled and evaluated without reprogramming them.

3.1.2 Software

The software was written using Code Composer Studio™ v7.1.0 in C. 図 33 shows a program flowchart describing what was programmed into each module. As long as one module is configured as a master, and one module is configured as a slave, which is described in 2.3.10, and they are both configured to the same data rate. The two modules will automatically begin communicating and error checking once powered up and connected to each other.

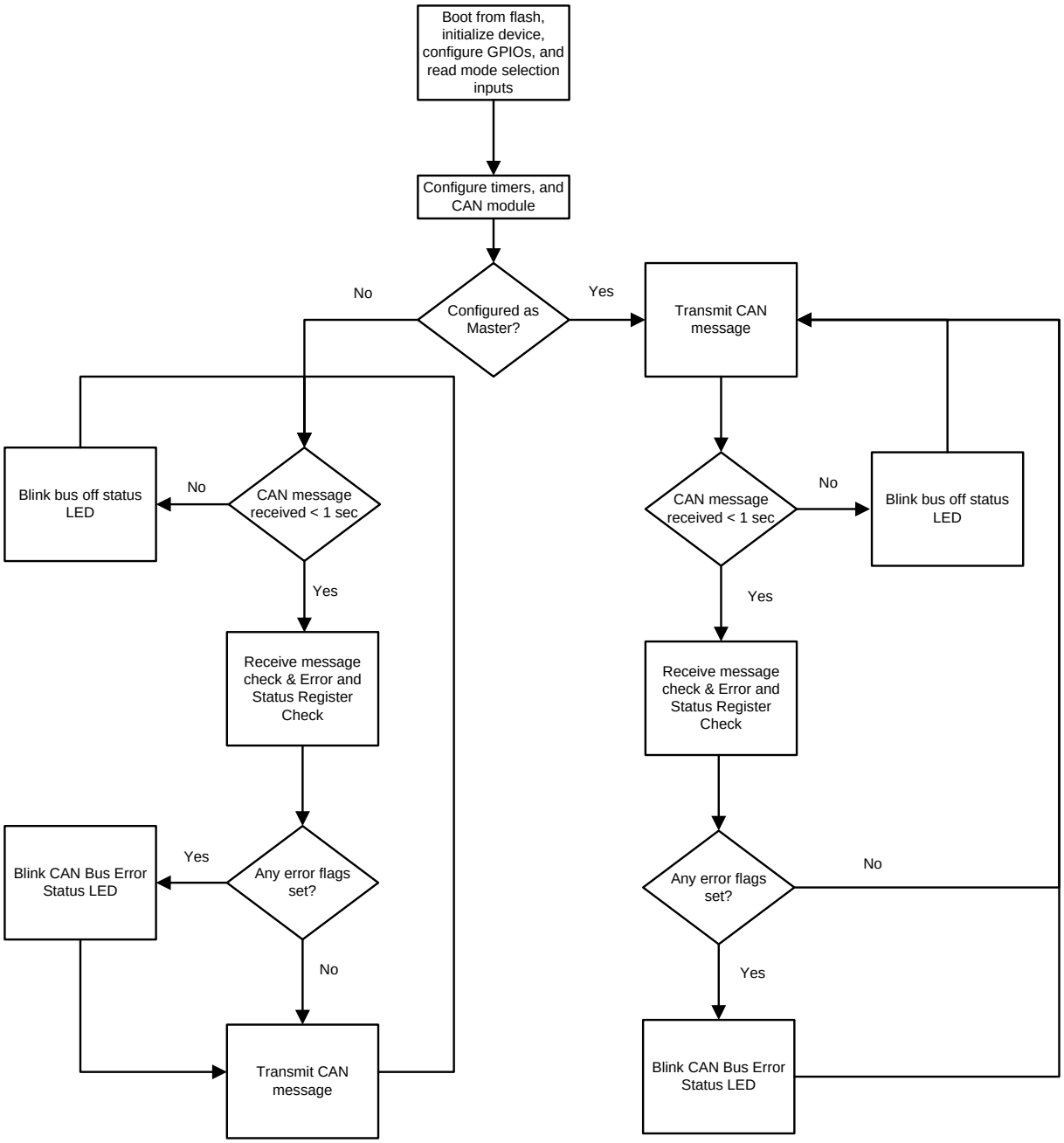


図 33. Program Flow Diagram

When the modules are powered up, first the bootloader checks the state GPIO34 and GPIO37. Once the modules have been initially programmed, the switches are set so both GPIO34 and GPIO37 are pulled high, which tells the bootloader to boot from flash.

In flash the module program first initializes the timers, interrupts, and GPIO pins. After initialization GPIO inputs GPIO4, GPIO5, GPIO10, and GPIO11 are read to determine how to configure the CAN module and whether the module will follow the slave program flow (left path) or the master program flow (right path) as shown in 図 33.

If the module is configured as the master node, the device will initiate traffic and indefinitely reattempt communication if a message is not received back. There is a 1-s timer that is started after each transmission of a CAN message. If this timer expires before a message is received, an error count is set, and the error status LED will blink four times at 1 Hz. If a message is received, the contents of the data field will be checked against a preprogrammed value. If the two do not match, or if any of the error flags are set in the error and status register, an error count is set, and the CAN error status LED will blink four times at 1 Hz. Additionally, if the I status flag is set, the bus off status LED will blink four times at 1 Hz. This send, receive, and error check process continues indefinitely.

If the module is configured as the slave node, the device will wait to receive a message before transmitting one. If the module does not receive a message within 1 s, an error count is set and the error status LED will blink four times at 1 Hz. Once a message is received, the contents of the data field will be checked against a preprogrammed value. If the two do not match, or if any of the error flags are set in the error and status register, an error count is set, and the CAN error status LED will blink four times at 1 Hz. Additionally, if the *Bus Off* status flag is set in the error and status register, the bus off status LED will blink four times at 1 Hz. After receiving and error checking the message, the module will transmit a CAN frame, and the process will start over. After transmitting, the 1-s timer will reset and begin counting down. If it expires before a message is received, the error status LED will blink four times at 1 Hz. This receive, error check, and transmit process continues indefinitely.

3.2 Testing and Results

The following items were evaluated on the TIDA-01429 design:

- Reverse blocking protection
- Boost controller input current versus input voltage
- Boost controller output voltage versus input voltage
- Boost controller UVLO pin's Zener diode clamping behavior
- Boost controller efficiency
- Buck converter input current versus input voltage
- Buck converter output voltage versus input voltage
- Buck converter efficiency
- Buck converter load step response
- LDO input current versus input voltage
- LDO output voltage versus input voltage
- CISPR 25 Radiated Emissions (RE) Testing
- CISPR 25 Conducted Emissions (CE) Testing - Voltage Method
- ISO 11452-4 Bulk Current Injection (BCI) Immunity Testing

3.2.1 Reverse Blocking Protection

For lower-current applications, a standard Schottky diode is the most cost-effective solution for reverse battery protection. A standard 40-V, 2-A Schottky diode in a SOD123 package was used. 図 34 shows the input leakage current versus the reverse polarity input voltage.

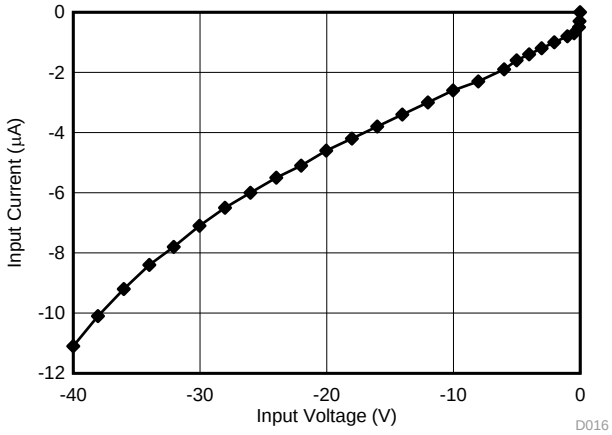


図 34. Reverse Blocking Performance

As shown in 図 34, the input leakage current with a –40-V input voltage applied was 11.1 µA at room temperature.

3.2.2 Boost Controller Input Current Versus Input Voltage

The input current versus input voltage data was taken with one module initialized and sending CAN messages at 500 KBPS. The input voltage measurements are taken from the input side of the regulator at C20. All of the status LEDs were all left open for these measurements. 図 35 shows the input current when the input voltage is ramped from 0 V to 40 V.

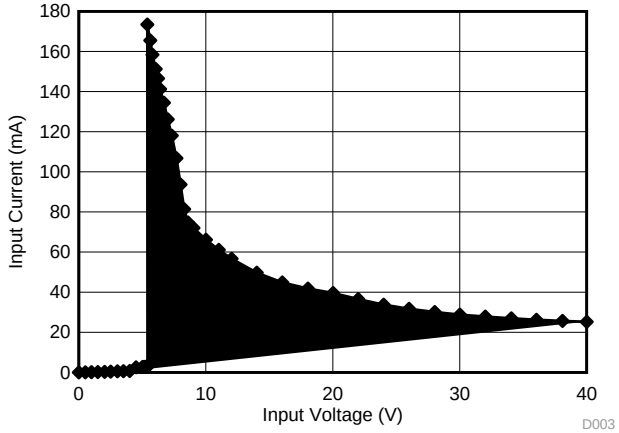


図 35. Boost Input Current Versus Rising Input Voltage

図 36 shows the input current when the input voltage is dropped from 40 V to 0 V.

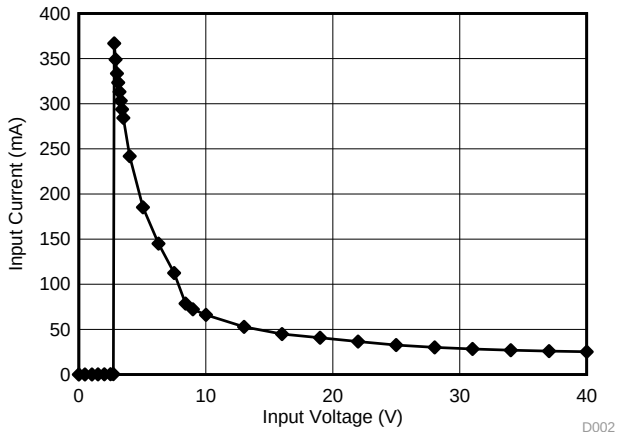


図 36. Boost Input Current Versus Falling Input Voltage

As shown, the boost controller does not begin turning on with a rising input voltage until approximately 6 V but remains on to just lower than 3 V with a falling input voltage. Additionally for lower input voltages, the regulator requires larger input currents to maintain the 8.1-V output.

3.2.3 Boost Controller Output Voltage Versus Input Voltage

The output voltage versus input voltage data was also taken with one module initialized and sending CAN messages at 500 KBPS. The input voltage measurements are taken from the input side of the regulator at C20. All of the status LEDs were left open for these measurements. 図 37 shows the output voltage for input voltages from 0 V to 40 V. As shown, when the input voltage rises higher than the boost controller's set output voltage of 8.1 V, the controller transitions to 0% duty cycle, and the output continues to ramp one diode drop below in the input voltage.

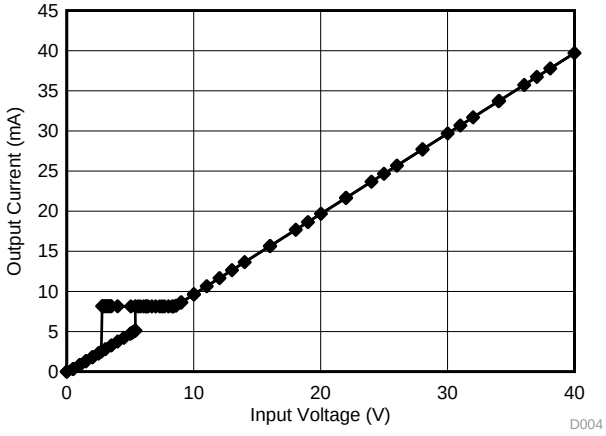


図 37. Boost Output Voltage Versus Input Voltage

To get a better look at the low-voltage behavior of the boost regulator, 図 38 shows the subset of data from 0 V to 10 V only. With a rising input voltage, the regulator turned out and began boosting the input voltage at approximately 5.5 V. Alternately, after initial power up with a falling edge, the regulator remained on and regulated down to approximately 2.8 V.

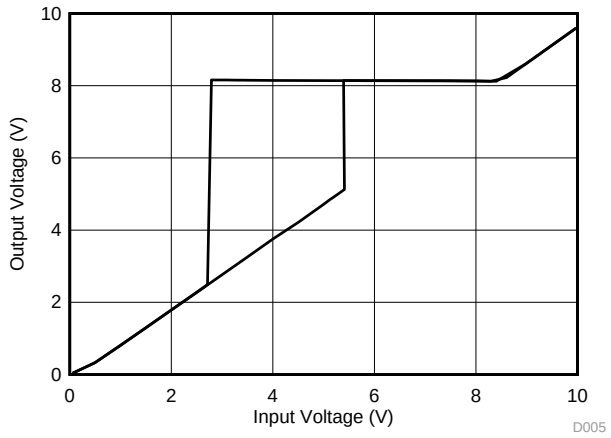


図 38. Boost Output Voltage Versus Low Input Voltages

3.2.4 Boost Controller UVLO Pin's Zener Diode Clamping Behavior

As stated in 2.3.2, the UVLO pin on the LM5022-Q1 required a Zener diode to clamp the input voltage and protect the input pin from voltages greater than 7 V. 図 39 shows the clamping behavior of the voltage divider and the Zener diode on the UVLO pin.

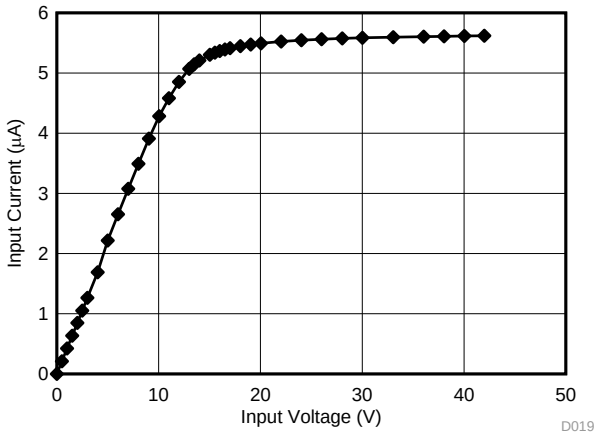


図 39. Voltage on UVLO Pin Versus Input Voltage

As shown in 図 39, the input voltage was clamped to a maximum of 5.6 V for input voltages up to 42 V.

3.2.5 Boost Controller Efficiency

The efficiency data for the boost controller was taken after completely disconnecting the boost portion of the design from the rest of the board (cutting traces). Once all of the external loads were disconnected from the output, and the input voltage could be applied directly to the VIN node of the boost controller, purely resistive loads were tied from the output of the regulator to ground.

Therefore, the input voltage measurements were taking directly at the input node of the regulator, and the output voltages were taken from C27 and C28 to GND. The extreme cold crank input voltage of 3 V was used for all efficiency measurements because during normal vehicle operating conditions, the boost controller will be at 0% duty cycle.

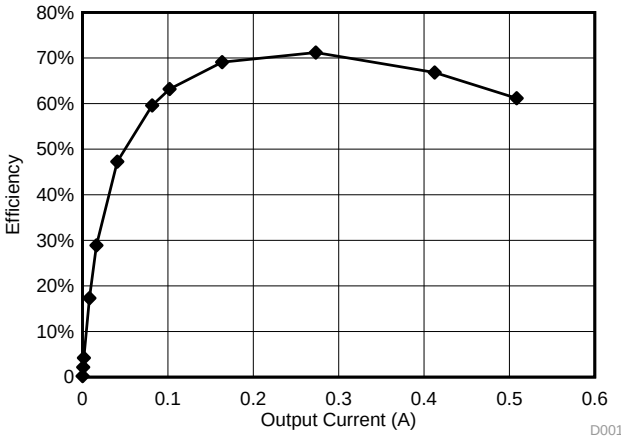


図 40. Boost Controller Efficiency Measurements

As shown the efficiency of the converter is between 60% and 70% from load currents of 100 mA to over 500 mA. For load currents greater than 500 mA, the regulator started current limiting and the output fell out of regulation. To handle larger loads at lower input voltages shunt resistor R43 can be adjusted to a lower resistance. Additionally, the switching frequency was monitored while performing the efficiency measurements. 図 41 shows the switching frequency of the buck converter with a 40-Ω load.

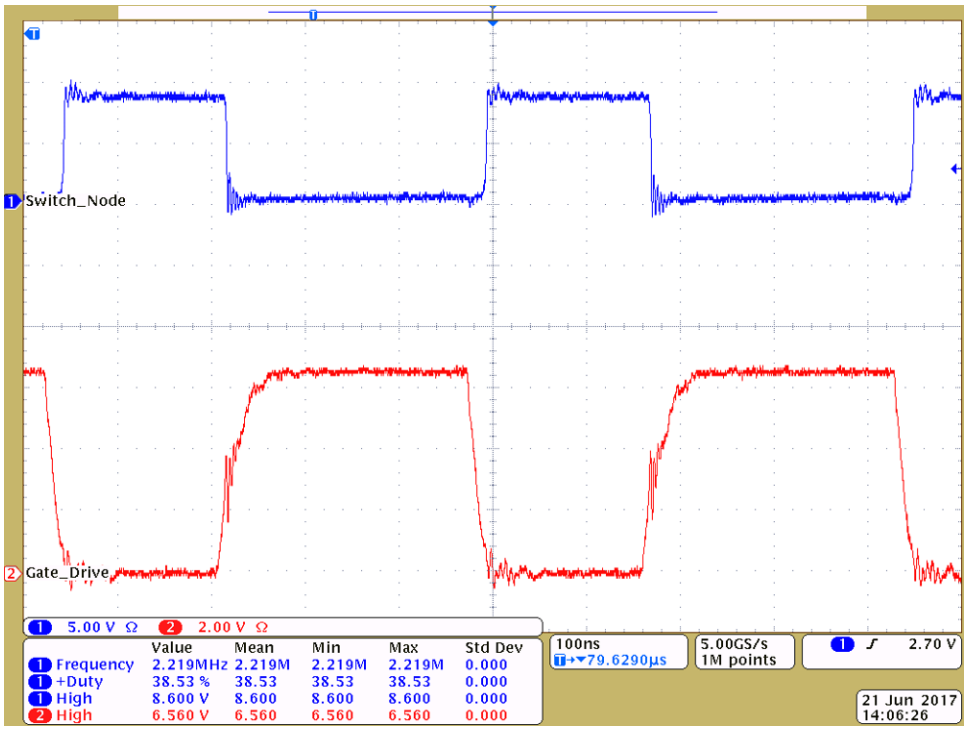


図 41. Boost Controller Switching Frequency

As shown in 図 41, the regulators switching frequency with a 125-mA load was 2.2 MHz.

3.2.6 Buck Converter Input Current Versus Input Voltage

To evaluate the buck converter's input current versus input voltage performance, the regulated LM5022-Q1 was disconnected, and a power supply was fed directly to the input node of the regulator at C23. The CAN transceiver and C2000 remained in normal mode in transmitting at 500 KBPS, and all the status LEDs were left open for all input current measurements.

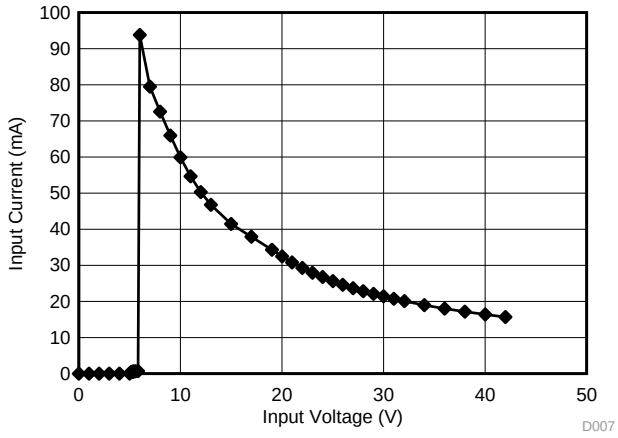


図 42. Buck Converter Input Current Versus Input Voltage

図 42 shows that the buck converter began to turn on and draw current at 5.1 V and was within regulation by 6 V.

3.2.7 Buck Converter Output Voltage Versus Input Voltage

To evaluate the buck converter's output voltage versus input voltage performance, the regulated LM5022-Q1 remained disconnected, and a power supply was fed directly to the input node of the regulator at C23. The CAN transceiver and C2000 remained in normal mode in transmitting at 500 KBPS, and all the status LEDs were left open for all output voltage measurements.

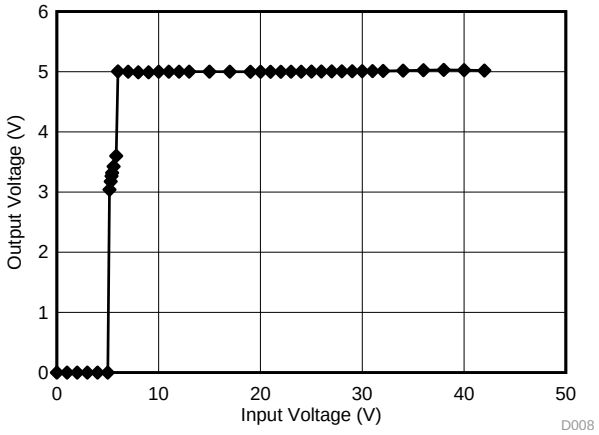


図 43. Buck Converter Output Voltage Versus Input Voltage

図 43 shows that the buck converter's output began to turn on at 5.1 V and was within regulation by 6 V. Additionally, the regulator remained in regulation all the way to 42 V.

3.2.8 Buck Converter Efficiency

The efficiency data for the buck converter was taken after disconnecting both the CAN transceiver and the 3.3-V LDO from the 5-V output and placing varying purely resistive loads on the output of the regulator. A constant input voltage of 12.5 V was applied to C23, the input node of the buck converter, for all efficiency measurements.

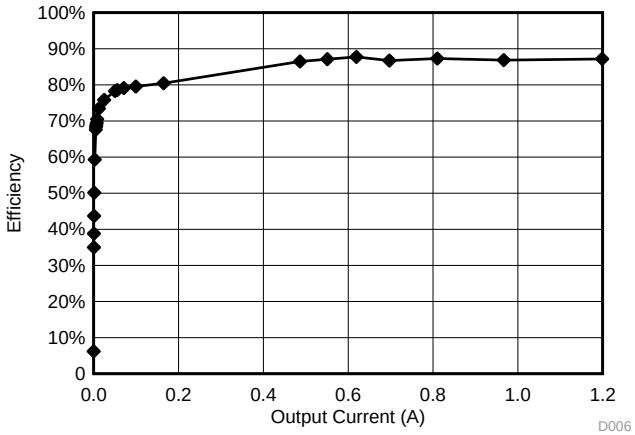


図 44. Buck Converter Efficiency Measurements

図 44 shows that for load currents between 8 mA and 100 mA, the efficiency was between 70% and 80%. Furthermore for output currents of 100 mA to 1.2 A, the efficiency remained between 80% and 90%.

3.2.9 Buck Converter Load Step Response

Lastly the buck converter was evaluated for output regulation accuracy when subjected to a step up in load current and a step down in load current. For this test, the dummy load resistor RF1 on the board was populated with a 10-Ω power resistor and transistor Q1 was used for quickly turning on and off this load. The 10-Ω load on the 5-V rail results in a 500-mA load step. The load step measurements were performed with the module initialized and sending CAN messages at 500 KBPS.

図 45 shows the converter's response to when the load is increased by 500 mA. As shown, the step increase in load current causes the output voltage of the regulator to droop 352 mV. 図 46 shows the converter's response time for the same load step. As shown, the step increase in load was fully recovered from in less than 50 µs.

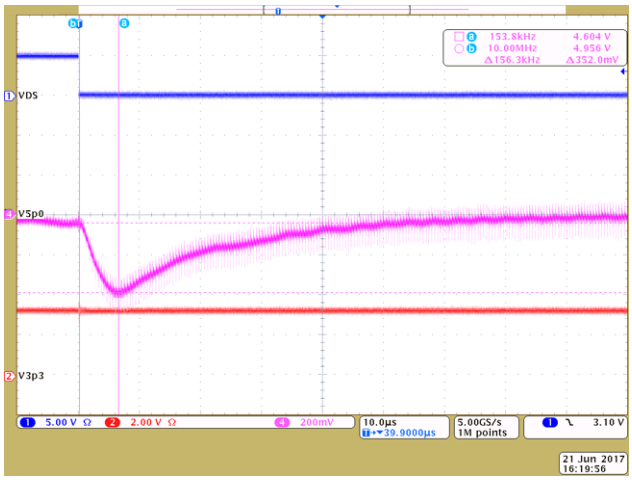


図 45. Buck Converter Load Step Increase Response

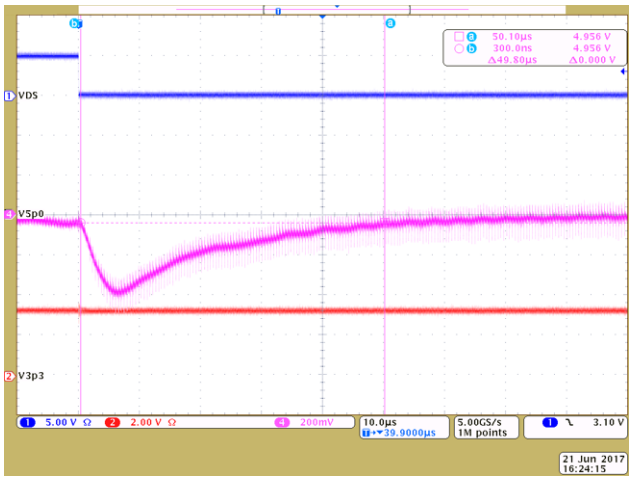


図 46. Buck Converter Load Step Increase Recovery Time

図 47 shows the converter's response to when the load is decreased by 500 mA. As shown, the step decrease in load current causes the output voltage of the regulator to increase by 344 mV. 図 48 shows the converter's response time for the same load step. As shown, the step decrease in load was fully recovered in 60 µs.

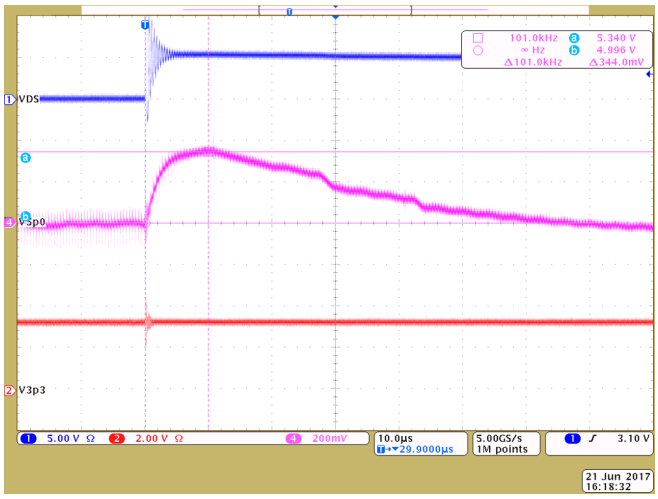


図 47. Buck Converter Load Step Decrease Response

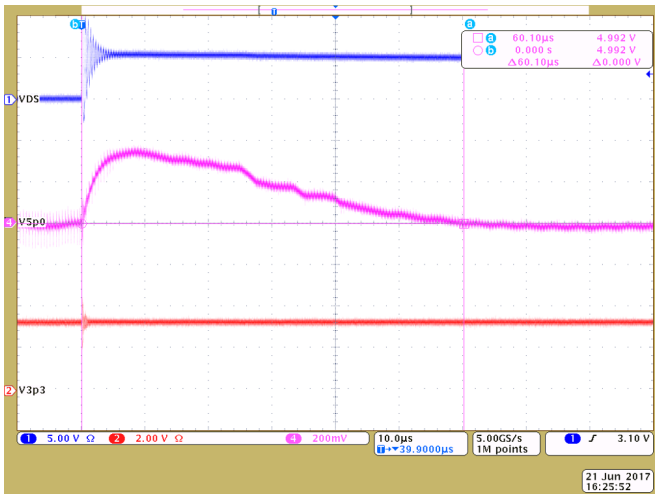


図 48. Buck Converter Load Step Decrease Recovery Time

3.2.10 LDO Input Current Versus Input Voltage

To evaluate the LDO's input current versus input voltage performance, the regulated 5-V rail was disconnected from the input and a power supply was fed directly to the input node of the regulator at C13. The CAN transceiver and C2000 remained in normal mode in transmitting at 500 KBPS, and all the status LEDs were left open for all input current measurements. The EN was tied to the input voltage of the device.

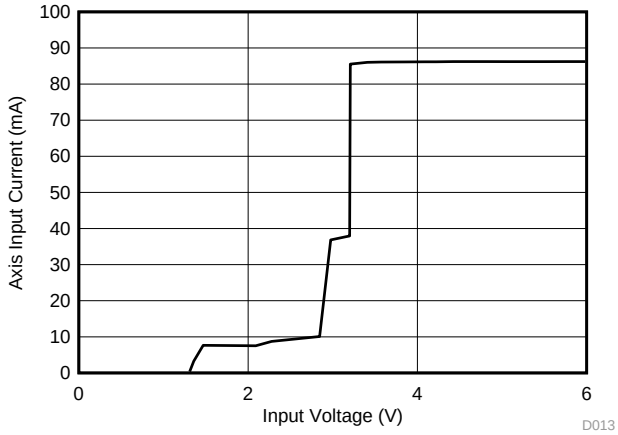


図 49. LDO Input Current Versus Input Voltage

図 49 shows that the LDO began to draw current at and turn on at 1.35 V and was in regulation at 3.57 V. In the actual application where the device would be held in low-power sleep mode by the TPS57140-Q1 until the 5-V rail was within regulation the device would remain disabled and draw less than 1 µA of current until being enabled. Additionally, the device was tested for input quiescent current from 0 V to 6 V with the enable pin tied low, and the maximum input current was 0.6 µA.

3.2.11 LDO Output Voltage Versus Input Voltage

To evaluate the LDO's output voltage versus input voltage performance, the regulated 5-V rail remained disconnected from the input and a power supply was fed directly to the input node of the regulator at C13. The CAN transceiver and C2000 remained in normal mode in transmitting at 500 KBPS, and all the status LEDs were left open for all input current measurements. The EN was tied to the input voltage of the device for this test.

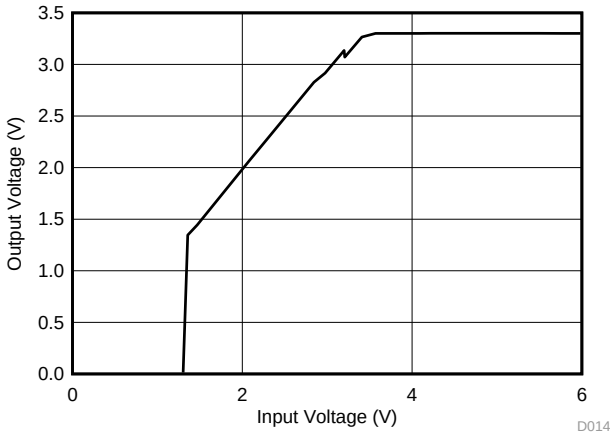


図 50. LDO Output Voltage Versus Input Voltage

図 50 shows that the LDO's output began to turn on at 1.35 V and was in regulation at 3.57 V. In the actual application where the device would be held in low-power sleep mode by the TPS57140-Q1 until the 5-V rail was within regulation the device's output would remain disabled, and the output voltage would not slowly ramp with input voltage. Additionally, the device was tested for output voltage when in low-power sleep mode when the input voltage was swept from 0 V to 6 V with the enable pin tied low. The output remained disabled and under 3 mV for the entire input range.

3.2.12 CISPR 25 Radiated Emissions Testing

Radiated emissions testing was performed for a pair of modules in an anechoic chamber per the ALSE test method in CISPR 25 Edition 4.0. In this test there are two modules placed 1.7-m apart from each other. The slave node, or equipment under test (EUT) as it is referred to in the standard, is placed on top of a low-relative permittivity support (raised off the ground plane by a material that resists electric fields). The master node, which is sometimes referred to as the monitoring node, is tied directly to the ground plane. This slave node setup is shown in 図 51, and the master node setup is shown 図 52.

図 51. Slave Node Setup for Radiated Emissions

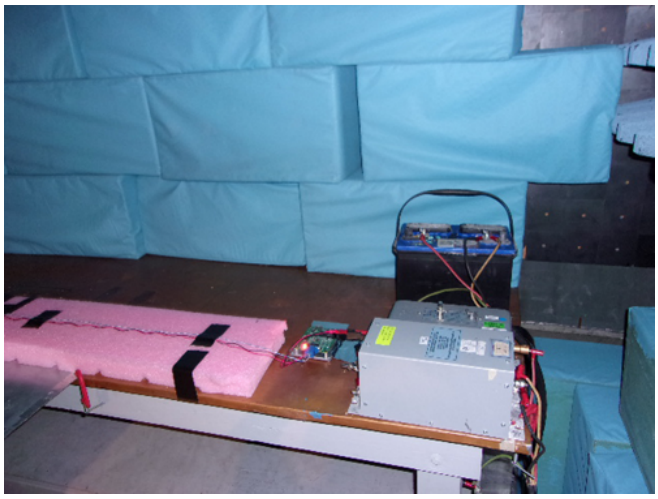


図 52. Master Node Setup for Radiated Emission

The test consists of multiple frequency ranges for three different antennas with two of the antennas oriented in both the horizontal and vertical positions. The setup description for the five measurement runs are described below:

- Test run 1: 150 KHz to 30 MHz with a dipole antenna in vertical orientation
- Test run 2: 30 MHz to 200 MHz with a biconical antenna in horizontal orientation
- Test run 3: 30 MHz to 200 MHz with a biconical antenna in vertical orientation
- Test run 4: 200 MHz to 1,000 MHz with a logarithmic antenna in horizontal orientation
- Test run 5: 200 MHz to 1,000 MHz with a logarithmic antenna in vertical orientation

Each graph will show a series of three limit lines: one for each of the three detectors that are used on the spectrum analyzer to gather the data—one for the peak detector, one for the quasi-peak detector, and one for the average detector. A limited number of quasi-peak and average data points were taken to save test time. The test program selected these data points based on the frequencies where the peak detector was closest to the limit line.

The TIDA-01429 passed Class 5 CISPR 25 radiated emissions per the ALSE method without the input pi filter populated or a CMC populated on the CAN bus lines.

図 53 shows the dipole antenna that is 1-m in front of the test setup in the vertical position.

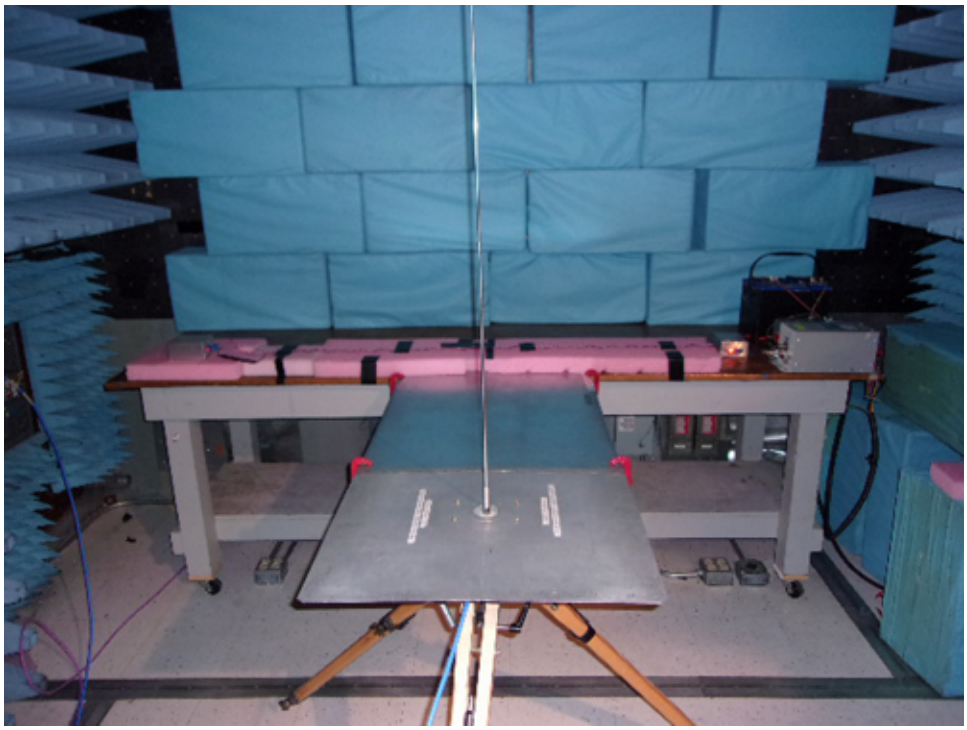


図 53. Radiated Emissions Dipole Antenna Setup

図 54 shows the radiated emissions results for test run one. As shown, the pair of modules pass the CISPR Class 5 broadcast radiated emissions limit lines.

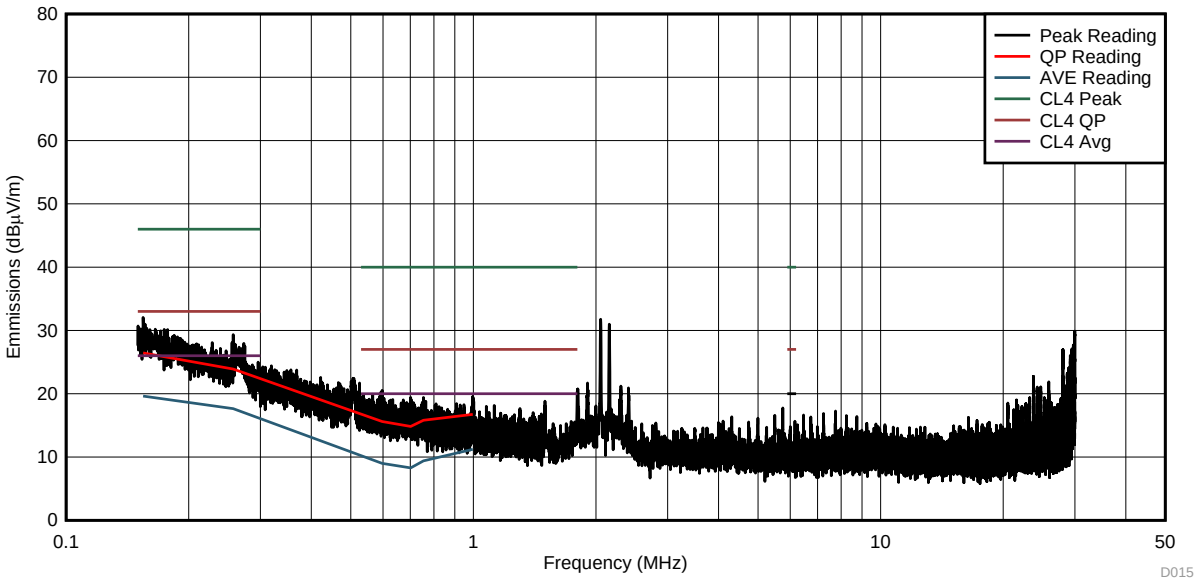


図 54. Radiated Emissions Dipole Antenna Results

Next to measure the emissions for the frequency range of 30 MHz to 200 MHz, a biconical antenna was used. The emissions measurements for this antenna must be performed in both the horizontal and vertical orientations. 図 55 shows the biconical antenna in the horizontal orientation that is 1-m in front of the test setup (test run two).

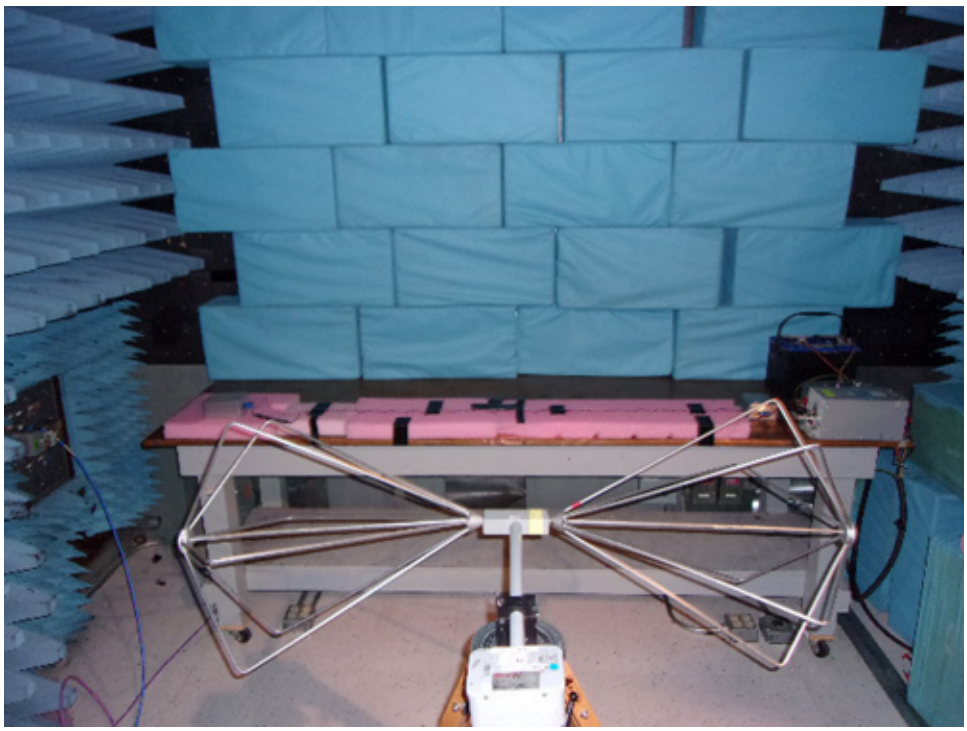


図 55. Radiated Emissions With Horizontal Biconical Antenna Setup

図 56 shows the radiated emissions results for this setup.

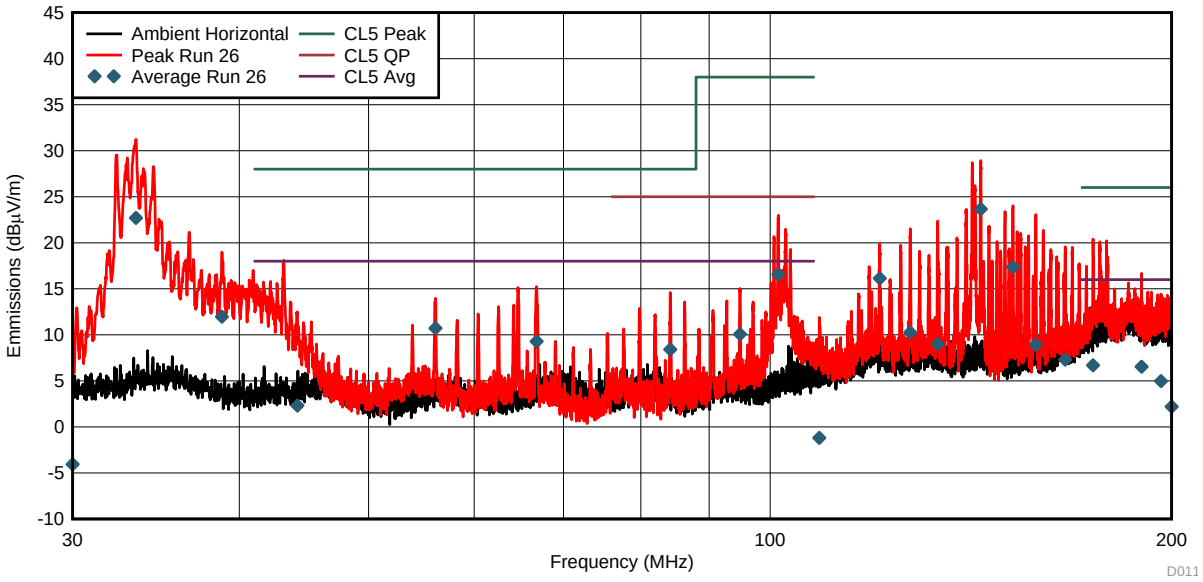


図 56. Horizontal Biconical Antenna Results

After running the emissions measurements in the horizontal orientation, the antenna was turned to the vertical orientation as shown in 図 57 (test run three).

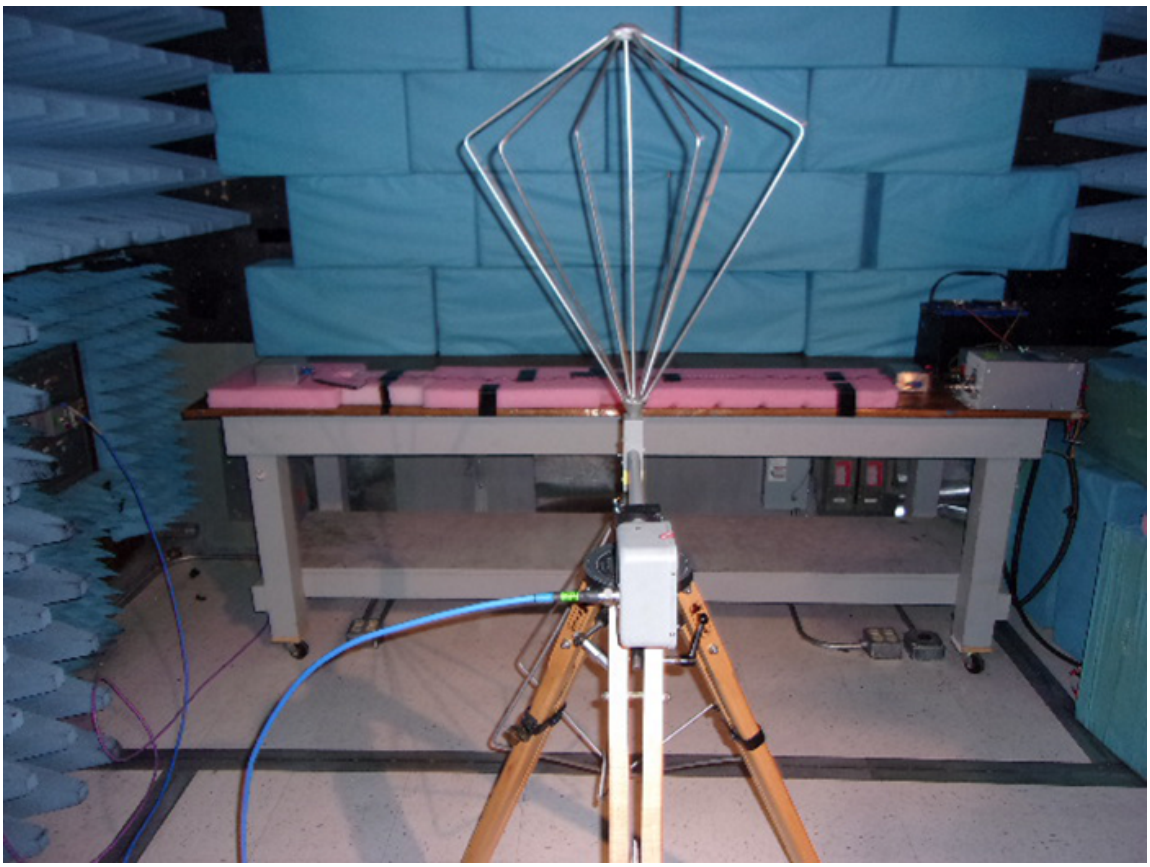


図 57. Radiated Emissions With Vertical Biconical Antenna Setup

図 58 shows the test results. As shown, the pair of modules pass the CISPR Class 5 broadcast radiated emissions limit lines with the biconical antenna in both horizontal and vertical orientations.

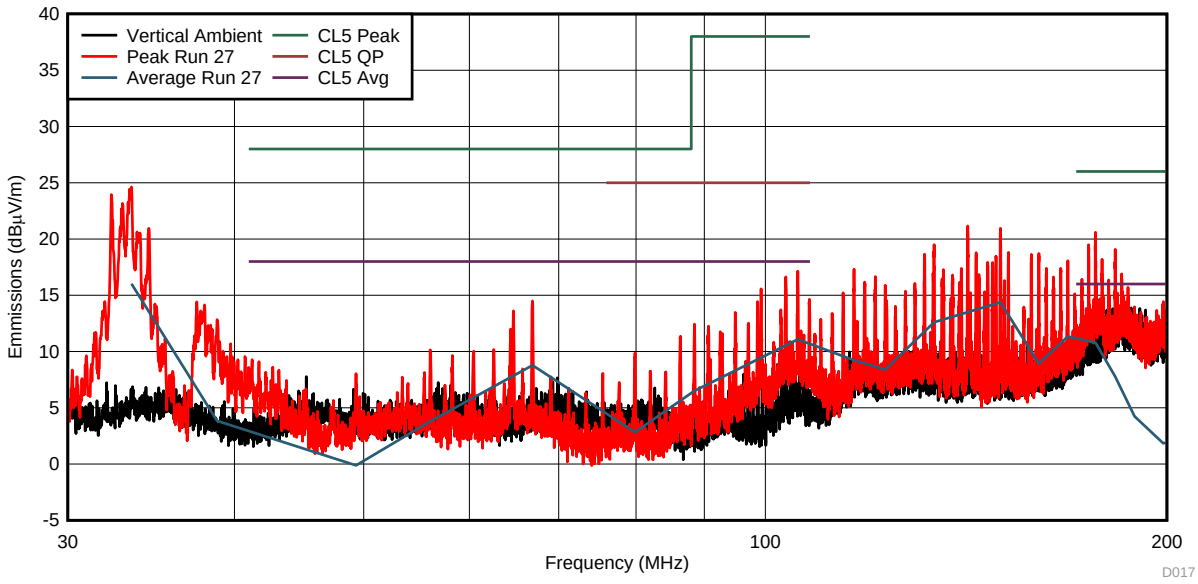


図 58. Vertical Biconical Antenna Results

Lastly to measure the emissions for the frequency range of 200 MHz to 1000 MHz, a logarithmic antenna was used. Again, the emissions measurements with this antenna must be performed in both the horizontal and vertical orientations. 図 59 shows the logarithmic antenna in the horizontal orientation that is 1-m in front of the test setup (test run four).

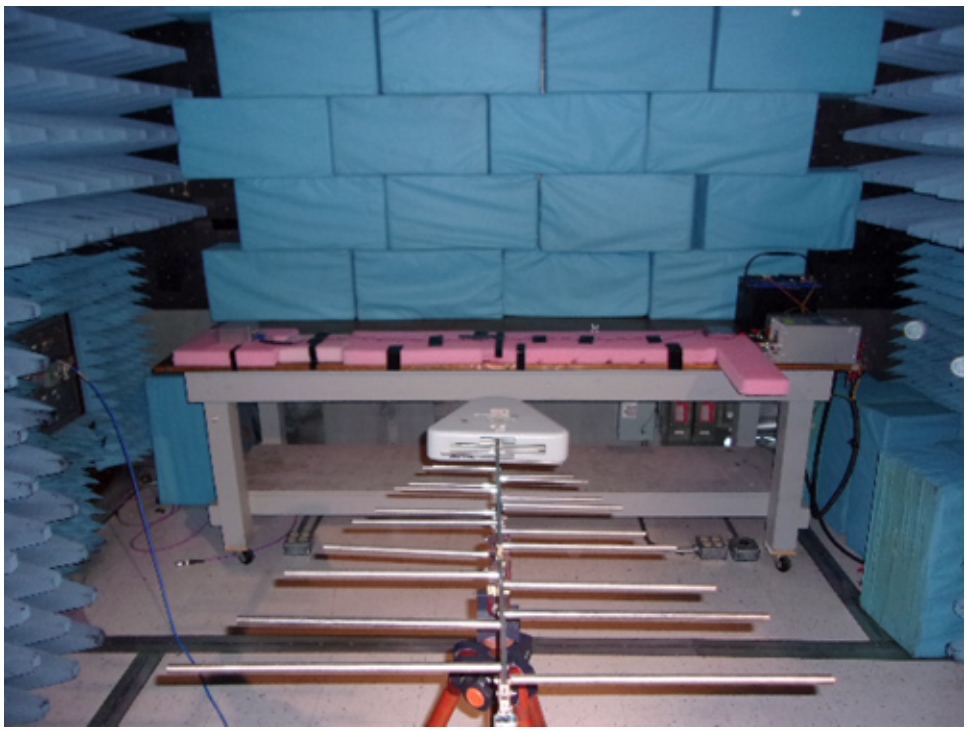


図 59. Radiated Emissions With Horizontal Logarithmic Antenna Setup

図 60 shows the radiated emissions results for this setup.

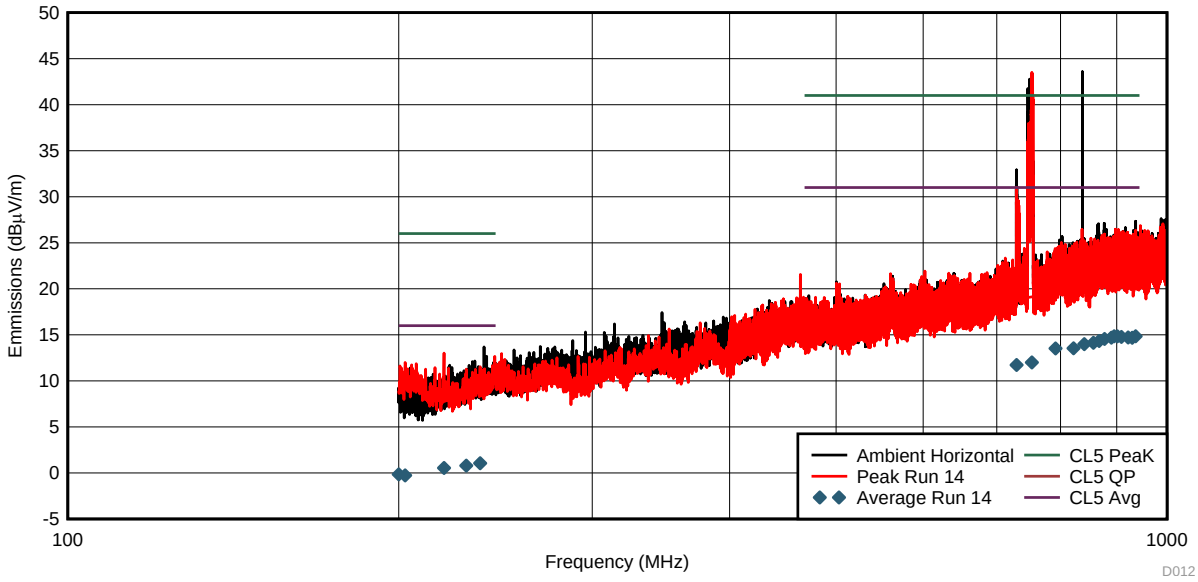


図 60. Horizontal Logarithmic Antenna Results

After running the emissions measurements in the horizontal orientation the antenna was turned to the vertical orientation as shown in 図 61 (test run five).

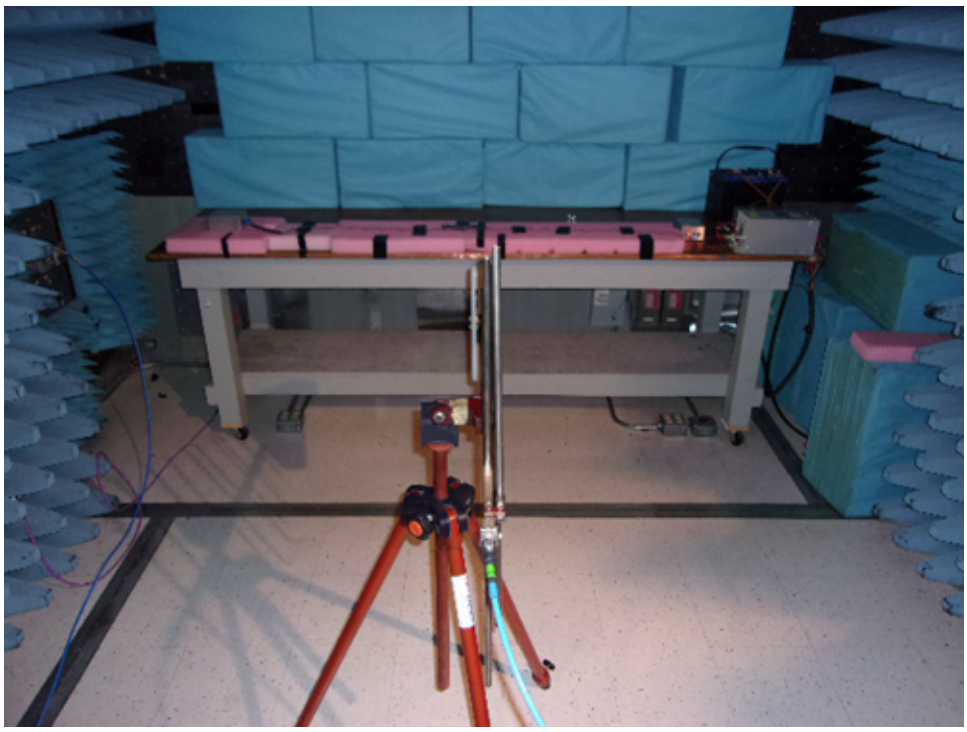


図 61. Radiated Emissions With Vertical Logarithmic Antenna Setup

図 62 shows the test results. As shown, the pair of modules pass the CISPR Class 5 broadcast radiated emissions limit lines with the logarithmic antenna in both horizontal and vertical orientations.

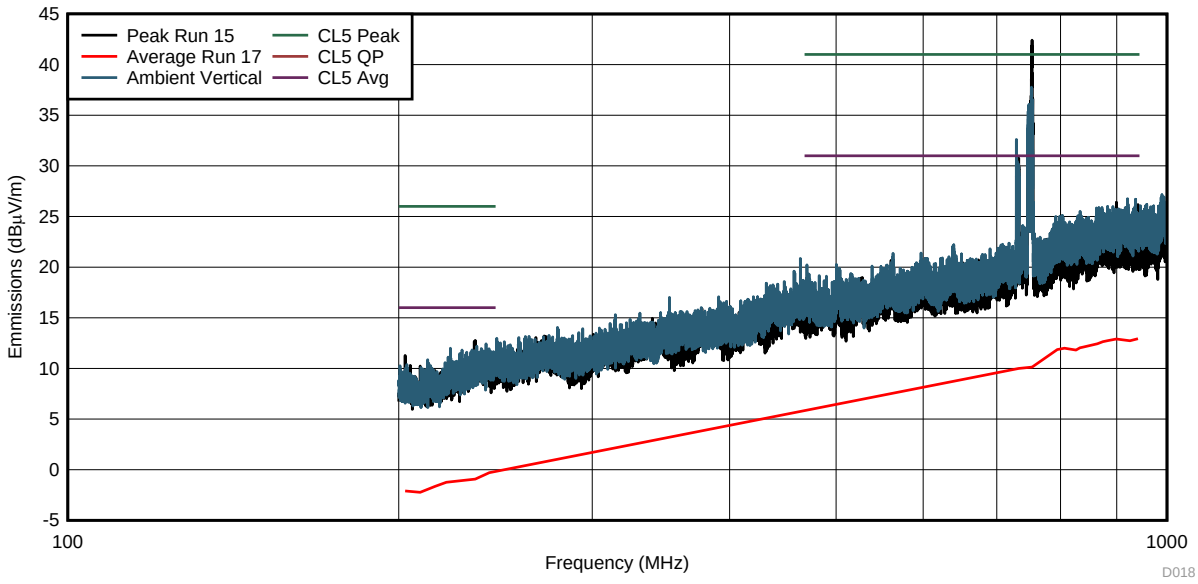


図 62. Vertical Logarithmic Antenna Results

3.2.13 CISPR 25 Conducted Emissions Testing - Voltage Method

Conducted emissions testing was also performed using a pair of modules in an anechoic chamber. The test methodology followed was the *Conducted emissions from components / modules - Voltage method* per the CISPR 25 Edition 4.0 standard. In this test supply lines between the connector of the module and the artificial network (sometimes referred to as a line impedance stabilization network or LISN) must be between 200 mm and 400 mm long. The same two modules with a 1.7-m harness between them were used for this testing. Both the slave node and the master node were placed on top of a low-relative permittivity support. This setup is shown in 図 63.

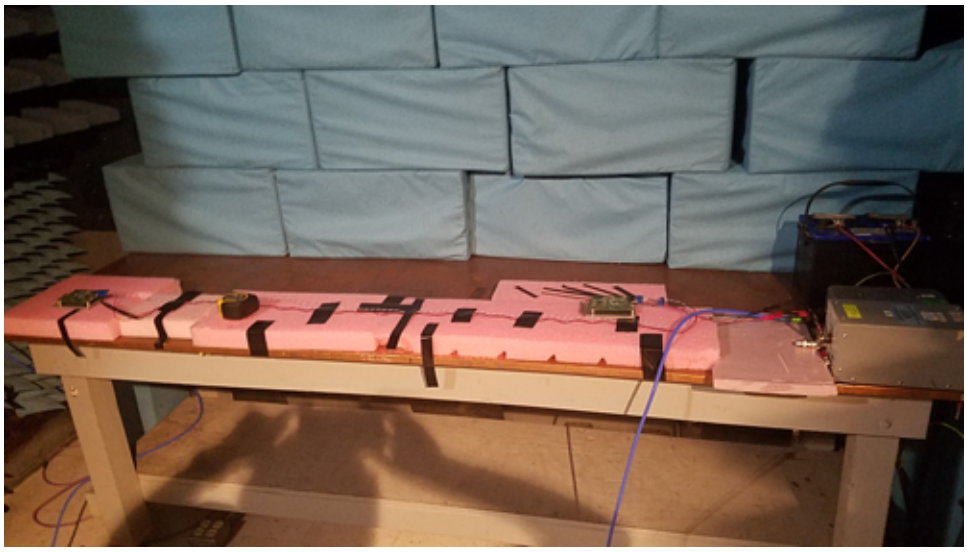


図 63. Conducted Emissions Setup

This test is performed two times: one on the positive power supply line and a second on the power return line (ground). The measurement is performed by connecting the spectrum analyzer to the measuring port of the artificial network for the battery supply line and the measuring port of the artificial network for the power return line, which are shown in 図 64.

図 64. Artificial Networks with Measuring Ports for Conducted Emissions

As shown in 図 65 and 図 66, the TIDA-01429 passes the CISPR 25 conducted emissions using the voltage method with the Class 4 limit lines.

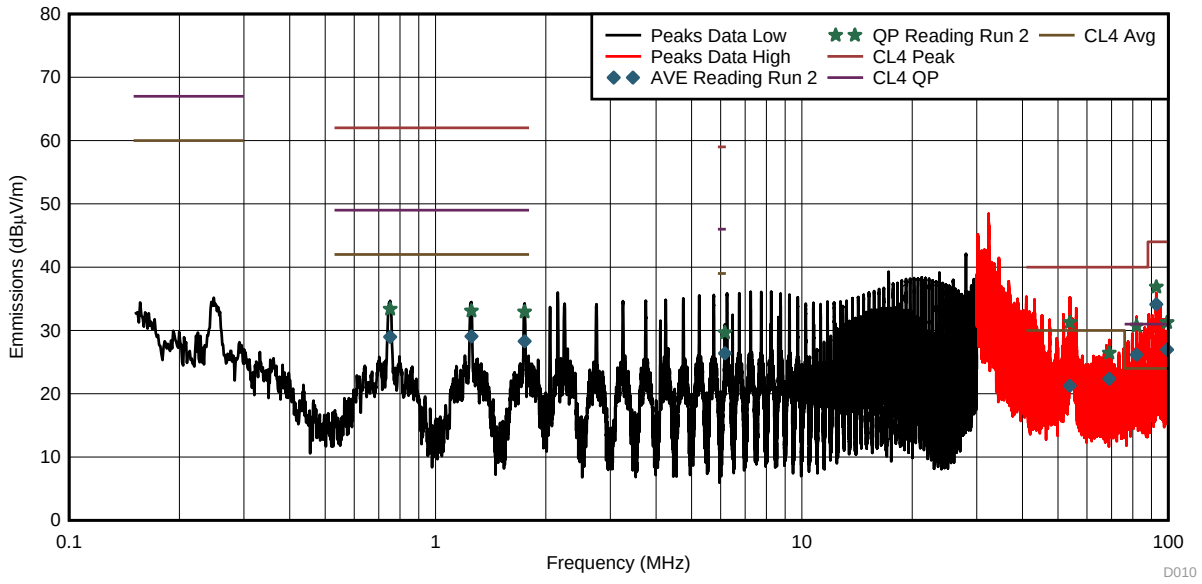


図 65. Conducted Emissions Results for Power Supply Line

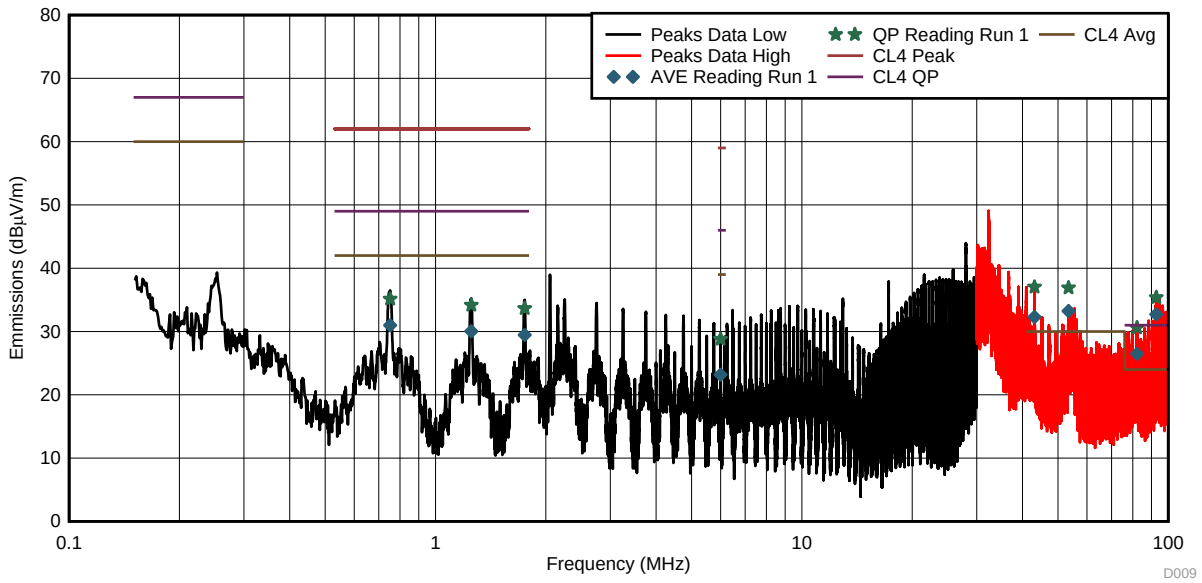


図 66. Conducted Emissions Results for Power Supply Return Line

3.2.14 ISO 11452-4 Bulk Current Injection Immunity Testing

BCI testing is an immunity test defined by ISO 11452-4 where noise is coupled onto a wire harness using a current injection probe. The amplitude at each frequency point is increased until there is a failure or the required level has been reached. To pass this immunity test the module has to continue to operate normally at all test frequencies for amplitudes greater than or equal to the limit line. This test was performed with all four conductors of the wire harness run through the current injection probe with the probe 450 mm from the slave node and 750 mm from the slave node as shown in 図 67.

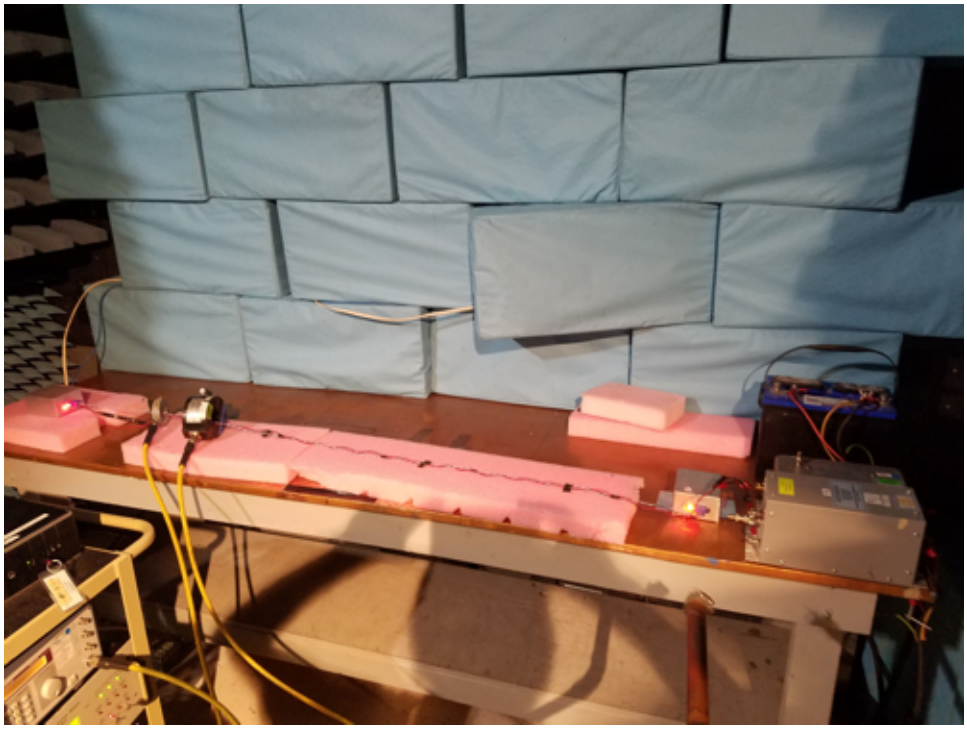


図 67. Bulk Current Injection Test Setup

The health of the units were tracked by monitoring the status LEDs using a coaxial camera feed that was run out of the shielded room to a television.

図 68 shows the immunity performance when the current injection probe was place 450 mm from the slave node, and 図 69 shows the immunity performance when the current injection probe was place 750 mm from the slave node. As shown in both figures, neither test showed any deviations and passed up to the required power levels.

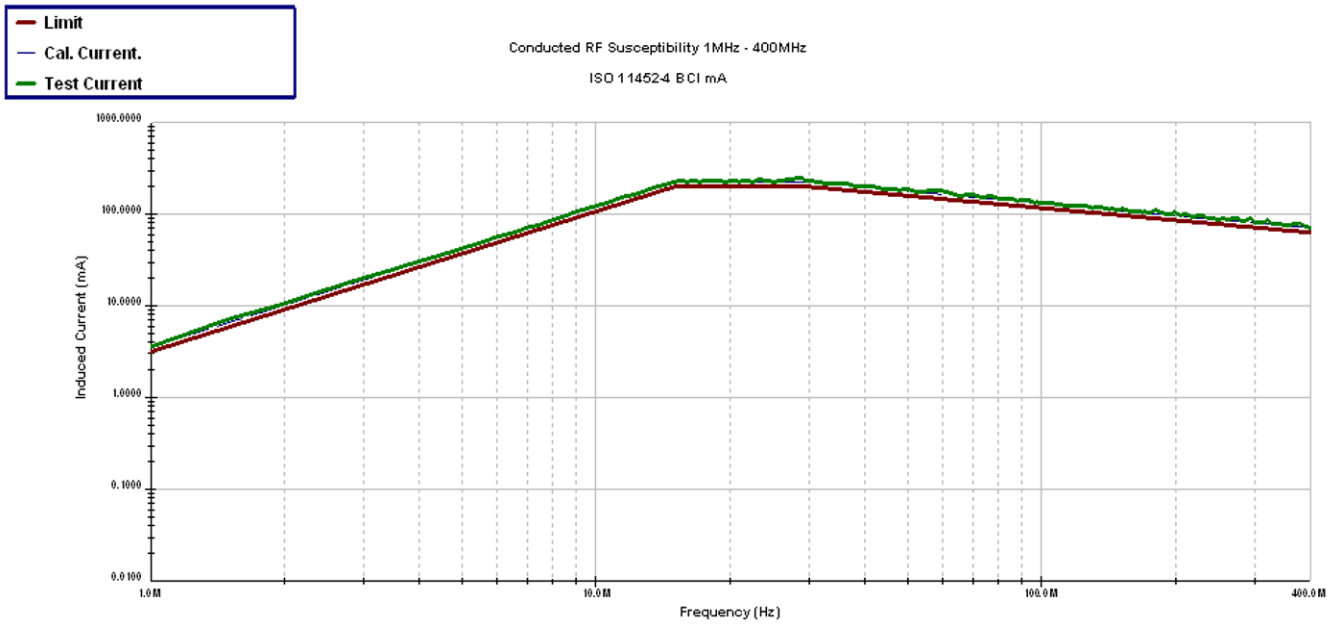


図 68. BCI Results With Current Injection Probe at 450 mm

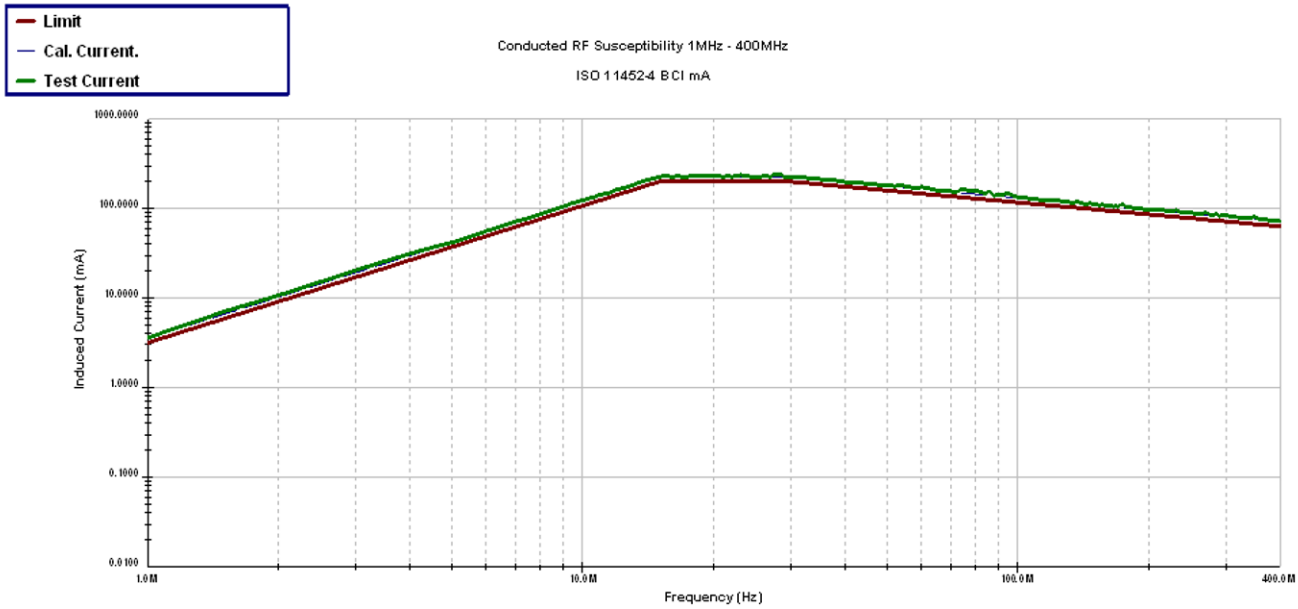


図 69. BCI Results With Current Injection Probe at 750 mm

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01429.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01429.

4.3 PCB Layout Recommendations

This section will cover the following topics:

- Layout considerations for the boost controller
- Layout considerations for the buck converter
- Layout considerations for the LDO
- Layout considerations for the CAN physical layer interface
- The board stackup
- Link to the layer plots for the PCB

4.3.1 Boost Controller Layout Considerations

To produce an optimal power solution with the LM5022-Q1, good layout and design of the PCB are as critical as component selection. The following are the several guidelines in order to create a good PCB layout:

- Using a low-ESR ceramic capacitor, place input capacitors as close as possible to the VIN and GND pins of the LM5022-Q1.
- Using a low-ESR ceramic capacitor, place output capacitors as close to the load as possible of the LM5022-Q1.
- Using a low-ESR ceramic capacitor place the VCC filtering capacitor as close to the VCC and GND pins of the LM5022-Q1.
- Minimize the loop area formed by the output capacitor connections, output diode, and sense resistor making sure the cathode of the diode and output capacitors are close to the sense resistor ground.
- The sense resistor should be connected to the CS pin with a separate trace made as short as possible. This trace should be routed away from the inductor and the switch node (where diode, FET, and inductor connect).
- Minimize the trace length to the FB pin by positioning feedback resistors close to the LM5022-Q1.
- Route the VOUT sense path away from noisy nodes and connect it as close as possible to the positive side of the output capacitors.

4.3.2 Buck Converter Layout Considerations

The following are some guidelines to follow for the TPS57140-Q1 layout:

- Providing a low-inductance, low-impedance ground path is critical. Therefore, use wide and short traces for the main current paths.
- Care should be taken to minimize the loop area formed by the input bypass capacitor, VIN pin, PH pin, catch diode, inductor, and output capacitors. Use thick planes and traces to connect these

components. For operation at a full-rated load, the top-side ground area must provide adequate heat dissipating area.

- The GND pin should be tied directly to the thermal pad under the device and the thermal pad.
- The thermal pad should be connected to any internal PCB ground planes using multiple vias directly under the device.
- The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pin as possible.
- Place the VSENSE voltage-divider resistor network away from switching node and route the feedback trace with minimum interaction with any noise sources associated with the switching components.
- The RT/CLK pin is sensitive to noise, so the RT resistor should be located as close as possible to the device and should be routed with minimal trace lengths.
- Place compensation network components away from switching components and route the connections away from noisy nodes.
- The bootstrap capacitor must be placed as close as possible to the IC pin.

4.3.3 LDO Layout Considerations

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for VIN and VOUT with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. Lastly, high-ESR capacitors may degrade PSRR performance.

4.3.4 CAN Physical Layer Layout Considerations

Because the CAN physical layer is an external wired interface and can be subjected to transients with frequencies ranging from 100s of Hz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The following are some guidelines to follow for the TCAN1042V-Q1 layout:

- TVS diodes and bus filtering capacitors should be placed as close to the onboard connectors as possible to prevent noisy transient events from propagating further into the PCB and system.
- Provide low-inductance supply and ground connections.
- Use at least two vias in parallel when connecting a power net to another layer on the PCB. This will minimize trace inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver (VCC and VIO).

4.3.5 Board Layer Stackup

The board has been designed using two layers. Both top and bottom layers have signals and power traces routed, but a majority of the bottom layer has been used for a large, low-impedance ground plane. See 表 5 for the board stackup. The board is 101.6 mm × 76.2 mm (4" × 3") and uses standard 1-oz copper foil on top and bottom layers. The total board thickness is approximately 63 mils.

表 5. TIDA-01429 Board Layer Stackup

LAYER NAME	TYPE	MATERIAL	THICKNESS (MIL)	DIELECTRIC MATERIAL	DIELECTRIC CONSTANT
Top overlay	Overlay	—	—	—	—
Top solder	Solder mask	Surface material	0.4	Solder resist	3.5
Top layer	Signal	Copper	1.4	—	—
Dielectric1	Dielectric	Core	59.2	FR-4	4.8
Bottom layer	Signal	Copper	1.4	—	—
Bottom solder	Solder mask	Surface material	0.4	Solder resist	3.5
Bottom overlay	Overlay	—	—	—	—

4.3.6 Layout Prints

To download the layer plots, see the design files at TIDA-01429.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01429.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01429.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01429.

5 Related Documentation

1. Texas Instruments, *LM5022-Q1 2.2MHz, 60 V Low-Side Controller For Boost and SEPIC*, LM5022-Q1 Datasheet (SNVSAG9)
2. Texas Instruments, *TPS57140-Q1 1.5-A 42-V Step-Down DC-DC Converter With Eco-mode™ Control*, TPS57140-Q1 Datasheet (SLVSAP3)
3. Texas Instruments, *TLV713P-Q1 Capacitor-Free, 150-mA, Low-Dropout Regulator With Foldback Current Limit for Portable Devices*, TLV71333P-Q1 Datasheet (SBVS266)
4. Texas Instruments, *TCAN1042-Q1 Automotive Fault Protected CAN Transceiver with CAN FD*, TCAN1042V-Q1 Datasheet (SLLSES9)
5. Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers*, TMS320F28030PAGQ Datasheet (SPRS584)
6. Texas Instruments, *Automotive Catalog Dual Inverter Buffer/Driver with Open-Drain Output*, SN74LVC2G06-Q1 Datasheet (SCES617)
7. Texas Instruments, *Automotive Single Inverter Gate*, SN74AHCT1G04-Q1 Datasheet (SCLS510)
8. Texas Instruments, *CSD17313Q2 30-V N-Channel NexFET™ Power MOSFET*, CSD17313Q2 Datasheet (SLPS260)

5.1 商標

6 Terminology

Body control module— An automotive electronic control unit responsible for monitoring and controlling vehicle loads. Some examples include interior lighting, exterior lighting, heating ventilation and air conditioning (HVAC), powered windows, and powered door locks.

Controller— The term controller is used when referring to a power regulator that has external FETs.

Converter— The term converter is used when referring to a power regulator that has integrated FETs.

Discrete SBC— The term Discrete SBC (System Basis Chip) is used to refer to the discrete implementation of functional blocks that are commonly integrated into a single IC. This includes power and networking blocks.

Non-synchronous — When used in reference to a power regulator, this term means that the regulator uses one FET and one diode for power conversion.

Synchronous — When used in reference to a power regulator this term means that the regulator uses two FETs for power conversion. By using a second FET instead of an external diode power losses can be reduced improving overall efficiency.

7 About the Author

JOHN P. GRIFFITH is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, John specializes on body control modules and gateway modules, creating end equipment block diagrams, and reference designs for automotive customers. John earned his bachelor of science and master of science in electrical engineering from Rochester Institute of Technology in Rochester, New York.

リビジョンAの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年7月発行のものから更新 **Page**

- 「*TIDA-01429リファレンス・デザインには、広い入力電圧範囲の昇圧コントローラに続いて、広い入力電圧範囲で8Vに設定された昇圧コンバータを含む、ディスクリート・システム・ベース・チップ(SBC)が実装されています。昇圧コンバータの後には、広い入力電圧範囲の5V固定降圧コンバータが続き、C2000™ マイクロコントローラ(MCU)へ電力を供給するための小型の3.3V固定リニア・ドロップアウト(LDO)レギュレータや、コントローラ・エリア・ネットワーク(CAN)トランシーバなどの駆動に使用されます。*」を「*TIDA-01429リファレンス・デザインは、広い入力電圧範囲の昇圧回路を持ち、出力電圧が8Vに設定されていてるディスクリート・システム・ベース・チップ(SBC)を実装します。昇圧回路の後に、広い入力電圧範囲を持ち、出力電圧が5Vに設定されている降圧コンバータが続き、C2000™ マイクロコントローラ(MCU)へ電力を供給するための小型の3.3V固定リニア・ドロップアウト(LDO)レギュレータや、コントローラ・エリア・ネットワーク(CAN)トランシーバなどの駆動に使用されます。*」に 変更 1

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。