参考資料

TI Designs: TIDA-01444
サーバーPSU用の、97%効率、180W、デュアル・チャネル降圧コンバータのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDA-01444デザインは、サーバーPSU、PC PSU、その他降圧コンバータのアプリケーション用で、180Wのデュアル・チャネル降圧DC/DCコンバータとレギュレートされた12V DC入力電圧を実装し、97%を超える効率と優れた熱性能で末端負荷電圧を提供します。デュアル・チャネル間で、スイッチング周波数の同期を簡単に実現できます。デュアル出力の真の差動リモート・センスにより、ラインの電圧降下が補償され、末端負荷についてより正確な電圧が得られます。この統合回路リファレンス・デザインは、より高い電力密度と低いプロファイルを実現するため、従来のディスクリート・インダクタの代わりに、平面状のインダクタを使用しています。このTIデザインには、完全な保護および温度センス機能が搭載されています。

リソース

TIDA-01444	デザイン・フォルダ
TPS543C20	プロダクト・フォルダ
LM20BIM7	プロダクト・フォルダ
TL431BQDBZR	プロダクト・フォルダ

TI E2E™ Community

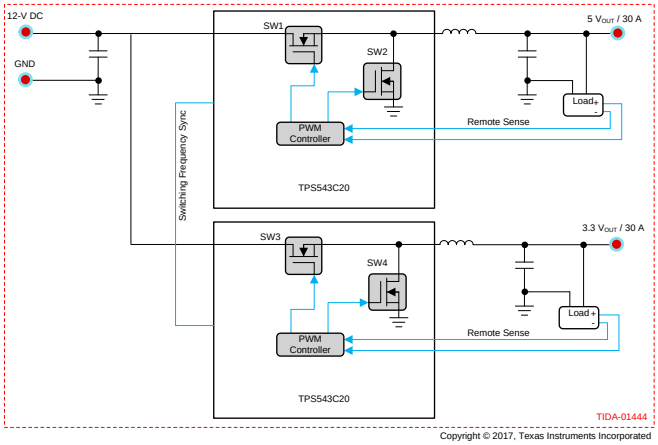
E2Eエキスパートに質問

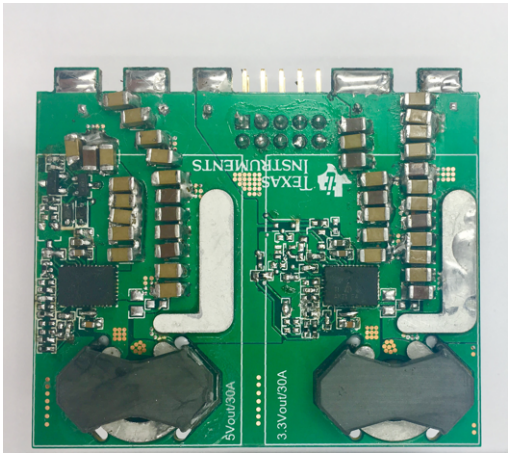
特長

- ハイサイドとローサイドのMOSFETを内蔵したデバイスのTPS543C20を使用して設計
- 少ないBOM数
- 入力電圧: 11.4V、12V、12.6V
- 効率: 180W負荷で96% (標準値)、83W負荷で97% (標準値)
- 両方の出力チャネルにおける差動リモート・センシング
- デュアル・チャネル間でのスイッチング周波数の同期
- ロスなしのローサイドMOSFET電流センシングと熱補償
- 保護: 出力OVP、UVP、OCP
- 平面状のインダクタを出力インダクタとして使用
- 小さな外形(47mm×59mm)により、サーバーPSUアプリケーションと互換

アプリケーション

- サーバーのPSU
- PCのPSU
- 非絶縁DC-DCモジュール
- 産業用電源





1 System Description

In server power supply units (PSUs) and PC PSU applications, the outputs are always configured with three groups of output voltage: 12-V DC, 5-V DC, and 3.3-V DC. Generally, in order to realize the high efficiency and excellent cross voltage regulation performance, 12-V DC is obtained from the front-end PFC stage and isolated DC-DC stage, and 5-V DC or 3.3-V DC is obtained through the dual-channel buck converter from 12-V DC. A typical block diagram of a server PSU system is shown in 図 1.

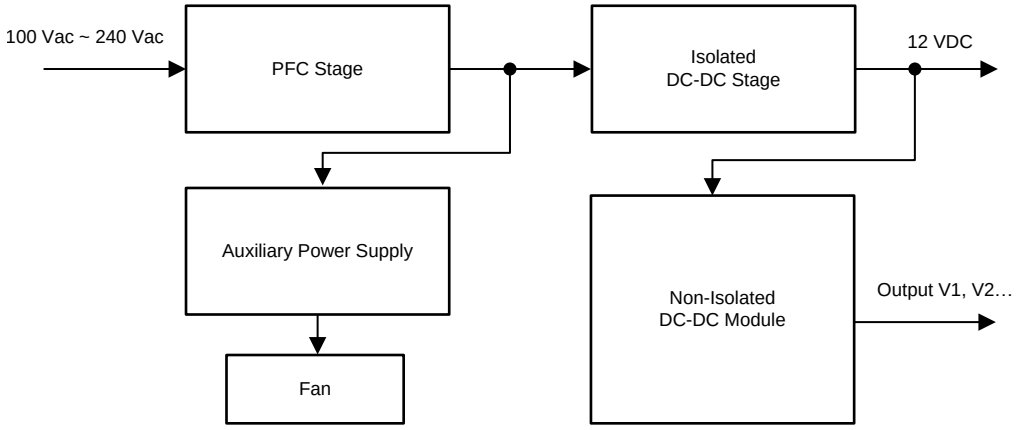


図 1. Typical Block Diagram of Server Power Supply

High efficiency, high power density, and excellent performance are the most important pursues of a switching power supply as well as in server and PC PSU applications. A high efficiency requirement means excellent component properties and excellent design capability; a high power density requirement means higher component integration; and a high performance requirement means reasonable design specification. The TIDA-01444 reference design is exactly based on this design thought. The high efficiency, high power density, and excellent performance of the TIDA-01444 design can meet the requirements for server and PC PSU applications.

The TIDA-01444 design is a 180-W buck module that converts the typical input voltage of 12-V DC to dual outputs 3.3 V_{OUT} and 5 V_{OUT}. This TI Design is designed specially to meet a high efficiency of > 97% at a typical load of 83 W and > 96% at a full load of 180 W, fewer BoM components, low profile requirement, true differential remote sense function, and switching frequency synchronization between dual-channel and excellent output voltage regulation of < 1%. It is important that each of these two outputs has a maximum 30-A output current capability. This reference design is a simple construction, low-component, dual-output buck converter implemented using the TPS543C20 device with integrated high-side and low-side MOSFETs with low-loss switching to facilitate high efficiency and deliver up to 40 A in a 5-mm×7-mm PowerStack™ package with a layout friendly thermal pad. The design operates the typical 12-V DC input voltage, delivering a total power of 180 W.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input voltage (V_{IN})	—	11.4	12.00	12.6	V
Maximum input current (I_{IN_MAX})	—	15.5	15.95	16.5	A
OUTPUT CHARACTERISTICS					
Output voltage	Output channel 1	—	3.3	—	V
	Output channel 2	—	5	—	V
Output voltage set point	Both for 3.3 V_{OUT} and 5 V_{OUT}	1	0	1	%
Maximum output current	Both for 3.3 V_{OUT} and 5 V_{OUT}	—	—	30	A
Load regulation	Both for 3.3 V_{OUT} and 5 V_{OUT}	1	0	1	%
Ripple and noise	V_{OUT} = 5-V DC	5	30	50	mV
	V_{OUT} = 3.3-V DC	5	20	30	mV
Output transient response	5 V_{OUT}: 30-A step, 0.5 A/µs	–250	0	250	mV
	3.3 V_{OUT}: 30-A step, 0.5 A/µs	–165	0	165	mV
Start-up time	Both for 3.3 V_{OUT} and 5 V_{OUT}	8	12	20	ms
Output OVP	Both for 3.3 V_{OUT} and 5 V_{OUT}	113	117	121	%
Output UVP	Both for 3.3 V_{OUT} and 5 V_{OUT}	79	83	87	%
Output OCP	Both for 3.3 V_{OUT} and 5 V_{OUT}	35	40	45	A
SYSTEM CHARACTERISTICS					
Maximum output power	Any combination			180.0	W
Efficiency	I_{OUT} = 10 A for 3.3 V_{OUT} and 5 V_{OUT}	96.5	97.0	97.5	%
	I_{OUT} = 21.7 A for 3.3 V and 5 V	96	96.4	97.0	%
Switching frequency (f_{SW})	—	—	500.0	—	kHz
Operating ambient temperature	200FLM Airflow	–10	—	65.0	°C
EMI/CE	EN55032 Class A	6	10.0	—	dB

2 System Overview

2.1 Block Diagram

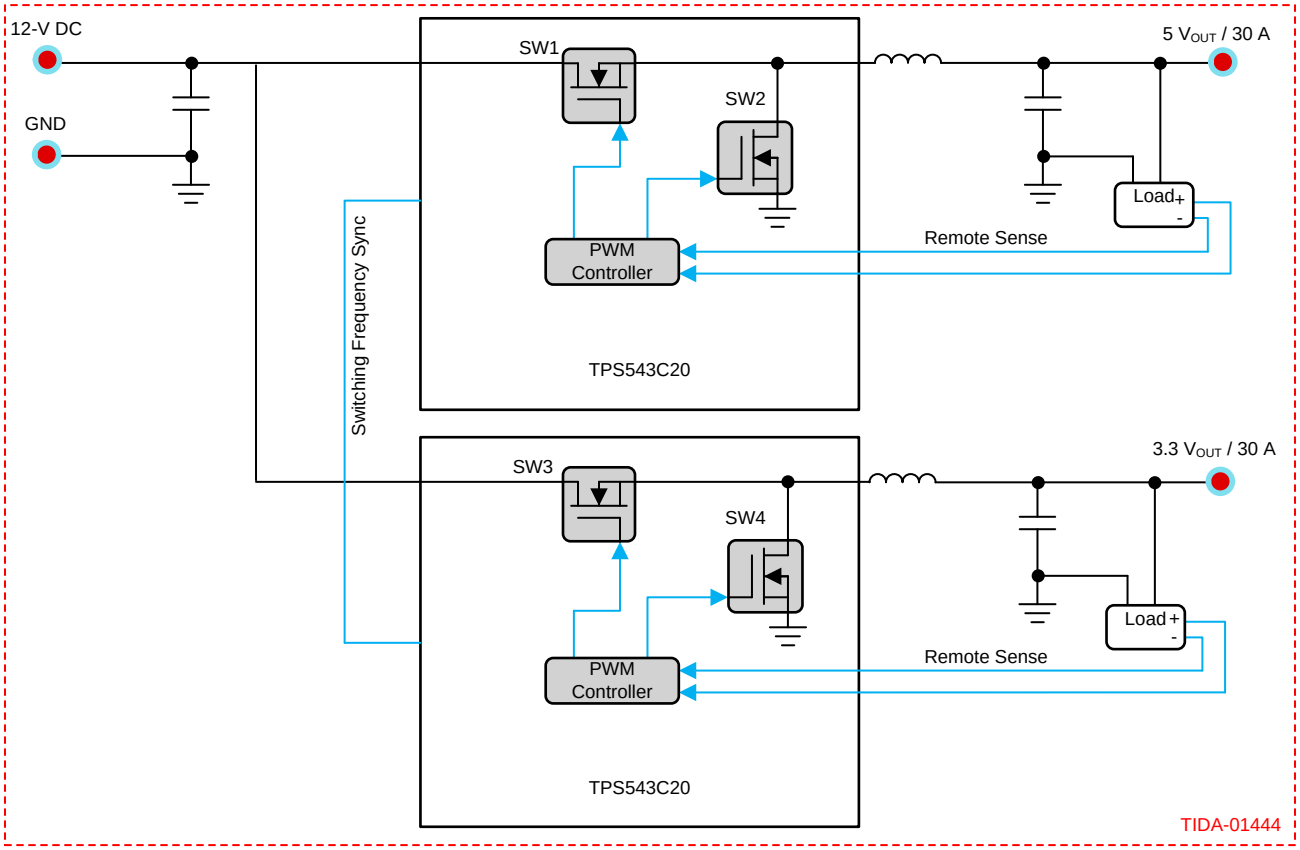


図 2. Block Diagram of 180-W Dual Buck Module

2.2 Highlighted Products

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. See their respective product datasheet for complete details on any highlighted device.

2.2.1 TPS543C20

To implement the high-performance, small form factor, dual-channel buck design of 180 W of power, the TPS543C20 is the preferred converter as it is a synchronous buck converter with two integrated N-channel NexFET™ power MOSFETs, enabling high power density and small PCB layout area. The TPS543C20 employs an internally compensated emulated peak current mode control, with a clock with a synchronizable, fixed frequency modulator for EMI sensitive point-of-load (POL). The internal integrator and directly amplifying ramp tracking loop eliminate the need for external compensation over a wide range of frequencies thereby making the system design flexible, dense, and simple. Optional asynchronous pulse injection (API) and Body Braking help improve transient performance by significantly reducing undershoot and overshoot, respectively. Integrated NexFET MOSFETs with low-loss switching facilitate high efficiency and deliver up to 40 A in a 5-mm×7-mm PowerStack package with a layout friendly thermal pad. Two TPS543C20 devices can be stacked together to provide up to 80-A POL.

The key features that make this device unique are:

- Integrated 3.0/0.9-mΩ Stacked NexFET Power
- Internally-compensated advanced current mode control 40-A POL
- Input voltage range: 4 to 16 V
- Output voltage range: 0.6- to 5.5-V stage with lossless low-side current sensing
- Fixed frequency: Synchronization to an external clock or sync out
- Stack 2× for up to 80 A with current share, voltage share, and CLK sync
- Pin strapping programmable switching frequency:
  - 300 kHz to 2 MHz for standalone
  - 300 kHz to 1 MHz for stackable
- Pin strapping programmable reference from 0.6 to 1.1 V with 0.5% accuracy
- Differential remote sensing
- Safe start-up into pre-biased output
- High accuracy hiccup current limit
- Asynchronous pulse injection (API) and body braking
- 40-pin, 5-mm×7-mm LQFN Package with a 0.5-mm pitch and a single thermal pad

2.2.2 TL431BQDBZR

The TL431 is a three-terminal adjustable shunt regulator with specified ranges for thermal stability over temperature. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in many applications. The "B-grade" version comes with initial tolerances (at 25°C) of 0.5% and TL431BQ devices are characterized to operate from –40°C to 125°C.

The key features that make this device unique are:

- I_{OUT}: 300 mA
- Low-power I_Q: 31 µA
- V_{OUT}: 2% accurate
- Low output noise: 48 mV_{RMS} (no bypass capacitor required)
- High PSRR: 68 dB at 1 kHz

2.2.3 LM20BIM7

The LM20 is a precision analog output CMOS integrated-circuit temperature sensor that operates over −55°C to 130°C. The power supply operating range is 2.4 to 5.5 V. The transfer function of LM20 is predominately linear, yet has a slight predictable parabolic curvature. The accuracy of the LM20 when specified to a parabolic transfer function is ±1.5°C at an ambient temperature of 30°C. The temperature error increases linearly and reaches a maximum of ±2.5°C at the temperature range extremes. The temperature range is affected by the power supply voltage. At a power supply voltage of 2.7 to 5.5 V, the temperature range extremes are 130°C and −55°C. Decreasing the power supply voltage to 2.4 V changes the negative extreme to −30°C, while the positive extreme remains at 130°C.

The LM20 quiescent current is less than 10 µA. Therefore, self-heating is less than 0.02°C in still air. Shutdown capability for the LM20 is intrinsic because its inherent low-power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown.

The key features that make this device unique are:

- Rated for −55°C to 130°C
- Available in SC70 and DSBGA package
- Predictable curvature error
- Suitable for remote applications
- Accuracy at 30°C ±1.5°C to 4°C (maximum)
- Accuracy at 130°C and −55°C ±2.5°C to 5°C (maximum)
- Power supply voltage range: 2.4 to 5.5 V
- Current drain: 10 µA (maximum)
- Nonlinearity: ±0.4% (typical)
- Output impedance: 160 Ω (maximum)
- Load Regulation: 0 µA < IL < 16 µA –2.5 mV (maximum)

2.3 System Design Theory

This reference design is a dual-channel output 180-W buck module, operating at a regulated DC input voltage of 12-V DC. The design has two buck power stages implemented using two pieces of the TPS543C20 integrated a with high-side MOSFET and low-side MOSFET to deliver two different outputs: 3.3 V_{OUT}/30 A and 5 V_{OUT}/30 A. The overall system efficiency is over 96% with a 12-V DC input under full load conditions. The design has protection built-in for output overcurrent protection (OCP), output short-current protection (OSCP), undervoltage protection (UVP), and overvoltage protection (OVP). The true differential remote sensing compensates the line voltage drop and provides more accurate voltage for terminal load.

In this TI Design, there would be no π frequency issue for the switching frequency difference between the dual-channel converter. Because of the switching frequency, synchronization is accomplished easily between dual-channel as the customer's expectation, which can resolve the π frequency noise issue for EMI. However, it could decrease the filter inductor and capacitor, which are needed for resolving the π frequency issue. So from this point, the switching frequency synchronization can decrease the total cost and improve the whole efficiency and power density.

2.3.1 Buck Circuit Component Design

This section details the design process and component selection a designer must follow to complete a buck converter using the TPS543C20.

2.3.1.1 Design Goal Parameters

表 2 states the design goal parameters for this TI Design. These parameters are used in further calculation to select components.

表 2. Design Goal Parameter

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input voltage (V_{IN})	—	11.4	12.00	12.6	V
Maximum input current (I_{IN_MAX})	—	15.5	15.95	16.5	A
OUTPUT CHARACTERISTICS					
Output voltage	Output channel 1	—	3.3	—	V
	Output channel 2	—	5.0	—	V
Output voltage set point	Both for 3.3 V_{OUT} and 5 V_{OUT}	1.0	0	1.0	%
Maximum output current	For both channels	0	—	30.0	A
Maximum output power	Any combination	—	—	180.0	W
Efficiency	I_{OUT} = 10 A for 3.3 V_{OUT} and 5 V_{OUT}	96.5	97.0	97.5	%
	I_{OUT} = 21.7 A for 3.3 V_{OUT} and 5 V_{OUT}	96.0	96.4	97.0	%

2.3.1.2 Output Inductor Selection

The inductor is typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE}). Given this target ripple current, the required inductor value can be calculated by 式 1:

$$L_O = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

In this TI Design, in order to decrease the design profile and save cost, the output inductor uses the planner inductor to replace the traditional finished inductor.

Based on the calculation and analysis, the output inductor typical value can be set as 0.65 µH for dual-channel, using RM7 size core with DMR95 material, and the inductor winding are two turns. The RMS current through the inductor is calculated by 式 2. The 3.3-V channel and 5-V channel RMS current through inductor are approximated by 式 3 and 式 4, respectively:

$$I_{L(RMS)} = \sqrt{I_{L(AVG)}^2 + \frac{1}{12} \times I_{RIPPLE}^2} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{RIPPLE}^2} \quad (2)$$

$$I_{3.3V\_L(RMS)} = \sqrt{30^2 + \frac{1}{12} \times 7.362^2} \approx 30.074 \text{ A} \quad (3)$$

$$I_{5V\_L(RMS)} = \sqrt{30^2 + \frac{1}{12} \times 8.974^2} \approx 30.109 \text{ A} \quad (4)$$

Also, this inductor design can ensure the inductor will not be saturated before the setting OCP.

2.3.1.3 Switching Frequency Selection

Select a switching frequency for the TPS543C20. There is a trade-off between higher and lower switching frequencies. A higher switching frequency may produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impact thermal performance.

This TI Design features a switching frequency of 500 kHz achieves both a small solution size and a high efficiency operation. The device supports continuous switching frequency programming (see 式 5).

$$R_{Rt} = \frac{20 \times 10^9}{f_{SW}} - 2 \times \frac{f_{SW}}{2000} \quad (5)$$

In this case, considering the frequency setting tolerance, a standard resistor value of 43.2 kΩ is selected. The switching frequency configuration for a standalone device is shown in 図 3; the MODE pin keeps no external resistor, and the RT pin sets the switching frequency.

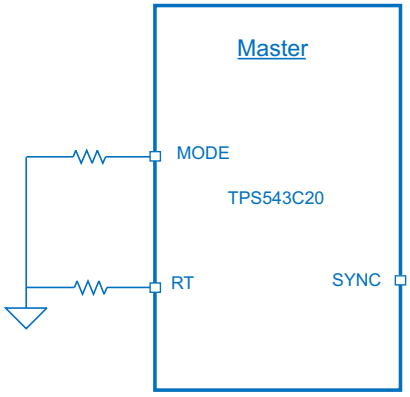


図 3. Stand-alone: RT Pin Sets Switching Frequency

2.3.1.4 Switching Frequency Synchronization Configuration

Many applications require synching the switching frequency for multiple outputs to resolve some unexpected issues. In this TI Design, the dual outputs are configured with the same frequency through the frequency synchronization function.

The TPS543C20 device can synchronize to an external clock, which must be equal to or higher than internal frequency setting. For a standalone device, the external clock must be applied to the SYNC pin. A sudden change in synchronization clock frequency causes an associated control loop response, resulting in an overshoot or undershoot on the output voltage.

The switching frequency synchronization configuration is accomplished through MODE and RT pin, as shown in 表 3:

表 3. MODE Pin-Strapping Selection

CONTROL MODE SELECTION	API OR BODY BRAKE	RESISTOR VALUE (kΩ)(1)	NOTE
Stand-alone	API OFF	Open	Sync pin to receive clock RT pin to set frequency
	BB OFF		
	API ON	15.4	
	BB OFF		
	API ON, BB OFF API threshold setting	121 (1×)	
		187 (2×)	
		8.66 (3×)	
		78.7 (4×)	
(Master sync out)	API OFF, BB OFF	23.7	Sync pin to send out clock RT pin to set frequency
(Master sync in)		34.8	Sync pin to receive clock RT pin to set sync point
(Slave sync out)		51.1	Sync pin to receive clock RT pin to set sync point

(1) The E48 series resistors with a tolerance of 1% or less are recommended.

For this application, the configuration principle is as follows: set one output channel as Stand-alone control mode, and set the other output as Master Sync In control mode. In this TI Design, the 5-V output channel is configured as the Stand-alone control mode to generate a switching frequency of 500 kHz, and then the 3.3-V output channel is configured as Master Sync In control mode to be synchronized with the 5-V output channel.

The detail configuration for MODE pin and RT pin is as follows:

1. 5-V output channel (5Vout-CH): Set the MODE pin to be open. Set the RT pin to be a 43.2-kΩ resistor;
2. 3.3-V output channel (3.3Vout-CH): Set the MODE pin to be a 34.8-kΩ resistor. Set the RT pin to be a resistor higher than 43.2 kΩ. This resistor selection is used to generate the switching frequency, which should be lower than the target switching frequency (F_SW < f_sw).

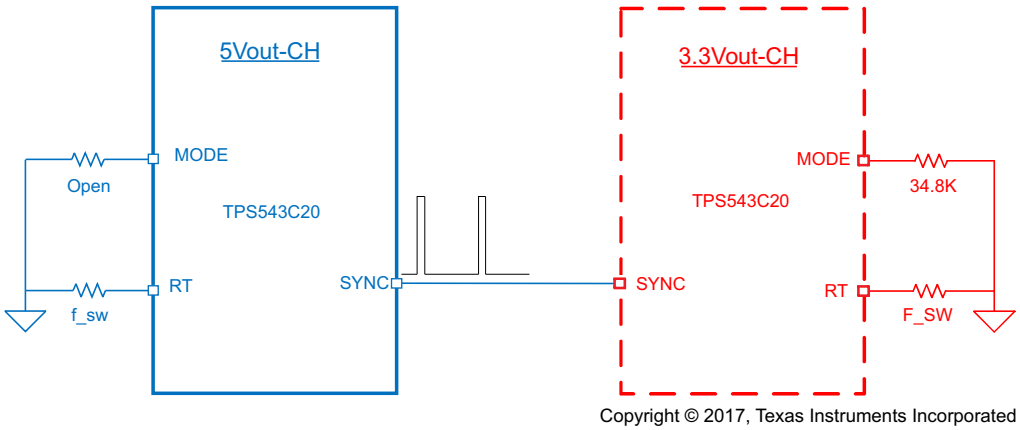


図 4. Switching Frequency Synchronization Configuration for Dual-Channel Converter

表 4 shows the configuration for these two pins of the converter:

表 4. MODE and RT Pin Configuration on TIDA-01444

CONFIGURATION	MODE PIN RESISTOR	RT PIN RESISTOR	NOTES
5-V_{OUT} channel	Open	43.2K	Set real switching frequency
3.3-V_{OUT} channel	34.8K	Higher than 43.2 kΩ (for example, 68.1 kΩ)	Set as master sync in

2.3.1.5 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects these three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

This TI Design features the following:

- 5-V output channel: 13pcs 16-V/22-µF X7R ceramic capacitor and 1pcs 16-V/1000-µF OSCON capacitor
- 3.3-V output channel: 14pcs 16-V/22-µF X7R ceramic capacitor and 1pcs 16-V/1000-µF OSCON capacitor

2.3.1.6 Feedback Loop Compensation

The RAMP pin sets internal ramp amplitude for the control loop compensation. RAMP amplitude is determined by internal RC, selected by the resistor connected from the MODE pin to GND, to optimize the control loop (see 表 5).

表 5. RAMP Pin-Strapping Selection

CRAMP (pF)	RESISTOR VALUE (kΩ)(1)
1.00	0
1.42	8.66
1.94	15.40
2.58	23.70
3.43	34.80
4.57	51.10
6.23	78.70
8.91	121.00
14.10	187.00
29.10	Open

(1) The E48 series resistors with a tolerance of 1% or less are recommended.

A certain criteria is recommended for the TPS543C20 to achieve optimized loop stability, bandwidth, and switching jitter performance. The internal ramp voltage should be two to four times bigger than the output capacitor ripple (capacitive ripple only). The TPS543C20 is defined to be ease-of-use, for most applications, we recommend ramp resistor to be 187 kΩ to achieve the optimized jitter and loop response. For a detailed design procedure, see the WEBENCH® Power Designer.

Through debugging results, this TI Design uses 187 kΩ for the 5-V_{OUT} channel and 51.1 kΩ for the 3.3-V_{OUT} channel at the RAMP pin.

2.3.1.7 BP and VDD

Bypass the BP pin to PGND with 4.7 µF of capacitance. In order for the regulator to function properly, it is important that these capacitors be localized to the TPS543C20 with low-impedance return paths.

For VDD decoupling capacitor, the TPS543C20 device requires a high-quality, ceramic, type X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the VDD pin, relative to AGND.

This TI Design uses a 4.7-µF ceramic capacitor for BP and 2.2-µF ceramic capacitor for VDD.

For more information, see the TPS543C20 datasheet[1].

2.3.1.8 Voltage Reference

The VSEL pin strap is used to program initial boot voltage value from 0.6 to 1.1 V by the resistor connected from VSEL to AGND. The initial boot voltage is used to program the main loop voltage reference point. VSEL voltage settings provide TI designated discrete internal reference voltages. 表 6 lists internal reference voltage selections.

This TI Design uses 1 V as its reference voltage, so the VSEL pin keeps open.

表 6. VSEL Pin Configuration

DEFAULT V_{REF} (V)	RESISTOR VALUE (kΩ)(1)
0.60	0
0.70	8.66
0.75	15.40
0.80	23.70
0.85	34.80
0.90	51.10
0.95	78.70
1.00	Open
1.05	121.00
1.10	187.00

(1) The E48 series resistors with a tolerance of 1% or less are recommended.

2.3.1.9 RSP/RSN Remote Sense Function

RSP and RSN pins are used for remote sensing purpose. If feedback resistors are required for output voltage programming, the RSP pin should be connected to the mid-point of the resistor divider and the RSN pin should always be connected to the load return.

In a lower output voltage application, as the VSEL programs the output voltage set point, the feedback resistors are not required. Because of this, the RSP pin could be connected to the positive sensing point of the load and the RSN pin could be connected to the load return.

RSP and RSN pins are extremely high-impedance input terminals of the true differential remote sense amplifier. The feedback resistor divider should use resistor values much less than 100 kΩ. A standard is to use a 10-kΩ lower divider resistor and then size the upper resistor to achieve the desired ratio.

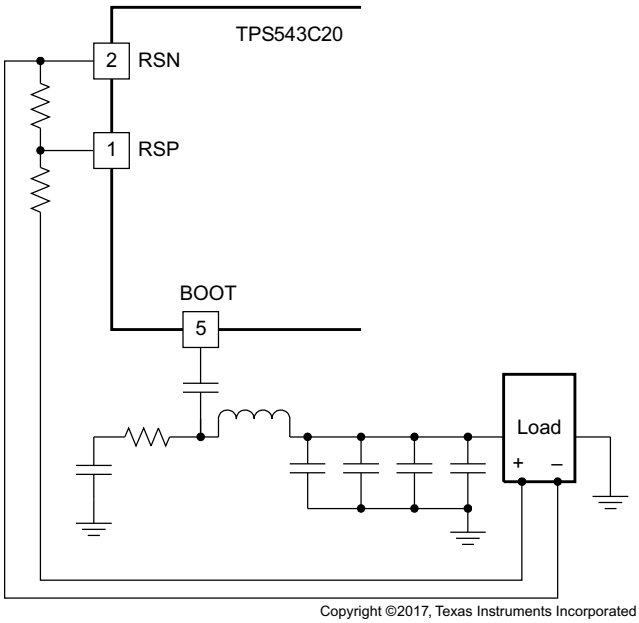


図 5. Remote Sensing With Feedback Resistors

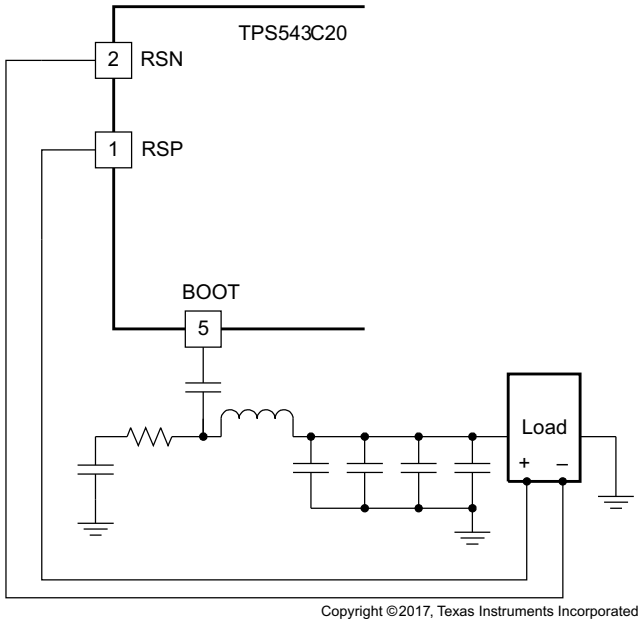


図 6. Remote Sensing Without Feedback Resistors

2.3.1.10 Auxiliary Power Supply

VDD is the controller power supply input and can be connected to PVIN directly to obtain the power supply easily. In this TI Design, in order to decrease the power loss, instead of from PVIN directly, VDD is configured with an external auxiliary power supply circuit which is mainly composed by TL431BQDBZR.

The operation principle is that after the PVIN is built, this auxiliary power supply circuit will produce a voltage that is just lower a bit than 5 V to provide the start-up voltage for the TPS543C20. When the 5-V output voltage is built successfully, this 5-V output voltage will take control for providing the energy for the TPS543C20 internal circuit operation.

As a result, this auxiliary power supply only provides the operation current for the TPS543C20 during the start-up process. After the 5-V output voltage is built, this auxiliary power supply circuit will be kept at a standby state.

2.3.1.11 Low-Side MOSFET Overcurrent Protection

The TPS543C20 uses the ILIM pin to set the OCP level. The ILIM pin should be connected to AGND through the ILIM voltage setting resistor, R_{ILIM}. The ILIM terminal sources I_{ILIM} current, which is around 11.2 μA typically at room temperature, and the ILIM level is set to the OCP ILIM voltage, V_{ILIM}. In order to provide both good accuracy and a cost-effective solution, the TPS543C20 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. Also, the TPS543C20 performs both positive and fixed negative inductor current limiting. The inductor current is monitored by the voltage between GND pin and SW pin during the OFF time. ILIM has 1200 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. The GND pin is used as the positive current sensing node. The device has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state, and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent ILIM level. V_{ILIM} sets the peak level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in 式 6:

$$I_{OCP} = \frac{V_{ILIM}}{16 \times R_{DS(on)}} - \frac{I_{IND(ripple)}}{2} = \frac{V_{ILIM}}{16 \times R_{DS(on)}} - \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (6)$$

Where

- $R_{DS(on)}$ is the on-resistance of the low-side MOSFET. $R_{DS(on)}$ must be 0.68 mΩ to calculate OCP

式 6 is valid for VDD ≥ 5 V.

If an overcurrent event is detected in a given switching cycle, the device increments an overcurrent counter. When the device detects three consecutive overcurrent (either high-side or low-side) events, the converter responds, entering continuous restart hiccup. In continuous hiccup mode, the device implements a 7 soft-start cycle time-out, followed by a normal soft-start attempt. When the overcurrent fault clears, normal operation resumes; otherwise, the device detects overcurrent and the process repeats.

2.3.1.12 High-Side MOSFET Overcurrent Protection

The device also implements a fixed high-side MOSFET OCP to limit the peak current at 60 A and prevent inductor saturation in the event of a short circuit. The device detects an overcurrent event by sensing the voltage drop across the high-side MOSFET during ON state. If the peak current reaches the IHOSC level on any given cycle, the cycle terminates to prevent the current from increasing any further. High-side MOSFET overcurrent events are counted. If the devices detect three consecutive overcurrent events (high-side or low-side), the converter responds by entering continuous restart hiccup.

2.3.1.13 Output Overvoltage and Undervoltage Protection

The TPS543C20 device configures with both output OVP and output UVP capabilities. The device compares the RSP pin voltage to internal selectable pre-set voltages. If the RSP voltage with respect to RSN voltage rises above the output OVP threshold, the device terminates normal switching and activates the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. Then, the device enters continuous restart hiccup.

If the RSP pin voltage falls below the UVP level, after soft-start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, then enters hiccup timeout delay prior to restart.

2.3.1.14 Temperature Sensing

In this TI Design, the temperature sensing is accomplished through the LM20BIM7 device, which provides a continuous analog voltage respecting the temperature information. A pin from the LM20BIM7 is used to connect with the system board to deliver temperature information to the customer's system.

An internal temperature sensor in the TPS543C20 protects the devices from thermal runaway. The internal thermal shutdown threshold, TSD, is fixed at 165°C typical. When the devices sense a temperature above TSD, power conversion stops until the sensed junction temperature falls by the thermal shutdown hysteresis amount. Then, the part starts up again.

3 Hardware, Testing Requirements, and Test Results

3.1 Test Equipment Needed to Validate Board

The required test equipment include:

- DC source
- Digital oscilloscope
- True RMS multimeter (×4)
- Electronic load (×2)
- Thermal imager

3.2 Test Conditions

For the input feature, the DC source must be capable of providing 12-V DC, and the total output power must be high than 360 W. Set the input current limit to 30 A.

For the output feature, connect an electronic load to each channel output. The load must be variable and capable of 45 A for both the 3.3-V and 5-V output channels.

3.3 Test Procedure

1. Solder wires from the DC input terminals of the reference boards, and then connect to an adjustable DC source, maintaining correct polarity. The input line should be capable of enduring a 20-A current.
2. Solder wires from output terminals of the reference boards, and then connect them to the electronic load, maintaining correct polarity. The output line should be capable of enduing higher than a 30-A current.
3. Set the limit input DC source current 0.2 A with open load for the first time power on.
4. Turn on the input DC source with 12-V DC.
5. Observe the startup conditions for smooth switching waveforms.
6. Increase the input current limit to 30 A, and then increase the output load current for the 3.3-V and 5-V output channels.
7. Observe the output voltage waveform to verify it works normally. The user can check the performance of power supply by electronic load for each output channel, specified as < 30 A.
8. Cool the module with a fan to prevent the module from overheating.

3.4 Testing and Results

The test results are divided into multiple sections that cover the performance data, performance curve, functional waveforms, transient performance waveforms, and thermal measurements.

3.4.1 Performance Data

3.4.1.1 Efficiency and Regulation with Load Variation

表 7 and 表 8 show the efficiency performance data at start-up and steady state.

注: There is an external fan to cool the module.

表 7. Efficiency Performance at Start-up State

V_{IN} (V)	I_{IN} (A)	V_{OUT1} (V)	I_{OUT1} (A)	VOUT2 (V)	I_{OUT2} (A)	P_{IN} (W)	P_{OUT} (W)	EFF (%)
11.94	2.201171	5.020	2.9943	3.325	2.985	26.28198	24.95651	94.95674
11.91	4.334387	5.019	5.9887	3.324	5.970	51.62255	49.90157	96.66621
11.88	6.489858	5.018	8.9850	3.323	8.955	77.09951	74.84420	97.07480
11.85	8.679107	5.018	11.9770	3.322	11.973	102.84740	99.87489	97.10977
11.81	10.886640	5.017	14.9740	3.321	14.955	128.57120	124.79010	97.05917
11.78	13.122780	5.016	17.9700	3.321	17.940	154.58630	149.71630	96.84962
11.73	15.919640	5.015	21.6560	3.320	21.630	186.73740	180.41640	96.61504

表 8. Efficiency Performance at Steady State

V_{IN} (V)	I_{in} (A)	V_{OUT1} (V)	I_{OUT1} (A)	V_{OUT2} (V)	I_{OUT2} (A)	P_{IN} (W)	P_{OUT} (W)	EFF (%)
11.94	2.204350	5.025	2.9906	3.325	2.9925	26.26775	24.97783	94.90078
11.91	4.337169	5.024	5.9868	3.323	5.9737	51.60835	49.92829	96.65595
11.89	6.487871	5.024	8.9812	3.322	8.9587	77.14078	74.88235	97.07232
11.86	8.677517	5.023	11.9730	3.320	11.9770	102.91540	99.90402	97.07397
11.83	10.885050	5.022	14.9700	3.319	14.9580	128.77010	124.82490	96.93628
11.80	13.122380	5.021	17.9660	3.318	17.9430	154.84410	149.74220	96.70512
11.75	15.926400	5.021	21.6500	3.317	21.6330	187.13520	180.46130	96.43366

3.4.1.2 Load Regulation

This reference design configures with a remote sense function. Comparing the output test results of load regulation shows the excellent performance when implements the remote sense function.

注: The output voltage is based on the test point of the terminal load voltage.

表 9. Load Regulation Performance between Local and Remote Sense

LOAD CONDITION	3.3 V_{OUT}		5 V_{OUT}	
	LOCAL SENSE	REMOTE SENSE	LOCAL SENSE	REMOTE SENSE
0 A	3.325	3.308	5.027	5.008
15 A	3.252	3.306	4.948	5.007
30 A	3.176	3.305	4.870	5.006
Regulation	149 mV	3 mV	187 mV	2 mV

3.4.2 Performance Curves

3.4.2.1 Efficiency With Load Variation

図 7 shows the efficiency curve of this reference design. For the efficiency test, 3.3 V_{OUT} and 5 V_{OUT} have the same load current, and the total maximum output power is 180 W. This test shows the overall unit efficiency feature at the start-up state and steady state separately.

注: There is a fan to cool the module.

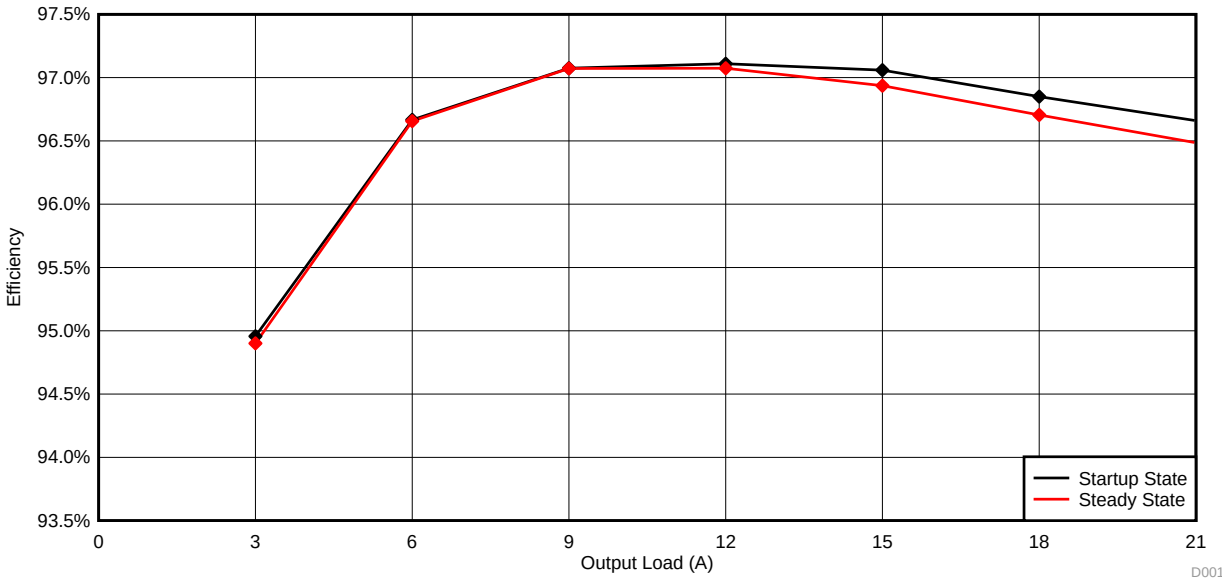


図 7. Overall Unit Efficiency Curve versus Output Load Current

図 8 shows the efficiency curve, which is based on 3.3 V_{OUT} and 5 V_{OUT} independently at the start-up state with a maximum output current of 30 A for each channel.

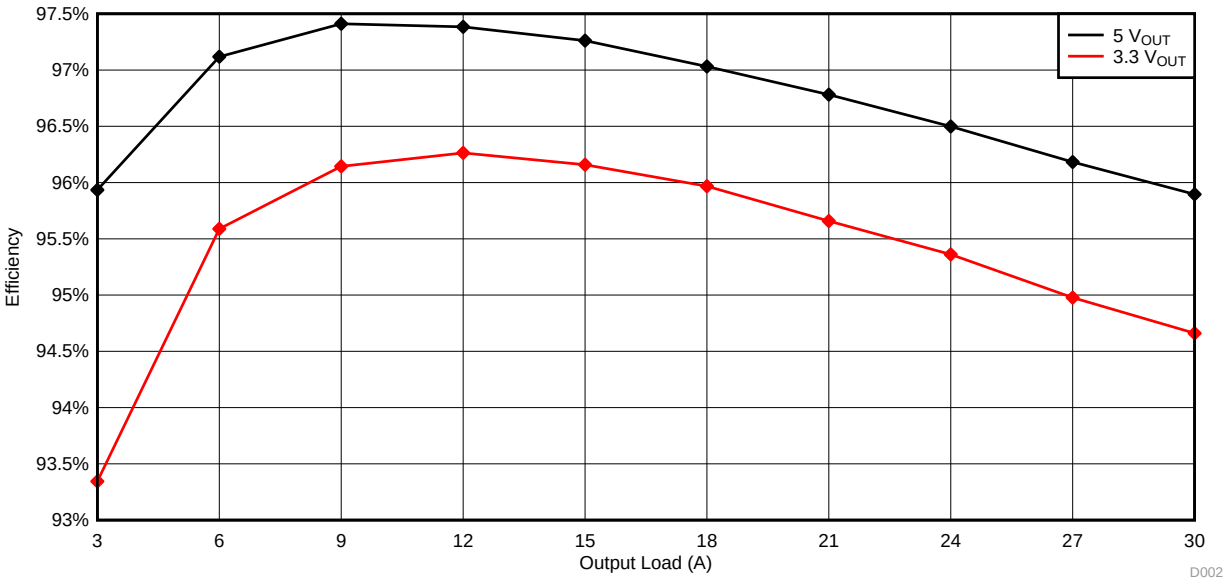


図 8. Efficiency Curve versus Output Load Current for 3.3 V_{OUT} and 5 V_{OUT} Independently

3.4.2.2 Load Regulation

図 9 shows the measured load regulation of the 3.3-V_{OUT} and 5-V_{OUT} channels.

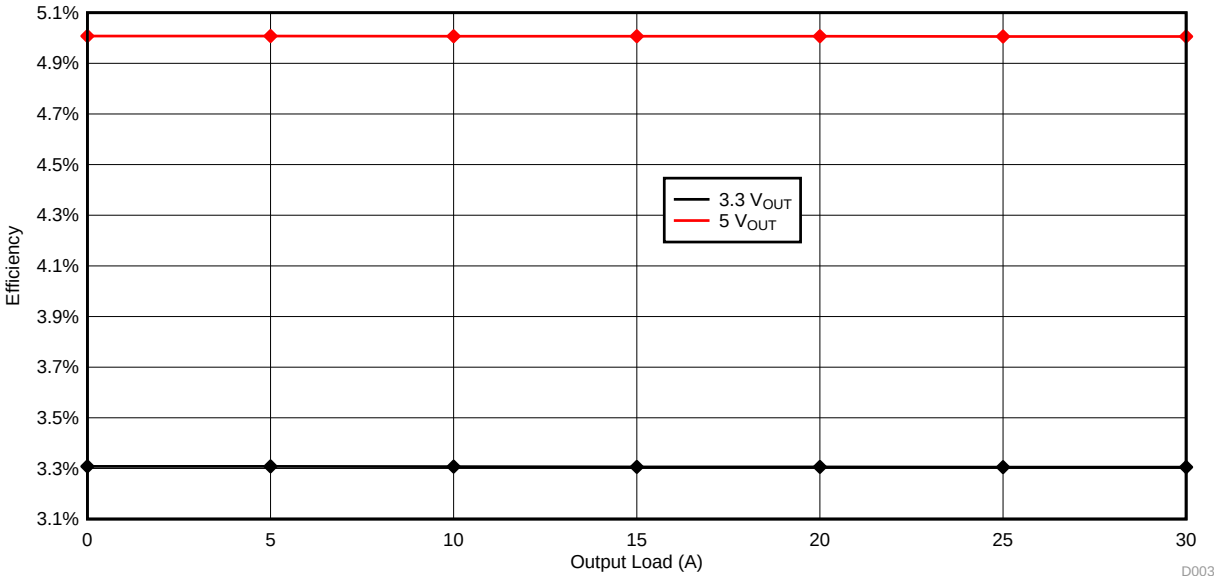


図 9. Output Voltage Regulation With Load Current for 3.3 V_{OUT} and 5 V_{OUT}

3.4.3 Functional Waveforms

3.4.3.1 Output Voltage Ripple

The output voltage ripple performance is observed for 3.3-V and 5-V output voltage and a half load of 15 A at 12-V DC inputs, as shown in 図 10 and 図 11.

注: CH2: 3.3-V output voltage ripple (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 15 A (2 mV/div, 1 µs/div)
Test result: 9.68 mV peak to peak

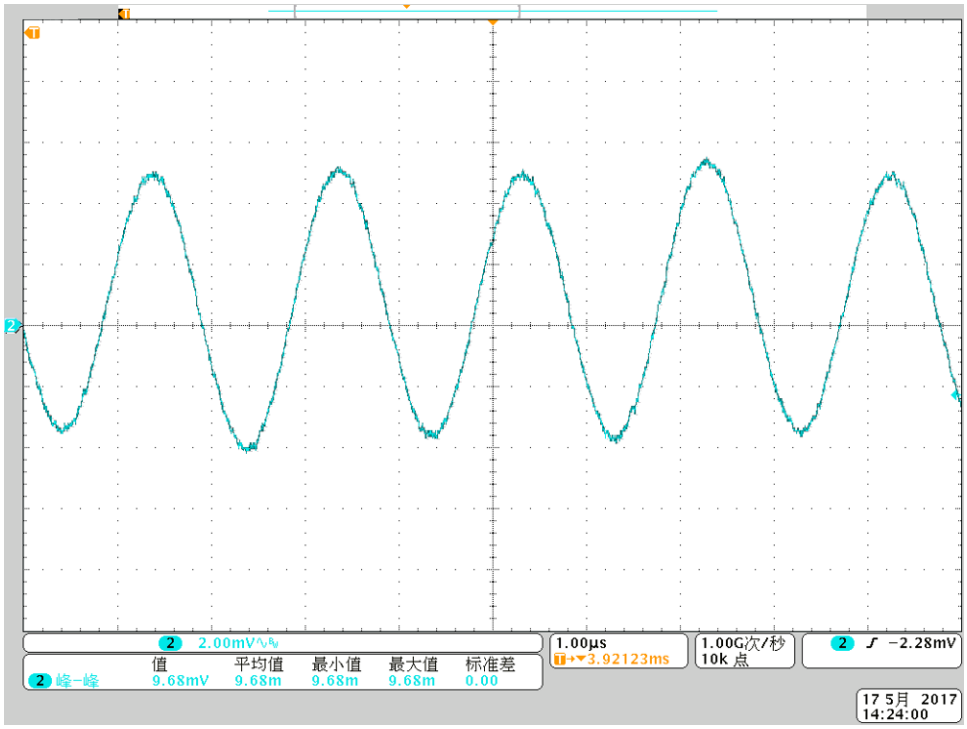


図 10. 3.3-V Output Voltage Ripple and Noise

注: CH2: 5-V output voltage ripple (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 15 A (10 mV/div, 1 µs/div)
Test result: 34.4mV peak to peak

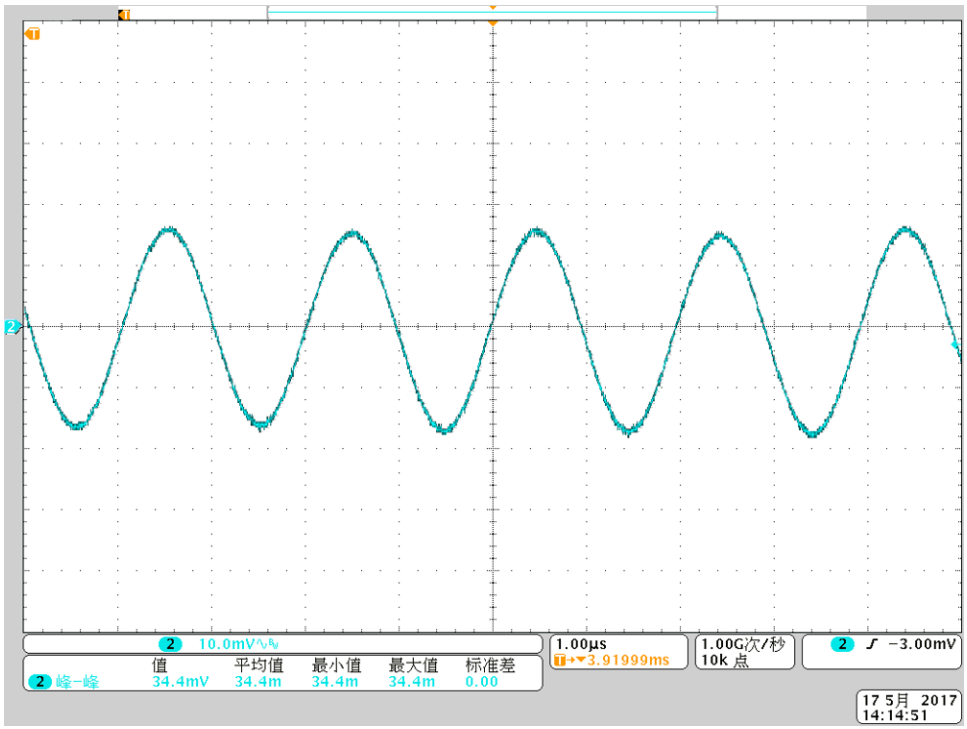


図 11. 5-V Output Voltage Ripple and Noise

3.4.4 Transient Performance Waveforms

3.4.4.1 Turnon Transient

The turnon transient performance is observed for 3.3-V and 5-V output voltages and a half load of 15 A at 12-V DC inputs, as shown in 図 12 and 図 13.

注: CH1: V_{IN}; CH2: 3.3 V_{OUT}; CH3: PGOOD_3.3Vout
Test condition: V_{IN} = 12-V DC; I_{OUT} = 15 A
Test result: Start-up time = 12 ms

図 12. 3.3-V Output Turnon Transient Waveform

注: CH1: V_{IN}; CH2: 5 V_{OUT}; CH3: PGOOD_5Vout
Test condition: V_{IN} = 12-V DC; I_{OUT} = 15 A
Test result: Start-up time = 12 ms

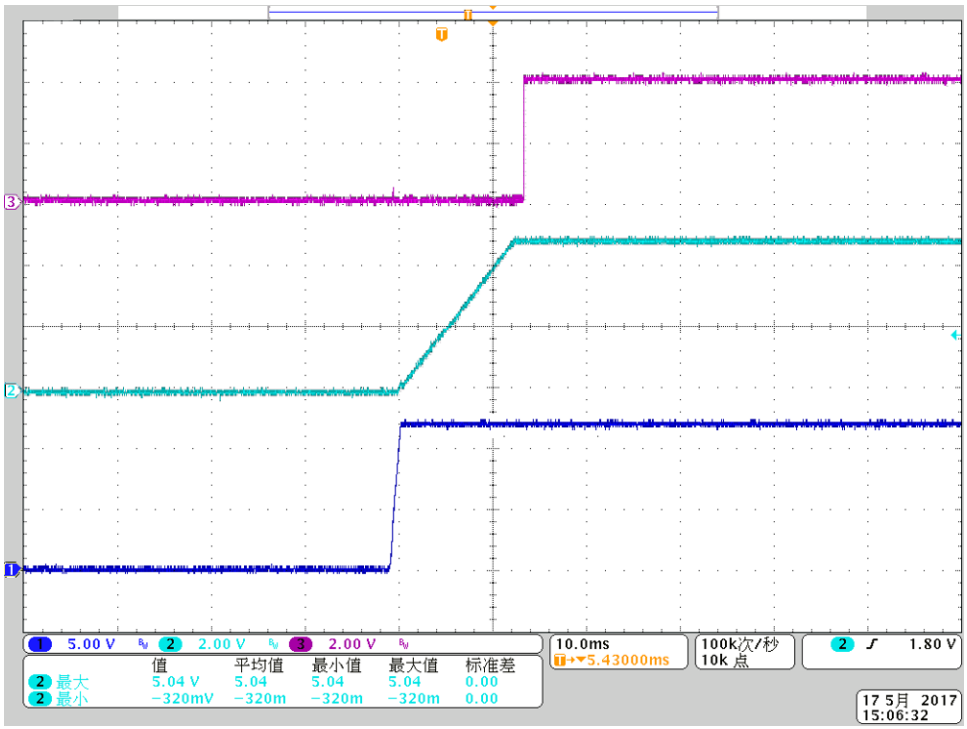


図 13. 5-V Output Turnon Transient Waveform

3.4.4.2 Output Load Transient

The load transient performance is observed for 3.3-V and 5-V output voltage at 12-V DC inputs, as shown in 図 14, 図 15, 図 16, and 図 17.

注: CH2: 3.3 V_{OUT}; CH4: Iout_3.3V (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 30 A to 0 A, di/dt = 0.5 A/µs
Test result: 75 mV for negative step change

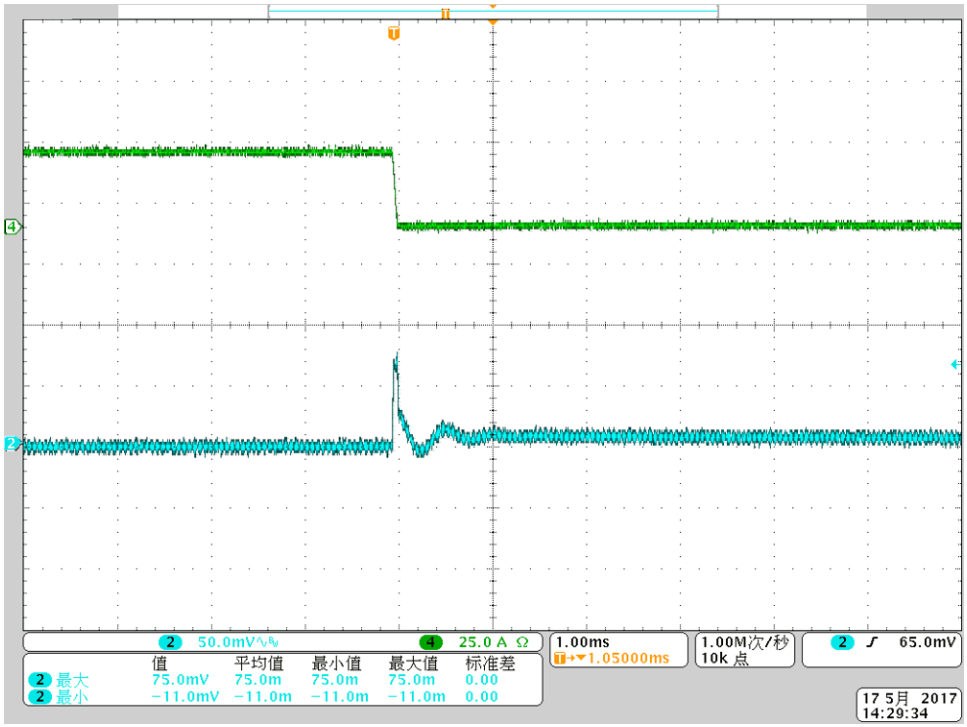


図 14. 3.3-V Output Load Transient From 30 A to 0 A

注: 3.3 V_{OUT}; CH4: Iout_3.3V (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 0 A to 30 A, di/dt = 0.5 A/µs
Test result: 87 mV for positive step change

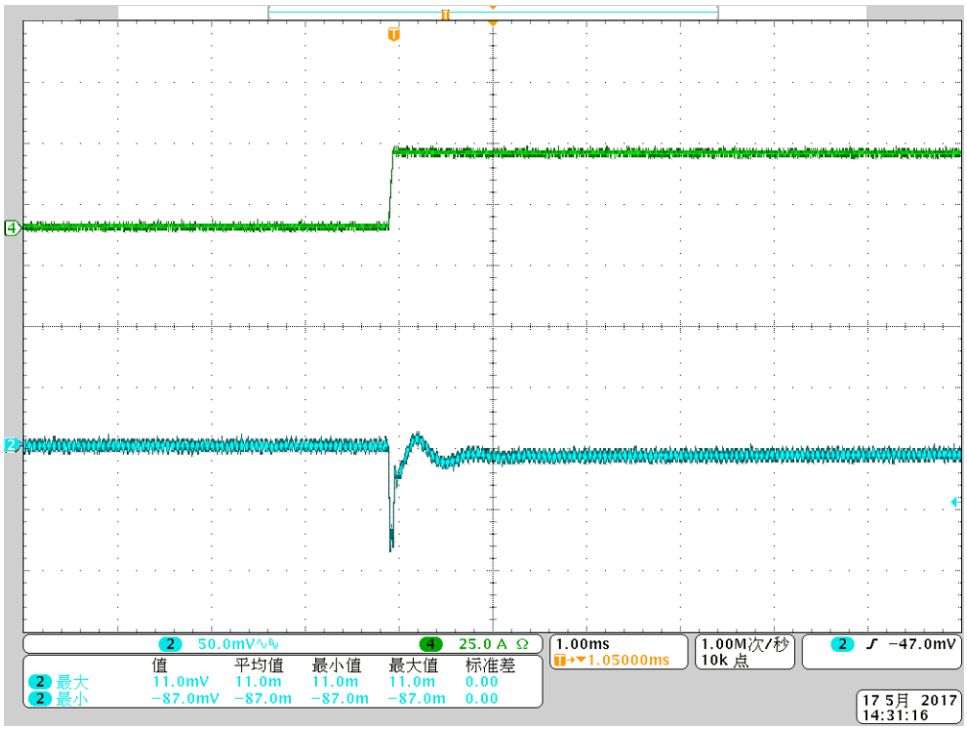


図 15. 3.3-V Output Load Transient From 0 A to 30 A

注: 5 V_{OUT}; CH4: Iout_5V (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 30 A to 0 A, di/dt = 0.5 A/µs
Test result: 95 mV for negative step change

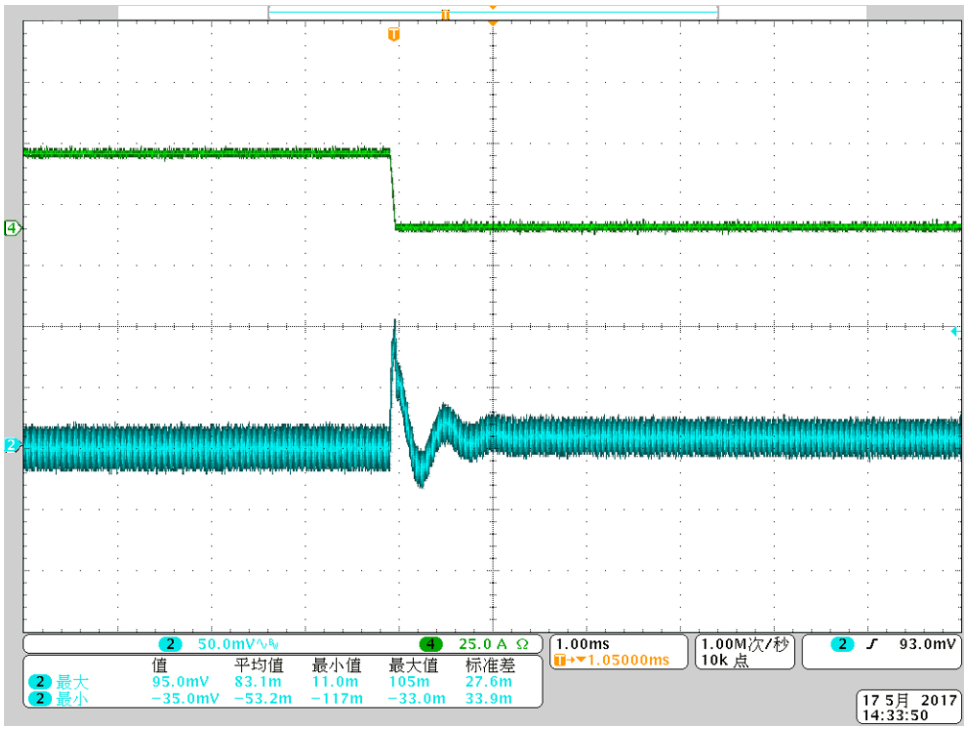


図 16. 5-V Output Load Transient From 30 A to 0 A

注: 5 V_{OUT}; CH4: Iout_5V (bandwidth: 20 MHz)
Test condition: V_{IN} = 12-V DC; I_{OUT} = 0 A to 30 A, di/dt = 0.5 A/µs
Test result: 103 mV for positive step change

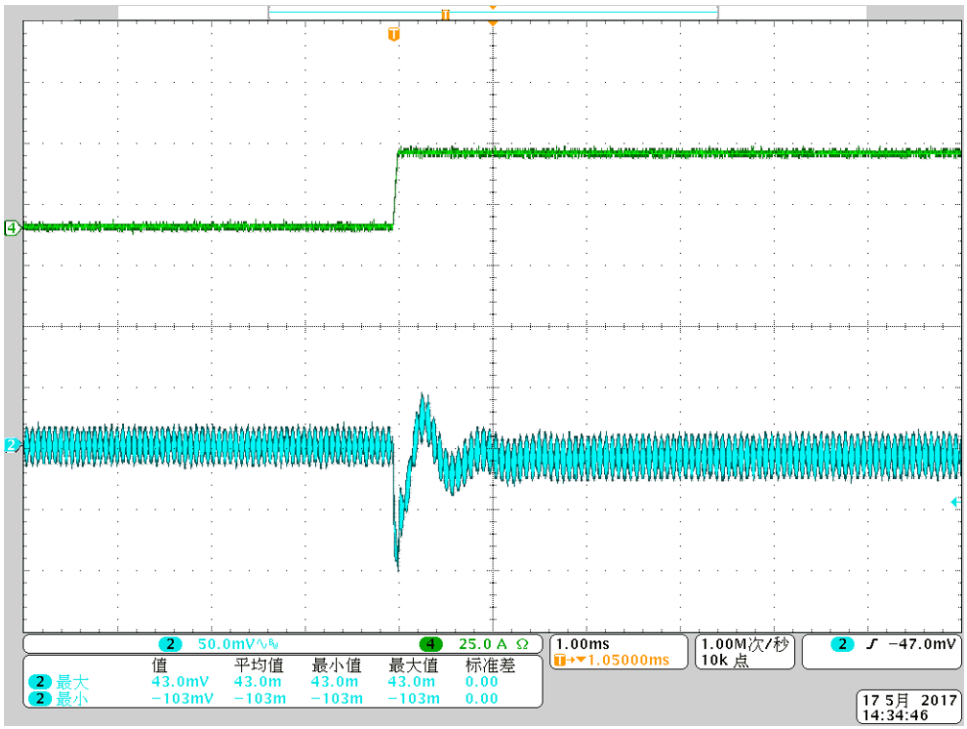


図 17. 5-V Output Load Transient From 0 A to 30 A

3.4.4.3 Overload and Overcurrent Response

The overcurrent response was recorded by applying an overcurrent condition in load from 30- to 45-A operation. 図 18 and 図 19 show that during the interval when the overcurrent condition is present, the converter goes into hiccup mode; when the overcurrent condition is removed, the converter recovers back to the normal operation.

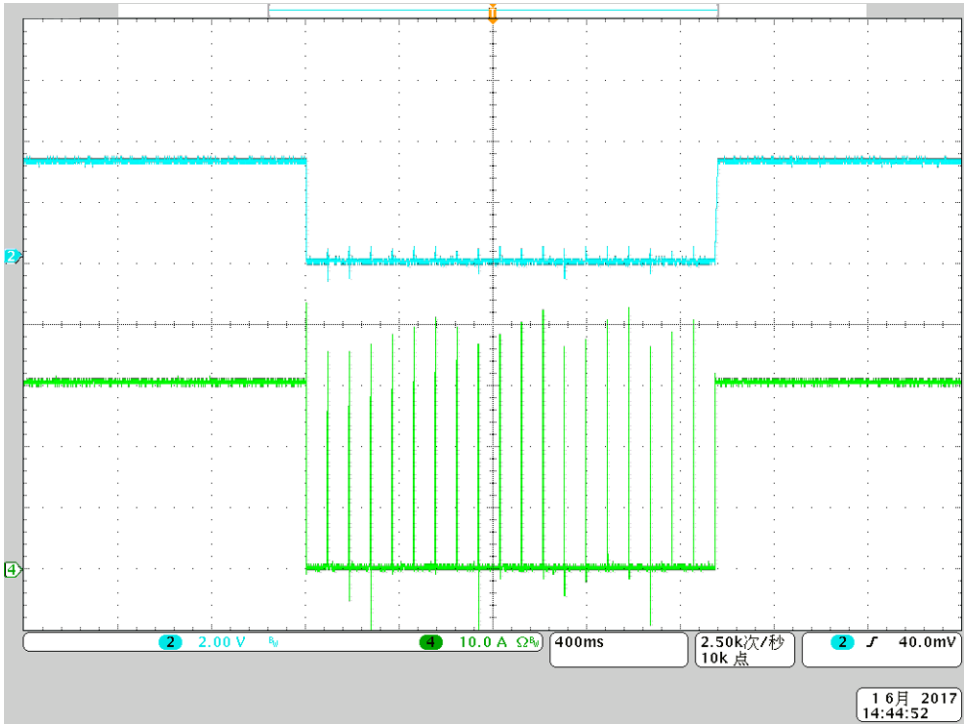


図 18. 3.3-V Output Voltage Response During Overcurrent and Recovery

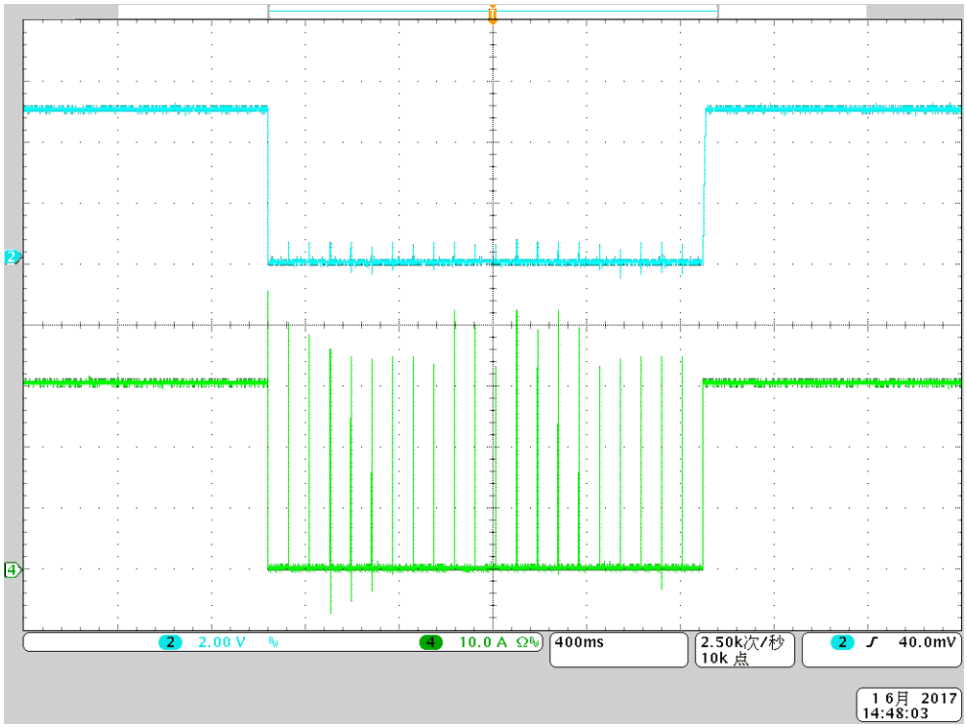


図 19. 5-V Output Voltage Response During Overcurrent and Recovery

3.4.4.4 Output Undervoltage and Overvoltage Protection

Due to the output OVP and UVP, sample the RSP voltage with respect to RSN voltage. As a result, the conventional trimming method through a external adjustable resistor to change the voltage divide network is not effective for this type of design because the RSP voltage with respect to RSN voltage is permanent during the trimming process.

To check the output UVP:

1. Have a resistor (1 Ω is fine) in series with the output inductor.
2. Turn on the electronic load with 5 A or 10 A.

The output capacitor delivers the energy to the load, and then the output voltage decreases to trigger the undervoltage threshold. The purpose of the resistor in series with the output inductor is to block the current feed to the output capacitor.

To check the output OVP:

1. Use an external power supply, which sets higher than 1.2 × V_{REF}.
2. When the module is powered on and enters into stable state, touch the RSP pin with the external voltage to trigger the overvoltage threshold.

3.4.5 Thermal Measurements

In this section, two sets of thermal images are provided. Based on the design requirements, each channel of the multiple outputs has a 30-A output current capability, and the total output power is 180 W. Therefore, check the two worst cases:

1. The 3.3-V output channel is with 30 A, and the total output power is 180 W.
2. The 5-V output channel is with 30 A, and the total output power is 180 W.

These two sets of thermal images are provided under room temperature with 100 LFM airflow measured at the board.

図 20 shows the thermal image for both the top and bottom side of the board. The input voltage is 12-V DC, and the loads are 30 A for 3.3 V_{OUT} and 16.2 A for 5 V_{OUT}.

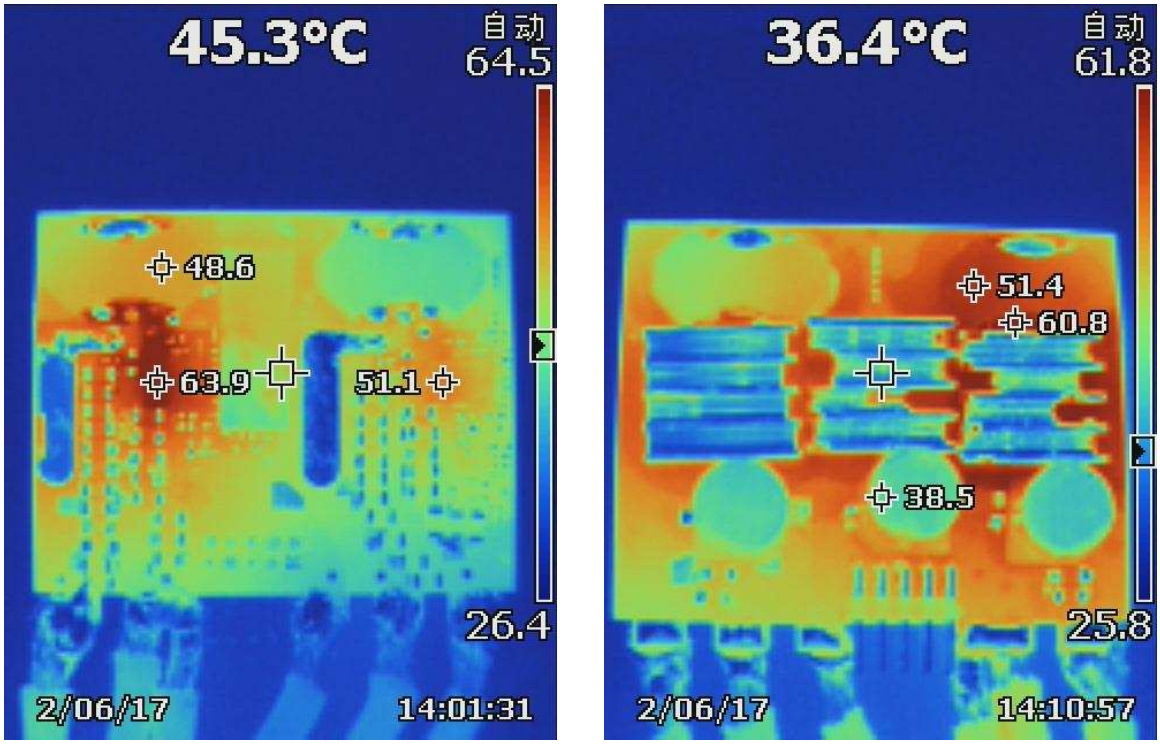


図 20. Thermal Performance at Worst Condition 1

表 10. Highlighted Image Makers at Worst Condition 1

PARAMETER	VALUE
Input voltage	12-V DC
Output power	180 W
Ambient temperature	25°C
Inductor_Core	51.4°C
Inductor_Winding	60.8°C
TPS543C20_3.3Vout	63.9°C
TPS543C20_5Vout	51.1°C
Input capacitor	38.5°C

図 21 shows the thermal images for both the top and bottom sides of the board. The input voltage is 12-V DC, and the loads are 9 A for 3.3 V_{OUT} and 30 A for 5 V_{OUT}.

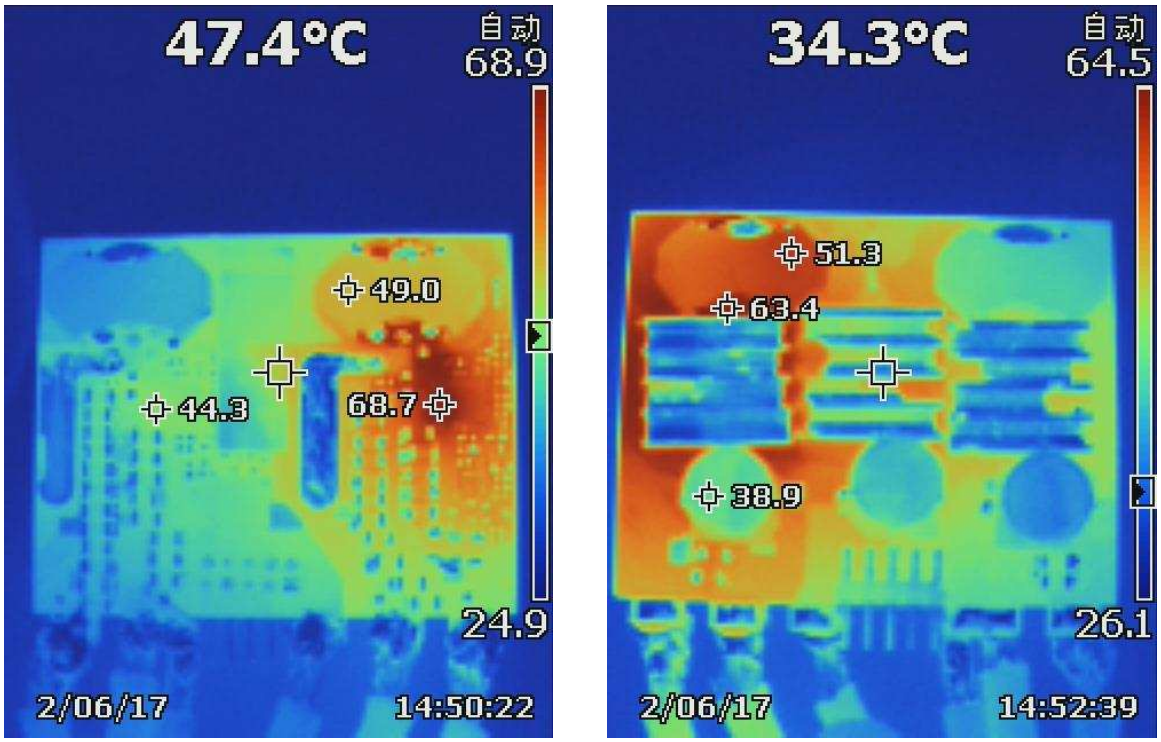


図 21. Thermal Performance at Worst Condition 2

表 11. Highlighted Image Makers at Worst Condition 2

PARAMETER	VALUE
Input voltage	12-V DC
Output power	180 W
Ambient temperature	25°C
Inductor_Core	51.3°C
Inductor_Winding	63.4°C
TPS543C20_3.3Vout	44.3°C
TPS543C20_5Vout	68.7°C
Output capacitor	38.9°C

3.4.6 Conducted Emissions

The TIDA-01444 design is a DC-DC module. The CE test setup is based on the module category. This test has the external EMI filter components based on the output power. 図 22 shows the external EMI filter configuration:

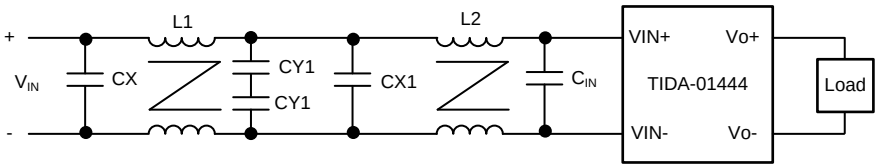


図 22. External EMI Filter Configuration

Where:

- CX is a 4.7-µF ceramic capacitor
- CX1 is a 4.7-µF ceramic capacitor
- CY1 is a 4.7-nF ceramic capacitor
- Cin is a 100-µF electrolytic capacitor
- L1 is a common-mode inductor, L1 = 0.08 mH
- L2 is a common-mode inductor, L2 = 0.24 mH

The conducted emissions were measured with a 12-V DC input voltage at a 21.7-A load for each output channel in a standard setup and were compared against EN55032 Class-A limits. (EN55032 standard has replaced EN55022/EN55013/EN55103-1 after March 2, 2017).

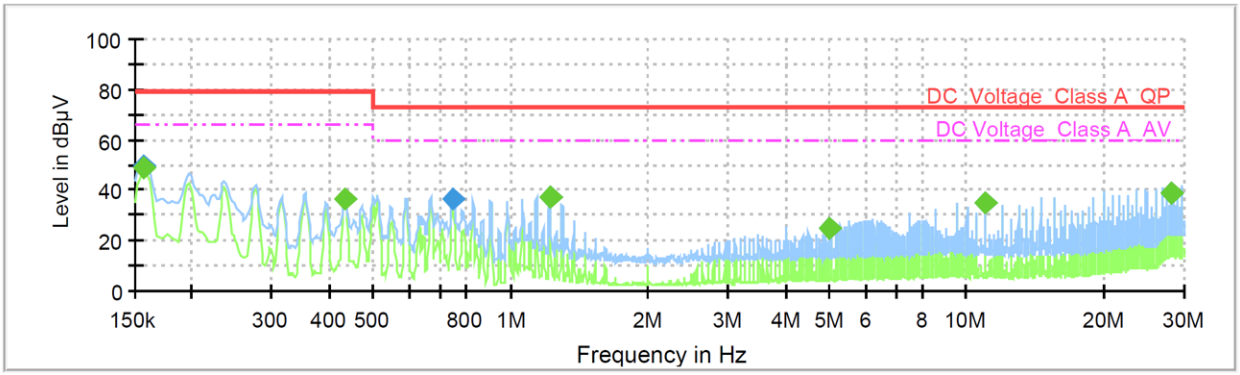


図 23. CE as per EN55032 Class A, Positive Line

表 12. CE Quasi-Peak And Average Margins Test Result, Positive Line

FREQ (MHz)	QUASIPEAK (dBµV)	AVERAGE (dBµV)	LIMIT (dBµV)	MARGIN (dB)	MEAS TIME (ms)	BANDWIDTH (kHz)	LINE	PE
0.15675	—	48.47	66.00	17.53	1000	9.000	L	GND
0.15675	49.42	—	79.00	29.58	1000	9.000	L	GND
0.43350	—	36.48	66.00	29.52	1000	9.000	L	GND
0.74625	36.19	—	73.00	36.81	1000	9.000	L	GND
1.21875	37.05	—	73.00	35.95	1000	9.000	L	GND
1.21875	—	37.07	60.00	22.93	1000	9.000	L	GND
5.00500	24.51	—	73.00	48.49	1000	9.000	L	GND
5.00500	—	24.59	60.00	35.41	1000	9.000	L	GND
11.01075	—	34.89	60.00	25.11	1000	9.000	L	GND
11.01300	35.19	—	73.00	37.81	1000	9.000	L	GND
28.02750	39.08	—	73.00	33.92	1000	9.000	L	GND
28.02975	—	38.97	60.00	21.03	1000	9.000	L	GND

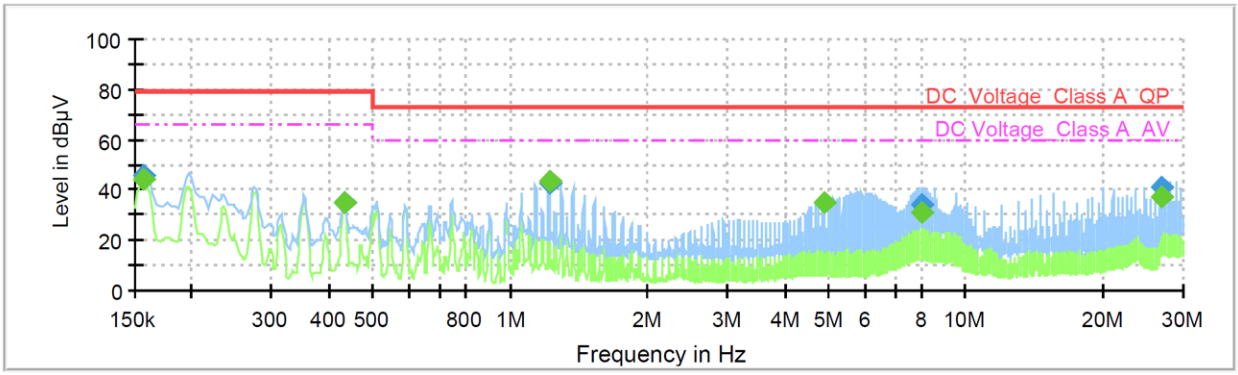


図 24. CE as per EN55032 Class A, Negative Line

表 13. CE Quasi-Peak And Average Margins Test Result, Negative Line

FREQ (MHz)	QUASIPEAK (dBµV)	AVERAGE (dBµV)	LIMIT (dBµV)	MARGIN (dB)	MEAS TIME (ms)	BANDWIDTH (kHz)	LINE	PE
0.15675	45.79	—	79.00	33.21	1000	9.000	N	GND
0.15675	—	44.12	66.00	21.88	1000	9.000	N	GND
0.43125	—	34.69	66.00	31.31	1000	9.000	N	GND
0.43125	34.81	—	79.00	44.19	1000	9.000	N	GND
0.43350	34.8	—	79.00	44.20	1000	9.000	N	GND
1.21650	42.32	—	73.00	30.68	1000	9.000	N	GND
1.21875	—	43.13	60.00	16.87	1000	9.000	N	GND
4.91100	—	34.53	60.00	25.47	1000	9.000	N	GND
7.97325	34.17	—	73.00	38.83	1000	9.000	N	GND
7.97325	—	31.3	60.00	28.70	1000	9.000	N	GND
27.03300	—	36.92	60.00	23.08	1000	9.000	N	GND
27.03525	41.18	—	73.00	31.82	1000	9.000	N	GND

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01444.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01444.

4.3 PCB Layout Recommendations

4.3.1 Power Stage Specific Guidelines

Follow these key guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A compact switch node reduces common-mode noise associated with the high dV/dt.
- Keep traces with high dV/dt and high di/dt away or shielded from sensitive signal traces with adequate clearance or ground shielding.
- It is absolutely critical that all TPS543C20 GND pins, including AGND (pin 29), GND (pin 27), and PGND (pins 13, 14, 15, 16, 17, 18, 19, and 20) are connected directly to the thermal pad underneath the device via traces or plane. The number of thermal vias needed to support 40-A thermal operation should be as many as possible.
- Place protection devices such as snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- Place the input capacitor close to the high-side MOS drain and low-side MOS source to reduce AC current loop in buck topology.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short-circuit current) before the activation of electronic protection.
- Adapt thermal management to fit the end-equipment requirements.

4.3.2 Controller Specific Guidelines

Follow these key guidelines to route controller components and signal circuits:

- Place VDD and BP decoupling capacitors as close to the device pins as possible. Do not use PVIN plane connection for VDD. VDD needs to be tapped off from PVIN with separate trace connection. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- Place all sensitive analog traces and components such as RAMP, RSP, RSN, ILIM, MODE, VSEL, and RT away from any high-voltage switch node (itself and others), such as SW and BOOT to avoid noise coupling. In addition, Place the MODE, VSEL, ILIM, RAMP, and RT programming resistors near the device or pins.
- See the placement and routing guidelines and layout examples presented in the TPS543C20 datasheet[1].

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-01444.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01444.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01444.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01444.

4.7 Design Calculator Spreadsheet

To download the design spreadsheet calculator for this reference design, see the link at TIDA-01444.

5 Related Documentation

1. Texas Instruments, *TPS543C20 4 Vin to 16 Vin, 40-A Stackable, Synchronous Step-down SWIFT™ Converter with Adaptive Internal Compensation*, TPS543C20 Datasheet (SLUSCD4)

5.1 商標

6 About the Author

CHENG LIU is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Cheng brings to this role his extensive experience in power electronics, high frequency high power density DC-DC and analog circuit design. Cheng earned his masters of electrical machinery and apparatus from Wuhan University of Technology in 2012.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。