参考資料

TI Designs: TIDA-00914
小型デルタ-シグマ変調器搭載、強化絶縁型位相電流センスのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDA-00914デザインは、絶縁されたIGBTゲート・ドライバと、絶縁された電流および電圧センサを使用する、強化絶縁の3相インバータ・サブシステムを実現します。AMC1306E25デルタ-シグマ(ΔΣ)変調器により、シャント・ベースの高精度インライン・モータ位相電流センシングが行われます。変調器の出力はマンチェスター・エンコードされるため、MCUと変調器との間のクロックおよびデータ信号の配線を簡素化できます。変調器のCMTIが高いため、インバータのスイッチング過渡電圧が原因でコントローラ側のデータが破壊されることを抑制できます。変調器のサイズが小さいので、コンパクトなソリューションを実現できます。TIDA-00914は外部のMCUまたはFPGAに接続するためのインターフェイスとなり、デジタルSINCフィルタを実装することでAMC1306E25の出力ビット・ストリームを復調できます。このTI DesignはF28379D Delfino™制御カードを使用し、このカードはアダプタ・カードによりTIDA-00914カードに接続され、電流センシング用のSINCフィルタを実装します。

リソース

TIDA-00914	デザイン・フォルダ
AMC1306E25	プロダクト・フォルダ
UCC5310MCDWV	プロダクト・フォルダ
UCC5320SCDWV	プロダクト・フォルダ
UCC5390ECDWV	プロダクト・フォルダ
LM3480	プロダクト・フォルダ
TLV704	プロダクト・フォルダ
TLV1117-33	プロダクト・フォルダ
SN74LVC1G17	プロダクト・フォルダ
TMDSCNCD28379D	ツール・フォルダ

TI E2E™ Community

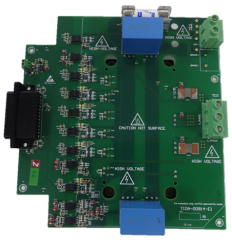
E2Eエキスパートに質問

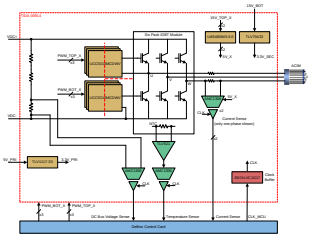
特長

- 200～480VのAC電源による駆動に適した、強化絶縁インバータの電力段
- 強化絶縁のΔΣ変調器のマンチェスター・エンコードされた出力により、シャント抵抗でインライン・モータの位相電流を測定
- マンチェスター・エンコードされたデータ出力により、ΔΣ変調器へのクロック配線を簡素化、クロック信号のデイジー・チェーンが可能
- ピン数が少ない(8)ため、コンパクトなソリューションを実現可能
- 変調器のCMTIが高い(50kV/μs超)ため、スイッチング過渡電圧へのノイズ耐性が向上
- SINC 3フィルタおよびOSR 8により短絡応答時間1.5μs未満
- 公称位相電流測定範囲28A_{RMS}、4mΩのシャント抵抗により過渡ピーク範囲±80Apk
- 0℃～55℃の温度範囲にわたってフルスケール誤差0.5%未満に較正済み
- ΔΣ変調器によりDCリンク電圧の絶縁測定が可能
- ΔΣ変調器とともにモジュールに搭載されているNTCを使用して、IGBT電力モジュールの温度の絶縁測定が可能

アプリケーション

- ACインバータおよびVFドライブ
- サーボ・ドライブおよびモーション・コントロール





1 System Description

High-resolution, accurate, isolated phase current measurement is vital in industrial motor drive applications where high-performance torque and motion control are required. These applications include servo drives, robotics, machine tools, industrial manufacturing, and CNC machines. The options available for phase current measurement are to use Hall effect sensors, flux gate sensors, current transformers, or shunt resistors. The first three options have inherent galvanic isolation benefits and a high current measurement range, but the linearity, bandwidth, and drift are of lower performance when compared to the shunt resistor option. When the maximum continuous current to be measured is less than 50 A, then using shunt resistors provides a highly linear, high-bandwidth, cost-effective measurement solution.

Isolated shunt-based current measurement can be done either by using an isolated amplifier or an isolated delta-sigma (ΔΣ) modulator. The amplifier-based solution has three conversion stages consisting of an isolated amplifier, a differential-to-single-ended amplifier with a filter, and a SAR ADC. Each stage adds error and achieves an accuracy of < 10 bits on the system level. For a higher resolution analog signal chain, the cost increases exponentially. Short-circuit detection using isolation amplifiers require additional circuitry, which consist of window comparators and reference generators for setting short-circuit thresholds. The short-circuit detection delay is higher in this case because of the propagation delays of the amplifier plus the comparator. The ΔΣ modulator-based solution has a single conversion stage, and most of the processing is done in the digital domain. which makes it less susceptible to noise in the system and it is possible to get accuracy of > 14 bits at the system level.

As shown in 図 1, there are two paths implemented in the sigma-delta (ΣΔ) filter module (SDFM) to demodulate data. One is a high-resolution, precise data filter unit. This unit has a configurable SINC filter and high oversampling ratio (OSR), preferably SINC 3 and OSR of > 64. The output of the filter unit is stored in data registers and used for position and torque control. The output of this filter is not preferred for drive protection because of the high latency of the path. The second path is a low-latency, lower resolution overcurrent sense comparator path. This unit also has configurable SINC filter and OSR. The OSR is usually limited to much lower range, which enables low latency. The output of the filter is passed through a digital window comparator with programmable thresholds. The comparator output is used to trip the PWM signals in case of short circuit. It is possible to achieve a response time of < 1.5 µs with a SINC 3 filter and OSR of 8.

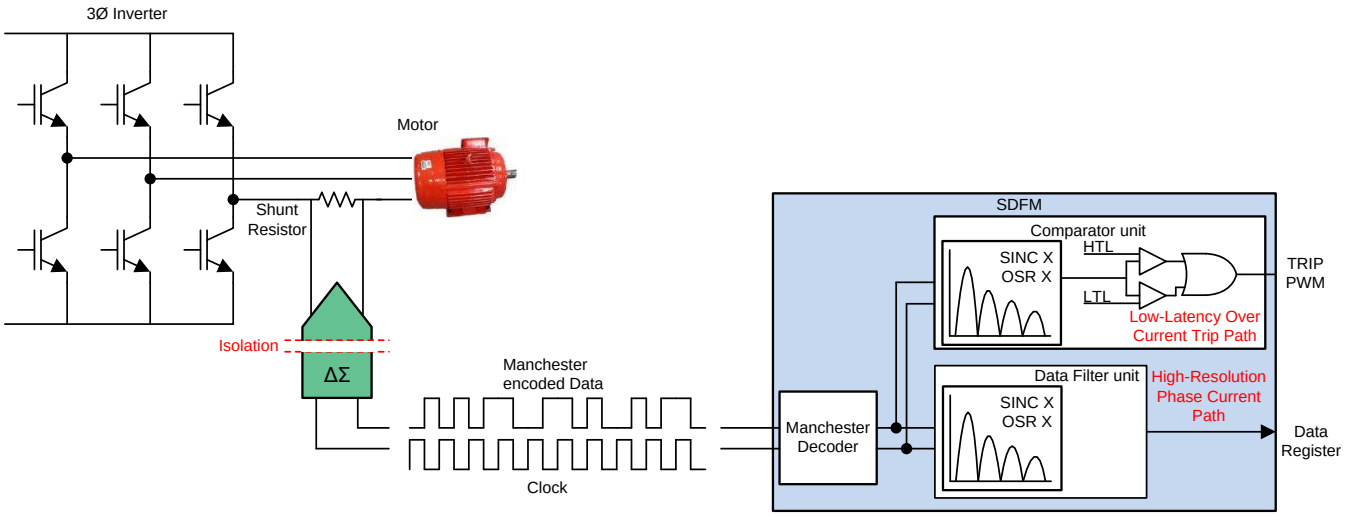


図 1. ΣΔ Modulators in Motor Drives

Different clock and data line lengths may cause propagation delay mismatch between the two signals. A delay mismatch may cause setup and hold time issues at the microcontroller (MCU). Avoiding this issue requires careful layout routing and signal length matching. The clock signal termination is more problematic. This setup and hold time issue can be solved by Manchester encoding the data signal. An Manchester encoded bit stream is shown in 図 2. In this coding scheme, the clock is embedded into the data stream, which enables easier routing of clock and data signals reducing wiring efforts. Clock termination is much easier as the clock signal can be daisy chained between multiple modulators.

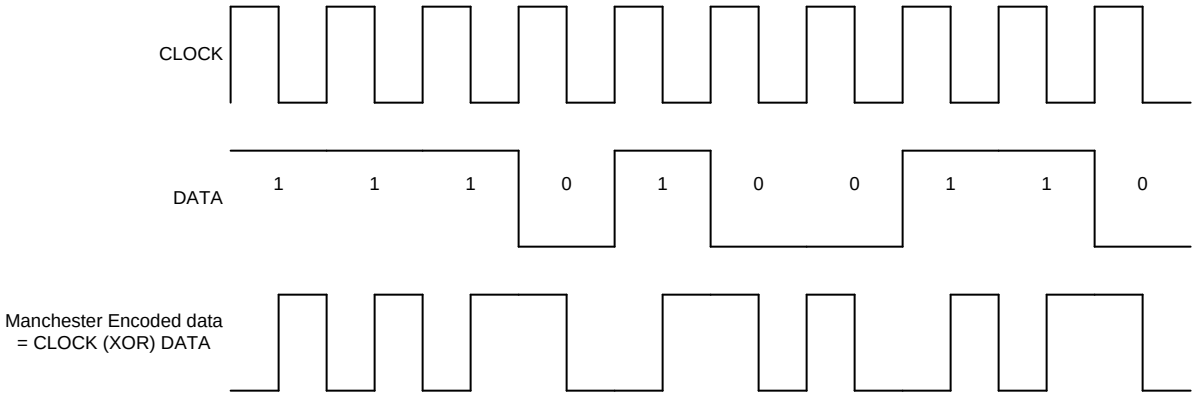


図 2. Manchester Encoded Data

This reference design consists of a 3φ power stage using TI's wide body package (DWV) small (8-pin) reinforced isolated ΔΣ modulator AMC1306E25 for in-line phase current sensing and is intended to drive motors for various industrial applications. The AMC1306E25 uses IEEE 802.3 compliant Manchester encoding. This TI Design demonstrates the following in a real system:

- Loss of hi-side power detection

- Modulator input overrange detection
- Short-circuit detection and response time
- Current measurement accuracy

1.1 Key System Specifications

表 1. Key System Specifications

SUBSECTION	PARAMETER	SPECIFICATIONS	COMMENT
Inverter	DC bus input voltage	200- to 900-V DC	Up to 1200-V DC absolute maximum by changing connectors and fuse
	Output frequency	0 to 100 Hz	—
	PWM switching frequency	2 to 16 kHz	—
	PWM dead band	1 µs	Inverter tested with 1-µs deadband; can be varied as long as there is no overlap between V_{GE} signals of top and bottom IGBT switches
	Power switch used	1200-V, 100-A six-pack inverter IGBT module	Part number: CM100TX-24S
Current sensing	Continuous motor phase current	28 A_{RMS} (40 A_{PK}) per phase maximum.	Can be increased to 44 A_{RMS} max by changing DC bus input and motor power connectors, fuse, and using appropriate heat sinking
	Transient overload maximum	80 A_{PK} with 4-mΩ shunt resistor	—
	Phase current measurement error	< 0.5% calibrated	—
	Maximum modulator clock frequency	20 MHz	—
	Logic Interface	3.3-V CMOS logic with Schmitt trigger	—
Feedback	Measured variables	2 phase currents, module temperature, DC-link voltage	Feedbacks required for motor control and protection
Protection	Phase current	Inverter shutdown on overload	User software implementation
	DC bus voltage	Overvoltage and undervoltage detection	User software implementation
	Current sensor	Holds output data constant when hi-side power is lost.	Indication to the controller that data is no longer valid
		Toggles every 128 bits when common-mode input voltage range of sensor is violated	
	Module temperature	Overtemperature shutdown	User software implementation
	Isolation	Reinforced isolated	Reinforced isolated current sensor and gate drivers used; 8.89-mm spacing between primary and secondary side
Operating conditions	Temperature range	0°C to 55°C	Components selected support the industrial temperature range of 85°C and the TIDA can operate outside the mentioned temperature range with sufficient derating. Tested only from 0°C to 55°C

表 1. Key System Specifications (continued)

SUBSECTION	PARAMETER	SPECIFICATIONS	COMMENT
Interface connectors	Microcontroller interface	7 PWM signals, current sense modulator bit streams for two motor phases, DC-link voltage sense modulator bit stream, temperature sense modulator bit stream, clock signal, 5 V for the controller board	See 表 5 for pin assignment
	Primary side power	5 V ± 5%, 500 mA	For powering primary side of gate drivers, modulators, and the controller card
	Secondary side power	15 V ± 5%, 200 mA	For powering the secondary side of gate drivers and LDOs, which generate 5 V for the current sense modulators and 3.3 V for the DC bus voltage sense and temperature sense modulators
PCB Information	PCB layer stack	4 layer, 1-oz copper	35-micron copper
	Laminate	FR4, high Tg	—
	PCB thickness	1.6 mm	—
	PCB size	167 mm × 178 mm	—

2 System Overview

2.1 Block Diagram

図 3 shows the system block diagram of the reinforced isolated three-phase inverter with in-line precision phase current sensing with a shunt resistor. The TIDA-00914 design is highlighted with a red dashed box.

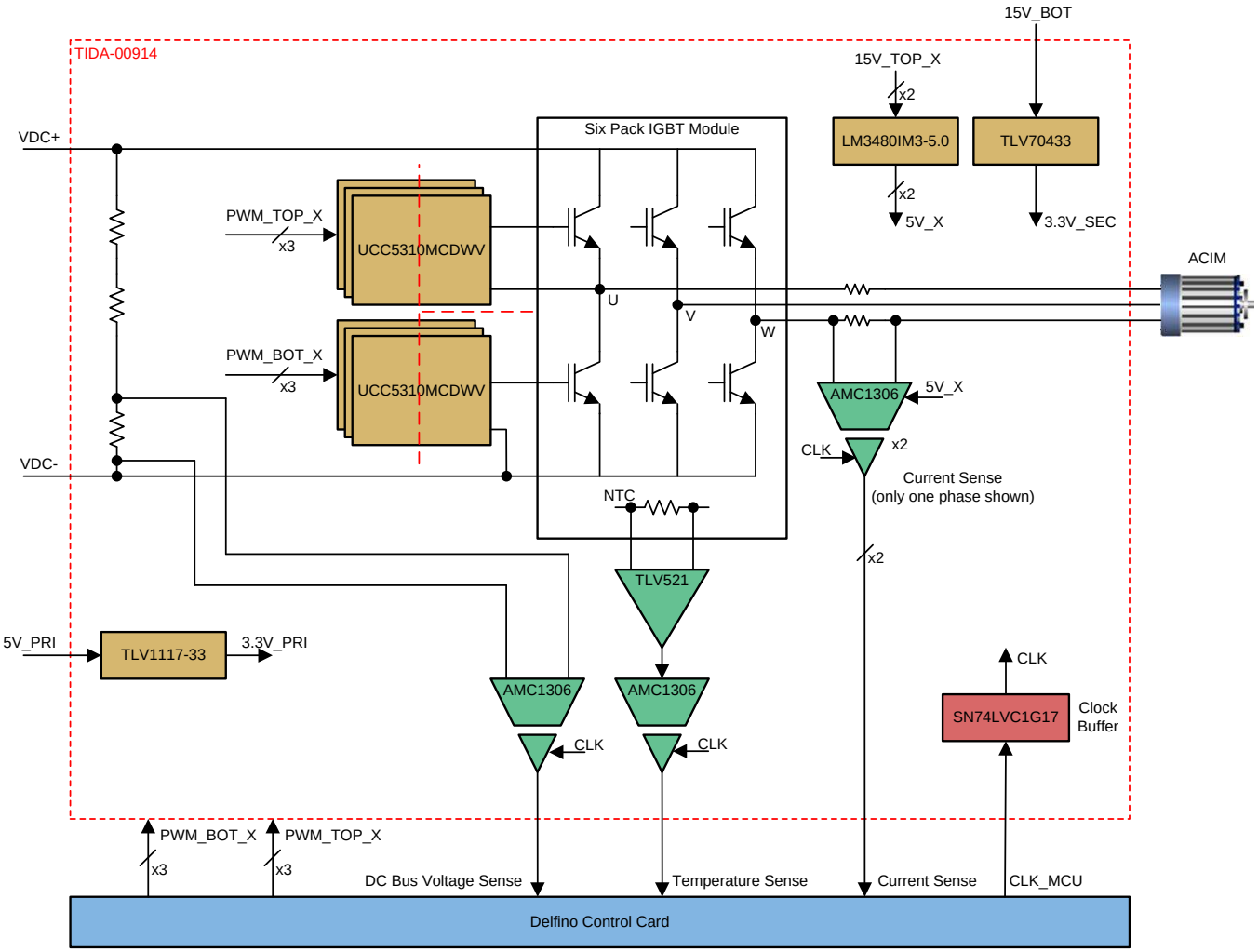


図 3. Block Diagram of TIDA-00914

The inverter section is composed of a six-pack IGBT module that contains three half bridges. Each IGBT of the module is driven by a reinforced, isolated-gate driver, UCC5310MCDWV. A unipolar 15-V power supply is used for driving the IGBT gates. The PWM input signals for the gate drivers are routed to a D-SUB 25-pin female connector, which is connected to the Delfino control card TMDSCNCD28379D through an adapter board. For more information on gate-driver design using UCC53x0 devices, see the TIDA-01420 reference design, which uses the basic isolated version of the gate driver.

The inverter power stage is designed to be protected against short circuits, DC bus under- and overvoltage, and IGBT module overtemperature. DC bus voltage is sensed with a voltage divider. The scaled voltage is sensed with the AMC1306E25. DC bus under- and overvoltage thresholds are set inside software. To monitor IGBT module temperature, a voltage divider is formed with an external resistor and the NTC integrated inside the module. The voltage drop across the NTC is sensed by the AMC1306E25 device. Because the resistance of the NTC and the input impedance of the AMC1306 device are comparable, an op-amp voltage follower buffer is inserted between the NTC and AMC1306 input stage to reduce error in temperature measurement. The op-amp buffer used is the cost-optimized TLV521. The actual temperature is derived from the voltage across NTC by software implemented in the controller.

In-line motor phase current sensing is done by inserting a shunt resistor between the phase output of the inverter and the phase terminals of the motor. The voltage drop across the shunt resistor is sensed by an AMC1306 device. The transfer function of the current sense signal chain path is used to derive the phase current values in the controller. The bit stream of the ΔΣ modulators are Manchester encoded; decoding of the data must be done before filtering it. Manchester encoding makes clock and data signal routing between the controller and the modulator much easier. A configurable digital SINC filter is implemented inside the controller to decimate the bit stream from the ΔΣ modulators. The short-circuit threshold value is set within software. The clock is routed to the PCB D-SUB 25-pin connector from the controller card through ribbon cable. A clock buffer is implemented on the PCB using SN74LVC1G17 Schmitt trigger buffer. The clock signal from the buffer is routed to each AMC1306 device by daisy chaining. In this TI Design, characterization the Manchester decoding and SINC filters are implemented within dedicated ΣΔ filter modules (SDFM) present within the TMS320F28379D.

A primary-side 3.3-V power supply is derived from the 5-V input with the LDO regulator TLV1117-33I. This 3.3 V is supplied to the primary side of the ΔΣ modulators, the gate drivers, and the clock buffer. A secondary-side 3.3-V power supply is generated from the secondary-side 15-V low-side gate driver power supply with the LDO regulator TLV70433. This supply powers the secondary side of the DC bus sensing and temperature sensing ΔΣ modulators and the TLV521 buffer. Secondary-side 5-V power supplies for the phase current sense ΔΣ modulators are derived from the corresponding 15-V secondary high-side gate driver power supplies using the LM3480IM3-5.0 LDO. The high-side gate drive power supplies are generated by bootstrapping the 15-V low-side gate driver power supply.

注: It is also possible to evaluate the split-output version (UCC5320SCDWV) and the bipolar-supply version (UCC5390ECDWV) with this reference design. The schematic file available on the TIDA-00914 product page shows the component changes needed.

2.2 Highlighted Products

2.2.1 AMC1306E25

The device is a precision, ΔΣ modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low voltage circuitry. The input of the AMC1306 is optimized for direct connection to shunt resistors or other low-voltage level signal sources. The output bit stream of the AMC1306Ex is Manchester encoded. By using an appropriate digital filter to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a rate of 78 kSPS. The small pin count (8 pins) of the modulator helps achieve a compact current sense solution.

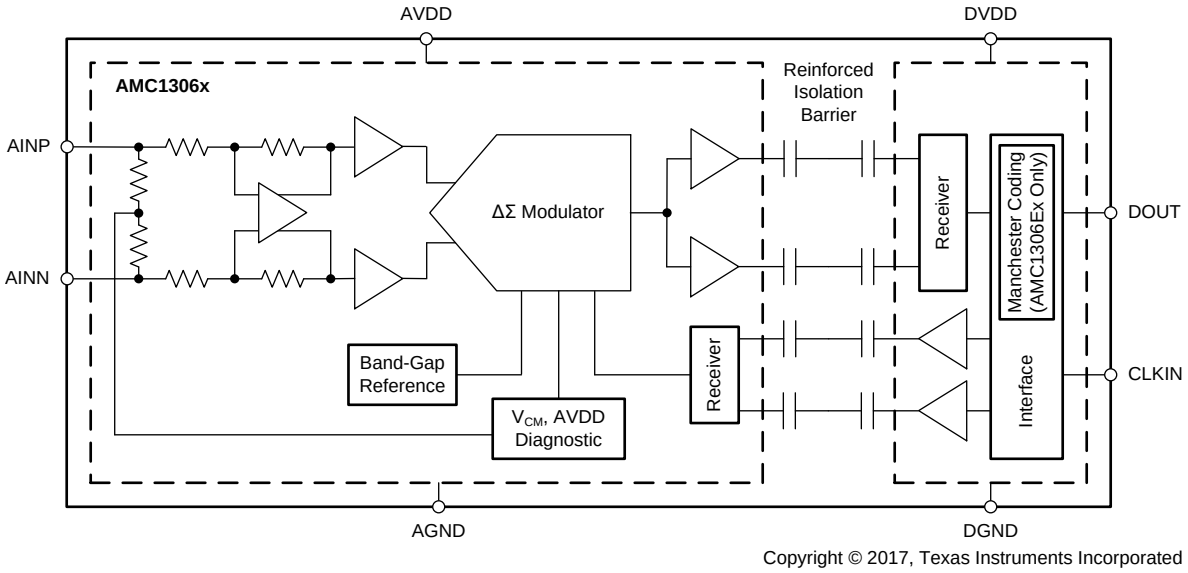


図 4. Functional Block Diagram of AMC1306E25

2.2.2 LM3480

This device is an integrated linear voltage regulator. It features operation from an input as high as 30 V and an ensured maximum dropout of 1.2 V at the full 100-mA load. A standard package for the device is SOT-23. The small package size and wide input range of this device makes it suitable to generate a 5-V floating power supply for the current sense ICs from the 15-V floating supply used to power up the high-side gate drivers.

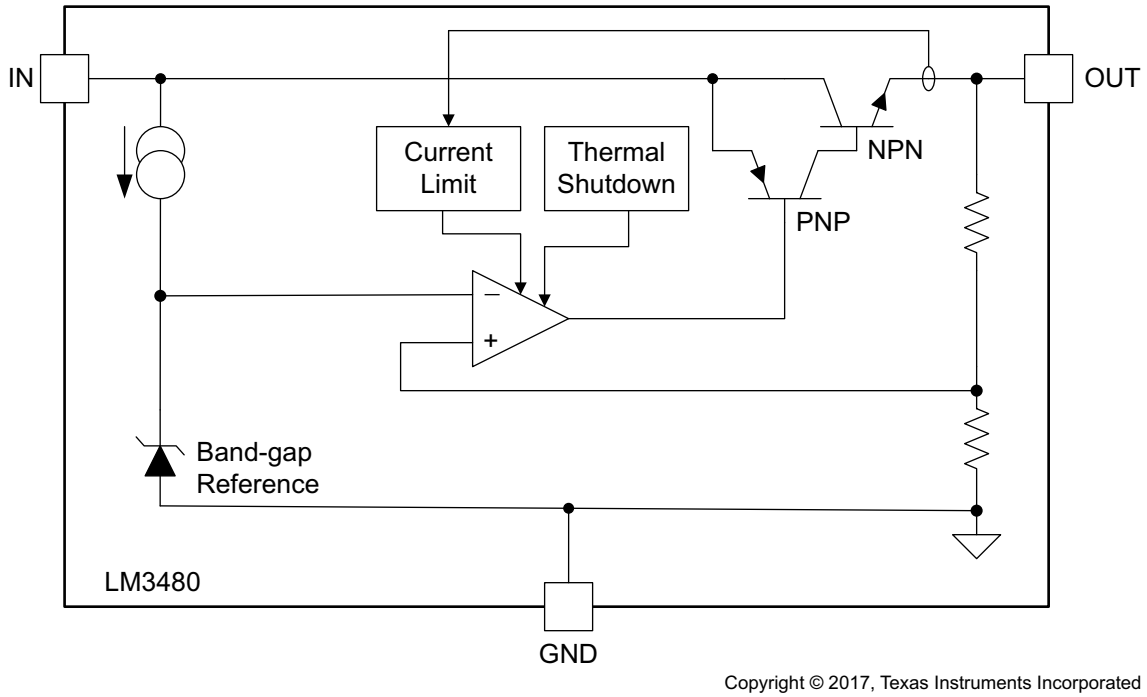


図 5. Functional Block Diagram of LM3480

2.2.3 TLV704

This device is a low dropout regulator with ultra-low quiescent current requirement. The TLV704 operates over a wide operating input voltage range of 2.5 to 24 V, making it ideal for generating a secondary-side 3.3-V power supply from the 15-V low-side gate driver power supply. The device is an excellent choice for industrial applications that undergo large line transients.

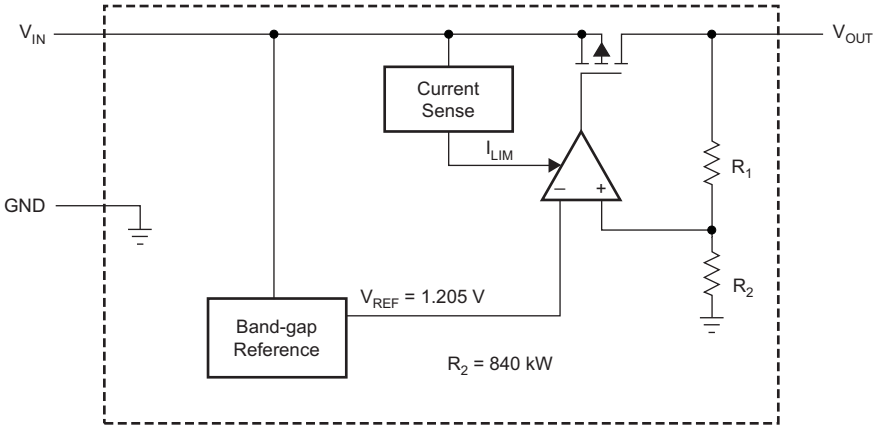


図 6. Functional Block Diagram of TLV704

2.2.4 TLV1117

This device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents. The device is used to generate a primary-side 3.3-V power supply from the 5-V input.

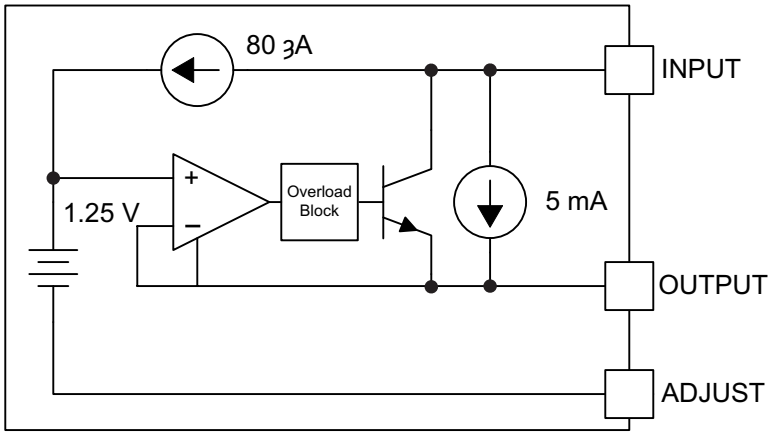


図 7. Functional Block Diagram of TLV1117

2.2.5 SN74LVC1G17

This device is a single Schmitt-trigger buffer designed for 1.65- to 5.5-V V_{CC} operation. The SN74LVC1G17 contains one buffer and performs the Boolean function Y = A. The CMOS device has a high output drive of 24 mA at 3.3 V while maintaining low static power dissipation over a broad V_{CC} operating range. The device is used to buffer the clock signal coming from the MCU into the PCB.

2.2.6 UCC5310MCDWV

The UCC53x0 family of devices are single-channel, isolated gate drivers, with variants for pinout configuration and drive strength. The UCC5310M variant is used in this design. This device connects the gate of the transistor to an internal clamp, to prevent false turnon caused by miller current. The SOIC-8 DWV (wide-body) package is used, which supports an isolation voltage up to 5 kVrms. This device has 2.4-A minimum source capability and 1.1-A minimum sink capability. Compared to the optocoupler, the UCC53x0 has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI.

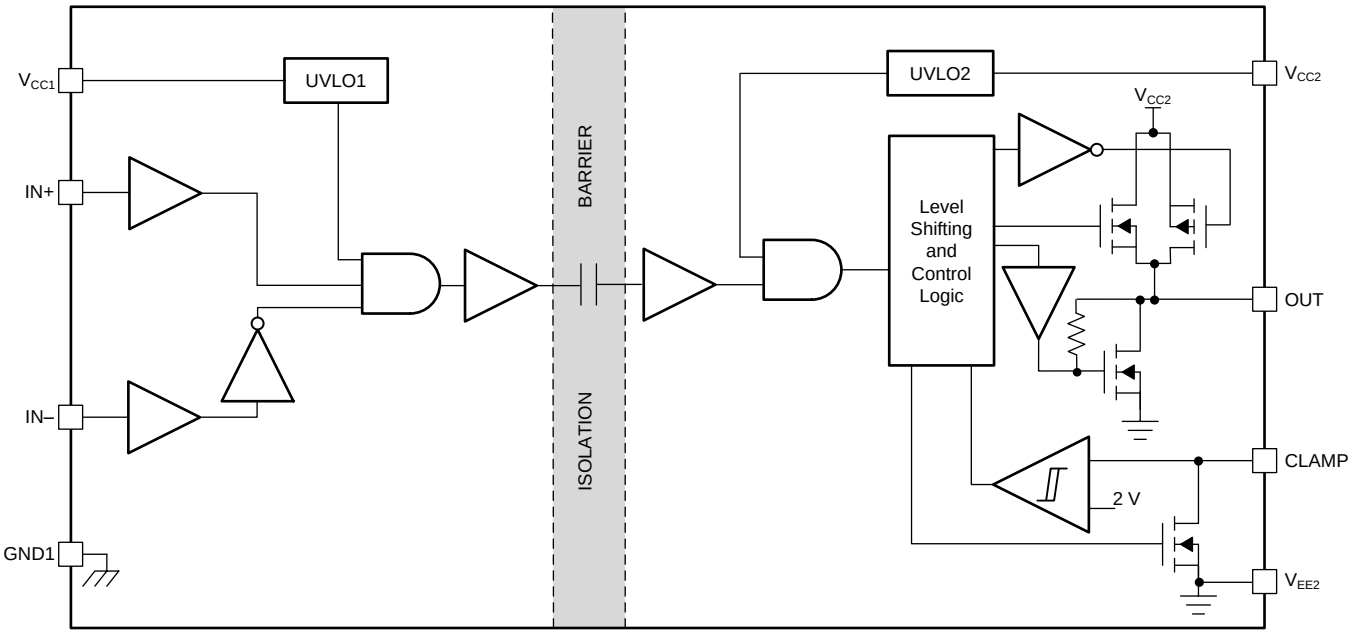


図 8. Functional Block Diagram of UCC5310MCDWV

3 System Design Theory

3.1 DC to Three-Phase AC Inverter Subsystem

A six-pack IGBT module CM100TX-24S is used to convert input DC bus voltage into 3φ AC for driving the induction motor. Each of the six IGBT power switches are controlled by reinforced isolated gate drivers using unipolar 15-V gate-to-emitter voltages. R20, R32, R112, R12, R38, and R26 are 10-kΩ resistors used to ensure that the IGBTs remain off in case the gate drivers get disconnected due to system malfunction. C72 to C77 are provisions for additional external gate-to-emitter capacitance. R118 and R120 are shunt resistors used for U and W phase current sensing.

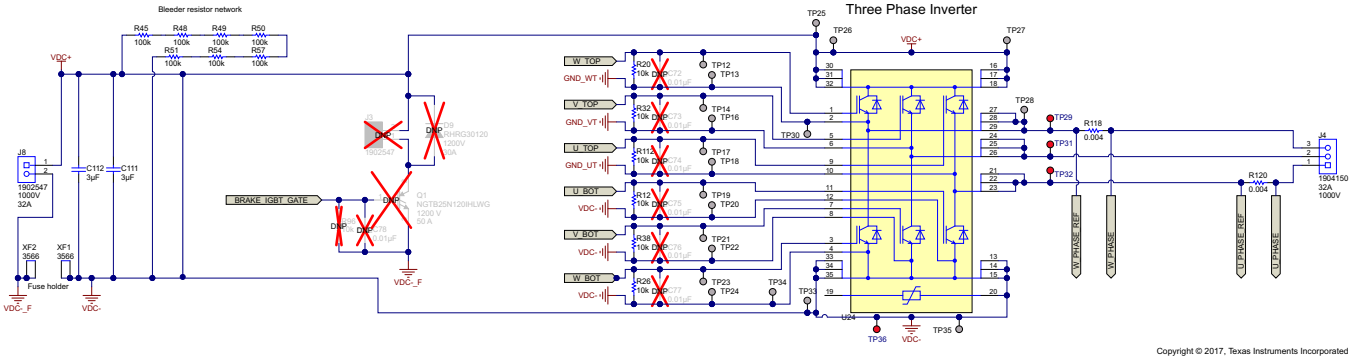


図 9. Schematic of DC to Three-Phase AC Inverter

Terminal block J8 is the DC bus voltage input connector. C112 and C111 are localized high-frequency DC bus decoupling capacitors. This TI Design uses 3-µF, 1300-V film capacitors. XF2 and XF1 are fuse holders. A 30-A, 1-kV DC cartridge fuse of dimension 10.3 mm × 38 mm has to be placed within the fuse holders. Once the DC bus voltage is powered off, some time is needed for the DC bus link capacitors to discharge. This creates a safety hazard. Therefore, bleeder resistors R45, R48, R49, R50, R51, R54, and R57 are added across the DC link. These resistors ensure quick discharge of the DC bus capacitors on power off. Provision is given to connect brake resistor to the DC bus. In case of motor regeneration, if the DC bus voltage goes above a specified threshold, the brake chopper can be initiated. J3 is the terminal block used to connect the braking resistor. D9 is the freewheeling diode connected across the braking resistor to prevent overshoots at the collector of brake chopping IGBT power switch Q1.

The inverter stage is designed to drive induction motors up to 11 kW. 表 2 shows the specifications of a sample 11-kW induction motor:

表 2. Motor Specification

PARAMETER	SPECIFICATION
Part number	M2BAX 160MLA
Output power	11 kW
International efficiency class	IE2
Motor efficiency	89.8%
Power factor	0.79
Poles	4
Speed	1500 rpm
Frequency	50 Hz
Line-to-line voltage	400 V_{RMS}

The inverter output power required is calculated in 式 1, and the maximum inverter output current taking a 15% tolerance on the minimum grid voltage is calculated in 式 2:

$$\text{Inverter output power} = \frac{\text{Motor shaft power}}{\text{Efficiency of motor}} = \frac{11000}{0.898} = 12.249\ \text{kW} \tag{1}$$

$$\text{Maximum inverter output current} = \frac{\text{Inverter output power}}{\sqrt{3} \times \text{PF} \times \text{Minimum motor input voltage}} \tag{2}$$

$$\text{Maximum inverter output current} = \frac{12249}{\sqrt{3} \times 0.79 \times \left(380 - \left(0.15 \times 380\right)\right)} = 27.71\ \text{A}_{\text{RMS}}$$

3.2 In-Line Phase Current Sensing

Accurate, linear motor phase current feedback is very important for an accurate position and torque control of the motor. Phase current information is also required to detect short circuits. In this TI Design, shunt-based in-line phase current sensing is done. Shunt-based current sensing provides the benefits of being highly accurate, linear, smallest form factor, and low cost when compared to Hall sensors or current transformers. The only disadvantage being higher power loss in the shunt resistors at higher currents and the resulting temperature drift. Shunt-based current sensing is ideal if the maximum continuous current to be measured is less than around 50 A. The AMC1306E25 ΔΣ modulators are used for isolated reading of the voltage drop across the shunt resistors. The exact phase current can be computed in software by multiplying the voltage across the shunt resistors by a scaling factor. The current sense scheme for measuring U phase current is shown in 図 10. The current sensing for the W phase is similar.

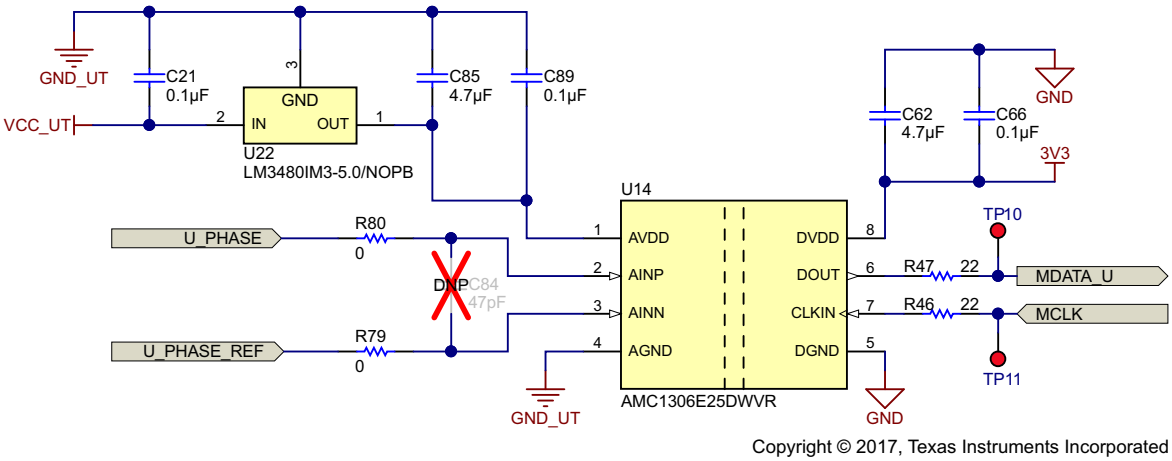


図 10. Schematic of U Phase Current Sensing

As mentioned in 3.1, the maximum continuous current to be measured is ≈ 28 A_{RMS}, which leads to a peak current of 40 A_{PK}. A 4-mΩ shunt resistor is used in this TI Design. The transfer function for the current sensor is shown in 式 3:

$$V_{R120} = I_{U-Phase} \times R120 = 0.004 I_{U-Phase} \tag{3}$$

A peak current rating of ±40 A_{PK} results in a ±0.16-V drop across the shunt resistor R120 and a maximum power dissipation of 3.2 W. A 7 W, a 1%, ±75 ppm/°C resistor in the 5931 package is selected. The AMC1306E25 has a high-linearity input voltage range of ±250 mV and clips at ±320 mV. This enables short-term overload current measurement of 1.5 times the maximum continuous current and short-circuit measurement up to 80 A_{PK}.

C85 and C89 are noise decoupling capacitors on the high-side power supply, and C62 and C66 are noise decoupling capacitors on the low-side power supply. R47 and R46 are termination resistors on the high-frequency data and clock digital signals. The high-side of the AMC1306 is powered from the high-side gate driver power supply of U Phase through LDO U22. The LDO LM3480 is available in a SOT23 package, which enables a very compact solution. The primary-side operating current of the AMC1306 is 9.8 mA (maximum). This leads to a maximum power dissipation of 98 mW across the LDO. The maximum junction temperature of the LDO at 55°C ambient will be ≈ 80°C.

The data output of the AMC1306E25 is Manchester encoded and connected to the Delfino controller TMS320F28379D. The controller SDFM peripheral decodes the Manchester data. The decoded data is simultaneously passed through two paths. One path is a high-OSR, SINC 3 filter path with high accuracy and latency suitable for motor position and torque control. The other path is a low-OSR path with low accuracy and latency suitable for short-circuit detection. It is recommended to use a 128-OSR, SINC 3 filter for motor phase current sensing and an 8-OSR, SINC 3 filter for short-circuit detection.

3.3 DC-Link Voltage Sensing

DC-link voltage feedback is required for under- and overvoltage protection as well as maintaining constant power delivery to the motor even with DC bus voltage tolerances. A high-impedance resistive voltage divider is implemented using R98, R108, R122, R125, R127, R128, R129, and R109 as shown in 図 11. The voltage across R109 is read by the ΔΣ modulator, which has to be scaled in software to get the exact DC bus voltage. 0- to 1200-V DC is read as 0- to 0.209-V DC by the AMC1306 as calculated in 式 4. R107 equaling to R109 has to be added to cancel out errors due to the AMC1306 input bias current flowing through R109.

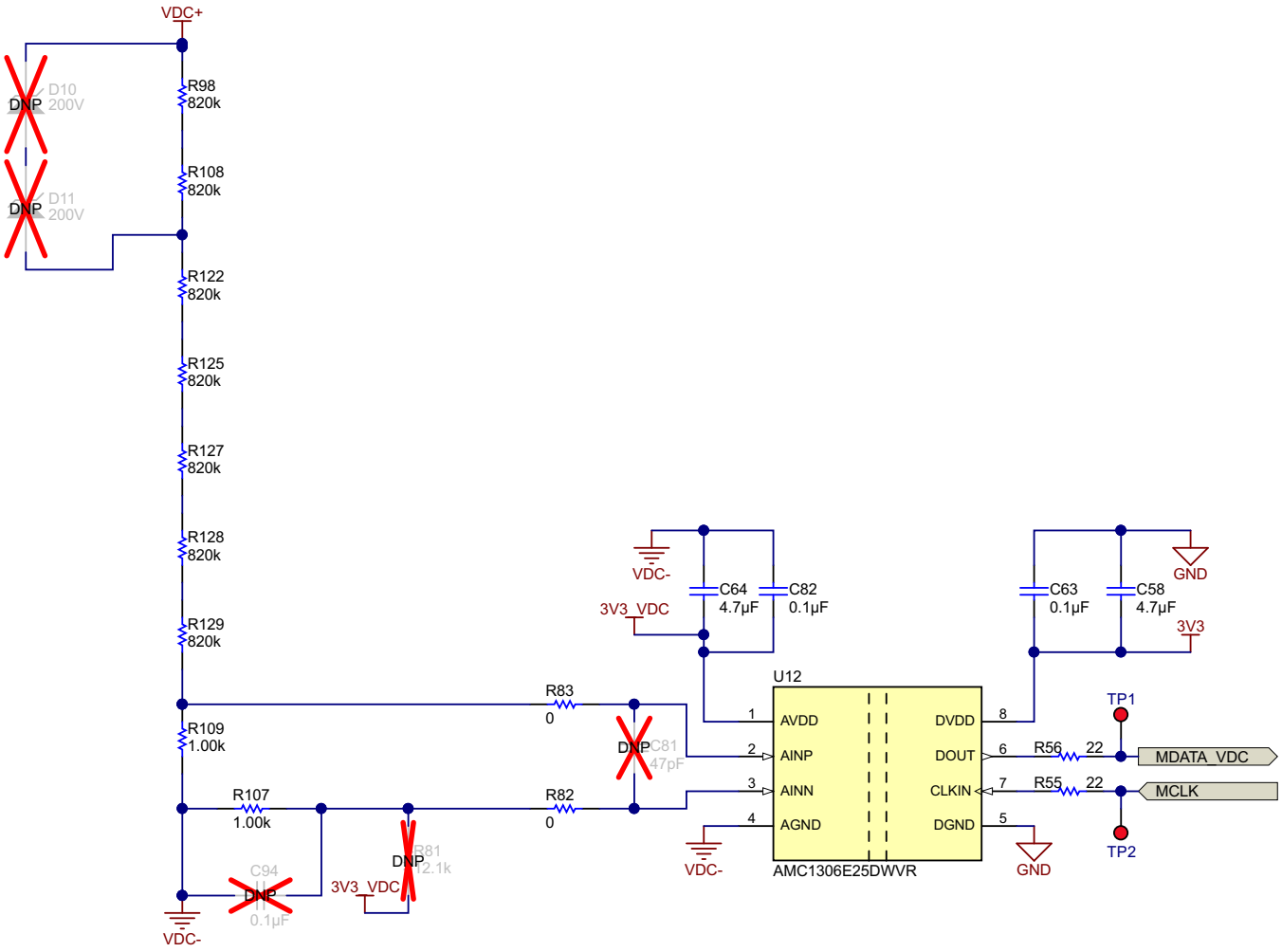


図 11. Schematic of DC-Link Voltage Sensing

$$V_{DCSENSE} = V_{DCBUS} \times \frac{R109}{(R98 + R108 + R122 + R125 + R127 + R128 + R129) + R109}$$

$$V_{DCSENSE} = 1200 \times \frac{1000}{(820000 \times 7) + 1000} = 1200 \times 0.1742\,m = 0.209\ V \quad (4)$$

A differential input filter can be implemented using R83, R82, and C81. This TI Design does not use this filter; R83 and R82 are equal to 0 Ω and C81 is DNP. The feedback from the voltage divider is unidirectional whereas the input of the AMC1306 can read bidirectional voltages. The complete input voltage range of the AMC1306 can be used by level shifting the negative input of the device to 0.250 V. In this TI Design, R81, R107, and C94 give a provision for level shifting. D10 and D11 are Zener diodes, which are unpopulated. By using these diodes, the input range of the AMC1306 can correspond from 400 to 1200 V instead of 0 to 1200 V. This feature is useful if there is no necessity to measure DC-link voltage below 400 V. C64 and C82 are noise decoupling capacitors for the secondary-side power supply whereas C62 and C58 are for the primary side. R56 and R55 are series line terminating resistors for the data line and clock input.

3.4 IGBT Power Module Temperature Sensing

Temperature feedback of the IGBT power module is necessary for overtemperature shutdown as well as derating the output of the inverter at higher temperatures. Module temperature is measured using the NTC integrated inside the module. The NTC thermal characteristics are shown in 図 12:

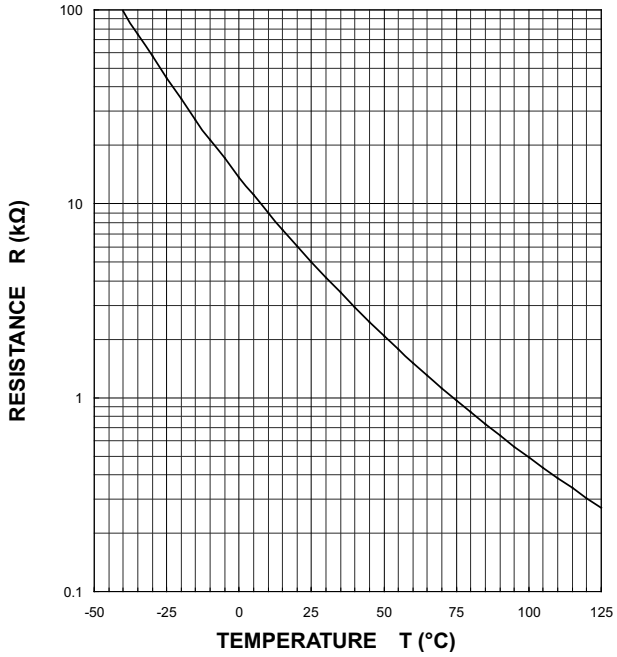


図 12. Temperature Characteristics of NTC Thermistor

A resistor divider is formed using R106 and the NTC resistor as shown in 図 13. The voltage across the NTC resistor is read by the AMC1306. The exact temperature can be calculated in software using 式 5 and 式 6.

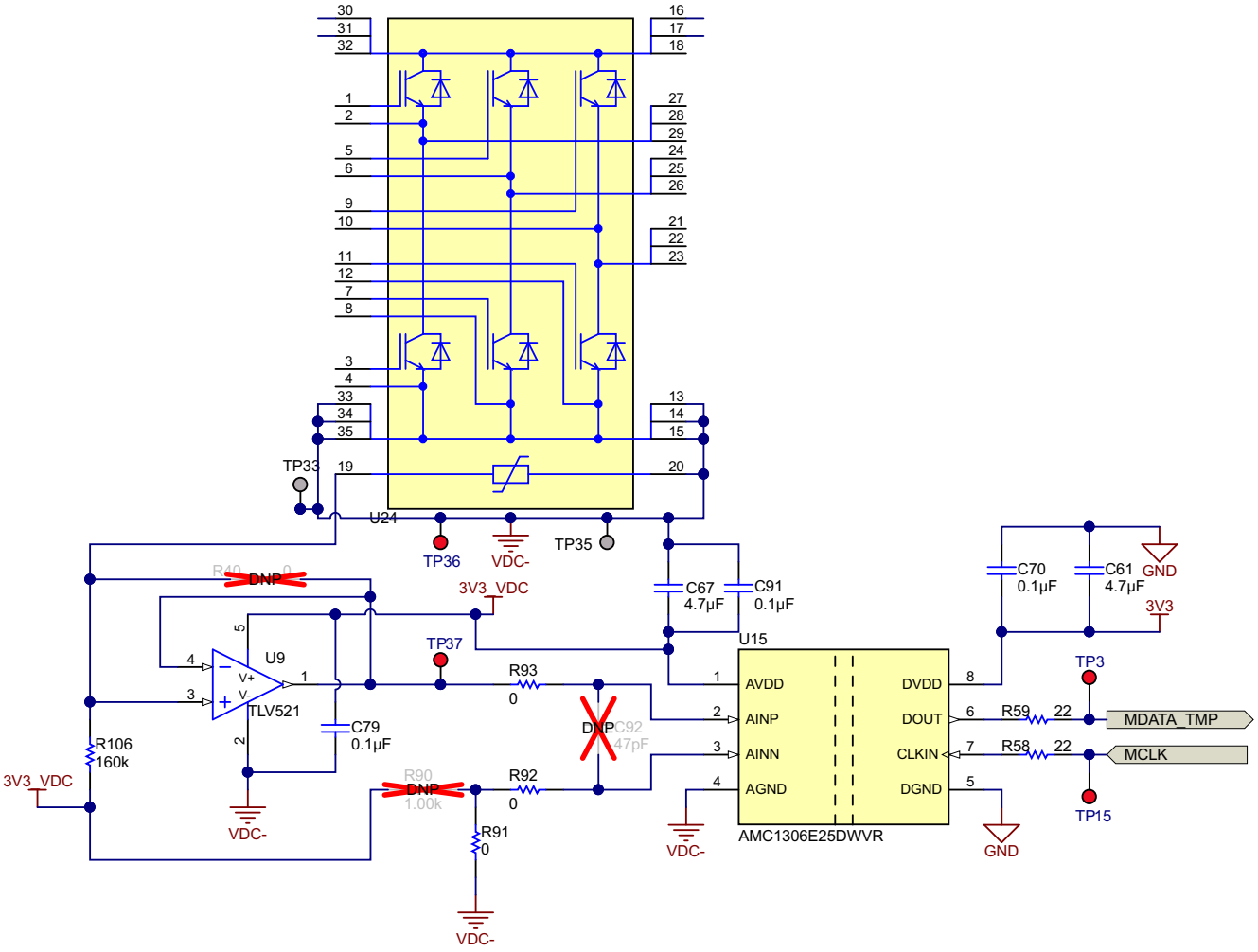


図 13. Schematic of Module Temperature Sensing

$$R_{NTC}(T) = R106 \times \frac{\text{AMC reading}}{3.3 - \text{AMC reading}} \quad (5)$$

$$T = \frac{1}{\ln\frac{R_{NTC}(T)}{R_{25}}\frac{1}{B} + \frac{1}{25}} \quad (6)$$

where:

- T is the temperature of the IGBT module
- $R_{NTC}(T)$ is the NTC resistance at temperature T calculated from the voltage drop across the NTC
- R_{25} is the NTC resistance at 25°C available from the IGBT module datasheet
- B(25/50) is the B-constant of the NTC resistor available in the module datasheet

The NTC resistance is 5 kΩ at 25°C. The input impedance of AMC1306E25 is 22 kΩ, which is in parallel with the NTC resistance. This alters the voltage divider scaling ratio. The input bias current of the AMC1306 also flows through the NTC resistor adding to the error. For good temperature measurement accuracy that is cost effective, use a voltage follower buffer like the TLV521 as shown in 図 13 to mitigate these error sources. R90, R91, and R92 are used to level shift the negative input to 0.250 V. This level shifting allows the use of the complete input range of the AMC1306. This TI Design does not use level shifting, so R90 is DNP and R91 is 0 Ω. Provision is given for the differential input filter using R93, R92, and C92. 22-Ω termination resistors are used on the data and clock lines for minimizing reflections.

3.5 Primary-Side 3.3-V Power Supply

The primary side of the board is provided with a 5-V input through terminal block J2 as shown in 図 14. D1 is a Schottky diode for reverse polarity input protection. C5 is the input bulk capacitor and C14 is for noise decoupling. A LDO TLV1117-33 is used to generate 3.3 V from the input supply. A 100-µF bulk capacitor and 0.1-µF noise decoupling capacitor are used on the output. The maximum output current required from the LDO is 40 mA calculated from 表 3. The maximum power dissipation is 68 mW, which leads to a maximum junction temperature of 57.6°C for 55°C ambient.

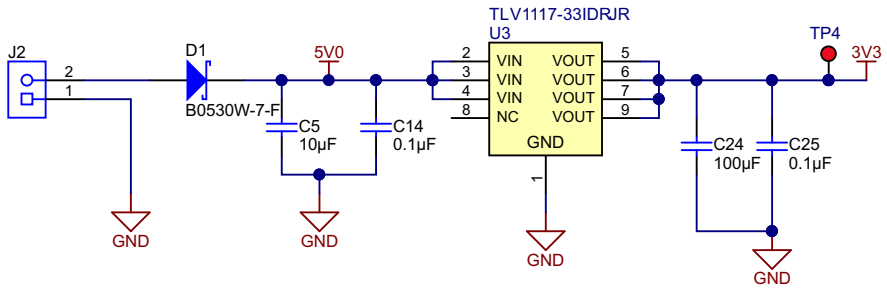


図 14. Schematic of Primary-Side 3.3-V Supply

表 3. Current Requirement

DEVICE	NUMBER OF DEVICES	MAXIMUM CURRENT REQUIREMENT
AMC1306E25	4	5.5 mA × 4 = 22 mA
Gate driver	7	2.5 mA × 7 = 17.5 mA

3.6 Secondary-Side 3.3-V Power Supply

The secondary-side 3.3-V power supply powers the DC bus voltage sensor and the temperature sensor. The LDO TLV70433 is used to generate 3.3 V from the 15-V low-side gate driver power supply. 4.7-µF bulk capacitors are placed on both the input and output of the LDO for fast transient response. The maximum current output requirement is 17 mA and the power dissipation across the LDO is 0.1989 W, which leads to a maximum junction temperature of 97°C for 55°C ambient.

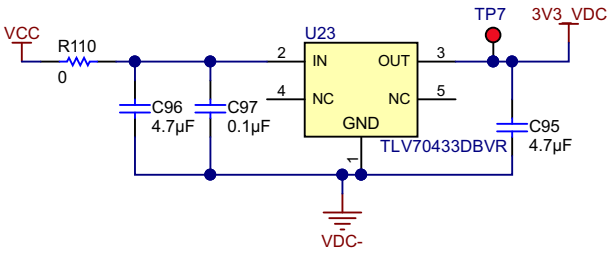


図 15. Schematic of Secondary-Side 3.3-V Power Supply

表 4. Current Requirement

DEVICE	NUMBER OF DEVICES	MAXIMUM CURRENT REQUIREMENT
AMC1306E25	2	2 × 8.5 mA = 17 mA
TLV521	1	500 nA
NTC Shunt divider	1	3.3 / (160K) = 20.6 µA

4 Getting Started Hardware

4.1 PCB Overview

図 16 shows the top view of the PCB. The DC bus input connector J8 and the three-phase motor output connector J4 are indicated. Provision is given to add a connector J3 for connecting an external brake resistor to the DC bus. The primary-side 5-V power supply is connected to J2, and the secondary-side isolated 15-V power supply is connected to J7. J1 is a female 25-pin D-SUB connector for interfacing to the controller.

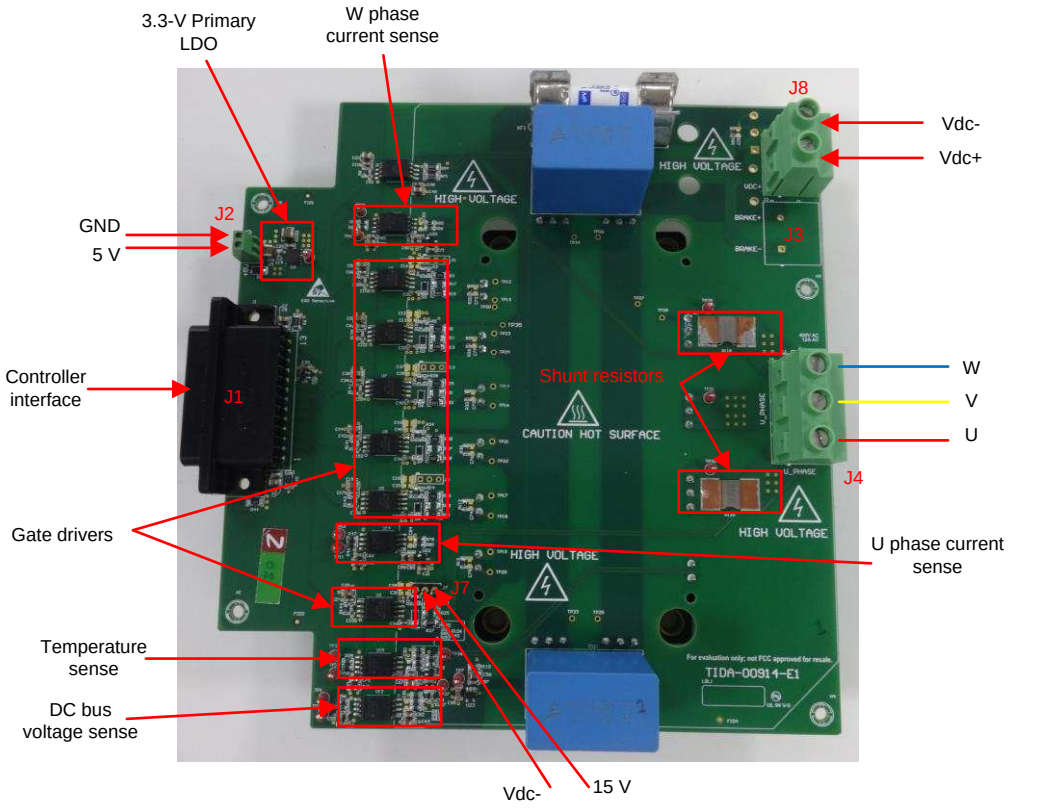


図 16. Top View of TIDA-00914 PCB

図 17 indicates the primary low-voltage side, the secondary high-voltage side, and the reinforced isolation barrier in between.

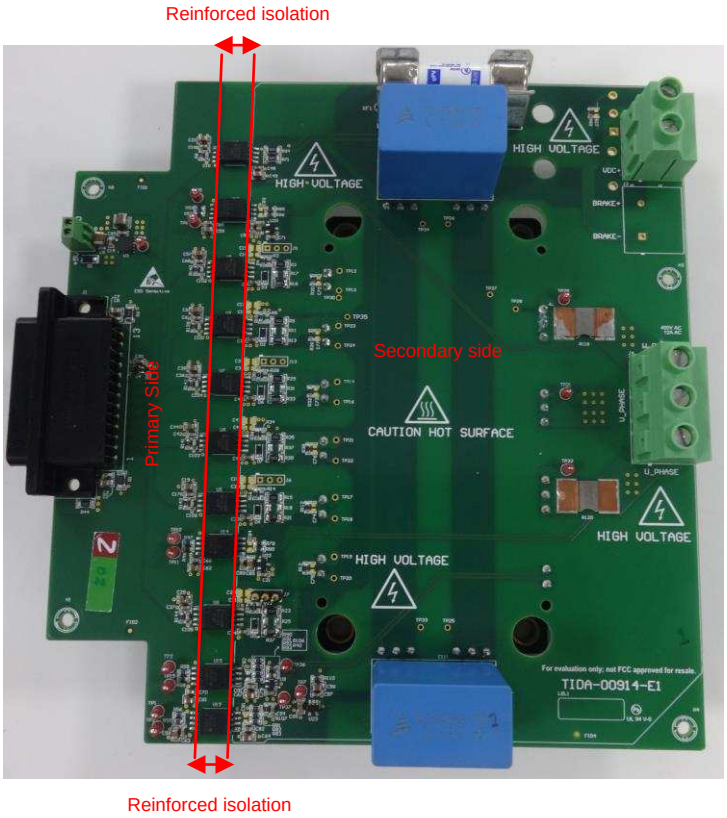


図 17. Primary Side, Secondary Side, and Isolation Barrier

図 18 shows the bottom view of the PCB. Provision is given for adding brake chopper IGBT Q1 and freewheeling diode D9. The pad of the IGBT module has to be connected to a heat sink. The thermal compound has to be used between the pad and the heat sink, and the module must be rigidly screwed to the heat sink as shown in 図 19. Choose an appropriate heat sink based on the maximum continuous power to be dissipated.

図 18. Bottom View of TIDA-00914 PCB

注: The heat sink shown in 図 19 is not optimized and is for testing purposes only.

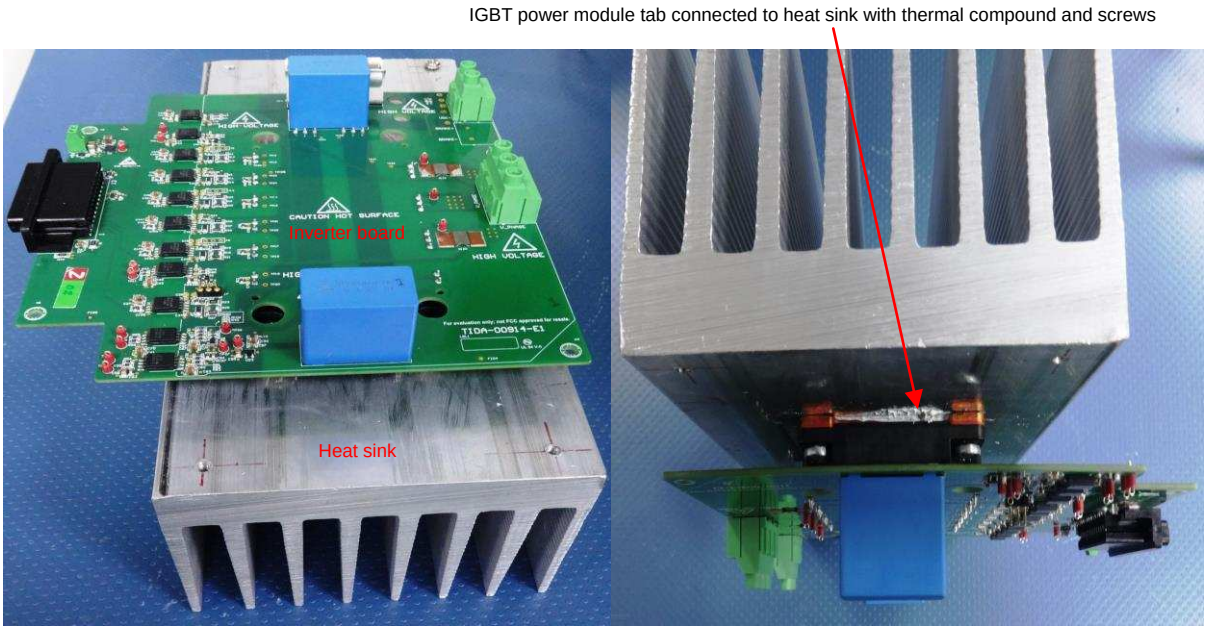


図 19. TIDA-00914 Connected to Heat Sink

4.2 Controller Interface Connector

The Delfino control card is connected to J1 on the TIDA-00914 board through an adaptor PCB as shown in 図 20. A ribbon cable is used to connect the two. The pin functions are described in 表 5.

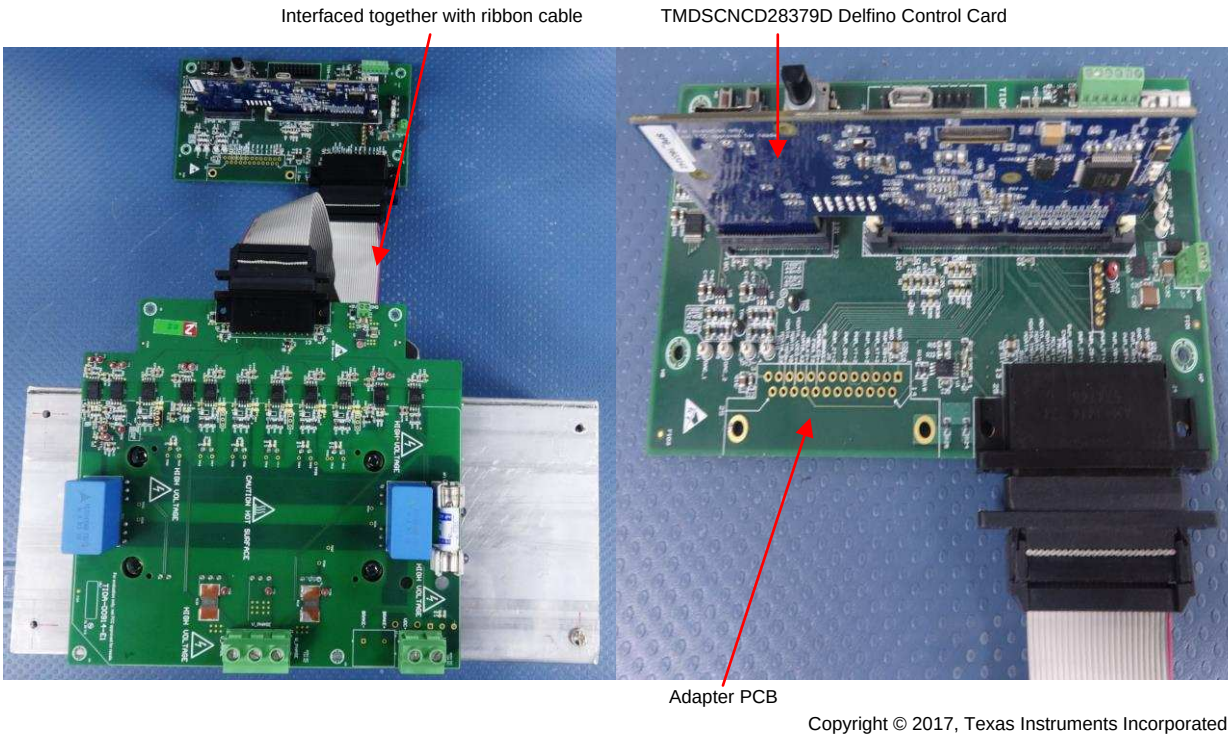


図 20. Controller Connection to TIDA-00914

表 5. Connector Pin Description

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	5V0	Power	5-V input to the primary side of the power stage
2	PWM_UB+	3.3-V input	Phase U low-side gate driver PWM input
3	PWM_UT+	3.3-V input	Phase U high-side gate driver PWM input
4	PWM_VB+	3.3-V input	Phase V low-side gate driver PWM input
5	PWM_VT+	3.3-V input	Phase V high-side gate driver PWM input
6	PWM_WB+	3.3-V input	Phase W low-side gate driver PWM input
7	PWM_WT+	3.3-V input	Phase W high-side gate driver PWM input
8	PWM_BRAKE+	3.3-V input	PWM input to brake IGBT gate driver
9	NC	NA	NA
10	MDATA_U	3.3-V output	U phase current measurement data from ΔΣ modulator
11	NC	NA	NA
12	MDATA_W	3.3-V output	W phase current measurement data from ΔΣ modulator
13	5V0	Power	5-V input to the primary side of the power stage
14	GND	Power	Primary-side ground
15	GND	Power	Primary-side ground
16	GND	Power	Primary-side ground
17	GND	Power	Primary-side ground
18	GND	Power	Primary-side ground
19	GND	Power	Primary-side ground
20	GND	Power	Primary-side ground
21	NC	NA	NA
22	CLK	3.3-V input	Clock input to TIDA-00914 from the control card
23	MDATA_VDC	3.3-V output	DC bus voltage measurement data from ΔΣ modulator
24	MDATA_TMP	3.3-V output	Temperature measurement data from ΔΣ modulator
25	GND	Power	Primary-side ground

5 Testing and Results

The focus of the tests is to evaluate the functionality and performance of the shunt resistor-based reinforced isolated in-line phase current sensing using the AMC1306E25 ΔΣ modulator. 表 6 lists the key test equipment used.

表 6. Key Test Equipment

DESCRIPTION	PART NUMBER
Oscilloscope	Tektronix MDO4104B-3
Single-ended probes	Tektronix TPP1000
Current probe	Keysight N2781B
Current probe amplifier	Agilent N2779A
Logic analyzer probes	Tektronix P6616
AC current standard	Yokogawa 2558A
Signal generator	Agilent 33220A
Multimeter	Keithley 2002, Fluke 87V
Power supply	Keithley 2230G-30-1
AC induction motor	3.7 kW, 1460 rpm (0.5 to 100 Hz), 415 V_{RMS} ± 10%, η = 83 %, cosφ = 0.74, 8.4 A_{MAX}
High-voltage power supply	Agilent N5772A

5.1 Software

This TI Design is tested using software modified from the application report *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x* [3]. The incremental build level 2 shown in 図 21 is modified. A switch is added to connect either the OUT signal coming from the RG MACRO or the angle variable to the sine cos block. Connecting OUT enables the design to pump sinusoidal current into the motor. Connecting the angle variable, which is made zero, enables driving DC current into the motor. The default ADC MACRO is used for reading data from a SAR ADC and is not suitable for ΔΣ modulators. This MACRO has been replaced by code for decoding the Manchester encoded data coming from the ΣΔ modulators and decimate the bit stream.

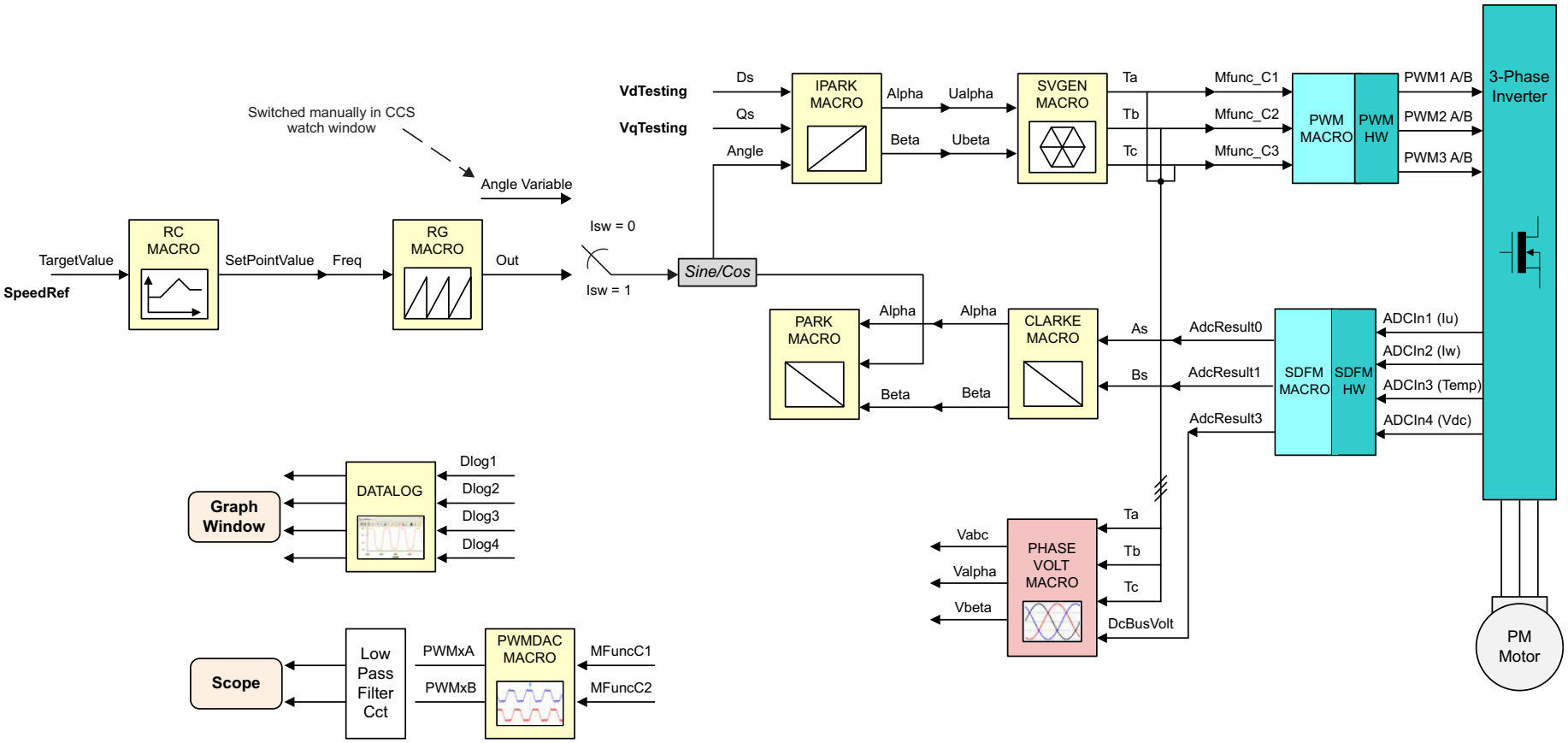


図 21. PWM Control and Current Sense Software

5.2 Detection of High-Side Power Loss in AMC1306E25

If the high-side power supply is missing, the output of the ΔΣ modulators is no longer valid. This causes loss of phase current feedback, resulting in system malfunction. The controller needs an indication that the high-side power is missing to take an appropriate action. This is done by the fail safe output feature of the AMC1306, as shown in 図 22.

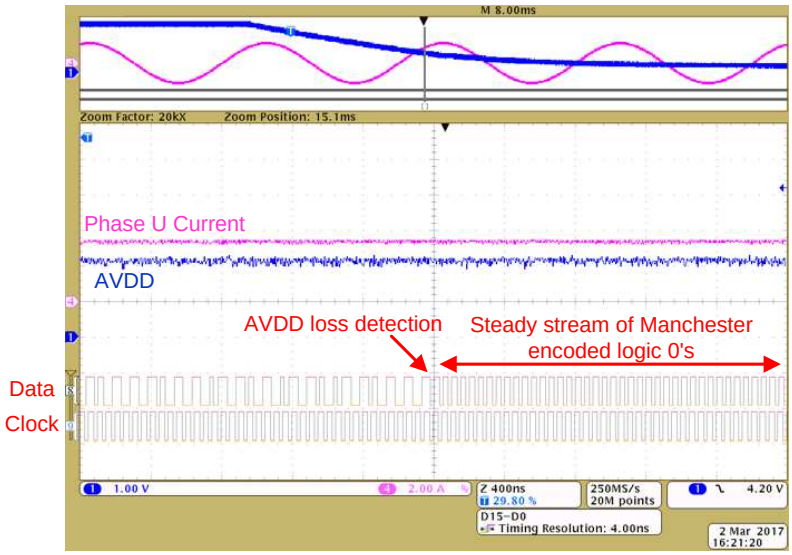


図 22. Loss of High-Side Power Detection

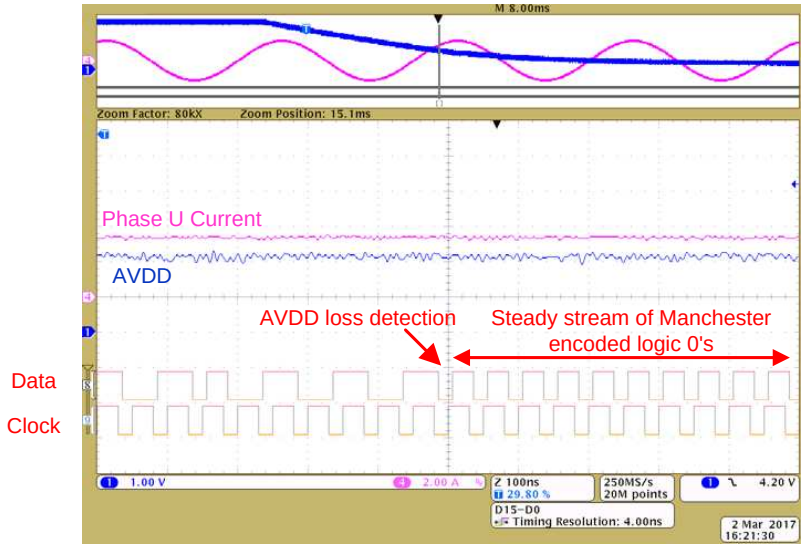


図 23. Loss of High-Side Power Detection, Zoomed in

- Blue waveform: Secondary side AVDD
- Pink waveform: Current through phase U shunt resistor
- Digital channel 8: Modulator data bit stream
- Digital channel 9: Modulator clock signal

When the AVDD signal is lost, the output data pin of the modulator D8 provides a steady stream of logic 0's. In this case, it outputs the clock signal as the data is Manchester encoded. Note that for this test, current is pumped into the shunt resistor with an AC current standard equipment. No motor is connected to the inverter.

5.3 Detection of Input Greater Than Full-Scale Input

When the phase current exceeds the maximum measurement range (that is, $V_{IN} \geq V_{CLIPPING} = \pm 0.320$ V), the modulator outputs a steady stream of logic 1's or 0's depending on the polarity of the current being measured. In order to differentiate from the loss of AVDD condition mentioned in 5.2, the device generates a toggle bit every 128 bits.

- Pink waveform: Current through phase U shunt resistor
- Digital channel 8: Modulator data bit stream
- Digital channel 9: Modulator clock signal

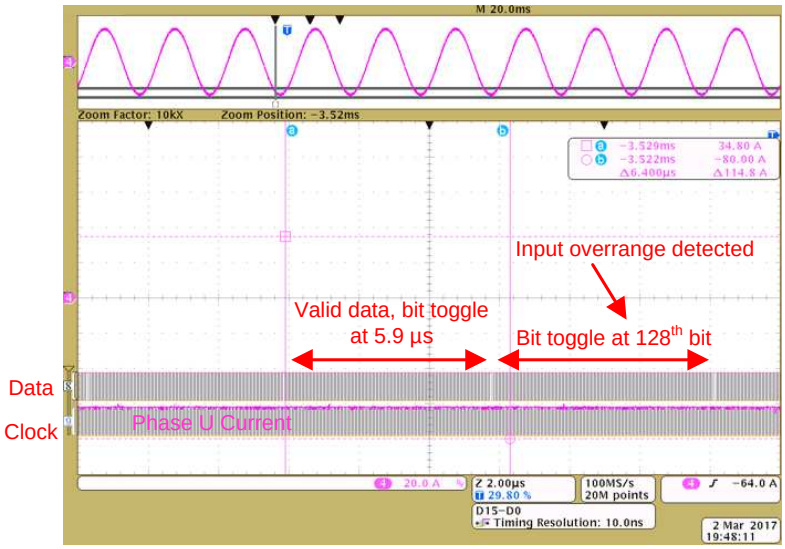


図 24. Negative Overrange Detection With Manchester Encoded Data

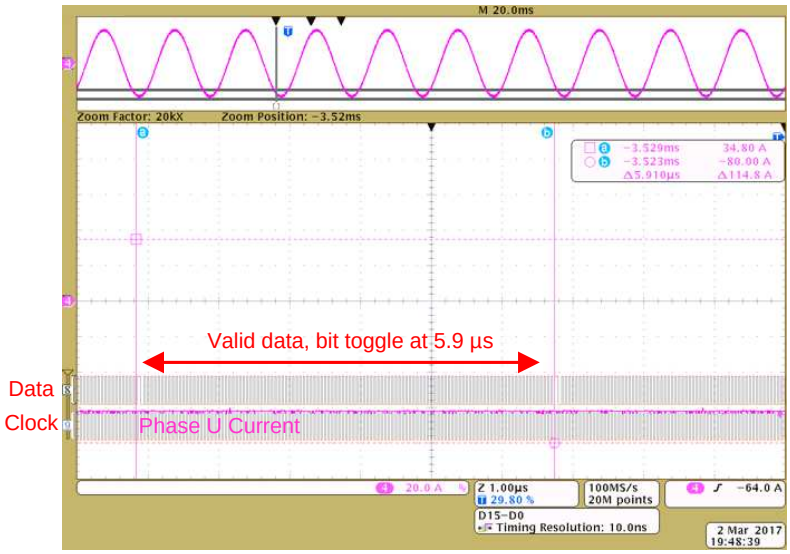


図 25. Bit Sequence Immediately Before Overrange Detected (Negative Overrange Detection With Manchester Encoded Data, Zoomed)

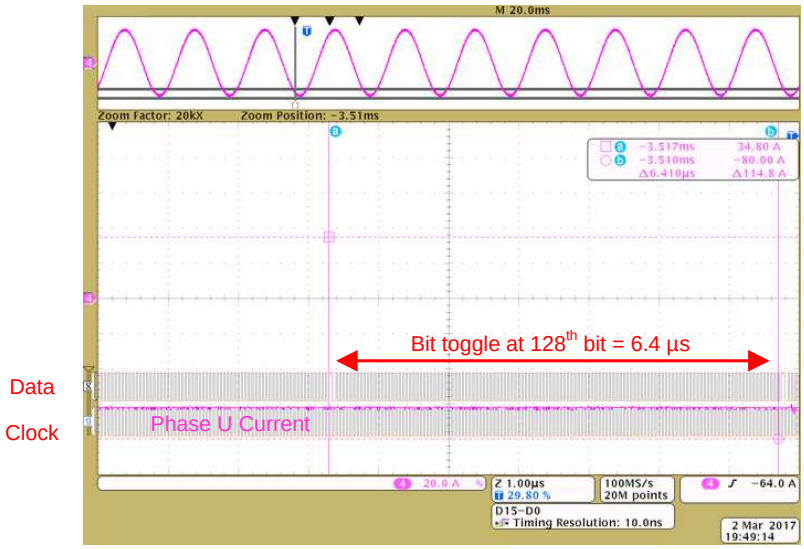


図 26. Negative Overrange Detection (Negative Overrange Detection With Manchester Encoded Data, Zoomed)

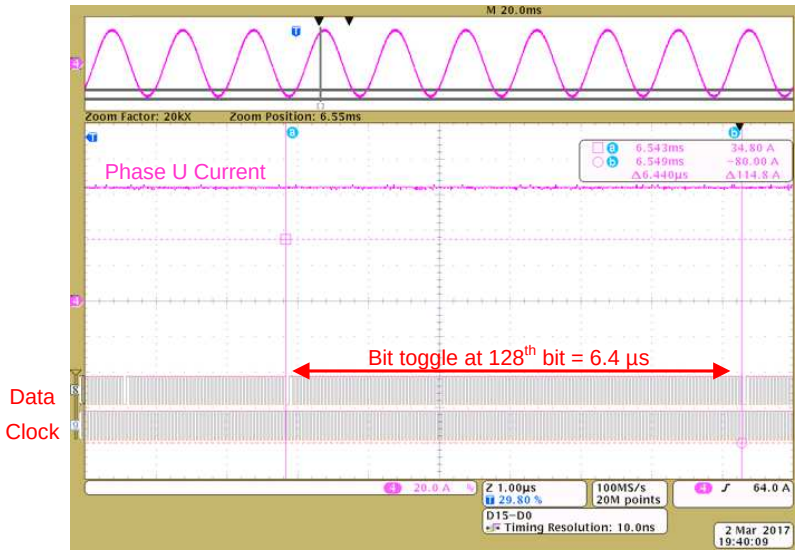


図 27. Positive Overrange Detection With Manchester Encoded Data

Due to test setup limitations in reaching a current to exceed the maximum measurement range, the tests in this section use a 5-mΩ shunt resistor instead of a 4-mΩ shunt resistor used for rest of the test. 図 24 shows the instant at which overrange is detected. 図 25 is the zoomed-in version of 図 24, showing that before overrange there is valid data shown by data bit toggle after 5.9 µs. After this bit, there are bit toggles every 128 bits, indicating that the AMC input has exceeded the maximum measurable input. 図 26 shows the detection of overrange at –62 A (–62 A × 5 mΩ = –0.31 V). The bit toggle at every 128-bit interval (1/20 MHz × 128 =
6.4 µs) is shown. 図 27 shows the detection of overrange at 64 A (64 A × 5 mΩ = 0.32 V). The bit toggle at every 128-bit interval (1/20 MHz × 128 = 6.4 µs) is shown.

注: Because the data is Manchester encoded, a constant logic one or zero translates to look like a clock signal. A logic bit toggle is when there is a 180° phase shift in the data signal.

5.4 Short-Circuit Response Time

Fast short-circuit protection is very important to protect both the motor and inverter power stage from damage. On short circuits, the IGBTs have to be switched off within 4 µs. Newer generation IGBTs switch faster but usually trade off with robustness against short circuit. These IGBTs have to be switched off in less than 2 µs. The response time to short circuit depends on the order of the SINC filter used and the OSR, as shown in 式 7.

$$\text{Response time, } tr = n \times \frac{OSR}{fs} \tag{7}$$

where:

- n is the order of the SINC filter
- OSR is the oversampling ratio of the SDFM
- fs is the modulator clock frequency

The short-circuit response time is captured for three different combinations of SINC filter order and OSR:

- SINC 1, 24 OSR

- SINC 2, 12 OSR
- SINC 3, 8 OSR

Each of the three combinations have the same theoretical response time of 1.2 µs. For the test setup, the shunt resistor is unpopulated and the AMC inputs are instead connected to a function generator. The function generator applies a positive and negative step input. The output of the SDFM comparator module is routed to a GPIO. The response time is equal to the time delay between the rising edges of the step input and the GPIO signal. An additional delay of ≈ 200 to 300 ns is captured in the test results, which is due to the time required to execute the instructions needed to toggle the GPIO pin. The short-circuit detection threshold has been set to ± 40 A. The threshold values required to be set in software for the different filter combinations are shown in 表 7.

表 7. Short-Circuit Threshold Values

FILTER ORDER	OSR	PEAK DATA VALUE	DATA VALUE FOR 0 A	DATA VALUE FOR 40 A	DATA VALUE FOR –40 A	CURRENT MEASUREMENT RESOLUTION
SINC 1	24	24	12	18	6	6.6600 A
SINC 2	12	144	72	108	36	1.1100 A
SINC 3	8	512	256	384	128	0.3125 A

表 7 shows that the SINC 3 filter with OSR 8 has the best current measurement resolution for the same response time.

図 28, 図 29, and 図 30 show the optimum response time for positive step input. 図 31, 図 32, and 図 33 show the optimum response time for negative step input.

図 34, 図 35, and 図 36 show the uncertainty in response time. This uncertainty is captured by putting the scope in high-persistence mode. This TI Design uses the C2000™ Delfino. The SINC filters implemented in the Delfino use the hardware-optimized Hogenauer structure to take advantage of decimation. This structure provides benefits in reducing the number of clock cycles needed to implement a SINC filter, resulting in a significant power saving. The disadvantage being the output of the filter is clocked at the modulator clock frequency divided by the OSR. Any event occurring between adjacent OSR/fs transitions will be reflected at the next transition only. This puts a maximum jitter uncertainty of OSR/fs.

As can be seen from the following figures, the higher the OSR, the higher the jitter. Using a SINC 3 filter with 8 OSR provides the least jitter as well as the best current measurement resolution. If the filter is implemented in an FPGA where concurrent processing is done and the SINC filter demodulation modules are clocked at the full modulator clock frequency, then the best response time shown in 表 7 is always achieved.

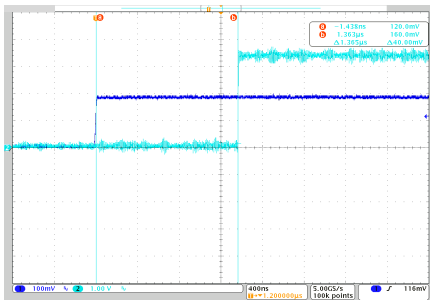


図 28. Positive Short-Circuit Optimum Response Time for SINC 1, 24 OSR

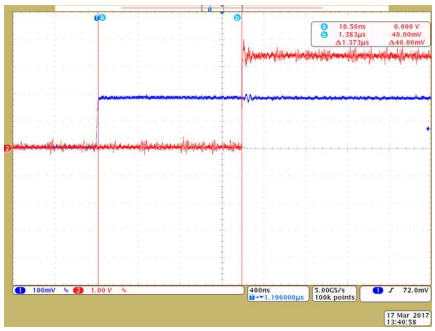


図 29. Positive Short-Circuit Optimum Response Time for SINC 2, 12 OSR

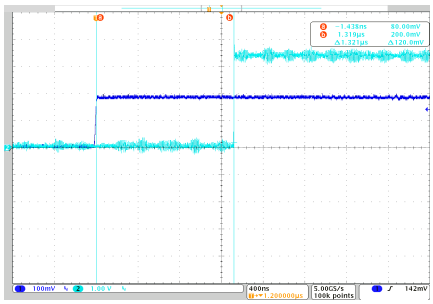


図 30. Positive Short-Circuit Optimum Response Time for SINC 3, 8 OSR

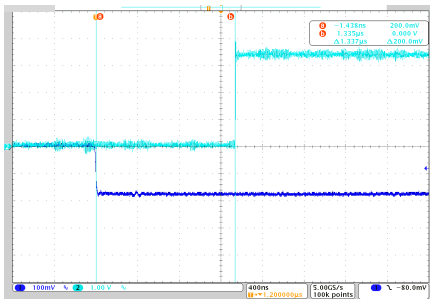


図 31. Negative Short-Circuit Optimum Response Time for SINC 1, 24 OSR

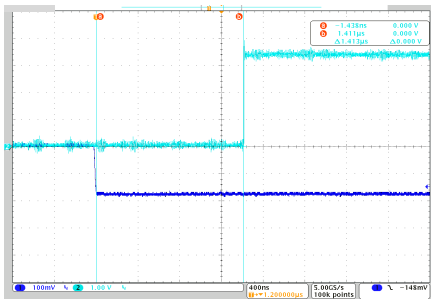


図 32. Negative Short-Circuit Optimum Response Time for SINC 2, 12 OSR

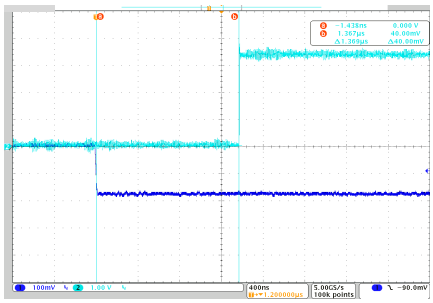


図 33. Negative Short-Circuit Optimum Response Time for SINC 3, 8 OSR

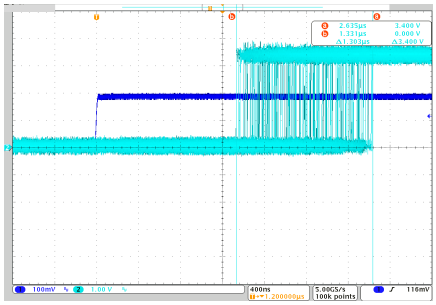


図 34. Response Time Jitter for SINC 1, 24 OSR

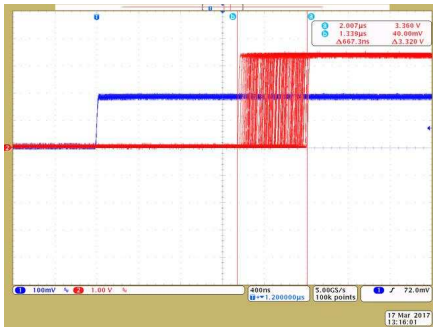


図 35. Response Time Jitter for SINC 2,12 OSR

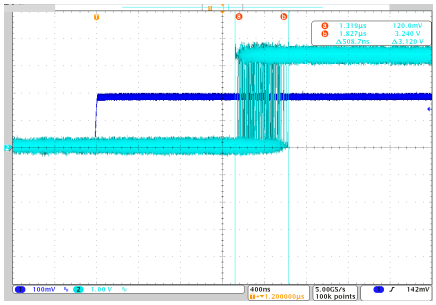


図 36. Response Time Jitter for SINC 3, 8 OSR

5.5 Current Sense Measurement Accuracy

図 37 shows the test setup for checking the performance of the current measurement. A 4-mΩ shunt resistor is used to measure the phase current. The voltage drop across the shunt resistor is measured by the AMC1306 ΔΣ modulator. The modulator output bit stream is channeled into the control card. The control card is configured to implement SINC filters of different orders and OSRs. The reading from the control card is compared with the actual phase current measured with a multimeter to determine the

measurement error. The center of the SINC filter window is synchronized to the center of the PWM pulse as shown in 図 38. This ensures that no switching noise gets into the SINC filter window and the measured current is the average current. For characterizing the current measurement performance, a DC current has been pumped into the motor by making the input to the sin/cos block zero as mentioned in 5.1. 図 39 shows the transfer function of the current sense circuit.

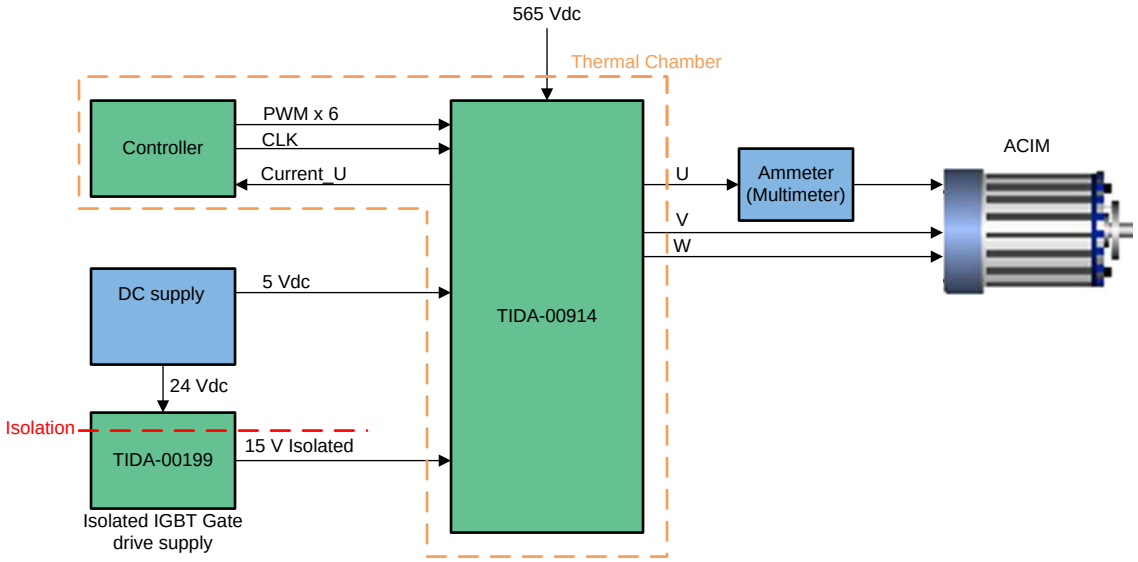


図 37. Test Setup

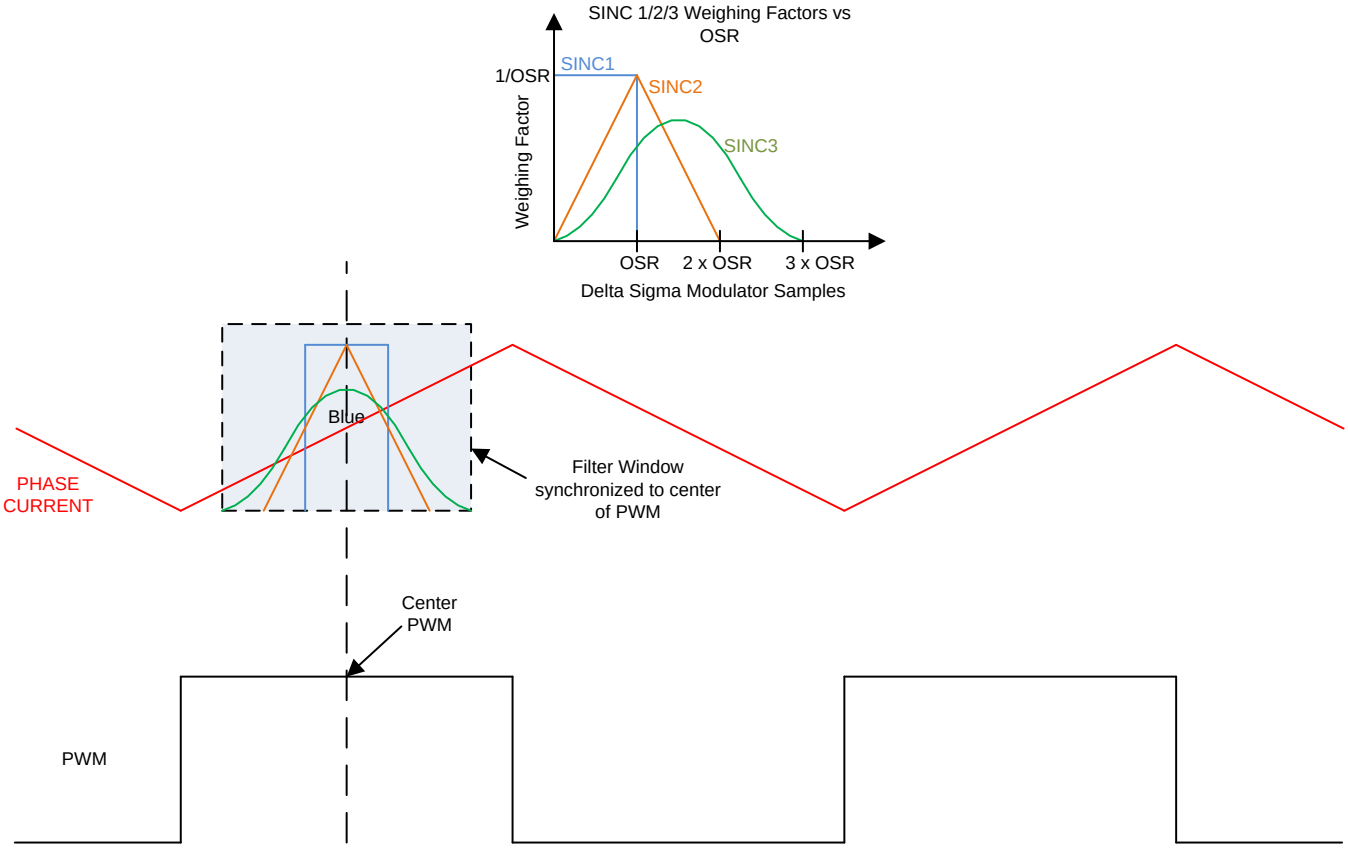


図 38. Sample Window

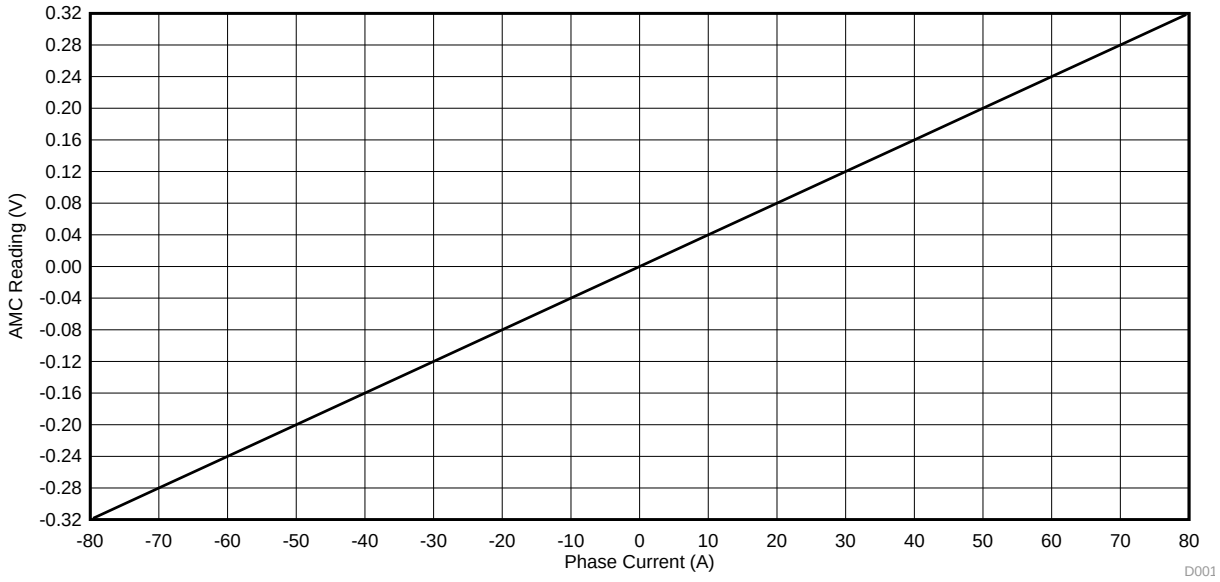


図 39. Transfer Function of Current Sensor

図 40 shows the absolute error and calibrated absolute error in amperes. The X-axis indicates the phase current and the Y-axis the current measurement error. The test has been done up to 10 A due to test setup limitations. A SINC 3 filter with 256 OSR is used, the modulator clock frequency is set to 20 MHz, and the PWM switching frequency is set to 4 kHz.

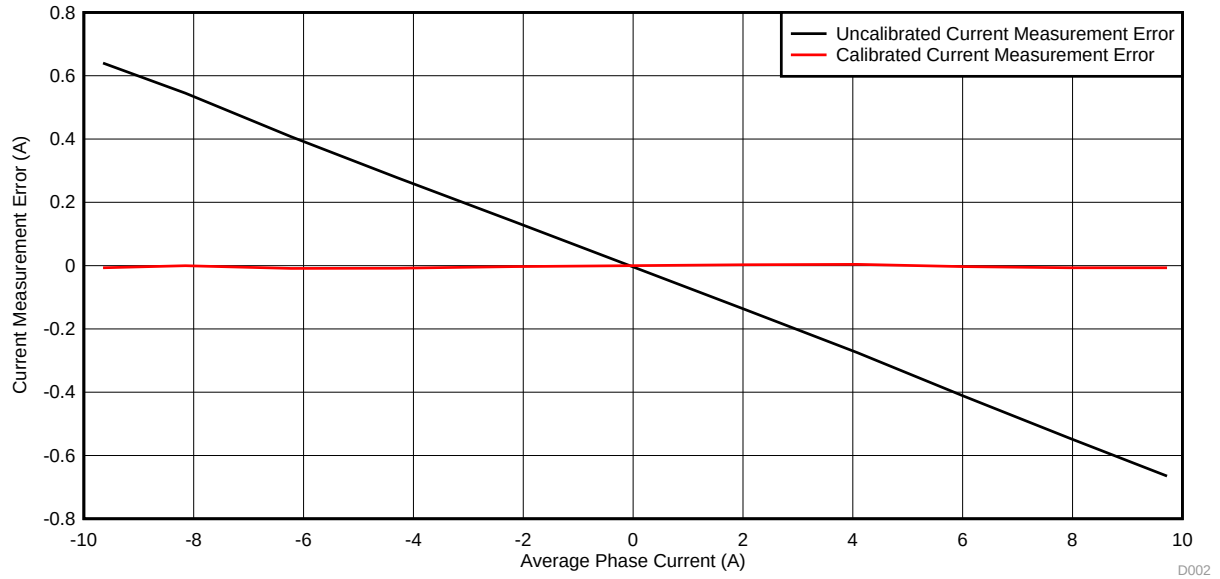


図 40. Absolute Error in Amperes

図 41 shows the % FSR error and the % calibrated FSR.

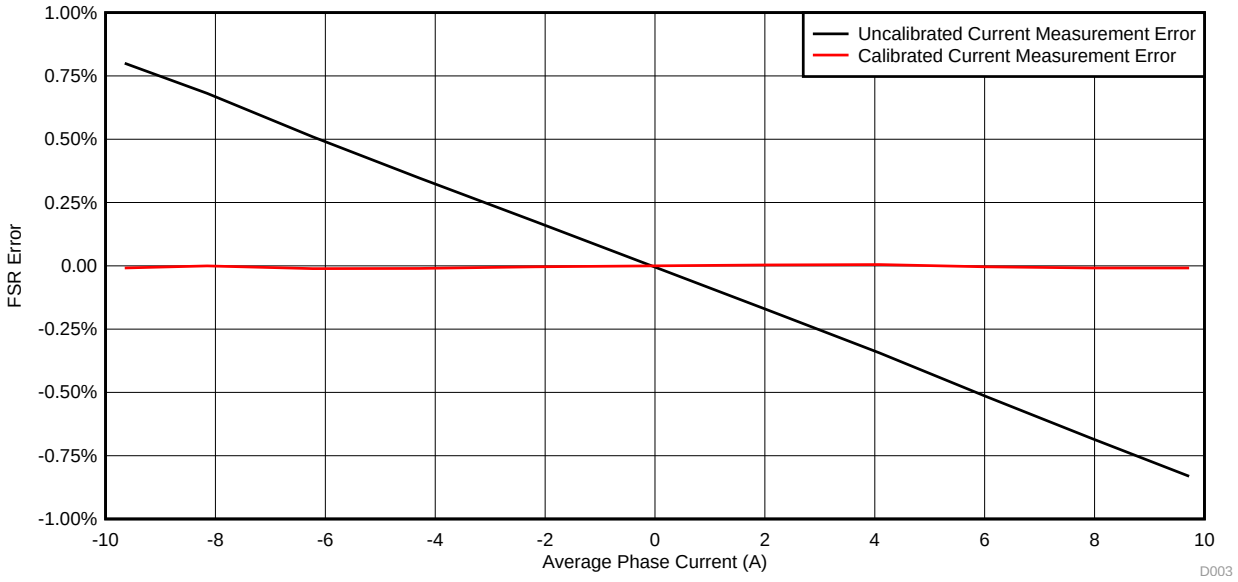


図 41. Error as Percentage of Full-Scale Range

図 42 shows the absolute calibrated error at different OSR values. The measurement error with a SINC 3 filter and OSRs of 256, 128, and 64 are plotted at 25 °C.

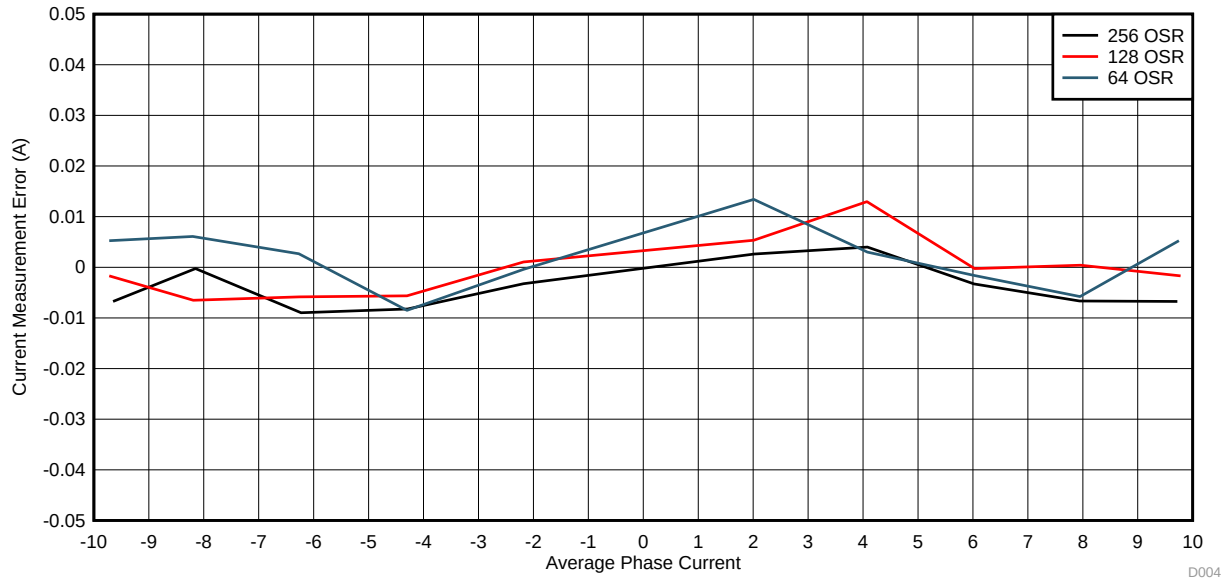


図 42. Error Versus OSR

図 43 shows the absolute calibrated error at different temperatures. A SINC 3 filter with 256 OSR is used, and the measurements are done at 0°C, 25°C, and 55°C.

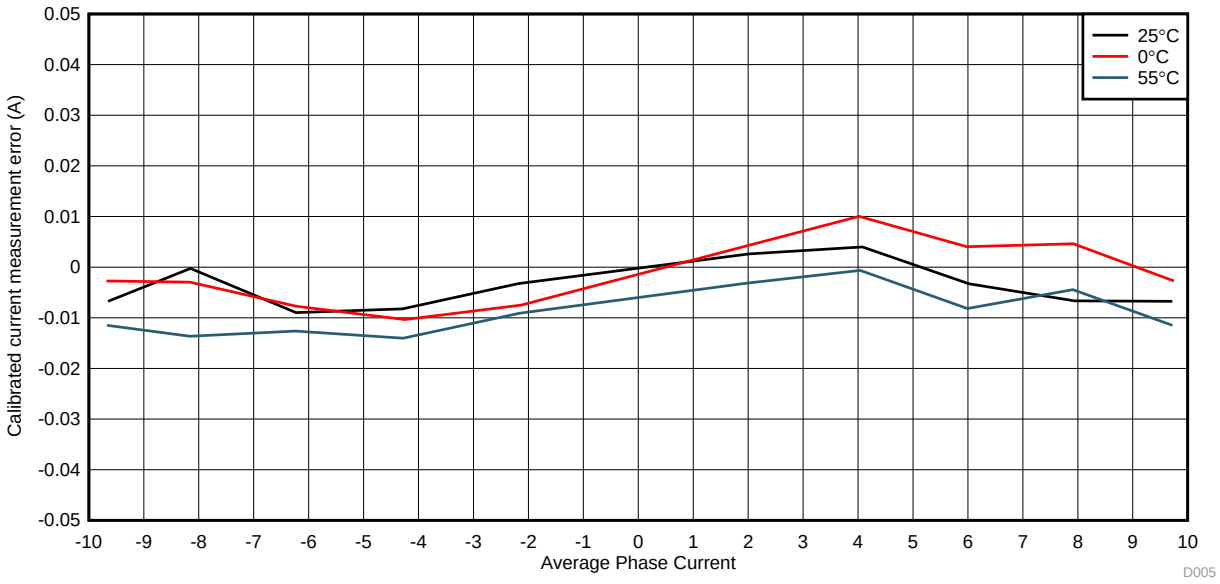


図 43. Error Versus Temperature

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00914.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00914.

6.3 PCB Layout Recommendations

図 44 shows the isolation barrier and ground split. The hot-side (high-voltage power side) and the cold-side (low-voltage controller side) copper tracks are separated from each other by a reinforced isolation barrier. The wide body package of the gate driver and ΔΣ modulators are placed across the isolation barrier. A copper-to-copper creepage spacing of 8.89 mm is maintained between the hot and cold sides.

The low-side gate driver grounds and DC bus negative are common. To avoid noise due to switching currents in the DC bus negative from interfering with the gate driver operation, a split is done in the ground plane and they are connected together at a single point as shown in 図 44.

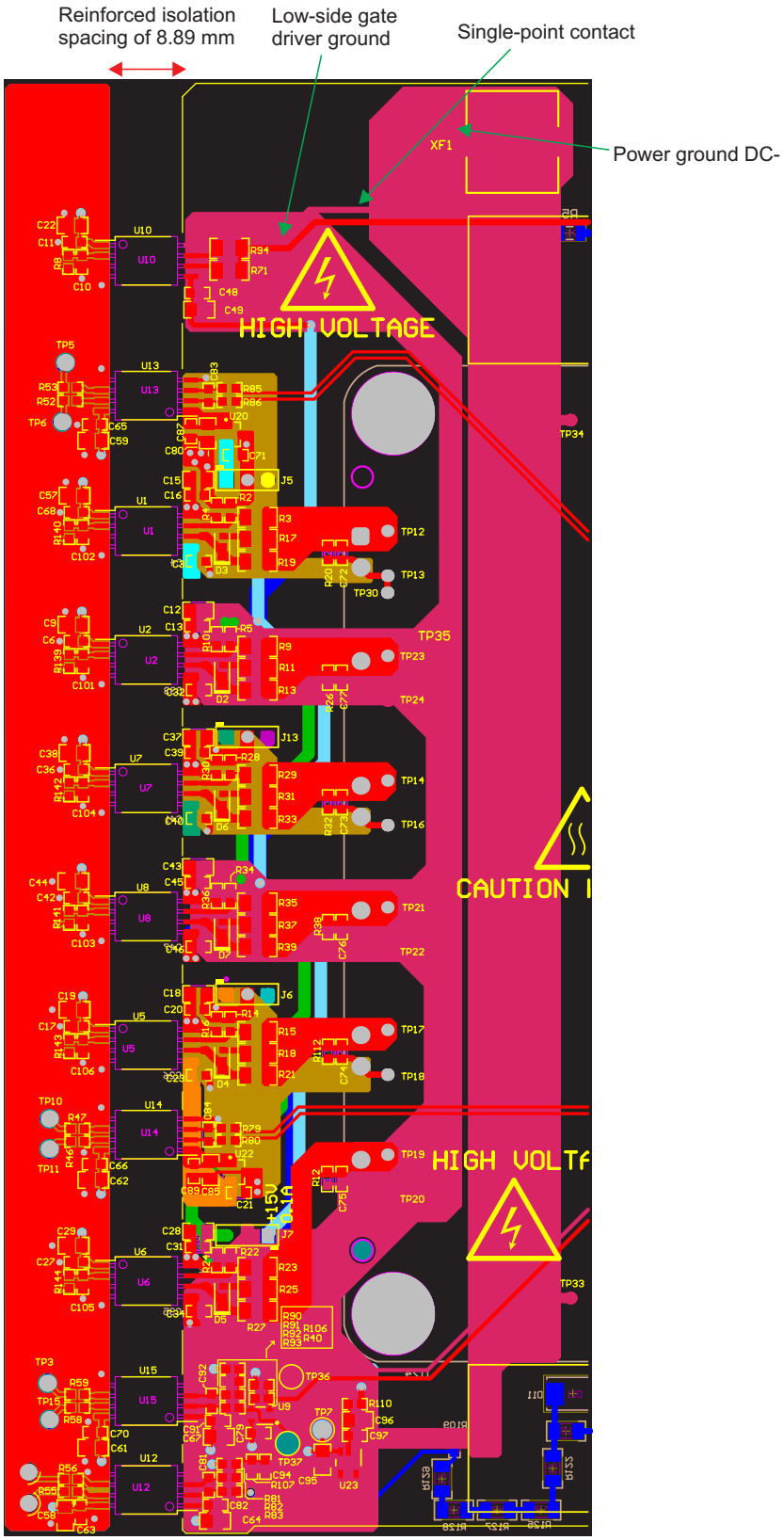


図 44. Reinforced Isolation Barrier and Ground Splits

The shunt resistance of 4 mΩ is in the same range as that of the stray parasitic trace resistances. For accurate shunt-based current sensing, it is important to sense the exact voltage across the shunt resistor only and avoid measuring the drop across the trace and contact parasitic resistance. This is done by implementing a Kelvin connection as shown in 図 45. Differential routing is done from the shunt resistor to the ΔΣ modulator. Any noise is common to both the traces and gets cancelled off in the differential input stage of the modulator.

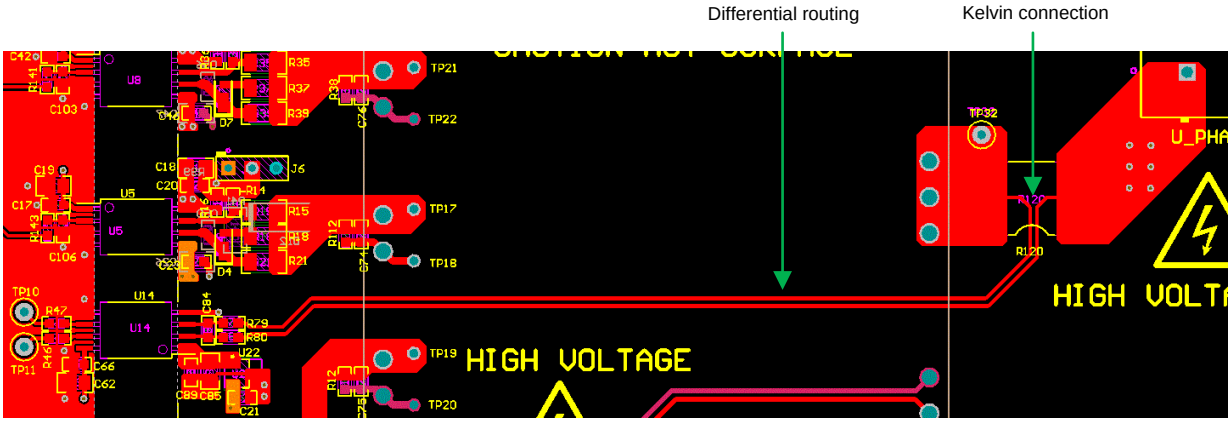


図 45. Shunt Resistor Connection to ΔΣ Modulator

図 46 shows the layout of the ΔΣ modulator circuit. R47 and R46 are 22-Ω termination resistors placed close to the clock and data signal pins. C62 and C66 are primary-side noise decoupling capacitors that have to be placed close to the power pin. R79, R80, and C84 form an external differential filter, which is placed symmetrically. C21 is the input capacitor for LDO U22, which converts 15 V to 5 V. C89 and C85 are secondary-side decoupling capacitors.

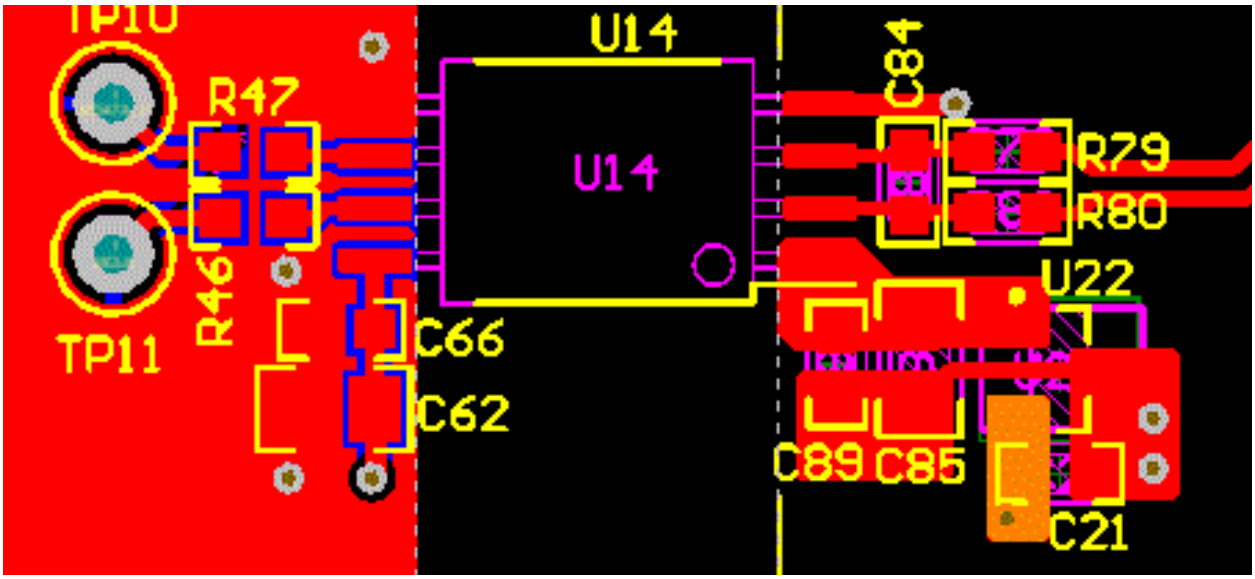


図 46. ΔΣ Modulator

図 47 shows the DC bus voltage sense circuit. The high-impedance resistor divider network is connected across the pins of the high-voltage DC-link film capacitor C111. The attenuated voltage is sensed by ΔΣ modulator U12. It is important to sense the voltage across the film capacitor for low-noise measurement.

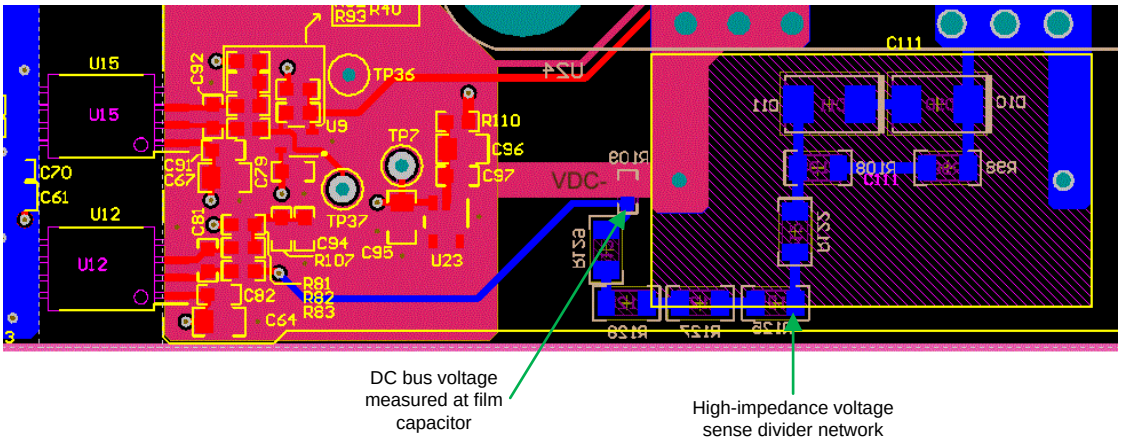


図 47. Connection of DC Bus Voltage Sensing

6.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00914.

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-00914.

6.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00914.

6.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00914.

7 Related Documentation

1. Texas Instruments, *Isolated Current Shunt and Voltage Measurement Kit* , TIDA-00171 reference design guide
2. Texas Instruments, *Isolated Current Shunt and Voltage Measurement for Motor Drives Using AM437x* , TIDA-00209 reference design guide
3. Texas Instruments, *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x* , application report
4. Texas Instruments, *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters* , TIDA-00199 reference design guide
5. Texas Instruments, *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection* , TIDA-00366 reference design guide
6. Texas Instruments, Basic Isolated Three-Phase Compact Power Stage Reference Design for Industrial Drives, TIDA-01420 reference design guide

7.1 商標

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8 Terminology

IGBT— Insulated gate bipolar transistor

ACIM— Alternating current induction motor

VFD— Variable frequency drive

PWM— Pulse width modulation

UVLO— Undervoltage lockout

SDFM— Sigma-delta filter module

DNP— Do not populate

OSR— Oversampling ratio

FSR— Full-scale range

9 About the Author

PAWAN NAYAK is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems.

9.1 Recognition

Pawan Nayak would like to recognize the excellent contributions from **MARTIN STAEBLER**, **N. NAVANEETH KUMAR**, and **NELSON ALEXANDER** during the design, test, and documentation phases of the TIDA-00914 device.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年5月発行のものから更新 **Page**

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